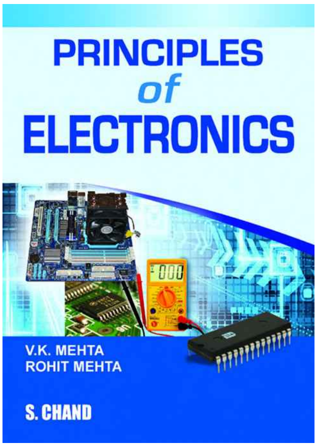


PRINCIPLES *of* ELECTRONICS

V.K. MEHTA
ROHIT MEHTA

S. CHAND

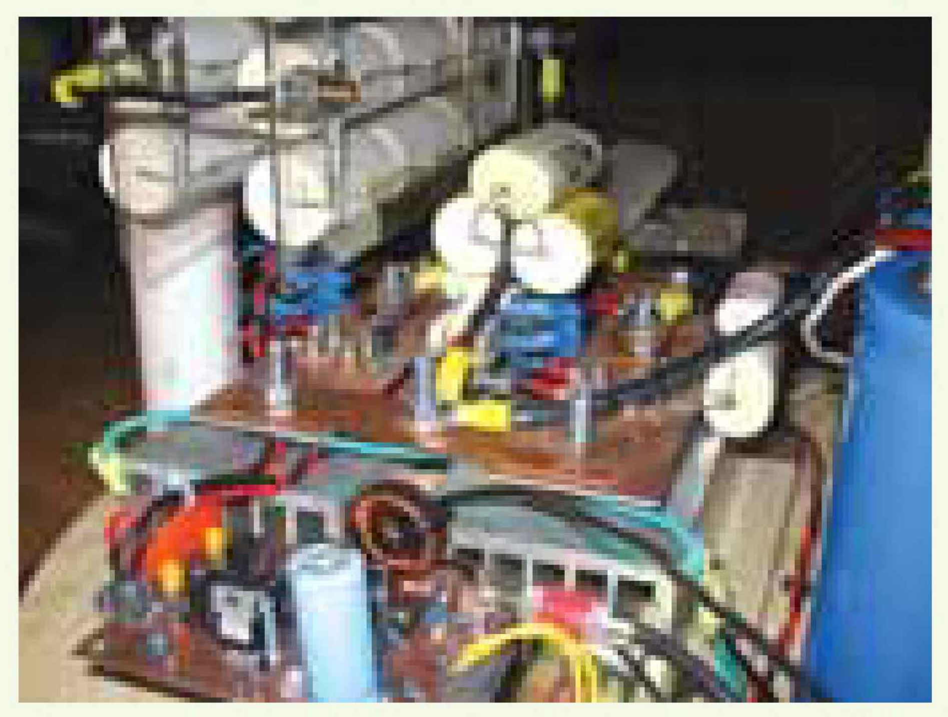
VISIT…

LANZAROTE

Caliente.COM

MULTICOLOUR REVISED EDITION

PRINCIPLES
OF
ELECTRONICS



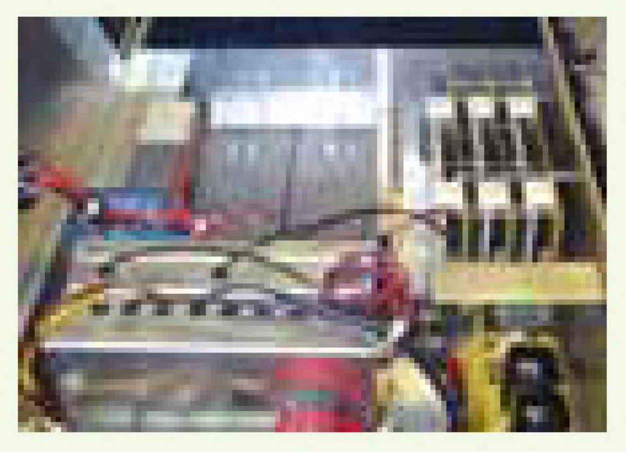
MULTICOLOUR REVISED EDITION

PRINCIPLES OF ELECTRONICS

(For B.E./ B.Tech & other Engg. Examinations)

FREE CD containing e-Book

V.K. MEHTA
ROHIT MEHTA



S. CHAND & COMPANY
RAM NAGAR, NEW DELHI-110 055

Sole Distributors :

S. CHAND & COMPANY LTD.

(An ISO 9001 : 2000 Company)

Head Office : 7361, RAM NAGAR, NEW DELHI - 110 055
Phones : 23672080-81-82, 9899107446, 9911310888; Fax : 91-11-23677446
Shop at: **schandgroup.com**; E-mail: **schand@vsnl.com**

Branches:

- 1st Floor, Heritage, Near Gujarat Vidhyapeeth, Ashram Road, **Ahmedabad**-380 014. Ph. 27541965, 27542369, ahmedabad@schandgroup.com
- No. 6, Ahuja Chambers, 1st Cross, Kumara Krupa Road, **Bangalore**-560 001. Ph : 22268048, 22354008, bangalore@schandgroup.com
- 238-A M.P. Nagar, Zone 1, **Bhopal** - 462 011. Ph : 4274723. bhopal@schandgroup.com
- 152, Anna Salai, **Chennai**-600 002. Ph : 28460026, chennai@schandgroup.com
- S.C.O. 2419-20, First Floor, Sector- 22-C (Near Aroma Hotel), **Chandigarh**-160022, Ph-2725443, 2725446, chandigarh@schandgroup.com
- 1st Floor, Bhartia Tower, Badambadi, **Cuttack**-753 009, Ph-2332580; 2332581, cuttack@schandgroup.com
- 1st Floor, 52-A, Rajpur Road, **Dehradun**-248 001. Ph : 2740889, 2740861, dehradun@schandgroup.com
- Pan Bazar, **Guwahati**-781 001. Ph : 2738811, guwahati@schandgroup.com
- Sultan Bazar, **Hyderabad**-500 195. Ph : 24651135, 24744815, hyderabad@schandgroup.com
- Mai Hiran Gate, **Jalandhar** - 144008 . Ph. 2401630, 5000630, jalandhar@schandgroup.com
- A-14 Janta Store Shopping Complex, University Marg, Bapu Nagar, **Jaipur** - 302 015, Phone : 2719126, jaipur@schandgroup.com
- 613-7, M.G. Road, Ernakulam, **Kochi**-682 035. Ph : 2378207, cochin@schandgroup.com
- 285/J, Bipin Bihari Ganguli Street, **Kolkata**-700 012. Ph : 22367459, 22373914, kolkata@schandgroup.com
- Mahabeer Market, 25 Gwynne Road, Aminabad, **Lucknow**-226 018. Ph : 2626801, 2284815, lucknow@schandgroup.com
- Blackie House, 103/5, Walchand Hirachand Marg , Opp. G.P.O., **Mumbai**-400 001. Ph : 22690881, 22610885, mumbai@schandgroup.com
- Karnal Bag, Model Mill Chowk, Umrer Road, **Nagpur**-440 032 Ph : 2723901, 2777666 nagpur@schandgroup.com
- 104, Citicentre Ashok, Govind Mitra Road, **Patna**-800 004. Ph : 2300489, 2302100, patna@schandgroup.com
- 291/1, Ganesh Gayatri Complex, 1st Floor, Somwarpeth, Near Jain Mandir, **Pune**-411011. Ph : 64017298, pune@schandgroup.com
- Flat No. 104, Sri Draupadi Smriti Apartment, East of Jaipal Singh Stadium, Neel Ratan Street, Upper Bazar, **Ranchi**-834001. Ph: 2208761, ranchi@schandgroup.com
- Kailash Residency, Plot No. 4B, Bottle House Road, Shankar Nagar, **Raipur**- Ph. 09981200834 raipur@schandgroup.com

© 1980, V.K. Mehta, Rohit Mehta

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior permission of the Publishers.

S. CHAND'S Seal of Trust

S. CHAND

In our endeavour to protect you against counterfeit/fake books we have put a Hologram Sticker on the cover of some of our fast moving titles. The hologram displays a unique 3D multi-level, multi-colour effect of our logo from different angles when tilted or properly illuminated under a single source of light.

Background artwork seems to be "under" or "behind" the logo, giving the illusion of depth. **A fake hologram does not give any illusion of depth.**

Multicolour edition conceptualized by R.K. Gupta, CMD

First Edition 1980
Subsequent Editions and Reprints 1981, 83, (Twice), 84, 85, (Twice), 86 (Twice), 87 (Twice), 1988 (Thrice), 89 (Twice), 90 (Twice), 91 (Twice), 92, 93 (Thrice), 94, 95 (Twice), 97, 1998 (Twice), 99, 2000, 2001 (Twice), 2002, 2003, 2004 (Twice), 2005, 2006, 2007
Thoroughly Revised Eleventh Edition 2008

ISBN : 81-219-2450-2
Code : 10A 297

PRINTED IN INDIA
By Rajendra Ravindra Printers (Pvt.) Ltd., 7361, Ram Nagar, New Delhi-110 055
and published by S. Chand & Company, 7361, Ram Nagar, New Delhi-110 055.

PREFACE TO THE ELEVENTH EDITION

The general response to the tenth edition of the book was very encouraging. Authors feel that their work has been amply rewarded and wish to express their deep sense of gratitude, in general to the large number of readers who have used it, and in particular to those of them who have sent helpful suggestions from time to time for the improvement of the book. The continuous feedback from the readers has helped the authors to make the book more useful.

The present edition has three notable features. First, the obsolete topics have been deleted to make way for fresh matter. Secondly, many new topics have been added and the present subject matter is strengthened. Thirdly, efforts have been made to make the book design oriented keeping in view the growing demand of the industry. It is hoped that these features will make the book more useful.

Authors wish to thank their colleagues and friends who have contributed many valuable suggestions regarding the scope and content-sequence of the book. Authors are also indebted to M/S S.Chand & Company Ltd., New Delhi for bringing out this revised edition in a short time and pricing the book moderately inspite of heavy cost of paper and printing.

Errors might have crept in despite utmost care to avoid them. Authors shall be grateful if these are pointed out along with other suggestions for the improvement of the book.

V.K. MEHTA
ROHIT MEHTA

CONTENTS

1. Introduction 1—27

Electronics–Atomic structure–Structure of elements–The electron–Energy of an electron–Valence electrons–Free electrons–Voltage source–Constant voltage source–Constant current source–Conversion of voltage source into current source–Maximum power transfer theorem–Thevenin's theorem–Procedure for finding thevenin equivalent circuit–Norton's theorem–Procedure for finding norton equivalent circuit– Chassis and ground.

2. Electron Emission 28—37

Electron emission–Types of electron emission–Thermionic emission–Thermionic emitter–Commonly used thermionic emitters–Cathode construction–Field emission–Secondary emission–Photo electric emission.

3. Gas-Filled Tubes 38—47

Gas-filled tubes–Conduction in a gas–Cold-cathode gas diode–Characteristics of cold-cathode diode–Applications of glow tubes–Hot-cathode gas diode–Thyratron–Applications of Thyratron.

4. Atomic Structure 48—54

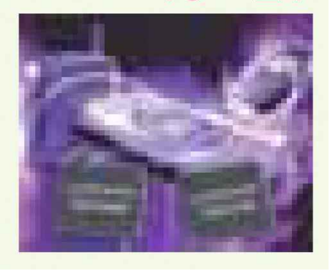
Bohr's atomic model–Energy levels–Energy bands–Important energy bands in solids– Classification of solids and energy bands– Silicon.

5. Semiconductor Physics 55—75

Semiconductor–Bonds in semiconductors–Crystals–Commonly used semiconductors –Energy band description of semiconductors–Effect of temperature on semiconductors–Hole current–Intrinsic semiconductor–Extrinsic semiconductor–*n*-type semiconductor–*p*-type semiconductor–Charge on *n*-type and *p*-type semiconductors– Majority and minority carriers–*pn*-junction–Properties of *pn*-junction–Applying D.C. voltage across–*pn* junction–Volt-ampere characteristics of *pn*-junction–Important terms–Limitations in the operating conditions of *pn*-junction.

6. Semiconductor Diode 76—124

Semiconductor diode–Crystal diode as a rectifier–Resistance of crystal Diode–Equivalent circuit of crystal diode–Crystal diode equivalent circuits–Important terms–Crystal diode rectifiers–Half-wave rectifier–Output frequency of Half-wave rectifier–Efficiency of half-wave rectifier–Full-wave rectifier–Centre-tap full-wave rectifier–Full-wave bridge rectifier–Output frequency of full-wave rectifier–Efficiency of full-wave rectifier–Faults in centre-tap full-wave rectifier–Nature of rectifier output–Ripple factor–Comparison of rectifiers–Filter circuits–Types of filter circuits–Voltage multipliers–Half-wave voltage doubler–Voltage stabilisation–Zener diode–Equivalent circuit of zener diode–Zener diode as voltage stabiliser–Solving zener diode circuits–Crystal diodes versus vacuum-diodes.



7. Special-Purpose Diodes 125—140

Zener diode–Light-emitting diode (LED)–LED voltage and current–Advantages of LED–Multicolour LEDs–Applications of LEDs–Photo-diode–Photo-diode operation–Characteristics of photo-diode–Applications of Photo-diodes–Optoisolator–Tunnel diode–Tunnel diode oscillator–Varactor diode–Application of varactor diode–Shockley diode.

8. Transistors 141—191

Transistor–Naming the transistor terminals–Some facts about the transistor–Transistor action–Transistor symbols–Transistor as an amplifier–Transistor connections–Common base connection–Characteristics of common base connection–Common emitter connection–Measurement of leakage current–Characteristics of common emitter connection–Common collector connection–Comparison of transistor connections–Commonly used transistor connection–Transistor as an amplifier in CE arrangement–Transistor load line analysis–Operating point–Practical way of drawing –CE circuit–Output from transistor amplifier–Performance of transistor amplifier–Cut off and saturation points–Power rating of transistor–Determination of transistor configuration–Semiconductor devices numbering system–Transistor lead identification–Transistor testing–Applications of common base amplifiers–Transistors versus vacuum tubes.

9. Transistor Biasing 192—239

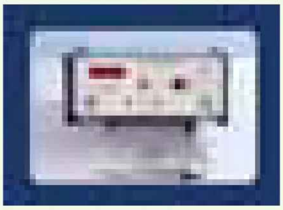
Faithful amplification–Transistor biasing–Inherent variations of transistor parameters–Stabilisation–Essentials of a transistor biasing circuit–Stability factor–Methods of transistor biasing–Base resistor method–Emitter bias circuit–Circuit analysis of emitter bias–Biasing with collector feedback resistor-Voltage divider bias method–Stability factor for potential divider bias–Design of transistor biasing circuits–Mid-point biasing–Which value of β to be used–Miscellaneous bias circuits –Silicon versus germanium–Instantaneous current and voltage waveforms—Summary of transistor bias circuits.

10. Single Stage Transistor Amplifiers 240—279

Single stage transistor amplifier–How transistor amplifies? –Graphical demonstration of transistor amplifier–Practical circuit of transistor amplifier–Phase reversal–Input/output phase relationships–D.C. and A.C. equivalent circuits–Load line analysis–Voltage gain–A.C. emitter resistance–Formula for A.C. emitter resistance–Voltage gain of CE amplifier–Voltage gain of unloaded CE amplifier–Voltage gain of CE amplifier without C_E–Input impedance of CE amplifier–Voltage gain stability–Swamped Amplifier–Classification of amplifiers–Amplifier equivalent circuit–Equivalent circuit with signal source–Gain and transistor configurations.

11. Multistage Transistor Amplifiers 280—305

Multistage transistor amplifier–Role of capacitors in transistor amplifiers–Important terms–Properties of db gain–R.C. coupled transistor amplifier–Transformer coupled amplifiers–Direct-coupled amplifier–Comparison of different types of coupling–Difference between transistor and tube amplifiers.



12. Transistor Audio Power Amplifiers 306—334

Transistor audio power amplifier–Small-signal and large-signal amplifiers–Output power of amplifier–Difference between voltage and power amplifiers–Performance quantities of power amplifiers–Classification of power amplifiers–Expression for collector efficiency–Maximum collector efficiency for series-fed class A amplifier–Maximum collector efficiency of transformer coupled class A power amplifier–Important points about class A power amplifier–Thermal runaway–Heat sink–Mathematical analysis–Stages of a practical power amplifier–Driver stage–Output stage–Push pull amplifier–Maximum efficiency for class B operation–Complementary-symmetry amplifier.

13. Amplifiers With Negative Feedback 335—363

Feedback–Principles of negative voltage feedback in amplifiers–Gain of negative voltage feedback amplifier–Advantages of negative voltage feedback–Feedback circuit–Principles of negative current feedback–Current gain with negative current feedback–Effects of negative current feedback–Emitter follower–D.C. analysis of emitter follower–Voltage gain of emitter follower–Input impedance of emitter follower–Output impedance of emitter follower– Applications of emitter follower–Darlington amplifier.

14. Sinusoidal Oscillators 364—388

Sinusoidal oscillator–Types of sinusoidal oscillations–Oscillatory circuit–Undamped oscillations from tank circuit–Positive feedback amplifier–Oscillator–Essentials of transistor oscillator–Explanation of barkhausen criterion–Different types of transistor oscillators–Tuned collector oscillator–Colpitt's

oscillators–Hartley oscillator–Principles of phase shift oscillators–Phase shift oscillator–Wien bridge oscillator –Limitations of LC and RC oscillators–Piezoelectric crystals–Working of quartz crystal–Equivalent circuit of crystal–Frequency response of crystal–Transistor crystal oscillator.

15. Transistor Tuned Amplifiers 389—410

Tuned amplifiers–Distinction between tuned amplifiers and other amplifiers–Analysis of paralled tuned circuit–Characteristics of parallel resonant circuit–Advantages of tuned amplifiers–Why not tuned amplifiers for low frequency amplification?–Frequency response of tuned amplifier–Relation between Q and bandwidth–Single tuned amplifier–Analysis of tuned amplifier–A.C. equivalent circuit of tuned amplifier–Double tuned amplifier–Bandwidth of double-tuned amplifier–Practical application of double tuned amplifier–Tuned class C amplifier–Class C operation–D.C. and A.C. loads–Maximum A.C. output power.

16. Modulation And Demodulation 411—441

Radio broadcasting, transmission and reception–Modulation–Types of modulation–Amplitude modulation–Modulation factor–Analysis of amplitude modulated wave–Sideband frequencies in AM wave–Transistor AM modulator–Power in AM wave-Limitations of amplitude modulation–Frequency modulation–Theory of frequency modulation–Comparison of FM and AM– Demodulation–Essentials in demodulation–A.M. diode detector–A.M. radio receivers–Types of A.M. radio receivers–Stages of superhetrodyne radio receiver–Advantages of superhetrodyne circuit–FM receiver–Difference between FM and AM receivers.

17. Regulated D.C. Power Supply 442–467

Ordinary D.C. power supply–Important terms–Regulated power supply–Types of voltage regulators–Zener diode voltage regulator–Condition for proper operation of zener regulator–Transistor series voltage regulator–Series feedback voltage regulator–Short-circuit protection–Transistor shunt voltage regulator–Shunt feedback voltage regulator–Glow-tube voltage regulator–Series triode voltage regulator–Series double triode voltage regulator–IC voltage regulators–Fixed positive voltage regulators–Fixed negative voltage regulators–Adjustable voltage regulators–Dual-tracking voltage regulators.

18. Solid-State Switching Circuits 468—505

Switching circuit–Switch–Mechanical switch–Electromechanical switch or relay–Electronic switches–Advantages of electronic switches–Important terms–Switching transistors–Switching action of a transistor–Multivibrators–Types of multivibrators–Transistor astable multivibrator–Transistor monostable multivibrator–Transistor bistable multivibrator–Differentiating circuit–Integrating circuit–Important applications of diodes–Clipping circuits–Applications of clippers–Clamping circuits–Basic idea of a clamper–Positive clamper–Negative clamper.

19. Field Effect Transistors 506—553

Types of field effect transistors–Junction field effect transistor (JFET)–Principle and working of JFET–Schematic symbol of JFET–Importance of JFET–Difference between JFET and bipolar transistor–JFET as an amplifier–Output characteristics of JFET–Salient features of of JFET–Important terms–Expression for drain current–Advantages of JFET–Parameters of JFET–Relation among JFET parameters–Variation of transconductance (g_m or g_{fs}) of JFET–JFET biasing–JFET biasing by bias battery–Self-bias for JFET–JFET with voltage-divider bias–JFET connections–Practical JFET amplifier–D.C. and A.C. equivalent circuits of JFET–D.C. load line analysis–Voltage gain of JFET amplifier (with source resistance R_S)–JFET applications–Metal oxide semiconductor FET (MOSFET)–Types of MOSFET–Symbols for D-MOSFET–Circuit operation of D-MOSFET–D-MOSFET transfer characteristic–Transconductance and input impedance of D-MOSFET–D-MOSFET biasing–Common source D-MOSFET amplifier–D-MOSFETs versus JFETs–E-MOSFET–E-MOSFET biasing circuits–D-MOSFETs versus E-MOSFETs.

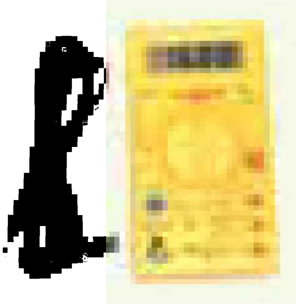
20. Silicon Controlled Rectifiers 554—576

Silicon Controlled rectifier (SCR)–Working of SCR–Equivalent circuit of SCR-V-I characteristics of SCR–SCR in normal operation–SCR as a switch–SCR switching–SCR half-wave rectifier–SCR full-wave rectifier–Single-phase SCR inverter circuit–Applications of SCR-Light-activated SCR.

21. Power Electronics 577—600

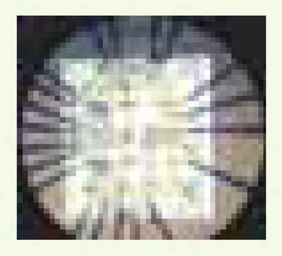
Power electronics–The triac–Triac construction–SCR equivalent circuit of triac–Triac operation–Triac phase control circuit–Applications of triac–The Diac–Applications of diac–Unijunction transistor (UJT)–Equivalent circuit of a UJT–Characteristics of UJT–Advantages of UJT–Applications of UJT.

22. Electronic Instruments 601–626



Electronic instruments–Multimeter–Applications of multimeter–Sensitivity of multimeter–Merits and demerits of multimeter–Meter protection–Electronic voltmeters–Vacuum tube voltmeter (VTVM)–Applications of VTVM–Merits and demerits of VTVM–Transistor voltmeter circuit–Bridge rectifier voltmeter–Cathode ray oscilloscope–Cathode ray tube–Deflection sensitivity of CRT–Applying signal across vertical plates–Display of signal waveform on CRO–Signal pattern on screen–Various controls of CRO–Applications of CRO.

23. Integrated Circuits 627–641



Integrated circuits–Advantages and disadvantages of integrated circuits–Inside an IC package–IC classifications–Making monolithic IC–Fabrication of components on monolithic IC–Simple monolithic ICs–IC packings–IC symbols–Scale of integration–Some circuits using ICs.

24. Hybrid Parameters 642—661

Hybrid parameters–Determination of *h* parameters–*h* parameter equivalent circuit–Performance of a linear circuit in *h* parameters–The *h* parameters of a transistor–Nomenclature for transistor *h* parameters–Transistor circuit performance in *h* parameters–Approximate hybrid formulas for transistor amplifier–Experimental determination of transistor *h* parameters–Limitations of *h* parameters.

25. Operational Amplifiers 662—728

Operational amplifier–Differential amplifier (DA)–Basic circuit of differential amplifier–Operation of differential amplifier–Common-mode and differential-mode signals–Double-ended input operation of DA–Voltage gains of DA–Common-mode rejection ratio (CMRR)–D.C. analysis of differential amplifier (DA)–Overview of differential amplifier–Parameters of DA (or OP-amp) due to mismatch of transistors–Input bias current–A.C. analysis of differential amplifier–Common-mode voltage gain–Operational amplifier (OP-amp)–Schematic symbol of operational amplifier–Output voltage from OP-amp–A.C. analysis of OP-amp–Bandwidth of an OP-amp–Slew rate–Frequency response of an OP-amp– OP-amp with negative feedback–Applications of OP-amp–Inverting amplifier–Input and output impedance of inverting amplifier–Noninverting amplifier–Voltage follower–Multistage OP-amp circuits–Effect of negative feedback on OP-amp impedances–Faults in feedback circuits–Summary of OP-amp configurations–Summing amplifiers–Applications of summing amplifiers–OP-amp integrators and differentiators–OP-amp integrator–Critical frequency of integrators–OP-amp differentiator–Comparators–Comparator circuits.

26. Digital Electronics 729—773

Analog and digital signals–Digital circuit–Binary number system–Place value–Decimal to binary conversion–Binary to decimal conversion–Octal number system–Hexadecimal number system–Binary-coded decimal code (BCD code)–Logic gates–Three basic logic gates–OR gate–AND gate–NOT gate or inverter–Combination of basic logic gates–NAND gate as a universal gate-Exclusive OR gate–Encoders and decoders–Advantages and disadvantages of digital electronics–Boolean algebra–Boolean theorems–DeMorgan's theorems–Operator precedence–Combinational logic circuits–Boolean expressions for combinational logic circuits–AND and OR operations in Boolean expression–Truth table from logic circuit–Developing logic circuit from its Boolean expression–Sum-of-products form–Simplification of Boolean expressions–Binary addition–Electronic adders–Flip-flops.

Index 775—778

1

Introduction

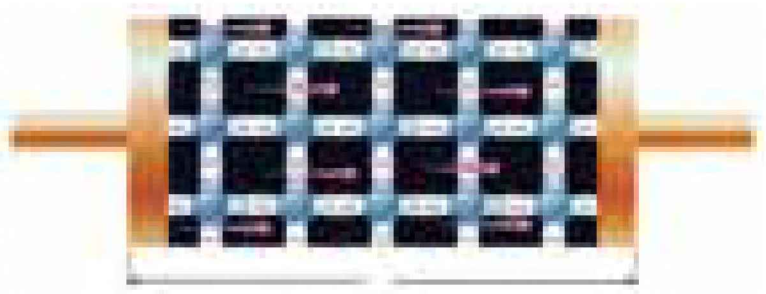
1.1 Electronics
1.2 Atomic Structure
1.3 Structure of Elements
1.4 The Electron
1.5 Energy of an Electron
1.6 Valence Electrons
1.7 Free Electrons
1.8 Voltage Source
1.9 Constant Voltage Source
1.10 Constant Current Source
1.11 Conversion of Voltage Source into Current Source
1.12 Maximum Power Transfer Theorem
1.13 Thevenin's Theorem
1.14 Procedure for Finding Thevenin Equivalent Circuit
1.15 Norton's Theorem
1.16 Procedure for Finding Norton Equivalent Circuit
1.17 Chassis and Ground

GENERAL

In this fast developing society, *electronics* has come to stay as the most important branch of engineering. Electronic devices are being used in almost all the industries for quality control and automation and they are fast replacing the present vast army of workers engaged in processing and assembling in the factories. Great strides taken in the industrial applications of electronics during the recent years have demonstrated that this versatile tool can be of great importance in increasing production, efficiency and control.

The rapid growth of electronic technology offers a formidable challenge to the beginner, who may be almost paralysed by the mass of details. However, the mastery of fundamentals can simplify the learning process to a great extent. The purpose of this chapter is to present the elementary knowledge in order to enable the readers to follow the subsequent chapters.

1.1 Electronics



Current conduction through semiconductor

The branch of engineering which deals with current conduction through a vacuum or gas or semiconductor is known as ***electronics.**

Electronics essentially deals with electronic devices and their utilisation. An *electronic device* is that in which current flows through a vacuum or gas or semiconductor. Such devices have valuable properties which enable them to function and behave as the friend of man today.

Importance. Electronics has gained much importance due to its numerous applications in industry. The electronic devices are capable of performing the following functions :

(*i*) **Rectification.** The conversion of a.c. into d.c. is called *rectification*. Electronic devices can convert a.c. power into d.c. power (See Fig. 1.1) with very high efficiency. This d.c. supply can be used for charging storage batteries, field supply of d.c. generators, electroplating etc.

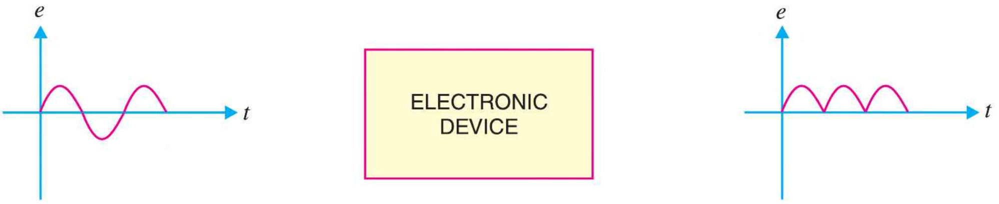


Fig. 1.1

(*ii*) **Amplification.** The process of raising the strength of a weak signal is known as *amplification*. Electronic devices can accomplish the job of amplification and thus act as amplifiers (See Fig. 1.2). The amplifiers are used in a wide variety of ways. For example, an amplifier is used in a radio-set where the weak signal is amplified so that it can be heard loudly. Similarly, amplifiers are used in public address system, television etc.

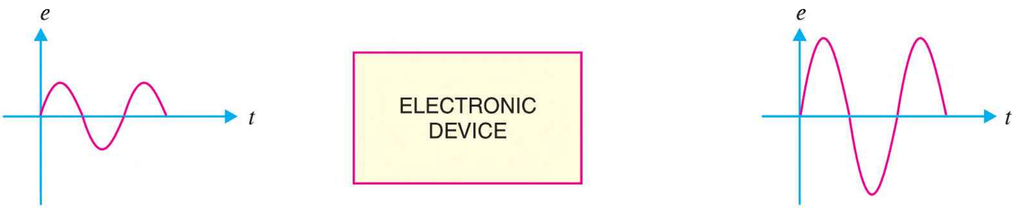


Fig. 1.2

(*iii*) **Control.** Electronic devices find wide applications in automatic control. For example, speed of a motor, voltage across a refrigerator etc. can be automatically controlled with the help of such devices.

(*iv*) **Generation.** Electronic devices can convert d.c. power into a.c. power of any frequency (See Fig. 1.3). When performing this function, they are known as *oscillators*. The oscillators are used in a wide variety of ways. For example, electronic high frequency heating is used for annealing and hardening.

---

* The word *electronics* derives its name from electron present in all materials.

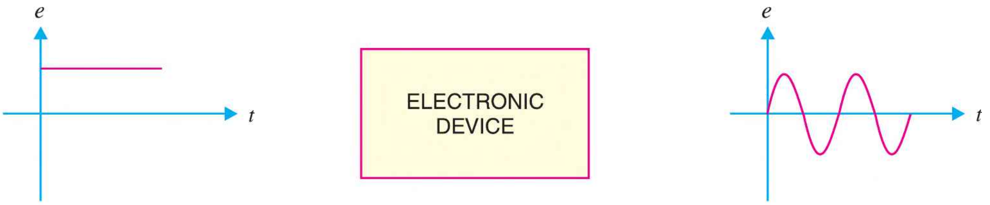
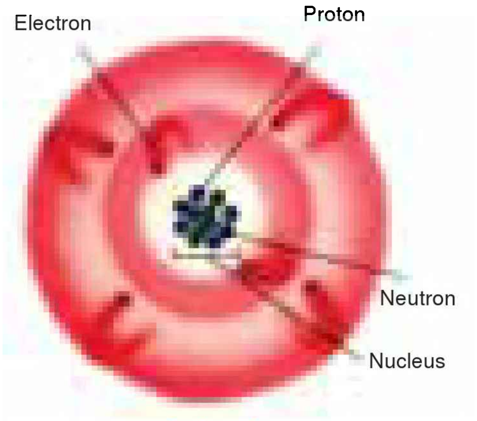


Fig. 1.3

(*v*) Conversion of light into electricity. Electronic devices can convert light into electricity. This conversion of light into electricity is known as *photo-electricity*. Photo-electric devices are used in Burglar alarms, sound recording on motion pictures *etc.*

(*vi*) Conversion of electricity into light. Electronic devices can convert electricity into light. This valuable property is utilised in television and radar.



Carbon Atom

1.2 Atomic Structure

According to the modern theory, matter is electrical in nature. All the materials are composed of very small particles called *atoms*. The atoms are the building bricks of all matter. An atom consists of a central *nucleus* of positive charge around which small negatively charged particles, called *electrons* revolve in different paths or orbits.

(1) Nucleus. It is the central part of an atom and *contains *protons* and *neutrons*. A proton is a positively charged particle, while the neutron has the same mass as the proton, but has no charge. Therefore, the nucleus of an atom is positively charged. The sum of protons and neutrons constitutes the entire weight of an atom and is called atomic weight. It is because the particles in the extra nucleus (*i.e.* electrons) have negligible weight as compared to protons or neutrons.

$$\therefore \quad \text{atomic weight} = \text{no. of protons} + \text{no. of neutrons}$$

(2) Extra nucleus. It is the outer part of an atom and contains *electrons* only. An electron is a negatively charged particle having negligible mass. The charge on an electron is equal but opposite to that on a proton. Also, the number of electrons is equal to the number of protons in an atom under ordinary conditions. Therefore, an atom is neutral as a whole. The number of electrons or protons in an atom is called *atomic number i.e.*

$$\text{atomic number} = \text{no. of protons or electrons in an atom}$$

The electrons in an atom revolve around the nucleus in different orbits or paths. The number and arrangement of electrons in any orbit is determined by the following rules :

(*i*) The number of electrons in any orbit is given by $2n^2$ where n is the number of the orbit. For example,

First orbit contains $2 \times 1^2 = 2$ electrons

Second orbit contains $2 \times 2^2 = 8$ electrons

Third orbit contains $2 \times 3^2 = 18$ electrons and so on.

---

* Although the nucleus of an atom is of complex structure, yet for the purpose of understanding electronics, this simplified picture of the nucleus is adequate.

(*ii*) The last orbit cannot have more than 8 electrons.

(*iii*) The last but one orbit cannot have more than 18 electrons.

1.3 Structure of Elements

We have seen that all atoms are made up of protons, neutrons and electrons. The difference between various types of elements is due to the different number and arrangement of these particles within their atoms. For example, the structure* of copper atom is different from that of carbon atom and hence the two elements have different properties.

The atomic structure can be easily built up if we know the atomic weight and atomic number of the element. Thus taking the case of copper atom,

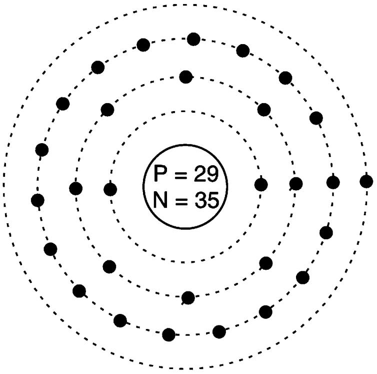
Atomic weight = 64

Atomic number = 29

∴ No. of protons = No. of electrons = 29

and No. of neutrons = 64 − 29 = 35

Fig. 1.4 shows the structure of copper atom. It has 29 electrons which are arranged in different orbits as follows. The first orbit will have 2 electrons, the second 8 electrons, the third 18 electrons and the fourth orbit will have 1 electron. The atomic structure of all known elements can be shown in this way and the reader is advised to try for a few commonly used elements.



COPPER

Fig. 1.4

1.4 The Electron

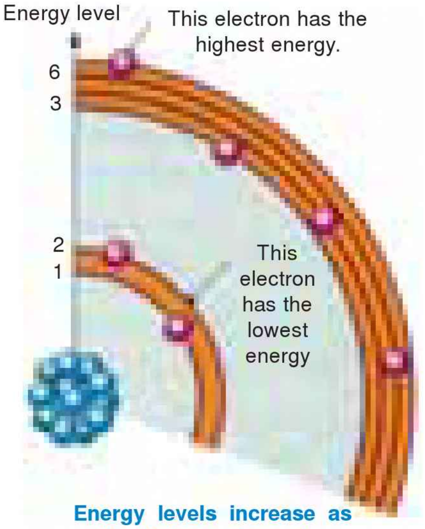
Since electronics deals with tiny particles called electrons, these small particles require detailed study. As discussed before, an electron is a negatively charged particle having negligible mass. Some of the important properties of an electron are :

(*i*) Charge on an electron, *e* = 1.602×10^{-19} coulomb

(*ii*) Mass of an electron, *m* = 9.0×10^{-31} kg

(*iii*) Radius of an electron, *r* = 1.9×10^{-15} metre

The ratio *e/m* of an electron is 1.77×10^{11} coulombs/kg. This means that mass of an electron is very small as compared to its charge. It is due to this property of an electron that it is very mobile and is greatly influenced by electric or magnetic fields.


Energy level
This electron has the highest energy.
6
3
2
1
This electron has the lowest energy

Energy levels increase as the distance from the nucleus increases

1.5 Energy of an Electron

An electron moving around the nucleus possesses two types of energies viz. kinetic energy due to its motion and potential energy due to the charge on the nucleus. The total energy of the electron is the sum of these two energies. The energy of an electron increases as its distance from the nucleus increases. Thus, an electron in the second orbit possesses more energy than the electron in the first orbit; electron in the third orbit has higher energy than in the second orbit.It is clear that electrons in the last orbit possess very high energy as compared to the electrons in the inner orbits. These last orbit electrons play an important role in determining the physical, chemical and electrical properties of a material.

---

* The number and arrangement of protons, neutrons and electrons.

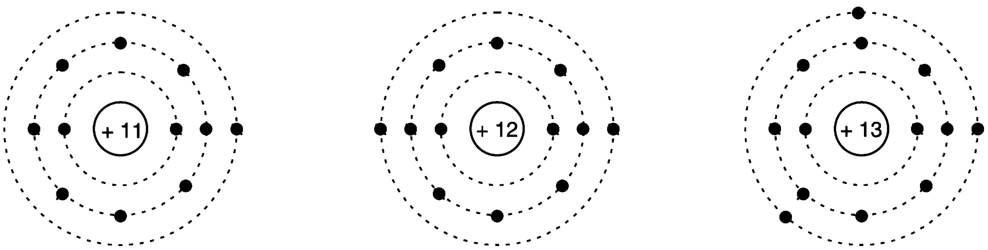
1.6 Valence Electrons

The electrons in the outermost orbit of an atom are known as **valence electrons.**

The outermost orbit can have a maximum of 8 electrons *i.e.* the maximum number of valence electrons can be 8. The valence electrons determine the physical and chemical properties of a material. These electrons determine whether or not the material is chemically active; metal or non-metal or, a gas or solid. These electrons also determine the electrical properties of a material.

On the basis of electrical conductivity, materials are generally classified into *conductors, insulators* and *semi-conductors.* As a rough rule, one can determine the electrical behaviour of a material from the number of valence electrons as under :

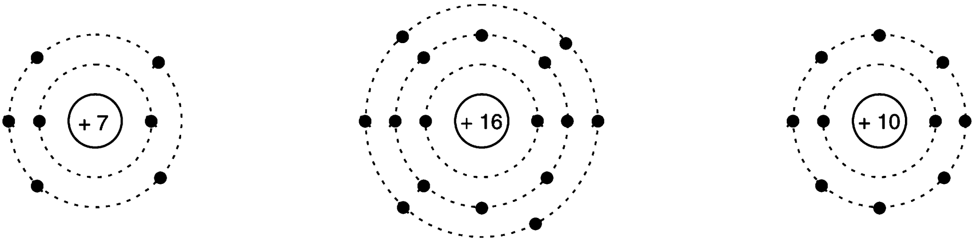
(*i*) When the number of valence electrons of an atom is less than 4 (*i.e.* half of the maximum eight electrons), the material is usually *a metal and a conductor.* Examples are sodium, magnesium and aluminium which have 1, 2 and 3 valence electrons respectively (See Fig. 1.5).



SODIUM (*i*) MAGNESIUM (*ii*) ALUMINIUM (*iii*)

Fig. 1.5

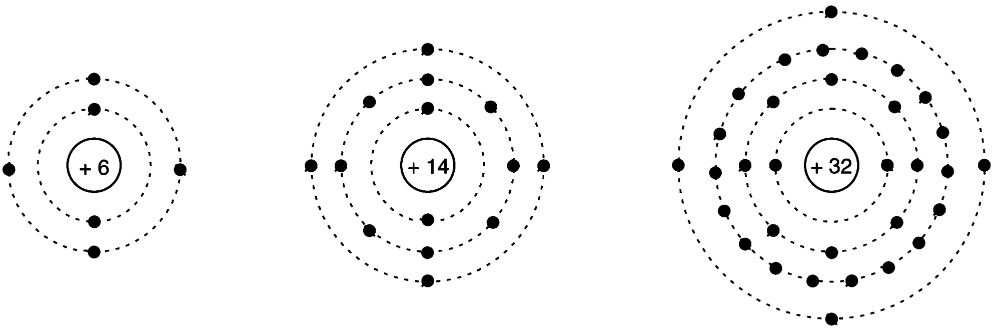
(*ii*) When the number of valence electrons of an atom is more than 4, the material is usually *a non-metal and an insulator.* Examples are nitrogen, sulphur and neon which have 5, 6 and 8 valence electrons respectively (See Fig. 1.6).



NITROGEN (*i*) SULPHUR (*ii*) NEON (*iii*)

Fig. 1.6

(*iii*) When the number of valence electrons of an atom is 4 (*i.e.* exactly one-half of the maximum 8 electrons), the material has both metal and non-metal properties and is usually a *semi-conductor.* Examples are carbon, silicon and germanium (See Fig. 1.7).



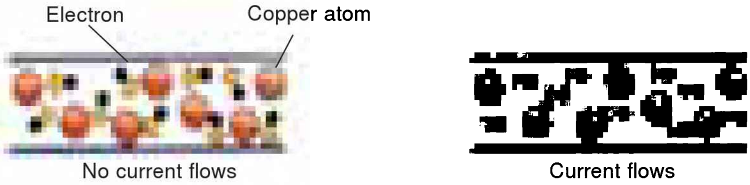
CARBON (*i*) SILICON (*ii*) GERMANIUM (*iii*)

Fig. 1.7

1.7 Free Electrons

The valence electrons of different materials possess different energies. The greater the energy of a valence electron, the lesser it is bound to the nucleus. In certain substances, particularly metals, the valence electrons possess so much energy that they are very loosely attached to the nucleus. These loosely attached valence electrons move at random within the material and are called *free electrons.*

The valence electrons which are very loosely attached to the nucleus are known as **free electrons.**



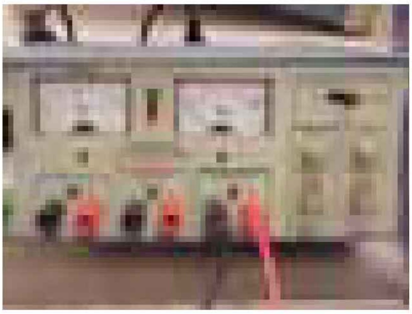
Current moves through materials that conduct electricity.

The free electrons can be easily removed or detached by applying a small amount of external energy. As a matter of fact, these are the free electrons which determine the electrical conductivity of a material. On this basis, conductors, insulators and semiconductors can be defined as under :

(*i*) A *conductor* is a substance which has a large number of free electrons. When potential difference is applied across a conductor, the free electrons move towards the positive terminal of supply, constituting electric current.

(*ii*) An *insulator* is a substance which has practically no free electrons at ordinary temperature. Therefore, an insulator does not conduct current under the influence of potential difference.

(*iii*) A *semiconductor* is a substance which has very few free electrons at room temperature. Consequently, under the influence of potential difference, a semiconductor *practically* conducts no current.

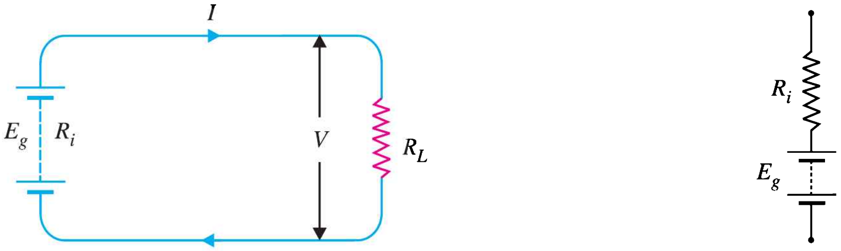


Voltage source

1.8 Voltage Source

Any device that produces voltage output continuously is known as a *voltage source*. There are two types of voltage sources, namely ; direct voltage source and alternating voltage source.

(*i*) **Direct voltage source.** A device which produces direct voltage output continuously is called *a direct voltage source.* Common examples are cells and d.c. generators. An important characteristic of a direct voltage source is that it maintains the same polarity of the output voltage *i.e.* positive and negative terminals remain the same. When load resistance R_L is connected across such a source,*current flows from positive terminal to negative terminal *via* the load [See Fig. 1.8 (*i*)]. This is called *direct current* because it has just one direction. The current has one direction as the source maintains the same polarity of output voltage. The opposition to load current inside the d.c. source is known as *internal resistance* R_i. The equivalent circuit of a d.c. source is the generated *e.m.f.* E_g in series with internal resistance R_i of the source as shown in Fig. 1.8 (*ii*). Referring to Fig. 1.8 (*i*), it is clear that:



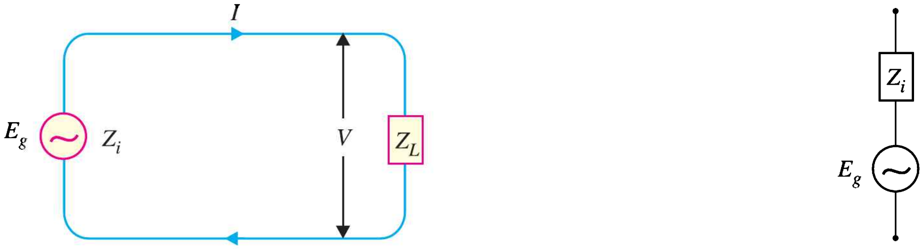
(*i*) (*ii*)

Fig. 1.8

$$\text{Load current, } I = \frac{E_g}{R_L + R_i}$$

$$\text{Terminal voltage, } V = (E_g - I R_i) \quad \text{or} \quad I R_L$$

(*ii*) Alternating voltage source. A device which produces alternating voltage output continuously is known as *alternating voltage source e.g.* a.c. generator. An important characteristic of alternating voltage source is that it periodically reverses the polarity of the output voltage. When load impedance Z_L is connected across such a source, current flows through the circuit that periodically reverses in direction. This is called *alternating current.*



(*i*) (*ii*)

Fig. 1.9

The opposition to load current inside the a.c. source is called its *internal impedance* Z_i. The equivalent circuit of an a.c. source is the generated *e.m.f.* E_g (*r.m.s.*) in series with internal impedance Z_i of the source as shown in Fig. 1.9 (*ii*). Referring to Fig. 1.9 (*i*), it is clear that :

$$\text{Load current, } I\ (r.m.s.) = \frac{E_g}{Z_L + Z_i}$$

$$\text{Terminal voltage, } V = (E_g - I Z_i)^{**} \quad \text{or} \quad I Z_L$$

---

* This is the conventional current. However, the flow of electrons will be in the opposite direction.

** Vector difference since a.c. quantities are vector quantities.

1.9 Constant Voltage Source

*A voltage source which has very low internal *impedance as compared with external load impedance is known as a* **constant voltage source.**

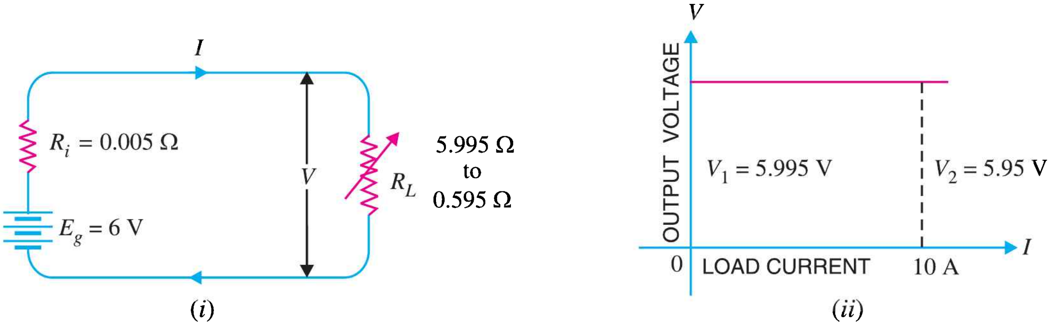


Fig. 1.10

In such a case, the output voltage nearly remains the same when load current changes. Fig. 1.10 (*i*) illustrates a constant voltage source. It is a d.c. source of 6 V with internal resistance $R_i = 0.005\ \Omega$. If the load current varies over a wide range of 1 to 10 A, for any of these values, the internal drop across R_i (= 0.005 Ω) is less than 0.05 volt. Therefore, the voltage output of the source is between 5.995 to 5.95 volts. This can be considered constant voltage compared with the wide variations in load current.

Fig. 1.10 (*ii*) shows the graph for a constant voltage source. It may be seen that the output voltage remains constant inspite of the changes in load current. Thus as the load current changes from 0 to 10 A, the output voltage essentially remains the same (*i.e.* $V_1 = V_2$). A constant voltage source is represented as shown in Fig. 1.11.

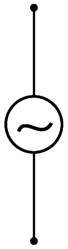


Fig. 1.11

Example 1.1. *A lead acid battery fitted in a truck develops 24V and has an internal resistance of 0.01 Ω. It is used to supply current to head lights etc. If the total load is equal to 100 watts, find :*

(i) voltage drop in internal resistance

(ii) terminal voltage

Solution.

$$\text{Generated voltage, } E_g = 24 \text{ V}$$

$$\text{Internal resistance, } R_i = 0.01\ \Omega$$

$$\text{Power supplied, } P = 100 \text{ watts}$$

(*i*) Let *I* be the load current.

Now $P = E_g \times I$ ($\because$ For an ideal source, $V \simeq E_g$)

$$\therefore \quad I = \frac{P}{E_g} = \frac{100}{24} = 4.17 \text{ A}$$

$$\therefore \quad \text{Voltage drop in } R_i = I R_i = 4.17 \times 0.01 = \mathbf{0.0417\ V}$$

$$(ii) \quad \text{Terminal Voltage, } V = E_g - I R_i$$

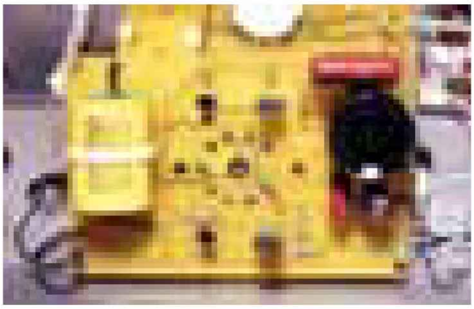
$$= 24 - 0.0417 = \mathbf{23.96\ V}$$

---

* resistance in case of a d.c. source.

Comments **:** It is clear from the above example that when internal resistance of the source is quite small, the voltage drop in internal resistance is very low. Therefore, the terminal voltage substantially remains constant and the source behaves as a constant voltage source irrespective of load current variations.

1.10 Constant Current Source

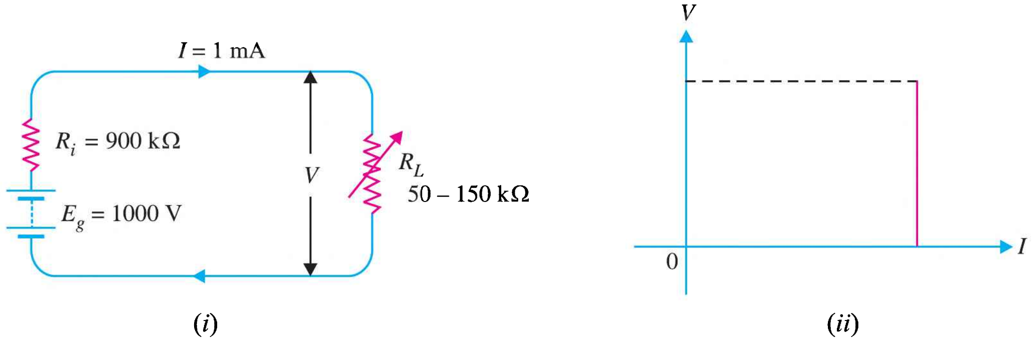


Constant Current Source

*A voltage source that has a very high internal *impedance as compared with external load impedance is considered as a* **constant current source.**

In such a case, the load current nearly remains the same when the output voltage changes. Fig. 1.12 (*i*) illustrates a constant current source. It is a d.c. source of 1000 V with internal resistance R_i = 900 kΩ. Here, load R_L varies over 3 : 1 range from 50 k Ω to 150 k Ω. Over this variation of load R_L, the circuit current I is essentially constant at 1.05 to 0.95 mA or approximately 1 mA. It may be noted that output voltage V varies approximately in the same 3 : 1 range as R_L, although load current essentially remains **constant at 1mA. The beautiful example of a constant current source is found in vacuum tube circuits where the tube acts as a generator having internal resistance as high as 1 MΩ.

Fig. 1.12 (*ii*) shows the graph of a constant current source. It is clear that current remains constant even when the output voltage changes substantially. The following points may be noted regarding the constant current source :



(*i*) (*ii*)

Fig. 1.12

(*i*) Due to high internal resistance of the source, the load current remains essentially constant as the load R_L is varied.

(*ii*) The output voltage varies approximately in the same range as R_L, although current remains constant.

(*iii*) The output voltage V is much less than the generated voltage E_g because of high $I R_i$ drop.

Fig. 1.13 shows the symbol of a constant current source.

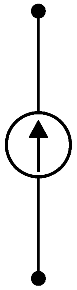


Fig. 1.13

---

* Resistance in case of a d.c. source

** Now $I = \dfrac{E_g}{R_L + R_i}$. Since $R_i >> R_L$, $I = \dfrac{E_g}{R_i}$

As both E_g and R_i are constants, I is constant.

Example 1.2. *A d.c. source generating 500 V has an internal resistance of 1000 Ω. Find the load current if load resistance is (i) 10 Ω (ii) 50 Ω and (iii) 100 Ω.*

Solution.

Generated voltage, $E_g = 500$ V

Internal resistance, $R_i = 1000\ \Omega$

(*i*) When $R_L = 10\ \Omega$

$$\text{Load current, } I = \frac{E_g}{R_L + R_i} = \frac{500}{10 + 1000} = \mathbf{0.495\ A}$$

(*ii*) When $R_L = 50\ \Omega$

$$\text{Load current, } I = \frac{500}{50 + 1000} = \mathbf{0.476\ A}$$

(*iii*) When $R_L = 100\ \Omega$

$$\text{Load current, } I = \frac{500}{100 + 1000} = \mathbf{0.454\ A}$$

It is clear from the above example that load current is essentially constant since $R_i >> R_L$.

1.11 Conversion of Voltage Source into Current Source

Fig. 1.14 shows a constant voltage source with voltage *V* and internal resistance R_i. Fig. 1.15 shows its equivalent current source. It can be easily shown that the two circuits behave electrically the same way under all conditions.

(*i*) If in Fig. 1.14, the load is open-circuited (*i.e.* $R_L \to \infty$), then voltage across terminals *A* and *B* is *V*. If in Fig. 1.15, the load is open-circuited (*i.e.* $R_L \to \infty$), then all current I (= V/R_i) flows through R_i, yielding voltage across terminals $AB = I R_i = V$. Note that open-circuited voltage across *AB* is *V* for both the circuits and hence they are electrically equivalent.

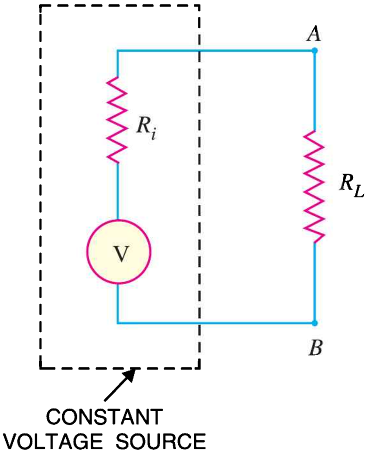


Fig. 1.14

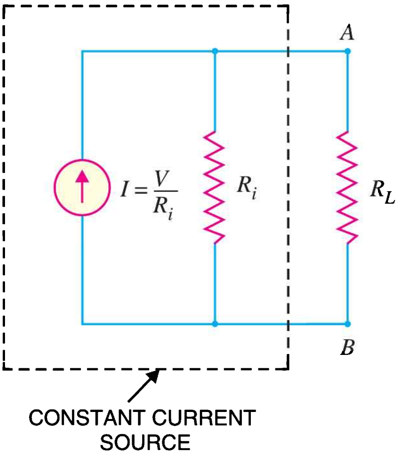


Fig. 1.15

(*ii*) If in Fig. 1.14, the load is short-circuited (*i.e.* $R_L = 0$), the short circuit current is given by:

$$I_{short} = \frac{V}{R_i}$$

If in Fig. 1.15, the load is short-circuited (*i.e.* $R_L = 0$), the current I (= V/R_i) bypasses R_i in favour of short-circuit. It is clear that current (= V/R_i) is the same for the two circuits and hence they are electrically equivalent.

Thus to convert a constant voltage source into a constant current source, the following procedure may be adopted :

(*a*) Place a short-circuit across the two terminals in question (terminals *AB* in the present case) and find the short-circuit current. Let it be *I*. Then *I* is the current supplied by the equivalent current source.

(*b*) Measure the resistance at the terminals with load removed and sources of *e.m.f.s* replaced by their internal resistances if any. Let this resistance be *R*.

(*c*) Then equivalent current source can be represented by a single current source of magnitude *I* in parallel with resistance *R*.

Note. To convert a current source of magnitude *I* in parallel with resistance *R* into voltage source,

Voltage of voltage source, $V = IR$

Resistance of voltage source, $R = R$

Thus voltage source will be represented as voltage *V* in series with resistance *R*.

Example 1.3. *Convert the constant voltage source shown in Fig. 1.16 into constant current source.*

Solution. The solution involves the following steps :

(*i*) Place a short across *AB* in Fig. 1.16 and find the short-circuit current *I*.

Clearly, $I = 10/10 = 1$ A

Therefore, the equivalent current source has a magnitude of 1 A.

(*ii*) Measure the resistance at terminals *AB* with load *removed and 10 V source replaced by its internal resistance. The 10 V source has negligible resistance so that resistance at terminals *AB* is $R = 10\ \Omega$.

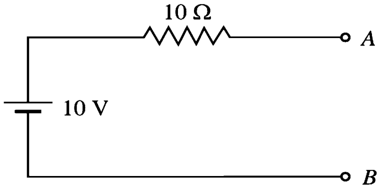


Fig. 1.16

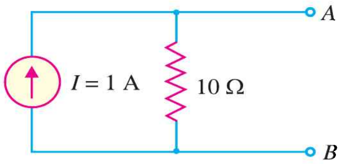


Fig. 1.17

(*iii*) The equivalent current source is a source of 1 A in parallel with a resistance of 10 Ω as shown in Fig. 1.17.

Example 1.4. *Convert the constant current source in Fig. 1.18 into equivalent voltage source.*

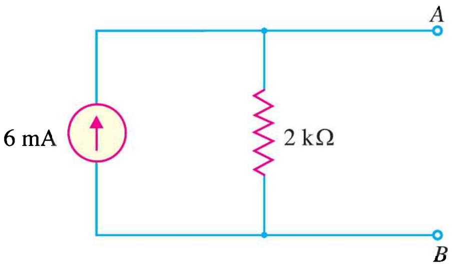


Fig. 1.18

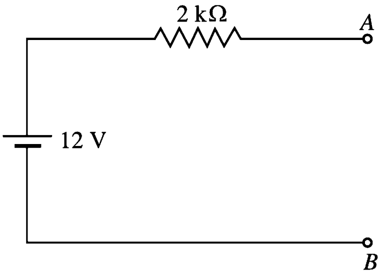


Fig. 1.19

Solution. The solution involves the following steps :

---

* Fortunately, no load is connected across *AB*. Had there been load across *AB*, it would have been removed.

(*i*) To get the voltage of the voltage source, multiply the current of the current source by the internal resistance *i.e.*

Voltage of voltage source $= IR = 6\ \text{mA} \times 2\ \text{k}\Omega = 12\text{V}$

(*ii*) The internal resistance of voltage source is 2 k Ω.

The equivalent voltage source is a source of 12 V in series with a resistance of 2 k Ω as shown in Fig. 1.19.

Note. The voltage source should be placed with +ve terminal in the direction of current flow.

1.12 Maximum Power Transfer Theorem

When load is connected across a voltage source, power is transferred from the source to the load. The amount of power transferred will depend upon the load resistance. If load resistance R_L is made equal to the internal resistance R_i of the source, then maximum power is transferred to the load R_L. This is known as *maximum power transfer theorem* and can be stated as follows :

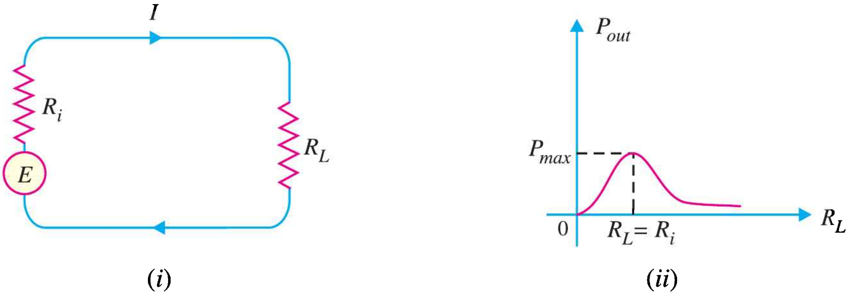
Maximum power is transferred from a source to a load when the load resistance is made equal to the internal resistance of the source.

This applies to d.c. as well as a.c. power.*

To prove this theorem mathematically, consider a voltage source of generated voltage E and internal resistance R_i and delivering power to a load resistance R_L [See Fig. 1.20 (*i*)]. The current I flowing through the circuit is given by :

$$I = \frac{E}{R_L + R_i}$$

Power delivered to the load, $$P = I^2 R_L = \left(\frac{E}{R_L + R_i}\right)^2 R_L \qquad \text{...(}i\text{)}$$



(*i*) (*ii*)

Fig. 1.20

For a given source, generated voltage E and internal resistance R_i are constant. Therefore, power delivered to the load depends upon R_L. In order to find the value of R_L for which the value of P is maximum, it is necessary to differentiate eq. (*i*) w.r.t. R_L and set the result equal to zero.

Thus, $$\frac{dP}{dR_L} = E^2 \left[\frac{(R_L + R_i)^2 - 2R_L(R_L + R_i)}{(R_L + R_i)^4}\right] = 0$$

or $$(R_L + R_i)^2 - 2R_L(R_L + R_i) = 0$$

or $$(R_L + R_i)(R_L + R_i - 2R_L) = 0$$

or $$(R_L + R_i)(R_i - R_L) = 0$$

---

* As power is concerned with resistance only, therefore, this is true for both a.c. and d.c. power.

Since $(R_L + R_i)$ cannot be zero,

$$\therefore \quad R_i - R_L = 0$$

or $$R_L = R_i$$

i.e. *Load resistance* = *Internal resistance*

Thus, for maximum power transfer, load resistance R_L must be equal to the internal resistance R_i of the source.

Under such conditions, the load is said to be *matched* to the source. Fig. 1.20 (*ii*) shows a graph of power delivered to R_L as a function of R_L. It may be mentioned that efficiency of maximum power transfer is *50% as one-half of the total generated power is dissipated in the internal resistance R_i of the source.

Applications. Electric power systems never operate for maximum power transfer because of low efficiency and high voltage drops between generated voltage and load. However, in the electronic circuits, maximum power transfer is usually desirable. For instance, in a public address system, it is desirable to have load (*i.e.* speaker) "matched" to the amplifier so that there is maximum transference of power from the amplifier to the speaker. In such situations, efficiency is **sacrificed at the cost of high power transfer.

Example 1.5. *A generator develops 200 V and has an internal resistance of 100 Ω. Find the power delivered to a load of (i) 100 Ω (ii) 300 Ω. Comment on the result.*

Solution.

$$\text{Generated voltage, } E = 200 \text{ V}$$

$$\text{Internal resistance, } R_i = 100\ \Omega$$

(*i*) $$\text{When load } R_L = 100\ \Omega$$

$$\text{Load current, } I = \frac{E}{R_L + R_i} = \frac{200}{100 + 100} = 1 \text{ A}$$

$$\therefore \quad \text{Power delivered to load} = I^2 R_L = (1)^2 \times 100 = \mathbf{100\ watts}$$

$$\text{Total power generated} = I^2 (R_L + R_i) = 1^2 (100 + 100) = 200 \text{ watts}$$

Thus, out of 200 W power developed by the generator, only 100W has reached the load *i.e.* efficiency is 50% only.

(*ii*) $$\text{When load } R_L = 300\ \Omega$$

$$\text{Load current, } I = \frac{E}{R_L + R_i} = \frac{200}{300 + 100} = 0.5 \text{ A}$$

$$\text{Power delivered to load} = I^2 R_L = (0.5)^2 \times 300 = \mathbf{75\ watts}$$

$$\text{Total power generated} = I^2 (R_L + R_i) = (0.5)^2 (300 + 100) = 100 \text{ watts}$$

Thus, out of 100 watts of power produced by the generator, 75 watts is transferred to the load *i.e.* efficiency is 75%.

Comments. Although in case of $R_L = R_i$, a large power (100 W) is transferred to the load, but there is a big wastage of power in the generator. On the other hand, when R_L is ***not*** equal to R_i, the

---

* $$\text{Efficiency} = \frac{\text{output power}}{\text{input power}} = \frac{I^2 R_L}{I^2 (R_L + R_i)}$$

$$= R_L/2\,R_L = 1/2 = 50\% \qquad (\because R_L = R_i)$$

** Electronic devices develop small power. Therefore, if too much efficiency is sought, a large number of such devices will have to be connected in series to get the desired output. This will distort the output as well as increase the cost and size of equipment.

power transfer is less (75 W) but smaller part is wasted in the generator *i.e.* efficiency is high. Thus, it depends upon a particular situation as to what the load should be. If we want to transfer maximum power (*e.g.* in amplifiers) irrespective of efficiency, we should make $R_L = R_i$. However, if efficiency is more important (*e.g.* in power systems), then internal resistance of the source should be considerably smaller than the load resistance.

Example 1.6. *An audio amplifier produces an alternating output of 12 V before the connection to a load. The amplifier has an equivalent resistance of 15 Ω at the output. What resistance the load need to have to produce maximum power ? Also calculate the power output under this condition.*

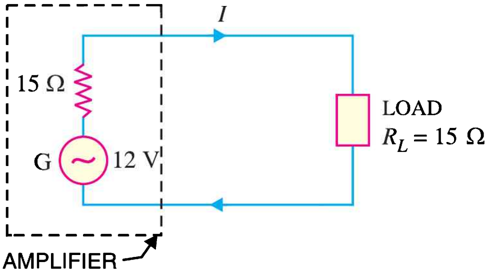


Fig. 1.21

Solution. In order to produce maximum power, the load (*e.g.* a speaker) should have a resistance of 15 Ω to match the amplifier. The equivalent circuit is shown in Fig. 1.21.

$$\therefore \quad \text{Load required, } R_L = \mathbf{15\ \Omega}$$

$$\text{Circuit current, } I = \frac{V}{R_T} = \frac{12}{15 + 15} = 0.4 \text{ A}$$

$$\text{Power delivered to load, } P = I^2 R_L = (0.4)^2 \times 15 = \mathbf{2.4\ W}$$

Example 1.7. *For the a.c. generator shown in Fig. 1.22 (i), find (i) the value of load so that maximum power is transferred to the load (ii) the value of maximum power.*

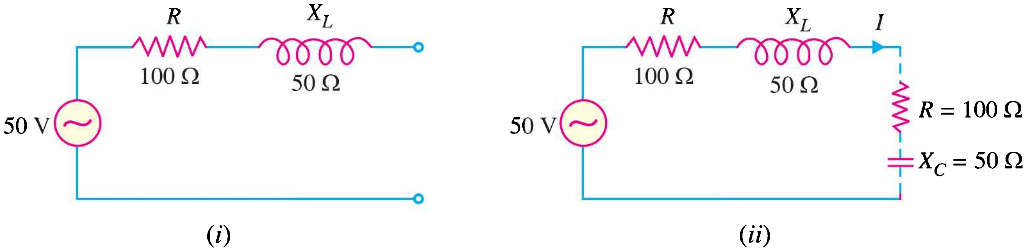


Fig. 1.22

Solution.

(*i*) In a.c. system, maximum power is delivered to the load impedance (Z_L) when load impedance is conjugate of the internal impedance (Z_i) of the source. Now in the problem, $Z_i = (100 + j50)\Omega$. For maximum power transfer, the load impedance should be conjugate of internal impedance *i.e.* Z_L should be $(100 - j50)$ Ω. This is shown in dotted line in Fig. 1.22 (*ii*).

$$\therefore \quad Z_L = \mathbf{(100 - j50)\ \Omega}$$

(*ii*)

$$\text{Total impedance, } Z_T = Z_i + Z_L = (100 + j50) + (100 - j50) = 200\ \Omega^*$$

$$\text{Circuit current, } I = \frac{V}{Z_T} = \frac{50}{200} = 0.25 \text{ A}$$

$$\text{Maximum power transferred to the load} = I^2 R_L = (0.25)^2 \times 100 = \mathbf{6.25\ W}$$

---

[*] Note that by making internal impedance and load impedance conjugate, the reactive terms cancel. The circuit then consists of internal and external resistances only. This is quite logical because power is only consumed in resistances as reactances (X_L or X_C) consume no power.

1.13 Thevenin's Theorem

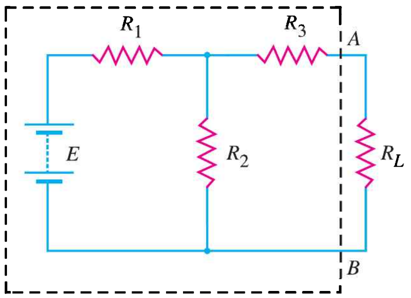
Sometimes it is desirable to find a particular branch current in a circuit as the resistance of that branch is varied while all other resistances and voltage sources remain constant. For instance, in the circuit shown in Fig. 1.23, it may be desired to find the current through R_L for five values of R_L, assuming that R_1, R_2, R_3 and E remain constant. In such situations, the *solution can be obtained readily by applying *Thevenin's theorem* stated below :

Any two-terminal network containing a number of e.m.f. sources and resistances can be replaced by an equivalent series circuit having a voltage source E_0 in series with a resistance R_0 where,

E_0 = open circuited voltage between the two terminals.

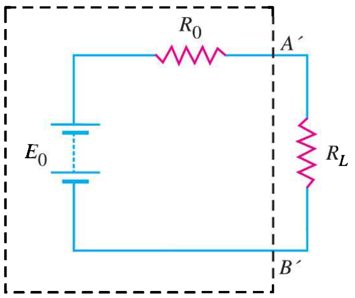
R_0 = the resistance between two terminals of the circuit obtained by looking "in" at the terminals with load removed and voltage sources replaced by their internal resistances, if any.

To understand the use of this theorem, consider the two-terminal circuit shown in Fig. 1.23. The circuit enclosed in the dotted box can be replaced by one voltage E_0 in series with resistance R_0 as shown in Fig. 1.24. The behaviour at the terminals AB and $A'B'$ is the same for the two circuits, independent of the values of R_L connected across the terminals.



ACTIVE CIRCUIT

Fig. 1.23



THEVENIN'S EQUIVALENT CKT.

Fig. 1.24

(*i*) **Finding E_0.** This is the voltage between terminals A and B of the circuit when load R_L is removed. Fig. 1.25 shows the circuit with load removed. The voltage drop across R_2 is the desired voltage E_0.

$$\text{Current through } R_2 = \frac{E}{R_1 + R_2}$$

$$\therefore \quad \text{Voltage across } R_2,\ E_0 = \left(\frac{E}{R_1 + R_2}\right) R_2$$

Thus, voltage E_0 is determined.

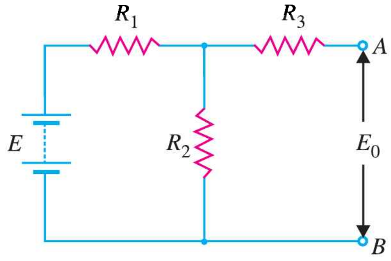


Fig. 1.25

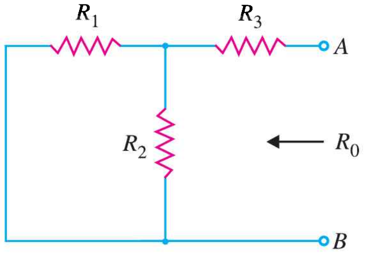


Fig. 1.26

---

* Solution can also be obtained by applying Kirchhoff's laws but it requires a lot of labour.

(*ii*) **Finding R_0.** This is the resistance between terminals *A* and *B* with load removed and e.m.f. reduced to zero (See Fig. 1.26).

∴ Resistance between terminals *A* and *B* is

$$R_0 = \text{parallel combination of } R_1 \text{ and } R_2 \text{ in series with } R_3$$

$$= \frac{R_1 R_2}{R_1 + R_2} + R_3$$

Thus, the value of R_0 is determined. Once the values of E_0 and R_0 are determined, then the current through the load resistance R_L can be found out easily (Refer to Fig. 1.24).

1.14 Procedure for Finding Thevenin Equivalent Circuit

(*i*) Open the two terminals (*i.e.* remove any load) between which you want to find Thevenin equivalent circuit.

(*ii*) Find the open-circuit voltage between the two open terminals. It is called Thevenin voltage E_0.

(*iii*) Determine the resistance between the two open terminals with all ideal voltage sources shorted and all ideal current sources opened (a non-ideal source is replaced by its internal resistance). It is called Thevenin resistance R_0.

(*iv*) Connect E_0 and R_0 in series to produce Thevenin equivalent circuit between the two terminals under consideration.

(*v*) Place the load resistor removed in step (*i*) across the terminals of the Thevenin equivalent circuit. The load current can now be calculated using only Ohm's law and it has the same value as the load current in the original circuit.

Example 1.8. *Using Thevenin's theorem, find the current through 100 Ω resistance connected across terminals A and B in the circuit of Fig. 1.27.*

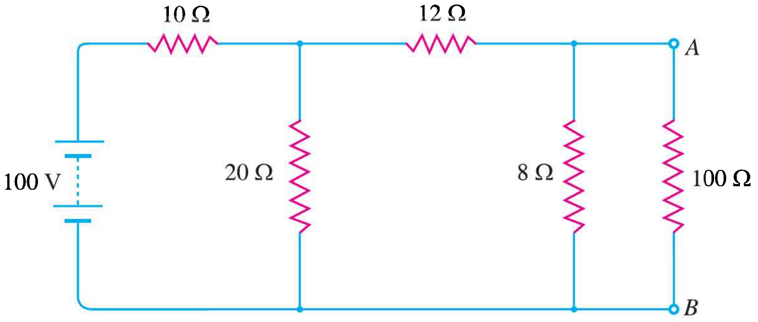


Fig. 1.27

Solution.

(*i*) **Finding E_0.** It is the voltage across terminals *A* and *B* with 100 Ω resistance removed as shown in Fig. 1.28.

$$E_0 = (\text{Current through } 8\ \Omega) \times 8\ \Omega = 2.5^{*} \times 8 = 20\ \text{V}$$

---

* By solving this series-parallel circuit.

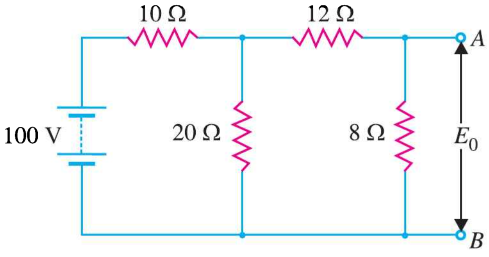


Fig. 1.28

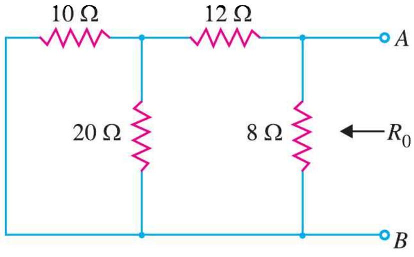


Fig. 1.29

(*ii*) **Finding R_0.** It is the resistance between terminals *A* and *B* with 100 Ω removed and voltage source short circuited as shown in Fig. 1.29.

R_0 = Resistance looking in at terminals *A* and *B* in Fig. 1.29

$$= \frac{\left[\frac{10 \times 20}{10 + 20} + 12\right] 8}{\left[\frac{10 \times 20}{10 + 20} + 12\right] + 8}$$

$= 5.6\ \Omega$

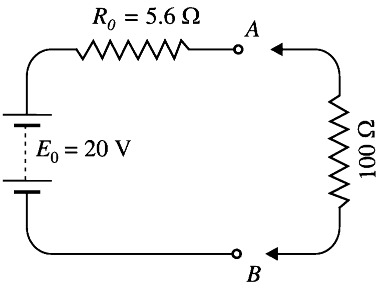


Fig. 1.30

Therefore, Thevenin's equivalent circuit will be as shown in Fig. 1.30. Now, current through 100 Ω resistance connected across terminals *A* and *B* can be found by applying Ohm's law.

$$\text{Current through } 100\ \Omega \text{ resistor} = \frac{E_0}{R_0 + R_L} = \frac{20}{5.6 + 100} = \mathbf{0.19\ A}$$

Example 1.9. *Find the Thevenin's equivalent circuit for Fig. 1.31.*

Solution. The Thevenin's voltage E_0 is the voltage across terminals *A* and *B*. This voltage is equal to the voltage across R_3. It is because terminals *A* and *B* are open circuited and there is no current flowing through R_2 and hence no voltage drop across it.

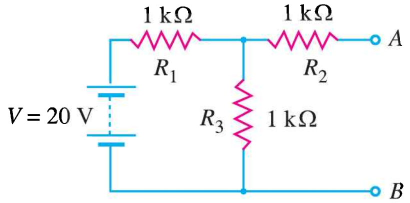


Fig. 1.31

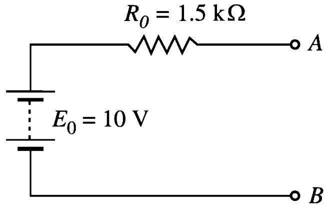


Fig. 1.32

$$\therefore \quad E_0 = \text{Voltage across } R_3$$

$$= \frac{R_3}{R_1 + R_3} \times V = \frac{1}{1+1} \times 20 = 10\ \text{V}$$

The Thevenin's resistance R_0 is the resistance measured between terminals *A* and *B* with no load (*i.e.* open at terminals *A* and *B*) and voltage source replaced by a short circuit.

$$\therefore \quad R_0 = R_2 + \frac{R_1 R_3}{R_1 + R_3} = 1 + \frac{1 \times 1}{1 + 1} = 1.5\ \text{k}\Omega$$

Therefore, Thevenin's equivalent circuit will be as shown in Fig. 1.32.

Example 1.10. *Calculate the value of load resistance R_L to which maximum power may be transferred from the circuit shown in Fig. 1.33 (i). Also find the maximum power.*

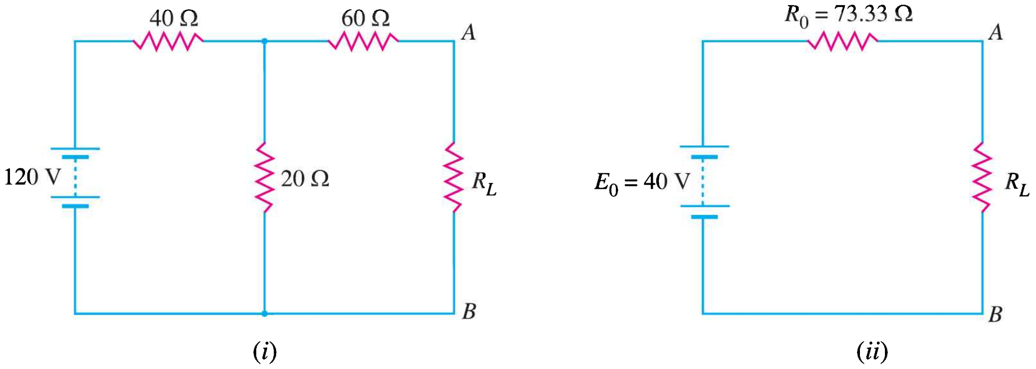


Fig. 1.33

Solution. We shall first find Thevenin's equivalent circuit to the left of terminals *AB* in Fig. 1.33 (*i*).

E_0 = Voltage across terminals *AB* with R_L removed

$$= \frac{120}{40 + 20} \times 20 = 40 \text{ V}$$

R_0 = Resistance between terminals *A* and *B* with R_L removed and 120 V source replaced by a short

$$= 60 + (40\ \Omega \parallel 20\ \Omega) = 60 + (40 \times 20)/60 = 73.33\ \Omega$$

The Thevenin's equivalent circuit to the left of terminals *AB* in Fig. 1.33 (*i*) is E_0 (= 40 V) in series with R_0 (= 73.33 Ω). When R_L is connected between terminals *A* and *B*, the circuit becomes as shown in Fig. 1.33 (*ii*). It is clear that maximum power will be transferred when

$$R_L = R_0 = \mathbf{73.33\ \Omega}$$

$$\text{Maximum power to load} = \frac{E_0^2}{4\,R_L} = \frac{(40)^2}{4 \times 73.33} = \mathbf{5.45\ W}$$

Comments. This shows another advantage of Thevenin's equivalent circuit of a network. Once Thevenin's equivalent resistance R_0 is calculated, it shows at a glance the condition for maximum power transfer. Yet Thevenin's equivalent circuit conveys another information. Thus referring to Fig. 1.33 (*ii*), the maximum voltage that can appear across terminals *A* and *B* is 40 V. This is not so obvious from the original circuit shown in Fig. 1.33 (*i*).

Example 1.11. *Calculate the current in the 50 Ω resistor in the network shown in Fig. 1.34.*

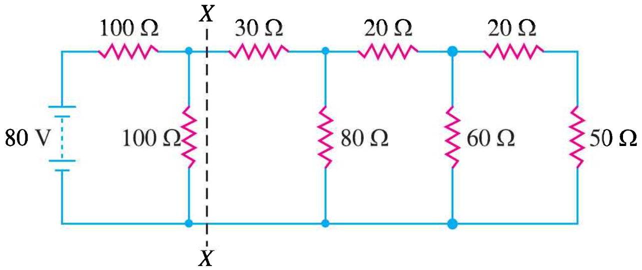


Fig. 1.34

Solution. We shall simplify the circuit shown in Fig. 1.34 by the repeated use of Thevenin's theorem. We first find Thevenin's equivalent circuit to the left of **XX*.

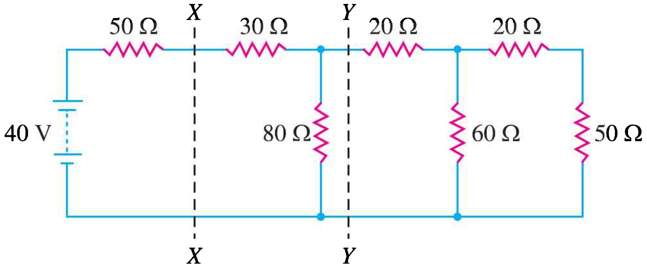


Fig. 1.35

$$E_0 = \frac{80}{100 + 100} \times 100 = 40\text{V}$$

$$R_0 = 100 \parallel 100 = \frac{100 \times 100}{100 + 100} = 50\ \Omega$$

Therefore, we can replace the circuit to the left of *XX* in Fig. 1.34 by its Thevenin's equivalent circuit *viz.* E_0 (= 40V) in series with R_0 (= 50 Ω). The original circuit of Fig. 1.34 then reduces to the one shown in Fig. 1.35.

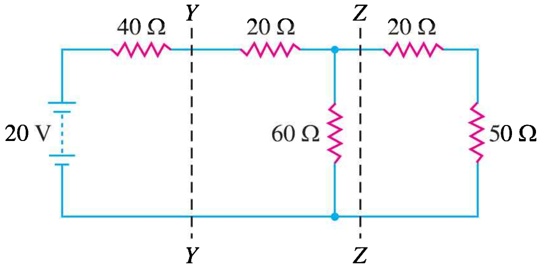


Fig. 1.36

We shall now find Thevenin's equivalent circuit to left of *YY* in Fig. 1.35.

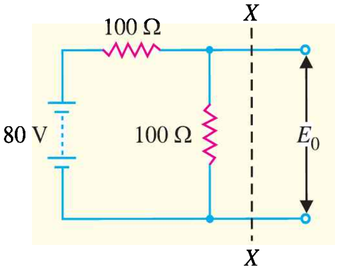
$$E_0' = \frac{40}{50 + 30 + 80} \times 80 = 20\ \text{V}$$

$$R_0' = (50 + 30) \parallel 80 = \frac{80 \times 80}{80 + 80} = 40\ \Omega$$

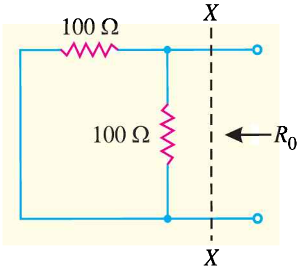
We can again replace the circuit to the left of *YY* in Fig. 1.35 by its Thevenin's equivalent circuit. Therefore, the original circuit reduces to that shown in Fig. 1.36.

---

*



(*a*)



(*b*)

$$E_0 = \text{Current in } 100\ \Omega \times 100\ \Omega = \frac{80}{100 + 100} \times 100 = 40\text{V} \quad [\text{See Fig. } (a)]$$

R_0 = Resistance looking in the open terminals in Fig. (*b*)

$$= 100 \parallel 100 = \frac{100 \times 100}{100 + 100} = 50\ \Omega$$

Using the same procedure to the left of *ZZ*, we have,

$$E''_0 = \frac{20}{40+20+60} \times 60 = 10\text{V}$$

$$R''_0 = (40+20) \parallel 60 = \frac{60 \times 60}{60+60} = 30\ \Omega$$

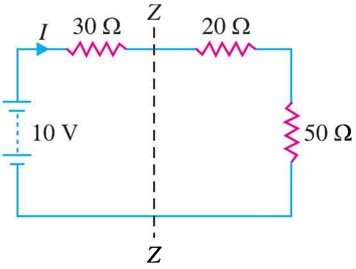


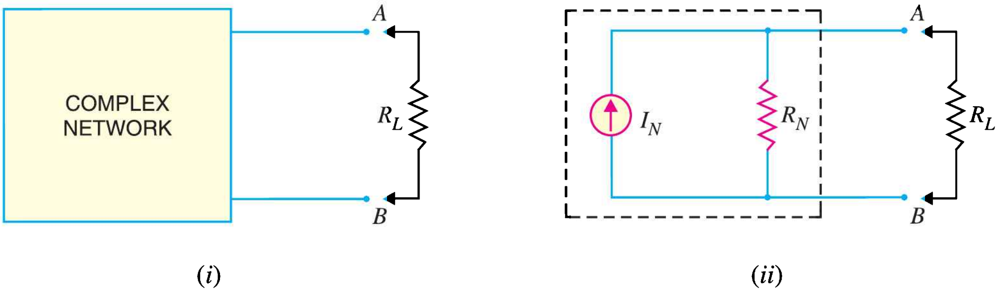
Fig. 1.37

The original circuit then reduces to that shown in Fig. 1.37. By Ohm's law, current *I* in 50 Ω resistor is

$$I = \frac{10}{30+20+50} = \mathbf{0.1\ A}$$

1.15 Norton's Theorem

Fig. 1.38 (*i*) shows a network enclosed in a box with two terminals *A* and *B* brought out. The network in the box may contain any number of resistors and e.m.f. sources connected in any manner. But according to Norton, the entire circuit behind terminals *A* and *B* can be replaced by a current source of output I_N in parallel with a single resistance R_N as shown in Fig. 1.38 (*ii*). The value of I_N is determined as mentioned in Norton's theorem. The resistance R_N is the same as Thevenin's resistance R_0. Once Norton's equivalent circuit is determined [See Fig. 1.38 (*ii*)], then current through any load R_L connected across terminals *AB* can be readily obtained.



(*i*) (*ii*)

Fig. 1.38

Hence Norton's theorem as applied to d.c. circuits may be stated as under :

Any network having two terminals A and B can be replaced by a current source of output I_N in parallel with a resistance R_N.

(*i*) *The output I_N of the current source is equal to the current that would flow through AB when terminals A and B are short circuited.*

(*ii*) *The resistance R_N is the resistance of the network measured between terminals A and B with load (R_L) removed and sources of e.m.f. replaced by their internal resistances, if any.*

Norton's theorem is *converse* of Thevenin's theorem in that Norton equivalent circuit uses a current generator instead of voltage generator and resistance R_N (which is the same as R_0) in parallel with the generator instead of being in series with it.

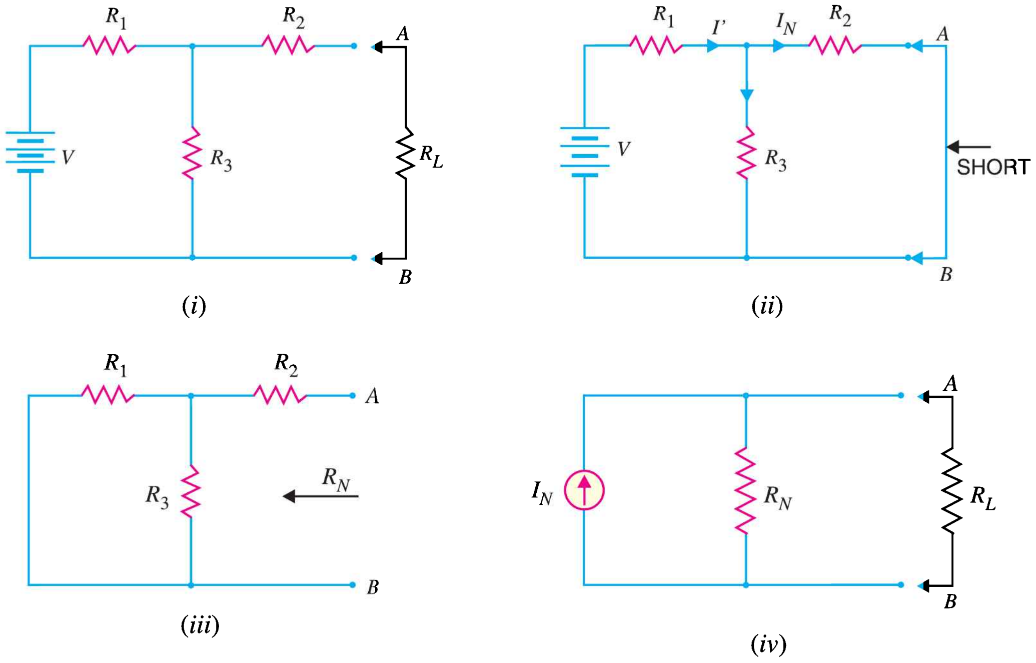
Illustration. Fig. 1.39 illustrates the application of Norton's theorem. As far as circuit behind terminals *AB* is concerned [See Fig. 1.39 (*i*)], it can be replaced by a current source of output I_N in parallel with a resistance R_N as shown in Fig. 1.39 (*iv*). The output I_N of the current generator is equal to the current that would flow through *AB* when terminals *A* and *B* are short-circuited as shown in Fig. 1.39 (*ii*). The load *R′* on the source when terminals *AB* are short-circuited is given by :

$$R' = R_1 + \frac{R_2 R_3}{R_2 + R_3} = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_2 + R_3}$$

$$\text{Source current, } I' = \frac{V}{R'} = \frac{V(R_2 + R_3)}{R_1 R_2 + R_1 R_3 + R_2 R_3}$$

$$\text{Short-circuit current, } I_N = \text{Current in } R_2 \text{ in Fig. 1.39 } (ii)$$

$$= I' \times \frac{R_3}{R_2 + R_3} = \frac{V R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3}$$



(*i*) (*ii*) (*iii*) (*iv*)

Fig. 1.39

To find R_N, remove the load R_L and replace the voltage source by a short circuit because its resistance is assumed zero [See Fig. 1.39 (*iii*)].

$$\therefore \qquad R_N = \text{Resistance at terminals } AB \text{ in Fig. 1.39 } (iii).$$

$$= R_2 + \frac{R_1 R_3}{R_1 + R_3}$$

Thus the values of I_N and R_N are known. The Norton equivalent circuit will be as shown in Fig. 1.39 (*iv*).

1.16 Procedure for Finding Norton Equivalent Circuit

(*i*) Open the two terminals (*i.e.* remove any load) between which we want to find Norton equivalent circuit.

(*ii*) Put a short-circuit across the terminals under consideration. Find the short-circuit current flowing in the short circuit. It is called Norton current I_N.

(*iii*) Determine the resistance between the two open terminals with all ideal voltage sources shorted and all ideal current sources opened (a non-ideal source is replaced by its internal resistance). It is called Norton's resistance R_N. It is easy to see that $R_N = R_0$.

(*iv*) Connect I_N and R_N in parallel to produce Norton equivalent circuit between the two terminals under consideration.

(*v*) Place the load resistor removed in step (*i*) across the terminals of the Norton equivalent circuit. The load current can now be calculated by using current-divider rule. This load current will be the same as the load current in the original circuit.

Example 1.12. *Using Norton's theorem, find the current in 8 Ω resistor in the network shown in Fig. 1.40 (i).*

Solution. We shall reduce the network to the left of *AB* in Fig. 1.40 (*i*) to Norton's equivalent circuit. For this purpose, we are required to find I_N and R_N.

(*i*) With load (*i.e.*, 8 Ω) removed and terminals *AB* short circuited [See Fig. 1.40 (*ii*)], the current that flows through *AB* is equal to I_N. Referring to Fig. 1.40 (*ii*),

$$\text{Load on the source} = 4\,\Omega + 5\,\Omega \,||\, 6\,\Omega$$

$$= 4 + \frac{5 \times 6}{5 + 6} = 6.727\,\Omega$$

$$\text{Source current, } I' = 40/6.727 = 5.94\text{ A}$$

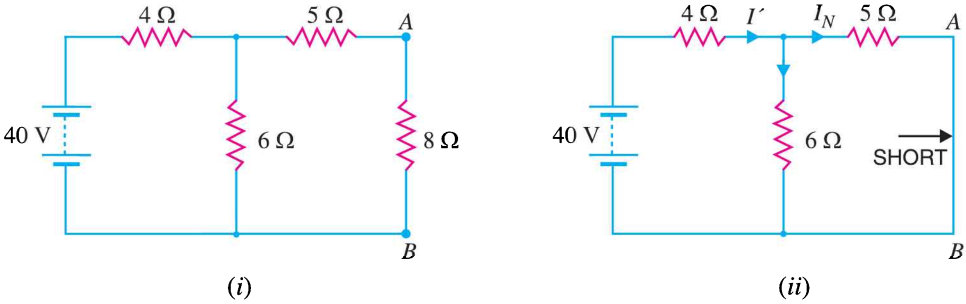


Fig. 1.40

$$\therefore \quad \text{Short-circuit current in } AB,\ I_N = I' \times \frac{6}{6+5} = 5.94 \times 6/11 = 3.24\text{ A}$$

(*ii*) With load (*i.e.*, 8 Ω) removed and battery replaced by a short (since its internal resistance is assumed zero), the resistance at terminals *AB* is equal to R_N as shown in Fig. 1.41 (*i*).

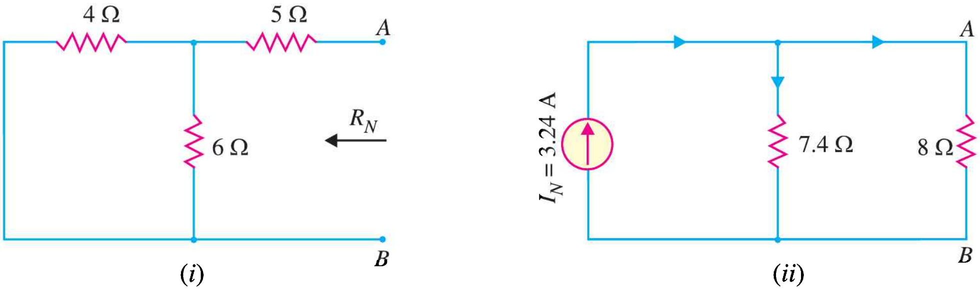


Fig. 1.41

$$R_N = 5\,\Omega + 4\,\Omega \,||\, 6\,\Omega = 5 + \frac{4 \times 6}{4 + 6} = 7.4\,\Omega$$

The Norton's equivalent circuit behind terminals *AB* is I_N (= 3.24 A) in parallel with R_N (= 7.4 Ω). When load (*i.e.*, 8 Ω) is connected across terminals *AB*, the circuit becomes as shown in Fig. 1.41 (*ii*). The current source is supplying current to two resistors 7.4 Ω and 8 Ω in parallel.

$$\therefore \quad \text{Current in 8 } \Omega \text{ resistor} = 3.24 \times \frac{7.4}{8 + 7.4} = \mathbf{1.55\ A}$$

Example 1.13. *Find the Norton equivalent circuit at terminals X – Y in Fig. 1.42.*

Solution. We shall first find the Thevenin equivalent circuit and then convert it to an equivalent current source. This will then be Norton equivalent circuit.

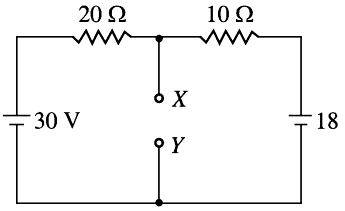


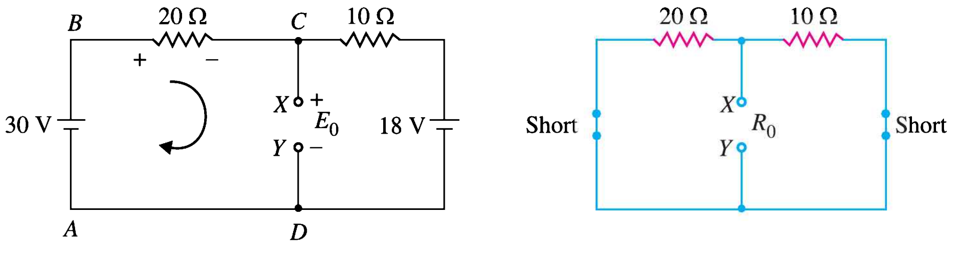
Fig. 1.42

Finding Thevenin Equivalent circuit. To find E_0, refer to Fig. 1.43 (*i*). Since 30 V and 18 V sources are in opposition, the circuit current *I* is given by :

$$I = \frac{30 - 18}{20 + 10} = \frac{12}{30} = 0.4 \text{ A}$$

Applying Kirchhoff's voltage law to loop *ABCDA*, we have,

$$30 - 20 \times 0.4 - E_0 = 0 \qquad \therefore \; E_0 = 30 - 8 = 22 \text{ V}$$



(*i*) (*ii*)

Fig. 1.43

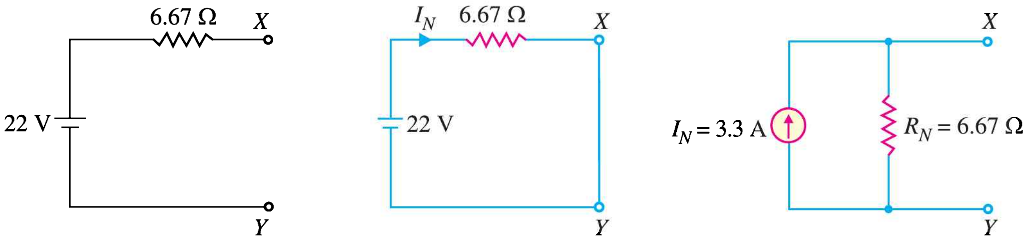
To find R_0, we short both voltage sources as shown in Fig. 1.43 (*ii*). Notice that 10 Ω and 20 Ω resistors are then in parallel.

$$\therefore \qquad R_0 = 10\,\Omega \,||\, 20\,\Omega = \frac{10 \times 20}{10 + 20} = 6.67\Omega$$

Therefore, Thevenin equivalent circuit will be as shown in Fig. 1.44 (*i*). Now it is quite easy to convert it into equivalent current source.

$$I_N = \frac{E_0}{R_0} = \frac{22}{6.67} = 3.3\text{A} \qquad \text{[See Fig. 1.44 (}ii\text{)]}$$

$$R_N = R_0 = 6.67\ \Omega$$



(*i*) (*ii*) (*iii*)

Fig. 1.44

Fig. 1.44 (*iii*) shows Norton equivalent circuit. Observe that the Norton equivalent resistance has the same value as the Thevenin equivalent resistance. Therefore, R_N is found exactly the same way.

Example 1.14. *Show that when Thevenin's equivalent circuit of a network is converted into Norton's equivalent circuit,* $I_N = E_0/R_0$ *and* $R_N = R_0$. *Here* E_0 *and* R_0 *are Thevenin voltage and Thevenin resistance respectively.*

Solution. Fig. 1.45 (*i*) shows a network enclosed in a box with two terminals *A* and *B* brought out. Thevenin's equivalent circuit of this network will be as shown in Fig. 1.45 (*ii*). To find Norton's equivalent circuit, we are to find I_N and R_N. Referring to Fig. 1.45 (*ii*),

I_N = Current flowing through short-circuited *AB* in Fig. 1.45 (*ii*)

$= E_0/R_0$

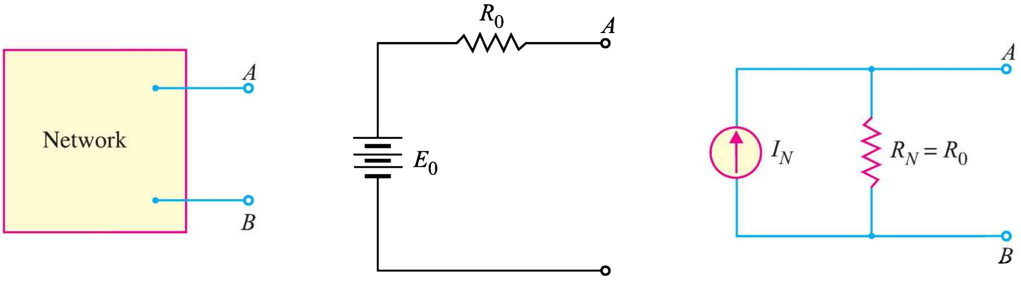
R_N = Resistance at terminals *AB* in Fig. 1.45 (*ii*)

$= R_0$

Fig. 1.45 (*iii*) shows Norton's equivalent circuit. Hence we arrive at the following two important conclusions :

(*i*) To convert Thevenin's equivalent circuit into Norton's equivalent circuit,

$$I_N = E_0/R_0 \quad ; \quad R_N = R_0$$



(*i*) (*ii*) (*iii*)

Fig. 1.45

(*ii*) To convert Norton's equivalent circuit into Thevenin's equivalent circuit,

$$E_0 = I_N R_N \quad ; \quad R_0 = R_N$$

1.17 Chassis and Ground

It is the usual practice to mount the electronic components on a metal base called *chassis*. For example, in Fig. 1.46, the voltage source and resistors are connected to the chassis. As the resistance of chassis is very low, therefore, it provides a conducting path and may be considered as a piece of wire.

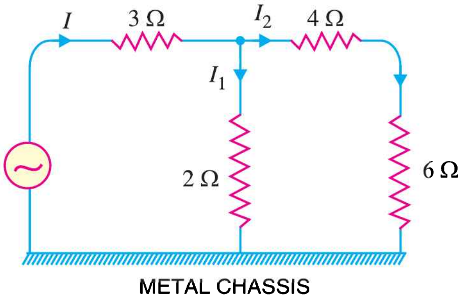


Fig. 1.46

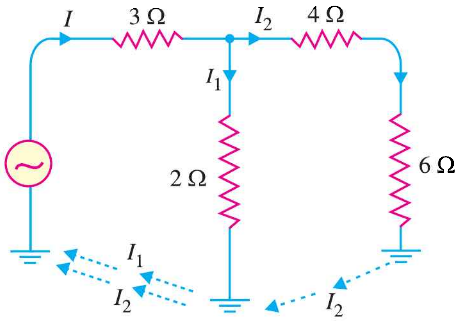


Fig. 1.47

It is customary to refer to the chassis as *ground*. Fig. 1.47 shows the symbol for chassis. It may be seen that all points connected to chassis are shown as grounded and represent the same potential. The adoption of this scheme (*i.e.* showing points of same potential as grounded) often simplifies the electronic circuits. In our further discussion, we shall frequently use this scheme.

MULTIPLE-CHOICE QUESTIONS

1. The outermost orbit of an atom can have a maximum of .... electrons.

(*i*) 8 (*ii*) 6
(*iii*) 4 (*iv*) 3

2. When the outermost orbit of an atom has less than 4 electrons, the material is generally a ....

(*i*) non-metal (*ii*) metal
(*iii*) semiconductor (*iv*) none of above

3. The valence electrons have ....

(*i*) very small energy
(*ii*) least energy
(*iii*) maximum energy
(*iv*) none of the above

4. A large number of free electrons exist in ....

(*i*) semiconductors (*ii*) metals
(*iii*) insulators (*iv*) non-metals

5. An ideal voltage source has .... internal resistance.

(*i*) small (*ii*) large
(*iii*) infinite (*iv*) zero

6. An ideal current source has .... internal resistance.

(*i*) infinite (*ii*) zero
(*iii*) small (*iv*) none of the above

7. Maximum power is transferred if load resistance is equal to .... of the source.

(*i*) half the internal resistance
(*ii*) internal resistance
(*iii*) twice the internal resistance
(*iv*) none of the above

8. Efficiency at maximum power transfer is ....

(*i*) 75% (*ii*) 25%
(*iii*) 90% (*iv*) 50%

9. When the outermost orbit of an atom has exactly 4 valence electrons, the material is generally ....

(*i*) a metal (*ii*) a non-metal
(*iii*) a semiconductor
(*iv*) an insulator

10. Thevenin's theorem replaces a complicated circuit facing a load by an ....

(*i*) ideal voltage source and parallel resistor
(*ii*) ideal current source and parallel resistor
(*iii*) ideal current source and series resistor
(*iv*) ideal voltage source and series resistor

11. The output voltage of an ideal voltage source is ....

(*i*) zero (*ii*) constant
(*iii*) dependent on load resistance
(*iv*) dependent on internal resistance

12. The current output of an ideal current source is ....

(*i*) zero (*ii*) constant
(*iii*) dependent on load resistance
(*iv*) dependent on internal resistance

13. Norton's theorem replaces a complicated circuit facing a load by an ....

(*i*) ideal voltage source and parallel resistor
(*ii*) ideal current source and parallel resistor
(*iii*) ideal voltage source and series resistor
(*iv*) ideal current source and series resistor

14. The practical example of ideal voltage source is ....

(*i*) lead-acid cell (*ii*) dry cell
(*iii*) Daniel cell (*iv*) none of the above

15. The speed of electrons in vacuum is .... than in a conductor.

(*i*) less (*ii*) much more
(*iii*) much less (*iv*) none of the above

16. Maximum power will be transferred from a source of 10 Ω resistance to a load of ....

(*i*) 5 Ω (*ii*) 20 Ω
(*iii*) 10 Ω (*iv*) 40 Ω

17. When the outermost orbit of an atom has more than 4 electrons, the material is generally a ....

(*i*) metal (*ii*) non-metal
(*iii*) semiconductor (*iv*) none of the above

18. An ideal source consists of 5 V in series with 10 kΩ resistance. The current magnitude of equivalent current source is ....

(*i*) 2 mA (*ii*) 3.5 mA
(*iii*) 0.5 mA (*iv*) none of the above

19. To get Thevenin voltage, you have to ....

(*i*) short the load resistor
(*ii*) open the load resistor
(*iii*) short the voltage source
(*iv*) open the voltage source

20. To get the Norton current, you have to ....

(*i*) short the load resistor
(*ii*) open the load resistor
(*iii*) short the voltage source
(*iv*) open the voltage source

21. The open-circuited voltage at the terminals of load R_L in a network is 30 V. Under the conditions of maximum power transfer, the load voltage will be ....

(*i*) 30 V (*ii*) 10 V
(*iii*) 5 V (*iv*) 15 V

22. Under the conditions of maximum power transfer, a voltage source is delivering a power of 30 W to the load. The power produced by the source is ....

(*i*) 45 W (*ii*) 60 W
(*iii*) 30 W (*iv*) 90 W

23. The maximum power transfer theorem is used in ....

(*i*) electronic circuits
(*ii*) power system
(*iii*) home lighting circuits
(*iv*) none of the above

24. The Norton resistance of a network is 20 Ω and the shorted-load current is 2 A. If the network is loaded by a resistance equal to 20 Ω, the current through the load will be ....

(*i*) 2 A (*ii*) 0.5 A
(*iii*) 4 A (*iv*) 1 A

25. The Norton current is sometimes called the ....

(*i*) shorted-load current
(*ii*) open-load current
(*iii*) Thevenin current
(*iv*) Thevenin voltage

Answers to Multiple-Choice Questions

1.	(*i*)	**2.**	(*ii*)	**3.**	(*iii*)	**4.**	(*ii*)	**5.**	(*iv*)
6.	(*i*)	**7.**	(*ii*)	**8.**	(*iv*)	**9.**	(*iii*)	**10.**	(*iv*)
11.	(*ii*)	**12.**	(*ii*)	**13.**	(*ii*)	**14.**	(*i*)	**15.**	(*ii*)
16.	(*iii*)	**17.**	(*ii*)	**18.**	(*iii*)	**19.**	(*ii*)	**20.**	(*i*)
21.	(*iv*)	**22.**	(*ii*)	**23.**	(*i*)	**24.**	(*iv*)	**25.**	(*i*)

Chapter Review Topics

1. What is electronics ? Mention some important applications of electronics.
2. Describe briefly the structure of atom.
3. Explain how valence electrons determine the electrical properties of a material.
4. Explain constant voltage and current sources. What is their utility ?
5. Derive the condition for transfer of maximum power from a source to a load.
6. State and explain Thevenin's theorem.
7. Write short notes on the following :
   (*i*) Atomic structure (*ii*) Valence electrons (*iii*) Free electrons

Problems

1. A dry battery developing 12 V has an internal resistance of 10 Ω. Find the output current if load is (*i*) 100 Ω (*ii*) 10 Ω (*iii*) 2 Ω and (*iv*) 1 Ω. **[(*i*) 0.1A (*ii*) 0.6A (*iii*) 1A (*iv*) 1.1A]**
2. Convert the current source in Fig. 1.48 into the equivalent voltage source. **[36 V in series with 900 Ω]**

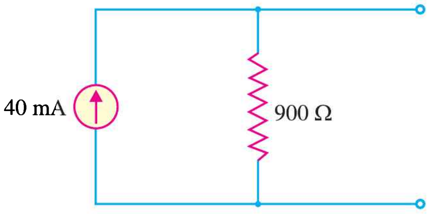


Fig. 1.48

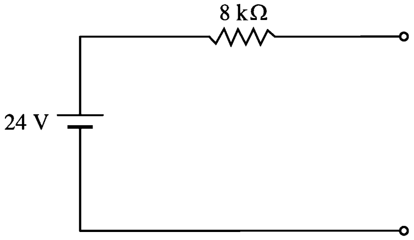


Fig. 1.49

3. Convert the voltage source in Fig. 1.49 into equivalent current source. **[3 mA in parallel with 8 kΩ]**
4. Using Norton's Theorem, find the current in branch *AB* containing 6 Ω resistor of the network shown in Fig. 1.50. **[0.466 A]**

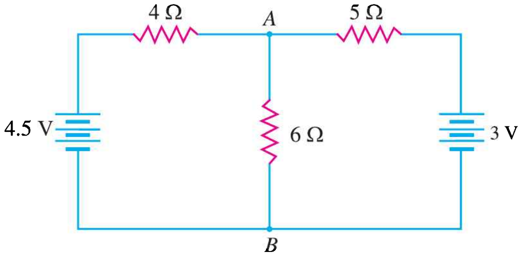


Fig. 1.50

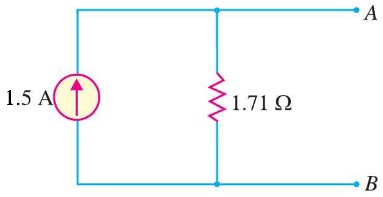


Fig. 1.51

5. Fig. 1.51 shows Norton's equivalent circuit of a network behind terminals *A* and *B*. Convert it into Thevenin's equivalent circuit. **[2.56 V in series with 1.71 Ω]**

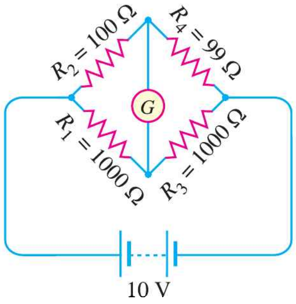


Fig. 1.52

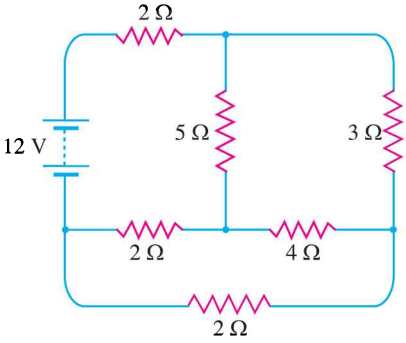


Fig. 1.53

6. A power amplifier has an internal resistance of 5 Ω and develops open circuited voltage of 12 V. Find the efficiency and power transferred to a load of (*i*) 20 Ω (*ii*) 5 Ω. **[(*i*) 80%, 4.6 W (*ii*) 50%, 7.2 W]**
7. Using Thevenin's theorem, find the current through the galvanometer in the Wheatstone bridge shown in Fig. 1.52. **[38.6 µA]**
8. Using Thevenin's theorem, find the current through 4 Ω resistor in the circuit of Fig. 1.53. **[0.305A[**

Discussion Questions

1. Why are free electrons most important for electronics ?
2. Why do insulators not have any free electrons ?
3. Where do you apply Thevenin's theorem ?
4. Why is maximum power transfer theorem important in electronic circuits ?
5. What are the practical applications of a constant current source ?

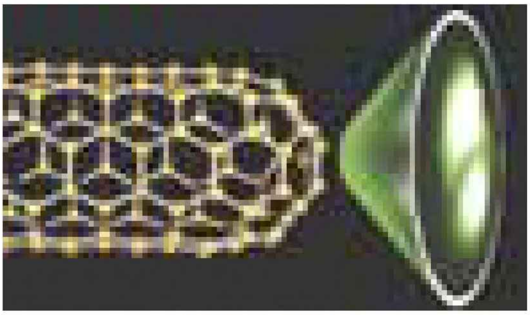
2

Electron Emission

2.1 Electron Emission
2.2 Types of Electron Emission
2.3 Thermionic Emission
2.4 Thermionic Emitter
2.5 Commonly Used Thermionic Emitters
2.6 Cathode Construction
2.7 Field Emission
2.8 Secondary Emission
2.9 Photo Electric Emission

INTRODUCTION

The reader is familiar with the current conduction (*i.e.* flow of electrons) through a conductor. The valence electrons of the conductor atoms are loosely bound to the atomic nuclei. At room temperature, the thermal energy in the conductor is adequate to break the bonds of the valence electrons and leave them unattached to any one nucleus. These unbound electrons move at random within the conductor and are known as *free electrons*. If an electric field is applied across the conductor, these free electrons move through the conductor in an orderly manner, thus constituting electric current. This is how these free electrons move through the conductor or electric current flows through a wire.



Electron Emission

Many electronic devices depend for their operation on the movement of electrons in an evacuated space. For this purpose, the free electrons must be ejected from the surface of metallic conductor by supplying sufficient energy from some external source. This is known as *electron emission*. The emitted electrons can be made to move in vacuum under the influence of an electric field, thus constituting electric current in vacuum. In this chapter, we shall confine our attention to the various aspects of electron emission.

2.1 Electron Emission

The liberation of electrons from the surface of a substance is known as **electron emission.**

For electron emission, metals are used because they have many free electrons. If a piece of metal is investigated at room temperature, the random motion of free electrons is as shown in Fig. 2.1. However, these electrons are free only to the extent that they may transfer from one atom to another within the metal but they cannot leave the metal surface to provide electron emission. It is because the free electrons that start at the surface of metal find behind them positive nuclei pulling them back and none pulling forward. Thus at the surface of a metal, a free electron encounters forces that prevent it to leave the metal. In other words, the metallic surface offers a barrier to free electrons and is known as *surface barrier*.

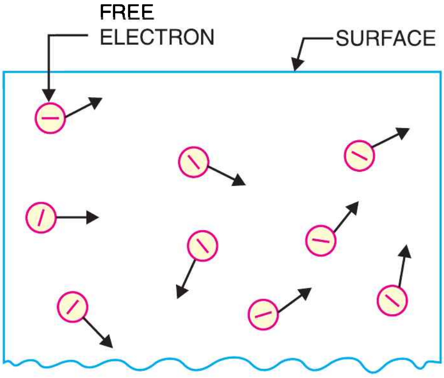


Fig. 2.1

However, if sufficient external energy is given to the free electron, its kinetic energy is increased and thus electron will cross over the surface barrier to leave the metal. This additional energy required by an electron to overcome the surface barrier of the metal is called *work function* of the metal.

The amount of additional energy required to emit an electron from a metallic surface is known as **work function** *of that metal.*

Thus, if the total energy required to liberate an electron from a metal is 4 eV* and the energy already possessed by the electron is 0.5 eV, then additional energy required (*i.e.*, work function) is 4.0– 0.5 = 3.5 eV. The work function of pure metals varies roughly from 2 to 6 eV. It depends upon the nature of metal, its purity and the conditions of its surface. It may be noted that it is desirable that metal used for electron emission should have low work function so that a small amount of energy is required to cause emission of electrons.

2.2 Types of Electron Emission

The electron emission from the surface of a metal is possible only if sufficient additional energy (*equal to the work function of the metal*) is supplied from some external source. This external energy may come from a variety of sources such as heat energy, energy stored in electric field, light energy or kinetic energy of the electric charges bombarding the metal surface. Accordingly, there are following four principal methods of obtaining electron emission from the surface of a metal :

---

* Work function is the additional energy required for the liberation of electrons. Therefore, it should have the conventional unit of energy *i.e.* joules. But this unit is very large for computing electronics work. Therefore, in practice, a smaller unit called *electron volt* (abbreviated as eV) is used.

One electron-volt is the amount of energy acquired by an electron when it is accelerated through a potential difference of 1 V.

Thus, if an electron moves from a point of 0 potential to a point of +10V, then amount of energy acquired by the electron is 10 eV.

Since charge on an electron = 1.602×10^{-19} C and voltage = 1 V,

$\therefore$ 1 electron-volt = $Q\,V = (1.602 \times 10^{-19}) \times 1$ J

or 1 eV = 1.602×10^{-19} J

(*i*) **Thermionic emission.** In this method, the metal is heated to sufficient temperature (about 2500°C) to enable the free electrons to leave the metal surface. The number of electrons emitted depends upon the temperature. The higher the temperature, the greater is the emission of electrons. This type of emission is employed in vacuum tubes.

(*ii*) **Field emission.** In this method, a strong electric field (*i.e.* a high positive voltage) is applied at the metal surface which pulls the free electrons out of metal because of the attraction of positive field. The stronger the electric field, the greater is the electron emission.

(*iii*) **Photo-electric emission.** In this method, the energy of light falling upon the metal surface is transferred to the free electrons within the metal to enable them to leave the surface. The greater the intensity (*i.e.* brightness) of light beam falling on the metal surface, the greater is the photo-electric emission.

(*iv*) **Secondary emission.** In this method, a high velocity beam of electrons strikes the metal surface and causes the free electrons of the metal to be knocked out from the surface.

2.3 Thermionic Emission

The process of electron emission from a metal surface by supplying thermal energy to it is known as **thermionic emission**.

At ordinary temperatures, the energy possessed by free electrons in the metal is inadequate to cause them to escape from the surface. When heat is applied to the metal, some of heat energy is converted into kinetic energy, causing accelerated motion of free electrons. When the temperature rises sufficiently, these electrons acquire additional energy equal to the work function of the metal. Consequently, they overcome the restraining surface barrier and leave the metal surface.

Metals *with lower work function* will require less additional energy and, therefore, will emit electrons at lower temperatures. The commonly used materials for electron emission are *tungsten, thoriated tungsten* and *metallic oxides of barium and strontium.* It may be added here that high temperatures are necessary to cause thermionic emission. For example, pure tungsten must be heated to about 2300°C to get electron emission. However, oxide coated emitters need only 750°C to cause thermionic emission.

Richardson-Dushman equation. The amount of thermionic emission increases rapidly as the emitter temperature is raised. The emission current density is given by Richardson-Dushman equation given below :

$$J_s = A\,T^2\, e^{-\frac{b}{T}} \text{ amp/m}^2 \qquad \ldots(i)$$

where J_s = emission current density *i.e.* current per square metre of the emitting surface

T = absolute temperature of emitter in K

A = constant, depending upon the type of emitter and is measured in amp/m^2/K^2

b = a constant for the emitter

e = natural logarithmic base

The value of b is constant for a metal and is given by :

$$b = \frac{\phi e}{k}$$

where ϕ = work function of emitter

e = electron charge = 1.602×10^{-19} coulomb

k = Boltzmann's constant = 1.38×10^{-23} J/K

$$\therefore \qquad b = \frac{\phi \times 1.602 \times 10^{-19}}{1.38 \times 10^{-23}} = 11600\,\phi\text{ K}$$

Putting the value of b in exp. (i), we get,

$$J_s = AT^2 e^{-\frac{11600\,\phi}{T}} \qquad \text{...}(ii)$$

The following points may be noted from eqn. (ii) :

(i) The emission is markedly affected by temperature changes. Doubling the temperature of an emitter may increase electron emission by more than 10^7 times. For instance, emission from pure tungsten metal is about 10^{-6} ampere per sq. cm. at 1300°C but rises to enormous value of about 100 amperes when temperature is raised to 2900°C.

(ii) Small changes in the work function of the emitter can produce enormous effects on emission. Halving the work function has exactly the same effect as doubling the temperature.

Example 2.1. *A tungsten filament consists of a cylindrical cathode 5 cm long and 0.01 cm in diameter. If the operating temperature is 2500 K, find the emission current. Given that* $A = 60.2 \times 10^4\ A/m^2/K^2$, $\phi = 4.517$ *eV.*

Solution. $A = 60.2 \times 10^4\ \text{amp/m}^2/\text{K}^2,\ T = 2500\ \text{K},\ \phi = 4.517\ \text{eV}$

$\therefore\quad b = 11600\,\phi\,\text{K} = 11600 \times 4.517\ \text{K} = 52400\ \text{K}$

Using Richardson-Dushman equation, emission current density is given by :

$$\begin{aligned} J_s &= AT^2 e^{-\frac{b}{T}}\ \text{amp/m}^2 = 60.2 \times 10^4 \times (2500)^2 \times (2.718)^{-\frac{52400}{2500}} \\ &= 0.3 \times 10^4\ \text{amp/m}^2 \end{aligned}$$

$$\text{Surface area of cathode, } a = \pi d l = 3.146 \times 0.01 \times 5 = 0.157\ \text{cm}^2 = 0.157 \times 10^{-4}\ \text{m}^2$$

$$\therefore \quad \text{Emission current} = J_s \times a = (0.3 \times 10^4) \times (0.157 \times 10^{-4}) = \mathbf{0.047\ A}$$

Example 2.2. *A tungsten wire of unknown composition emits 0.1 amp/cm² at a temperature of 1900 K. Find the work function of tungsten filament. Determine whether the tungsten is pure or contaminated with substance of lower work function. Given that* $A = 60.2$ *amp/cm²/K².*

Solution. $J_s = 0.1\ \text{amp/cm}^2;\ A = 60.2\ \text{amp/cm}^2/\text{K}^2;\ T = 1900\ \text{K}$

Let ϕ electron-volt be the work function of the filament.

$\therefore\quad b = 11600\,\phi\ \text{K}$

Using Richardson-Dushman equation, emission current density is given by :

$$\begin{aligned} J_s &= A\,T^2 e^{-\frac{b}{T}}\ \text{amp/cm}^2 \\ \text{or} \quad 0.1 &= 60.2 \times (1900)^2 \times e^{-\frac{11600\phi}{1900}} \\ \text{or} \quad e^{-\frac{11600\phi}{1900}} &= \frac{0.1}{60.2 \times (1900)^2} = 4.6 \times 10^{-10} \\ \text{or} \quad e^{-6.1\,\phi} &= 4.6 \times 10^{-10} \\ \text{or} \quad -6.1\,\phi \log_e e &= \log_e 4.6 - 10 \log_e 10 \\ \text{or} \quad -6.1\,\phi &= 1.526 - 23.02 \\ \therefore \quad \phi &= \frac{1.526 - 23.02}{-6.1} = \mathbf{3.56\ eV} \end{aligned}$$

Since the work function of pure tungsten is 4.52 eV, the sample must be contaminated. Thoriated tungsten has a work function ranging from 2.63 eV to 4.52 eV, depending upon the percentage of metallic thorium. Therefore, the sample is most likely to be thoriated tungsten.

2.4 Thermionic Emitter

Thermionic Emitter

The substance used for electron emission is known as an *emitter* or *cathode*. The cathode is heated in an evacuated space to emit electrons. If the cathode were heated to the required temperature in open air, it would burn up because of the presence of oxygen in the air. A cathode should have the following properties:

(*i*) **Low work function.** The substance selected as cathode should have low work function so that electron emission takes place by applying small amount of heat energy *i.e.* at low temperatures.

(*ii*) **High melting point.** As electron emission takes place at very high temperatures (>1500°C), therefore, the substance used as a cathode should have high melting point. For a material such as copper, which has the advantage of a low work function, it is seen that it cannot be used as a cathode because it melts at 810°C. Consequently, it will vaporise before it begins to emit electrons.

(*iii*) **High mechanical strength.** The emitter should have high mechanical strength to withstand the bombardment of positive ions. In any vacuum tube, no matter how careful the evacuation, there are always present some gas molecules which may form ions by impact with electrons when current flows. Under the influence of electric field, the positive ions strike the cathode. If high voltages are used, the cathode is subjected to considerable bombardment and may be damaged.

2.5 Commonly Used Thermionic Emitters

The high temperatures needed for satisfactory thermionic emission in vacuum tubes limit the number of suitable emitters to such substances as *tungsten, thoriated tungsten* and certain *oxide coated metals.*

Thoriated Tungsten

(*i*) **Tungsten.** It was the earliest material used as a cathode and has a slightly higher work function (4.52 eV). The important factors in its favour are : high melting point (3650 K), greater mechanical strength and longer life. The disadvantages are : high operating temperature (2500 K), high work function and low emission efficiency. Therefore, it is used in applications involving voltages exceeding 5 kV *e.g.* in X-ray tubes.

(*ii*) **Thoriated tungsten.** A mixture of two metals may have a lower work function than either of the pure metals alone. Thus, a tungsten emitter with a small quantity of thorium has a work function of 2.63 eV, compared with 3.4 eV for thorium and 4.52 eV for tungsten. At the same time, thoriated tungsten provides thermionic emission at lower temperature (1700°C) with consequent reduction in the heating power required.

In the manufacture of this type of cathode, tungsten filament is impregnated with thorium oxide and heated to a very high temperature (1850°C to 2500°C). The thorium oxide is reduced to metallic thorium and coats the filament surface with a thin layer of thorium. Thoriated tungsten cathodes are used for intermediate power tubes at voltages between 500 to 5000 volts.

(*iii*) **Oxide-coated cathode.** The cathode of this *type consists of a nickel ribbon coated with barium and strontium oxides. The oxide-coated cathode has low work function (1.1 eV), operates at comparatively low temperature (750°C) and has high emission efficiency. However, the principal limitation of oxide-coated cathode is that it cannot withstand high voltages. Therefore, it is mostly used in receiving tubes or where voltages involved do not exceed 1000 volts.

---

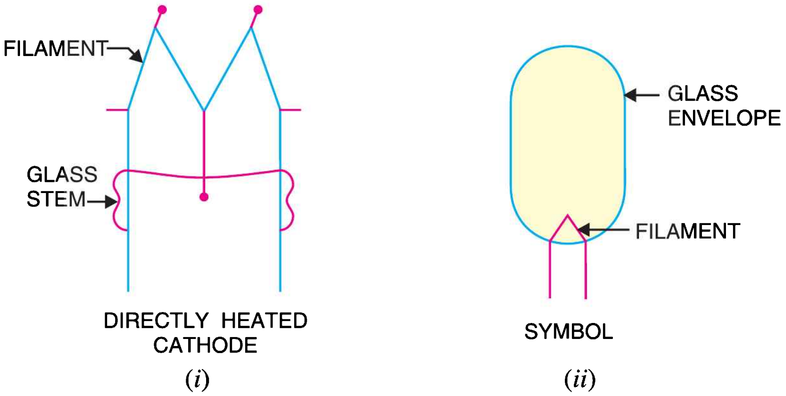
* Oxides of any alkaline-earth metal (*e.g.* calcium, strontium, barium etc.) have very good emission characteristics. In the manufacture of this type of emitter, the base metal (*e.g.* nickel) is first coated with a mixture of strontium and barium carbonates. It is then heated to a high temperature in vacuum glass tube until the carbonates decompose into oxides. By proper heating, a layer of oxides of barium and strontium is coated over the cathode surface to give oxide-coated emitter.

S.No.	Emitter	Work Function	Operating temperature	Emission efficiency
1	*Tungsten*	4.52 eV	2327°C	4 mA/watt
2	*Thoriated tungsten*	2.63 eV	1700°C	60 mA/watt
3	*Oxide-coated*	1.1 eV	750°C	200 mA/watt

2.6 Cathode Construction

As cathode is sealed in vacuum, therefore, the most convenient way to heat it is electrically. On this basis, the thermionic cathodes are divided into two types viz directly heated cathode and indirectly heated cathode.

(*i*) **Directly heated cathode.** In this type, the cathode consists of oxide-coated nickel ribbon, called the *filament. The heating current is directly passed through this ribbon which emits the electrons. Fig. 2.2 (*i*) shows the structure of directly heated cathode whereas Fig. 2.2 (*ii*) shows its symbol.



(*i*) (*ii*)

Fig. 2.2

The directly heated cathode is more efficient in converting heating power into thermionic emission. Therefore, it is generally used in power tubes that need large amounts of emission and in small tubes operated from batteries where efficiency and quick heating are important. The principal limitation of this type of cathode is that any variation in heater voltage affects the electron emission and thus produces *hum* in the circuit.

(*ii*) **Indirectly heated cathode.** In this type, the cathode consists of a thin metal sleeve coated with barium and strontium oxides. A filament or heater is enclosed within the sleeve and insulated from it. There is no electrical connection between the heater and the cathode. The heating current is passed through the heater and the cathode is heated indirectly through heat transfer from the heater element. Fig. 2.3 (*i*) shows the structure of indirectly heated cathode whereas Fig. 2.3 (*ii*) shows its symbol.

---

* ***Filament.*** The term filament (literally means a thin wire) denotes the element through which the cathode heating current flows. In case of directly heated, cathode is itself the filament. If indirectly heated, heater is the filament.

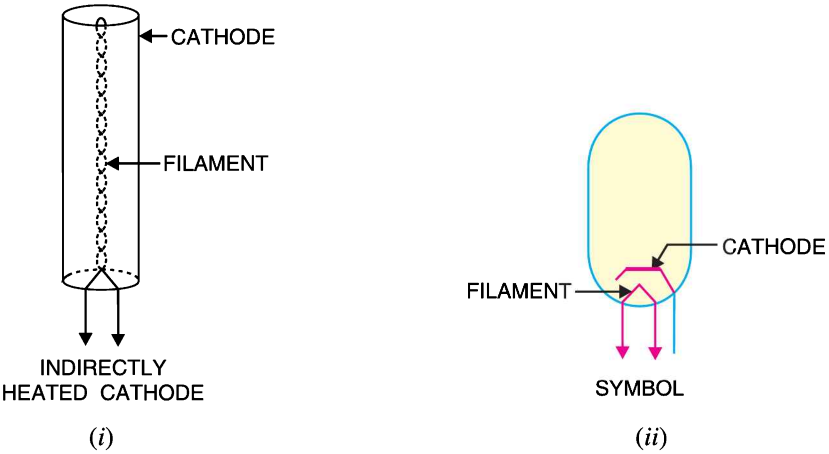


Fig. 2.3

Indirectly heated cathode has many advantages. As cathode is completely separated from the heating circuit, therefore, it can be readily connected to any desired potential as needed, independent of the heater potential. Furthermore, because of relatively large mass of cylindrical cathode, it takes time to heat or cool and as such does not introduce hum due to heater voltage fluctuations. Finally, a.c. can be used in the heater circuit to simplify the power requirements. Almost all modern receiving tubes use this type of cathode.

2.7 Field Emission

The process of electron emission by the application of strong electric field at the surface of a metal is known as **field emission.**

When a metal surface is placed close to a high voltage conductor which is positive *w.r.t.* the metal surface, the electric field exerts attractive force on the free electrons in the metal. If the positive potential is great enough, it succeeds in overcoming the restraining forces of the metal surface and the free electrons will be emitted from the metal surface as shown in Fig. 2.4.

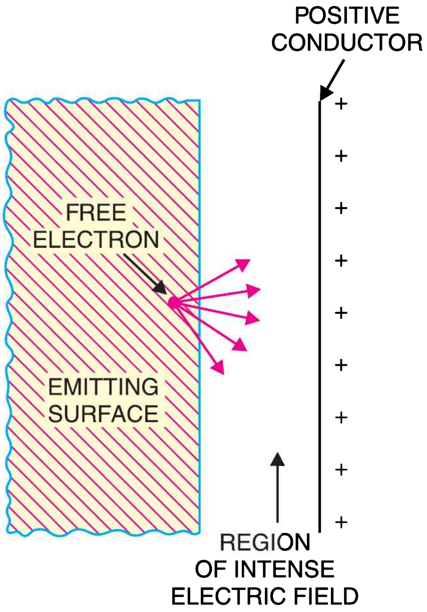


Fig. 2.4

Very intense electric field is required to produce field emission. Usually, a voltage of the order of a million volts per centimetre distance between the emitting surface and the positive conductor is necessary to cause field emission. Field emission can be obtained at temperatures much lower (*e.g.* room temperature) than required for thermionic emission and, therefore, it is also sometimes called *cold cathode emission* or *auto- electronic emission.*

2.8 Secondary Emission

Electron emission from a metallic surface by the bombardment of high-speed electrons or other particles is known as **secondary emission.**

When high-speed electrons suddenly strike a metallic surface, they may give some or all of their kinetic energy to the free electrons in the metal. If the energy of the striking electrons is sufficient, it may cause free electrons to escape from the metal surface. This phenomenon is called *secondary emission*. The electrons that strike the metal are called *primary electrons* while the emitted electrons are known as *secondary electrons*. The intensity of secondary emission depends upon the emitter material, mass and energy of the bombarding particles.

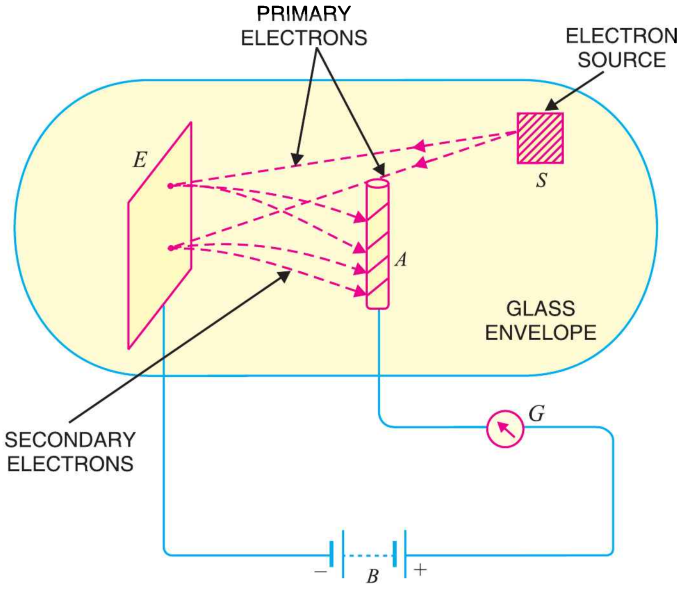


Fig. 2.5

The principle of secondary emission is illustrated in Fig. 2.5. An evacuated glass envelope contains an emitting surface *E*, the collecting anode *A* and a source of primary electrons *S*. The anode is maintained at positive potential *w.r.t.* the emitting surface by battery *B*. When the primary electrons strike the emitting surface *E*, they knock out secondary electrons which are attracted to the anode and constitute a flow of current. This current may be measured by connecting a sensitive galvanometer *G* in the anode circuit.

The effects of secondary emission are very undesirable in many electronic devices. For example, in a tetrode valve, secondary emission is responsible for the negative resistance. In some electronic devices, however, secondary emission effects are utilised *e.g.* *electron multiplier, cathode ray tube etc.

2.9 Photo Electric Emission

Electron emission from a metallic surface by the application of light is known as **photo electric emission.**

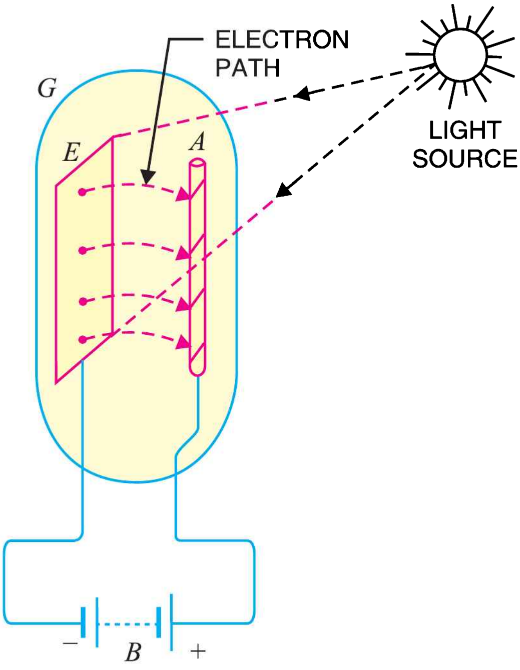


Fig. 2.6

When a beam of light strikes the surface of certain metals (*e.g.* potassium, sodium, cesium), the energy of photons of light is transferred to the free electrons within the metal. If the energy of the striking photons is greater than the work function of the metal, then free electrons will be knocked out from the surface of the metal. The emitted electrons are known as *photo electrons* and the phenomenon is known as *photoelectric emission*. The amount of photoelectric emission depends upon the intensity of light falling upon the emitter and frequency of radiations. The greater the intensity and frequency of radiations, the greater is the photo electric emission. Photo-electric emission is utilised in photo tubes which form the basis of television and sound films.

---

* An interesting aspect of secondary emission is that a high-speed bombarding electron may liberate as many as 10 "secondary electrons". This amounts to a multiplication of electron flow by a ratio as great as 10 and is utilised in current multiplier devices.

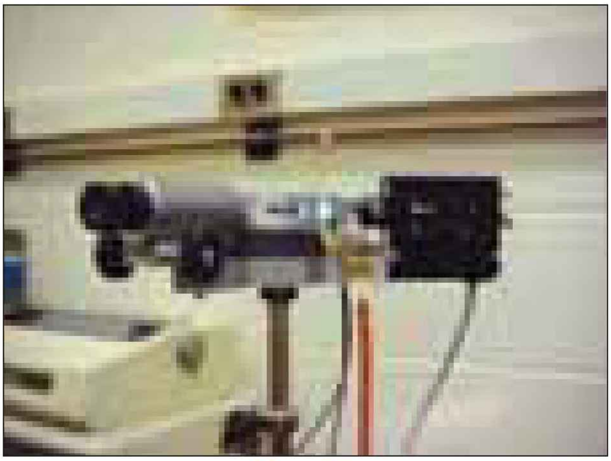


Photo Tube

Fig. 2.6 illustrates the phenomenon of photoelectric emission. The emitter *E* and anode *A* are enclosed in an evacuated glass envelope *G*. A battery *B* maintains the anode at positive potential w.r.t. emitter. When light of suitable intensity and frequency falls on the emitter, electrons are ejected from its surface. These electrons are attracted by the positive anode to constitute current in the circuit. It may be noted that current will exist in the circuit so long as illumination is maintained.

MULTIPLE-CHOICE QUESTIONS

1. Work function of metals is generally measured in ....

(*i*) joules (*ii*) electron-volt
(*iii*) watt-hour (*iv*) watt

2. The operating temperature of an oxide-coated emitter is about ....

(*i*) 750°C (*ii*) 1200°C
(*iii*) 2300°C (*iv*) 3650°C

3. .... is used in high voltage (> 10 kV) applications.

(*i*) tungsten emitter
(*ii*) oxide-coated emitter
(*iii*) thoriated-tungsten emitter
(*iv*) none of the above

4. A desirable characteristic of an emitter is that it should have .... work function.

(*i*) large (*ii*) very large
(*iii*) small (*iv*) none of the above

5. The thermionic emitter that has the highest operating temperature is ....

(*i*) oxide-coated (*ii*) thoriated-tungsten
(*iii*) tungsten (*iv*) none of the above

6. If the temperature of an emitter is increased two times, the electron emission is ....

(*i*) increased two times
(*ii*) increased four times
(*iii*) increased several million times
(*iv*) none of the above

7. In X-ray tubes, ... emitter is used.

(*i*) thoriated tungsten
(*ii*) tungsten
(*iii*) oxide-coated
(*iv*) none of the above

8. The life of an oxide-coated emitter is about ....

(*i*) 500 hours (*ii*) 1000 hours
(*iii*) 200 hours (*iv*) 10,000 hours

9. The electrons emitted by a thermionic emitter are called ....

(*i*) free electrons
(*ii*) loose electrons
(*iii*) thermionic electrons
(*iv*) bound electrons

10. The work function of an oxide-coated emitter is about ....

(*i*) 1.1 eV (*ii*) 4 eV

(*iii*) 2.63 eV (*iv*) 4.52 eV

11. The warm-up time of a directly heated cathode is .... that of indirectly heated cathode.

(*i*) more than (*ii*) less than

(*iii*) same as (*iv*) data incomplete

12. The most commonly used emitter in the tubes of a radio receiver is ....

(*i*) tungsten (*ii*) thoriated-tungsten

(*iii*) oxide-coated (*iv*) none of the above

13. Field emission is utilised in ....

(*i*) vacuum tubes

(*ii*) TV picture tubes

(*iii*) gas-filled tubes

(*iv*) mercury pool devices

14. Oxide-coated emitters have electron emission of .... per watt of heating power.

(*i*) 5-10 mA (*ii*) 40-90 mA

(*iii*) 50-100 mA (*iv*) 150-1000 mA

15. The oxide-coated cathodes can be used for voltages upto ....

(*i*) 1000 V (*ii*) 3000 V

(*iii*) 4000 V (*iv*) 10,000 V

Answers to Multiple-Choice Questions

1.	(*ii*)	**2.**	(*i*)	**3.**	(*i*)	**4.**	(*iii*)	**5.**	(*iii*)
6.	(*iii*)	**7.**	(*ii*)	**8.**	(*iv*)	**9.**	(*iii*)	**10.**	(*i*)
11.	(*ii*)	**12.**	(*iii*)	**13.**	(*iv*)	**14.**	(*iv*)	**15.**	(*i*)

Chapter Review Topics

1. What is electron emission ? Explain the terms : surface barrier and work function.
2. What general conditions must be satisfied before an electron can escape from the surface of a material ?
3. Name and explain briefly four practical ways by which electron emission can occur.
4. What are the materials used for thermionic emitters ? Compare the relative merits of each.
5. Discuss briefly construction and relative advantages of directly and indirectly heated cathodes.

Problems

1. An oxide-coated emitter has a surface area of 0.157 cm^2. If the operating temperature is 110 K, find the emission current. Given $A = 100\ \text{A/m}^2/\text{K}^2$, work function = 1.04 eV. **[0.0352 A]**
2. A tungsten filament of unknown composition emits 1000 A/m^2 at an operating temperature of 1900 K. Find the work function of tungsten filament. Given $A = 60.2 \times 10^4\ \text{A/m}^2/\ \text{K}^2$. **[3.44 eV]**
3. Calculate the total emission available from barium-strontium oxide emitter, 10 cm long and 0.01 cm in diameter, operated at 1900 K. Given that $A = 10^{-12}\ \text{Amp/cm}^2/\text{K}^2$ and b = 12,000. **[0.345 A]**

Discussion Questions

1. Why does electron emission not occur at room temperature ?
2. Why are high temperatures necessary for thermionic emission ?
3. Why are electron emitters heated electrically ?
4. Why are thermionic emitters heated in vacuum ?
5. Why are tungsten and thoriated tungsten cathodes always of directly heated type ?
6. Why cannot oxide-coated cathodes be used for voltages exceeding 1000 volts?
7. Why do directly heated cathodes introduce hum in the circuit ?
8. Why are directly heated cathodes used in high power applications ?

3

Gas-Filled Tubes

3.1 Gas-Filled Tubes
3.2 Conduction in a Gas
3.3 Cold-Cathode Gas Diode
3.4 Characteristics of Cold-Cathode Diode
3.5 Applications of Glow Tubes
3.6 Hot-Cathode Gas Diode
3.7 Thyratron
3.8 Applications of Thyratron

INTRODUCTION

In the vacuum tubes, the electrons flow from cathode to anode in vacuum. In such tubes, extreme care is taken to produce as perfect a vacuum as possible to prevent ionisation of gases and the resulting large uncontrolled currents. It may be mentioned here that the secret of triode is the fine control of free electrons within valve by the electrostatic fields of grid and anode. If gas is present even in small amount, the electrons flowing from cathode to anode will cause ionisation of the gas. The ionised molecules would interfere with the control and make the device useless as an amplifier.

In certain applications, fine control of electrons within the valve is of less importance than the efficient handling and turning on and off of heavy currents. In such situations, some inert gases (*e.g.* argon, neon, helium) at low pressures are purposely introduced into the valve envelope. Such tubes are known as *gas-filled tubes*. The gas-filled tubes are capable of doing various jobs that vacuum tubes cannot perform and which are especially useful in industrial and control circuits. In this chapter, we shall focus our attention on some important types of gas-filled tubes with special reference to their characteristic properties.

Gas-filled Tube

3.1 Gas-Filled Tubes

A **gas-filled** *tube is essentially a vacuum tube having a small amount of some inert gas at low pressure.*

The gas pressure in a gas-filled tube usually ranges from 10 mm of Hg to 50 mm. The construction of gas-filled tubes is similar to that of vacuum tubes, except that the cathodes, grids and anodes are usually larger in order to carry heavier current. However, the characteristic properties of the two are markedly different. Firstly, a gas-filled tube can conduct much *more current than the equivalent vacuum tube. It is because the electrons flowing from cathode to anode collide with gas molecules and ionise them *i.e.* knock out electrons from them. The additional electrons flow to the anode together with the original electrons, resulting in the increase in plate current. Secondly, a gas filled tube has far less control on the electrons in the tube than that of vacuum tube. Once the ionisation starts, the control of gas-filled tube is tremendously reduced.

Classification. Gas-filled tubes are usually classified according to the type of electron emission employed. On this basis, they may be classified into two types namely; *cold-cathode type* and *hot-cathode type.*

Cold-cathode type. In this type of gas-filled tubes, the cathode is not heated as in a vacuum tube. The ionisation of the gas is caused by the energy available from natural sources such as cosmic rays, sun rays or radioactive particles in air. These natural sources are the underlying reasons for the start of conduction in cold-cathode gas tubes. Most cold-cathode tubes are used as diodes.

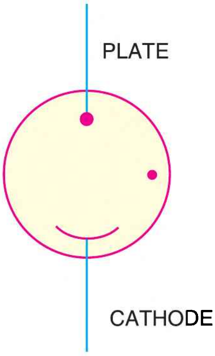


Fig. 3.1

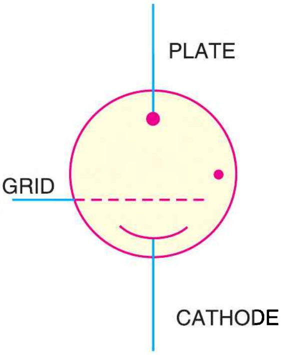


Fig. 3.2

Fig. 3.1 shows the schematic symbol for a cold-cathode gas diode, known as *glow tube.* The dot within the circle indicates the presence of gas. Fig. 3.2 shows the schematic symbol of cold-cathode gas triode, known as *grid glow tube.*

Hot-cathode type. In this type of gas-filled tubes, the cathode is heated just as in an ordinary vacuum tube. The electrons flowing from cathode to plate cause ionisation of the gas molecules. Such tubes are used as diodes, triodes and tetrodes.

---

* The ability of a gas-filled tube to carry large current is, of course, no recommendation in itself. A copper wire will do the same thing and with better efficiency. But a gas filled tube has one special ability which the wire does not possess ; the ability to carry current in one direction.

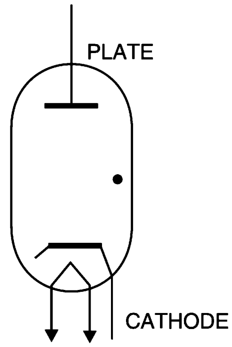


Fig. 3.3

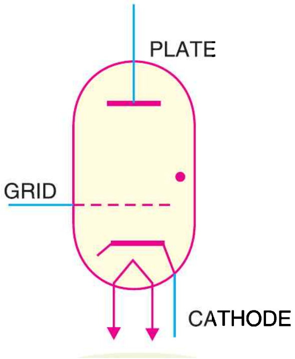


Fig. 3.4

Fig. 3.3 shows the schematic symbol of a hot-cathode gas diode, known as *phanotron* whereas Fig. 3.4 shows the symbol of hot-cathode gas triode, known as *thyratron*.

3.2 Conduction in a Gas

A gas under ordinary pressure is a perfect insulator and cannot conduct current. However, if the gas pressure is low, it is possible to produce a large number of free electrons in the gas by the process of ionisation and thus cause the gas to become a conductor. This is precisely what happens in gas-filled tubes. The current conduction in a gas at low pressure can be beautifully illustrated by referring to the hot-cathode gas diode shown in Fig. 3.5. The space between cathode and anode of the tube contains gas molecules. When cathode is heated, it emits a large number of electrons. These electrons form a cloud of electrons near the cathode, called **space charge.** If anode is made positive *w.r.t.* cathode, the electrons (magenta dots) from the space charge speed towards the anode and collide with gas molecules (cyan circles) in the tube.

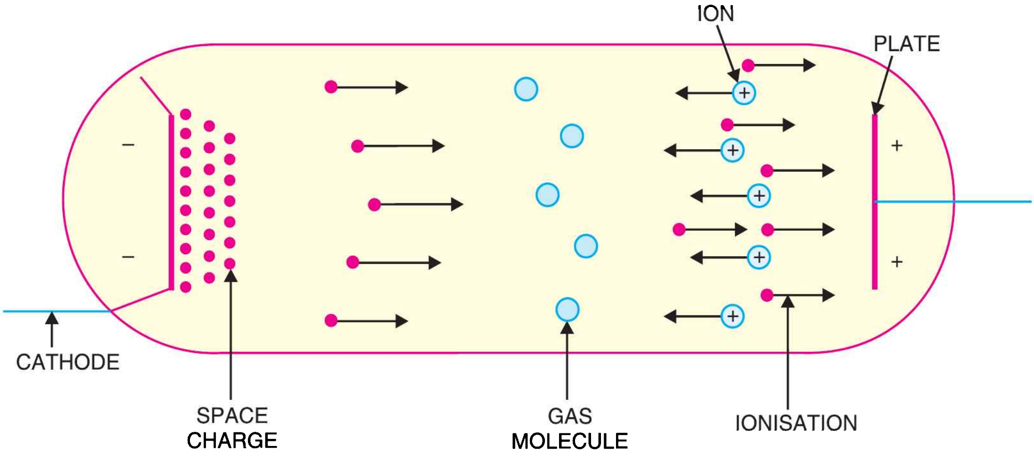


Fig. 3.5

If the anode-cathode voltage is low, the electrons do not possess the necessary energy to cause ionisation of the gas. Therefore, the plate current flow in the tube is only due to the electrons emitted by the cathode. As the anode-cathode voltage is increased, the electrons acquire more speed and energy and a point–called *ionisation voltage* is reached, where ionisation of the gas starts. The ionisation of gas produces free electrons and positive gas ions (cyan circles with +ve signs). The additional free electrons flow to the anode together with the original electrons, thus increasing plate current. However, the increase in plate current due to these added electrons is practically negligible. But the major effect is that the positive gas ions slowly drift towards the cathode and neutralise the space charge. Consequently, the resistance of the tube decreases, resulting in large plate current. *Hence, it is due to the neutralisation of space charge by the positive gas ions that plate current in a gas tube is too much increased.*

The following points may be noted regarding the conduction in a gas at low pressure :

(*i*) At low anode-cathode voltage, the ionisation of the gas does not occur and the plate current is about the same as for a vacuum tube at the same anode voltage.

(*ii*) At some anode-cathode voltage, called ionisation voltage, ionisation of the gas takes place. The plate current increases dramatically to a large value due to the neutralisation of space charge by the positive gas ions. The ionisation voltage depends upon the type and pressure of gas in the tube.

(*iii*) Once ionisation has started, it is maintained at anode-cathode voltage much lower than ionisation voltage. However, minimum anode-cathode voltage, called *deionising voltage*, exists below which ionisation cannot be maintained. Under such conditions, the positive gas ions combine with electrons to form neutral gas molecules and conduction stops. Because of this switching action, a gas-filled tube can be used as an electronic switch.

3.3 Cold-Cathode Gas Diode

Fig. 3.6 shows the cut-away view of cold-cathode gas diode. It essentially consists of two electrodes, cathode and anode, mounted fairly close together in an envelope filled with some inert gas at low pressure. The anode is in the form of a thin wire whereas cathode is of cylindrical metallic surface having oxide coating. The anode is always held at positive potential *w.r.t.* cathode.

Operation. Fig. 3.7 shows a circuit that can be used to investigate the operation of cold-cathode gas diode. Electric conduction through the tube passes through three successive discharge phases *viz.* Townsend discharge, the glow discharge and the arc discharge.

(*i*) **Townsend discharge.** At low anode-cathode voltage, the tube conducts an extremely small current (1mA). It is because the cathode is cold and as such no source of electrons is present. However, natural sources (*e.g.* cosmic rays *etc.*) cause some ionisation of the gas, creating a few free electrons. These electrons move towards the anode to constitute a small current. This stage of conduction is known as **Townsend discharge*. In this phase of conduction, no visible light is associated.

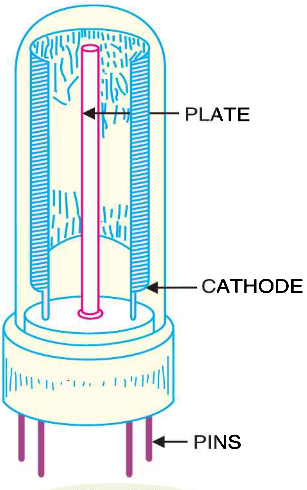


Fig. 3.6

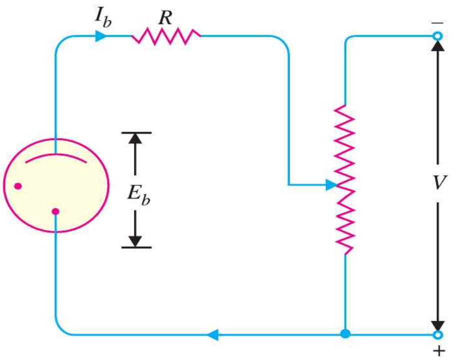


Fig. 3.7

---

* The volt-ampere characteristics of glow tube were first investigated by J. S. Townsend in 1901 and hence the name.

(*ii*) **Glow discharge.** As the anode-cathode voltage is increased, the electrons acquire more and more energy. At some voltage, known as *ionisation voltage*, ionisation of the gas starts and the tube current rises to a large value. The voltage across the tube drops to a low value, which remains constant regardless of the plate current. At the same time, glow is seen in the gas and on a portion of the cathode. This phase of conduction is known as *glow discharge*.

The fact that glow tube maintains constant voltage across it in the glow discharge region needs some explanation. In this region, any increase in supply voltage causes more current to flow; the drop across series resistance R increases but the voltage E_b across the tube remains constant. As the current increases, the degree of ionisation increases and the glow covers a greater part of cathode surface and hence the ionised gas path between cathode and anode has greater area of cross-section. As resistance is inversely proportional to the area of cross-section, therefore, resistance of the tube decreases. Hence, the voltage across the tube remains constant. Reverse is also true should the supply voltage decrease. Thus in the glow discharge region, the resistance of the tube changes so as to maintain constant voltage across it.

(*iii*) **Arc discharge.** Once the cathode glow covers the entire surface of the cathode, the x-sectional area of gas path cannot increase further. This region is known as *abnormal glow*. If the current density is further increased, the discharge becomes an arc.

3.4 Characteristics of Cold-Cathode Diode

The volt-ampere characteristic of a cold-cathode diode is shown in Fig. 3.8. At low anode-cathode voltage, the tube current is very small (1mA) and is due to the ionisation of gas molecules by the natural sources. This stage of conduction upto voltage B is known as *Townsend discharge* and is non-self maintained discharge because it requires an external source to cause ionisation. At some critical voltage such as B, the tube fires and the voltage across the tube drops (from B to C) and remains constant regardless of plate current. This is the start of second conduction and is known as *glow discharge*. In this region (C to D), voltage across the tube remains constant even if the plate current increases.

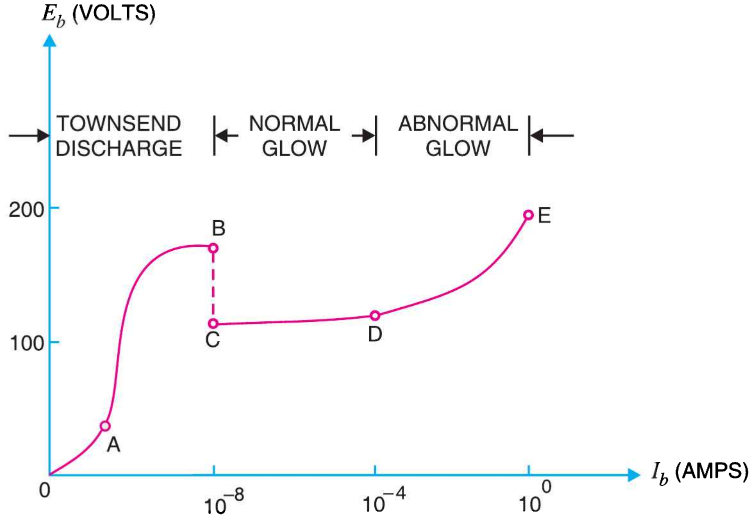


Fig. 3.8

After the glow discharge, the voltage across the tube no longer remains constant. Now, if the supply voltage is raised, not only will the circuit current increase but the voltage across the tube will start to rise again. This stage of conduction (D to E) is known as *abnormal glow*.

3.5 Applications of Glow Tubes

The outstanding characteristic of a cold-cathode gas diode (or glow tube) to maintain constant voltage across it in the glow discharge region renders it suitable for many industrial and control applications. A few of such applications are mentioned below :

(*i*) *As a voltage regulating tube.* A glow tube maintains constant voltage across it in the glow discharge region. This characteristic permits it to be used as a voltage regulating tube. Fig. 3.9 shows a simple circuit commonly used to maintain constant voltage across a load. The glow tube (*VR* tube) is connected in parallel with the load R_L across which constant voltage is desired. So long as the tube operates in the glow discharge region, it will maintain constant voltage (= 150V) across the load. The extra voltage is dropped across the series resistance *R*.

Voltage Regulating Tube

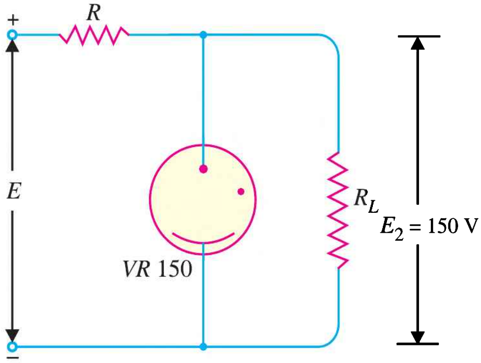


Fig. 3.9

(*ii*) *As a polarity indicator.* As the cathode is surrounded by a characteristic glow, therefore, it can be useful to indicate the polarity of a direct voltage.

(*iii*) *As an electronic switch*, which closes at ionisation potential, permitting a large current to flow, and opens at the deionising voltage, blocking the current flow.

(*iv*) *As a radio frequency field detector.* A strong radio-frequency field is capable of ionising the gas without direct connection to the tube. Therefore, the tube can indicate the presence of radio-frequency field.

3.6 Hot-Cathode Gas Diode

A hot-cathode gas diode is frequently used as a rectifier for moderate voltages because of high efficiency and better regulation. A hot-cathode gas diode consists of an oxide-coated cathode and a metallic anode enclosed in a glass envelope containing some inert gas under reduced pressure. For proper operation of the tube, anode is always held at a positive potential *w.r.t.* cathode.

Operation. Fig. 3.10 shows a circuit that can be used to investigate the operation of a hot-cathode gas diode. When cathode is heated, a large number of electrons are emitted. At low anode-cathode voltage, the tube conducts very small current. Under such conditions, the gas is not ionised and the tube acts similar to a vacuum diode — the voltage across the tube increases with plate current. This action continues until anode-cathode voltage becomes equal to the ionisation potential of the gas. Once this potential is reached, the gas begins to ionise, creating free electrons and positive gas ions. The positive gas ions move towards the cathode and tend to neutralise the space charge, thus decreasing the internal resistance of the tube. If now the plate voltage is increased, the plate current also increases due to increased degree of ionisation. This further reduces the tube resistance. As a result, increase in plate current is offset by the decrease in tube resistance *and the voltage across the tube remains constant.* Therefore, in a hot-cathode gas diode, not only the internal drop within the tube is small but also it remains constant. For this reason, a gas diode has better efficiency and regulation than for a vacuum diode when used as a rectifier.

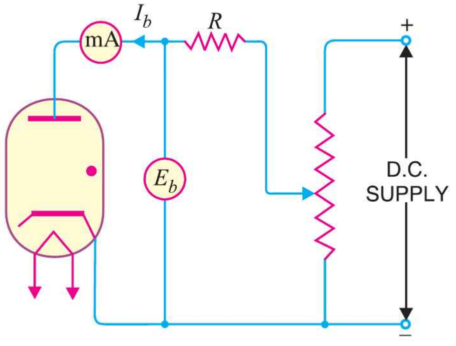


Fig. 3.10

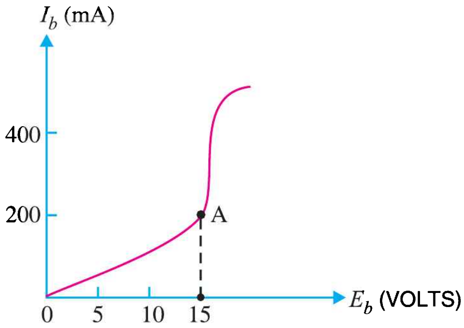


Fig. 3.11

Plate Characteristics. Fig. 3.10 shows the circuit that can be used to determine the volt-ampere (E_b/I_b) characteristics of a hot-cathode gas diode. The series resistance *R* is used to limit the current to reach a dangerously high value. Fig. 3.11 shows the plate characteristic of hot-cathode diode. It is clear that at first, plate current rises slowly with increase in anode-cathode voltage. However, at some voltage, known as ionisation voltage (point *A*), the plate current rises sharply and the voltage drop across the tube remains constant. The extra voltage is dropped across the series resistance *R*. Any attempt to raise the anode-cathode voltage above the ionising value is fruitless. Increasing the voltage E_b above point *A* results in higher plate current (I_b) and large drop across *R* but the voltage E_b across the tube remains constant.

3.7 Thyratron

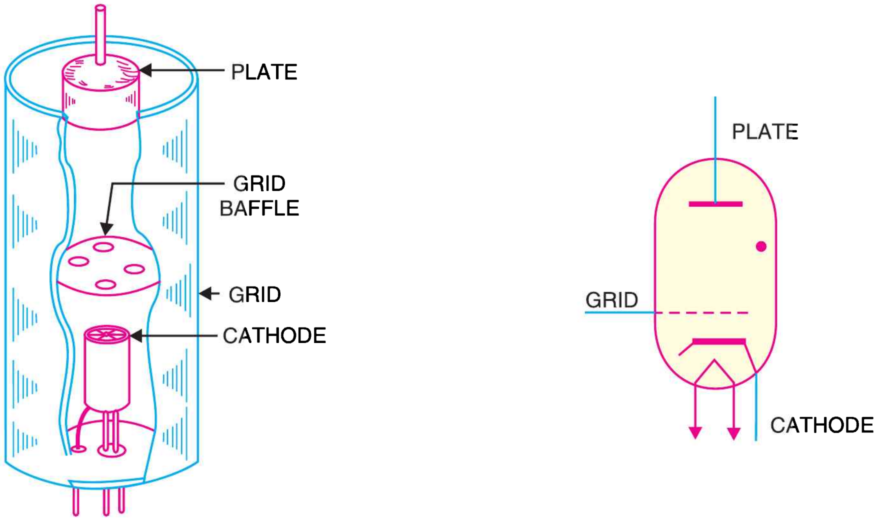
A hot-cathode gas triode is known by the trade name *thyratron*. As discussed before, a gas diode fires at a fixed plate potential, depending upon the type of gas used and gas pressure. Very often it is necessary to control the plate potential at which the tube is to fire. Such a control is obviously impossible with a gas diode. However, if a third electrode, known as *control grid* is introduced in a gas diode, this control is possible. The tube is then known as hot-cathode gas triode or thyratron. By controlling the negative potential on the control grid, the tube can be fired at any plate potential.

Construction. Figs. 3.12 (*i*) and 3.12 (*ii*) respectively show the cut-away view and schematic symbol of a thyratron. It consists of three electrodes, namely; *cathode, anode* and *control grid* enclosed in a glass envelope containing some inert gas at low pressure. The cathode and anode are approximately planar. The control grid of thyratron has a special structure quite different from that of a vacuum tube. It consists of a metal cylinder surrounding the cathode with one or more perforated discs known as *grid baffles* near the centre.

Operation. When cathode is heated, it emits plenty of electrons by thermionic emission. If the control grid is made sufficiently negative, the electrons do not have the necessary energy to ionise the gas and the plate current is substantially zero. As the negative grid voltage is reduced, the electrons acquire more speed and energy. At some grid voltage, called *critical grid voltage*, ionisation of the gas occurs and the plate current rises to a large value.

The negative grid voltage, for a given plate potential, at which ionisation of the gas starts is known as **critical grid voltage.**

At critical grid voltage, gas ionises, creating free electrons and positive gas ions. The positive ions tend to neutralise the space charge, resulting in large plate current. In addition, these positive ions are attracted by the negative grid and neutralise the normal negative field of the grid, thereby



(*i*) (*ii*)

Fig. 3.12

preventing the grid from exerting any further control on the plate current of the tube. The grid now loses all control and the tube behaves as a diode. *Therefore, the function of control grid is only to start the conduction of anode current.* Once the conduction is started, the tube acts as a gas diode. It is important to realise the usefulness of control grid. We have seen that the ionisation does not start at low values of plate current. In a gas diode, it requires that the plate potential should be increased until sufficient plate current is flowing to cause ionisation. However, by adjusting the negative voltage on the grid, the desired plate current can be obtained to cause ionisation.

It may be mentioned here that once the thyratron fires, the only way to stop conduction is to reduce plate voltage to zero for a period *long enough for deionisation of the gas in the tube.

3.8 Applications of Thyratron

As the grid voltage has no control over the magnitude of plate current once the thyratron fires, therefore, it cannot be used as an amplifier like a vacuum triode. However, because of its triggering action, it is useful in switching and relay applications. Thyratrons are also used as controlled rectifiers for controlling the amount of d.c. power fed to the load. They are also used in motor control circuits.

MULTIPLE-CHOICE QUESTIONS

1. A gas diode can conduct .... the equivalent vacuum diode for the same plate voltage.

(*i*) less current than
(*ii*) more current than
(*iii*) same current as
(*iv*) none of the above

2. A gas-filled tube has .... resistance before ionisation.

(*i*) very high (*ii*) small
(*iii*) very small (*iv*) zero

3. The PIV of a hot cathode gas diode is .... the equivalent vacuum diode.

(*i*) the same as that of
(*ii*) more than that of
(*iii*) less than that of
(*iv*) none of the above

---

* 100 to 1000 μsec.

4. The anode-to-cathode potential of a gas-filled tube at which gas deionises and stops conduction is called ....potential.
(*i*) extinction (*ii*) striking
(*iii*) ionising (*iv*) none of the above

5. A thyratron can be used as ....
(*i*) an oscillator (*ii*) an amplifier
(*iii*) a controlled switch
(*iv*) none of the above

6. The internal resistance of a gas-filled tube is .... that of a vacuum tube.
(*i*) the same as (*ii*) more than
(*iii*) less than (*iv*) none of the above

7. A cold cathode tube is generally used as a ....
(*i*) diode (*ii*) triode
(*iii*) tetrode (*iv*) pentode

8. Conduction in a cold cathode tube is started by ....
(*i*) thermionic emission
(*ii*) secondary emission
(*iii*) natural sources
(*iv*) none of the above

9. The cathode heating time of thermionic gas diode is .... that of a vacuum diode.
(*i*) the same as (*ii*) much more than
(*iii*) much less than (*iv*) none of the above

10. The solid state equivalent of thyratron is ....
(*i*) FET (*ii*) transistor
(*iii*) SCR (*iv*) crystal diode

11. The solid state equivalent of cold cathode diode is ....
(*i*) zener diode (*ii*) crystal diode
(*iii*) LED (*iv*) transistor

12. The noise in a gas-filled tube is .... that in a vacuum tube.
(*i*) the same as (*ii*) more than
(*iii*) less than (*iv*) none of the above

13. The ionisation potential in a gas diode depends upon ....
(*i*) plate current
(*ii*) cathode construction
(*iii*) size of the tube
(*iv*) type and pressure of gas

14. If the gas pressure in a gas-filled diode is increased, its PIV rating ....
(*i*) remains the same
(*ii*) is increased
(*iii*) is decreased
(*iv*) none of the above

15. Once a thyratron is fired, its control grid .... over the plate current.
(*i*) loses all control
(*ii*) exercises fine control
(*iii*) exercises rough control
(*iv*) none of the above

16. To stop conduction in a thyratron, the .... voltage should be reduced to zero.
(*i*) grid (*ii*) plate
(*iii*) filament (*iv*) none of the above

17. Ionisation of cold cathode diode takes place at .... plate potential compared to hot cathode gas diode.
(*i*) the same (*ii*) much higher
(*iii*) much lesser (*iv*) none of the above

18. A gas-filled tube has .... internal resistance after ionisation.
(*i*) low (*ii*) high
(*iii*) very high (*iv*) moderate

19. The gas-filled tubes can handle .... peak inverse voltage (PIV) as compared to equivalent vacuum tubes.
(*i*) more (*ii*) less
(*iii*) the same (*iv*) none of the above

20. A cold cathode diode is used as .... tube.
(*i*) a rectifier
(*ii*) a power-controlled
(*iii*) a regulating
(*iv*) an amplifier

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*i*)	**3.** (*iii*)	**4.** (*i*)	**5.** (*iii*)
6. (*iii*)	**7.** (*i*)	**8.** (*iii*)	**9.** (*ii*)	**10.** (*iii*)
11. (*i*)	**12.** (*ii*)	**13.** (*iv*)	**14.** (*iii*)	**15.** (*i*)
16. (*ii*)	**17.** (*ii*)	**18.** (*i*)	**19.** (*ii*)	**20.** (*iii*)

Chapter Review Topics

1. Explain the differences between a gas tube and equivalent vacuum tube.
2. Explain how ionisation takes place in a hot-gas diode. How does current conduction take place in such a tube ?
3. Give the schematic symbols of glow tube, hot-cathode gas diode and thyratron.
4. Explain the construction, operation and characteristics of a glow tube.
5. Discuss some applications of glow tubes.
6. What is a thyratron ? How does it differ from a vacuum triode ?
7. Write short notes on the following :
   (*i*) Characteristics of hot-cathode gas diode
   (*ii*) Applications of thyratrons

Discussion Questions

1. What are the advantages of gas tubes over vacuum tubes ?
2. What is the difference between the action of thyratron and vacuum triode ?
3. Why cannot thyratrons be used as rectifiers for high voltages ?
4. Can gas diodes be used as rectifiers for high voltages ?
5. What is the drawback of a gas diode compared to a thyratron ?

4

Atomic Structure

4.1 Bohr's Atomic Model

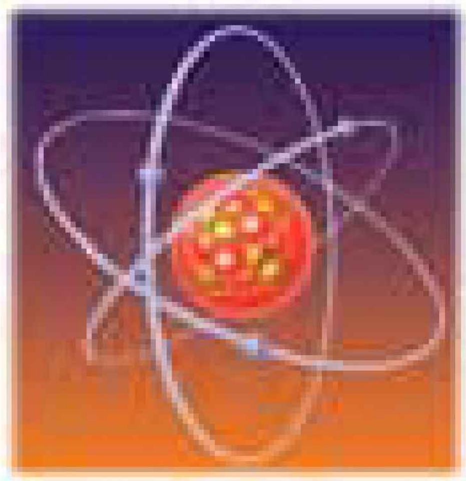
4.2 Energy Levels

4.3 Energy Bands

4.4 Important Energy Bands in Solids

4.5 Classification of Solids and Energy Bands

4.6 Silicon



INTRODUCTION

The study of atomic structure is of considerable importance for electronics engineering. Unfortunately, the size of an atom is so small that it is virtually impossible to see it even with the most powerful microscope. Therefore, we have to employ indirect method for the study of its structure. The method consists of studying the properties of atom experimentally. After this, a *guess* is made regarding the possible structure of atom, which should satisfy the properties studied experimentally.

Various scientists have given different theories regarding the structure of atom. However, for the purpose of understanding electronics, the study of Bohr's atomic model is adequate. Although numerous refinements on Bohr's atomic model have since been made, we still believe in the laws that Bohr applied to the atomic world. In this chapter, we shall deal with Bohr's atomic model in order to understand the problems facing the electronic world.

4.1 Bohr's Atomic Model

In 1913, Neils Bohr, Danish Physicist gave clear explanation of atomic structure. According to Bohr:

(*i*) An atom consists of a positively charged nucleus around which negatively charged electrons revolve in different *circular orbits*.

(*ii*) The electrons can revolve around the nucleus only in certain permitted orbits *i.e.* orbits of certain radii are allowed.

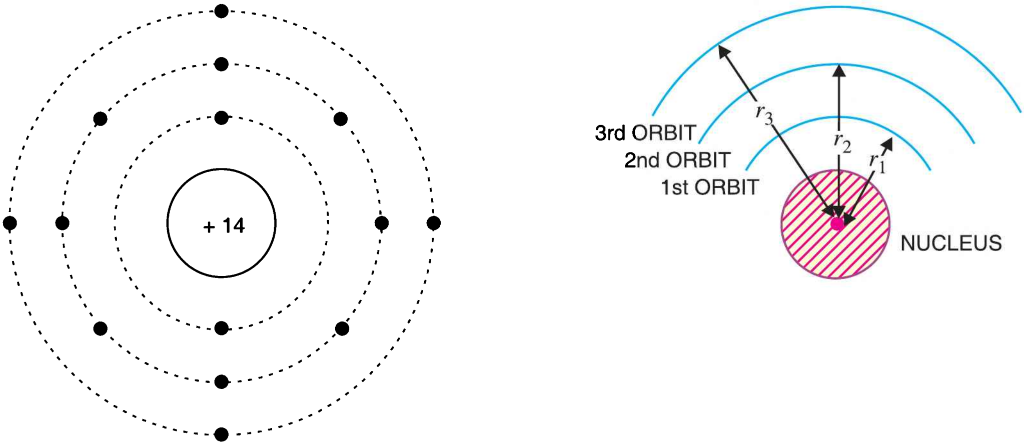
(*iii*) The electrons in each permitted orbit have a certain fixed amount of energy. The larger the orbit (*i.e.* larger radius), the greater is the energy of electrons.

(*iv*) If an electron is given additional energy (*e.g.* heat, light etc.), it is lifted to the higher orbit. The atom is said to be in a state of *excitation*. This state does not last long, because the electron soon falls back to the original lower orbit. As it falls, it gives back the acquired energy in the form of heat, light or other radiations.

Neils Bohr (1885-1962)

Fig. 4.1 shows the structure of silicon atom. It has 14 electrons. Two electrons revolve in the first orbit, 8 in the second orbit and 4 in the third orbit. The first, second, third orbits etc. are also known as *K*, *L*, *M* orbits respectively.

These electrons can revolve only in permitted orbits (*i.e.* orbits of *radii r_1, r_2 and r_3) and not in any arbitrary orbit. Thus, all radii between r_1 and r_2 or between r_2 and r_3 are forbidden. Each orbit has fixed amount of energy associated with it. If an electron in the first orbit is to be lifted to the second orbit, just the **right amount of energy should be supplied to it. When this electron jumps from the second orbit to first, it will give back the acquired energy in the form of electromagnetic radiations.



(*i*) (*ii*)

Fig. 4.1

4.2 Energy Levels

It has already been discussed that each orbit has fixed amount of energy associated with it. The electrons moving in a particular orbit possess the energy of that orbit. The larger the orbit, the greater is its energy. It becomes clear that outer orbit electrons possess more energy than the inner orbit electrons.

A convenient way of representing the energy of different orbits is shown in Fig. 4.2 (*ii*). This is known as energy level diagram. The first orbit represents the *first energy level*, the second orbit indicates the *second energy level* and so on. The larger the orbit of an electron, the greater is its energy and higher is the energy level.

---

* The values of radii are determined from quantum considerations.

** So that its total energy is equal to that of second orbit.

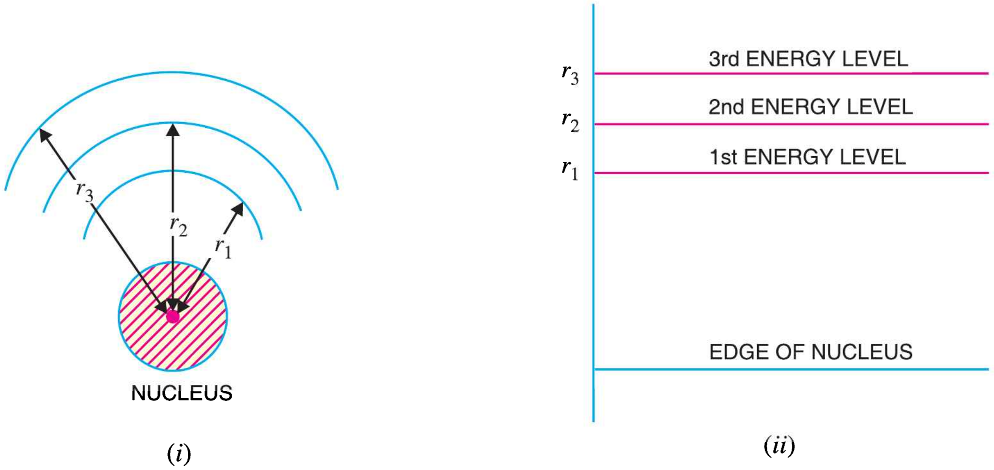

r_3
r_2
r_1
NUCLEUS
(i)
3rd ENERGY LEVEL
2nd ENERGY LEVEL
1st ENERGY LEVEL
EDGE OF NUCLEUS
(ii)

Fig. 4.2

4.3 Energy Bands

In case of a single isolated atom, the electrons in any orbit possess definite energy. However, an atom in a solid is greatly influenced by the closely-packed neighbouring atoms. The result is that the electron in any orbit of such an atom can have a range of energies rather than a single energy. This is known as *energy band.*

The range of energies possessed by an electron in a solid is known as **energy band.**

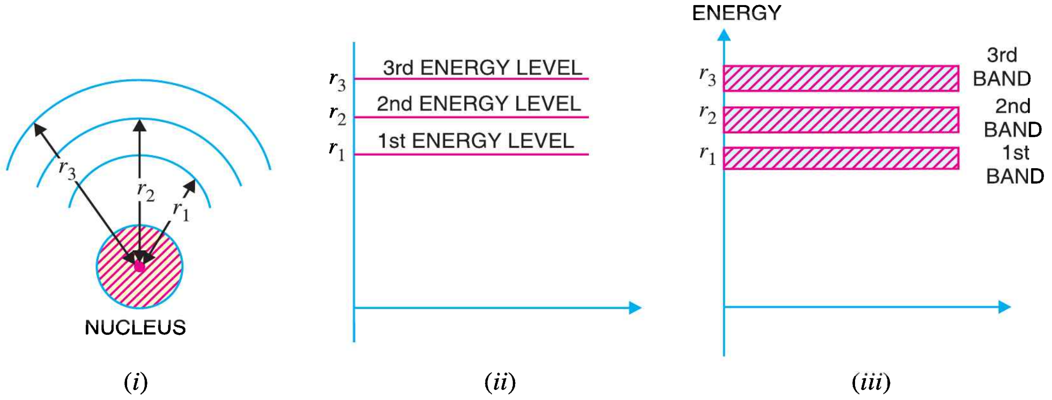

r_3
r_2
r_1
NUCLEUS
(i)
3rd ENERGY LEVEL
2nd ENERGY LEVEL
1st ENERGY LEVEL
(ii)
ENERGY
3rd BAND
2nd BAND
1st BAND
(iii)

Fig. 4.3

The concept of energy band can be easily understood by referring to Fig. 4.3. Fig. 4.3 (*ii*) shows the energy levels of a single isolated atom of silicon. Each orbit of an atom has a single energy. Therefore, an electron can have only single energy corresponding to the orbit in which it exists. However, when the atom is in a solid, the electron in any orbit can have a range of energies. For instance, electrons in the first orbit have slightly different energies because no two electrons in this orbit see exactly the same charge environment. Since there are millions of first orbit electrons, the slightly different energy levels form a band, called 1st energy band [See Fig. 4.3 (*iii*)]. The electrons in the first orbit can have any energy range in this band. Similarly, second orbit electrons form second energy band and so on.

4.4 Important Energy Bands in Solids

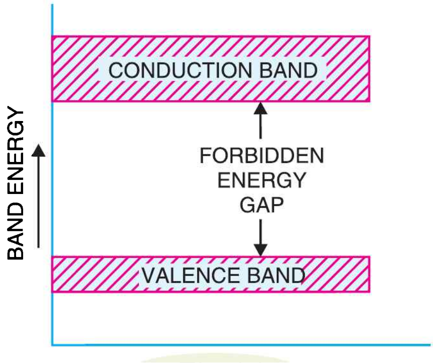


Fig. 4.4

As discussed before, individual *K*, *L*, *M* etc. energy levels of an isolated atom are converted into corresponding bands when the atom is in a solid. Though there are a number of energy bands in solids, the following are of particular importance [See Fig. 4.4] :

(*i*) **Valence band.** *The range of energies* (*i.e. band*) *possessed by valence electrons is known as* **valence band.**

The electrons in the outermost orbit of an atom are known as valence electrons. In a normal atom, valence band has the electrons of highest energy. This band may be completely or partially filled. For instance, in case of inert gases, the valence band is full whereas for other materials, it is only partially filled. The partially filled band can accommodate more electrons.

(*ii*) **Conduction band.** In certain materials (*e.g.* metals), the valence electrons are loosely attached to the nucleus. Even at ordinary temperature, some of the valence electrons may get detached to become free electrons. In fact, it is these free electrons which are responsible for the conduction of current in a conductor. For this reason, they are called *conduction electrons.*

The range of energies (*i.e. band*) *possessed by conduction band electrons is known as* **conduction band.**

All electrons in the conduction band are free electrons. If a substance has empty conduction band, it means current conduction is not possible in that substance. Generally, insulators have empty conduction band. On the other hand, it is partially filled for conductors.

(*iii*) **Forbidden energy gap.** *The separation between conduction band and valence band on the energy level diagram is known as* **forbidden energy gap.**

No electron of a solid can stay in a forbidden energy gap as there is no allowed energy state in this region. The width of the forbidden energy gap is a measure of the bondage of valence electrons to the atom. The greater the energy gap, more tightly the valence electrons are bound to the nucleus. In order to push an electron from valence band to the conduction band (*i.e.* to make the valence electron free), external energy equal to the forbidden energy gap must be supplied.

4.5 Classification of Solids and Energy Bands

We know that some solids are good conductors of electricity while others are insulators. There is also an intermediate class of semiconductors. The difference in the behaviour of solids as regards their electrical conductivity can be beautifully explained in terms of energy bands. The electrons in the lower energy band are tightly bound to the nucleus and play no part in the conduction process. However, the valence and conduction bands are of particular importance in ascertaining the electrical behaviour of various solids.

(*i*) **Insulators.** Insulators (*e.g.* wood, glass etc.) are those substances which do not allow the passage of electric current through them. In terms of energy band, the valence band is full while the conduction band is empty. Further, the energy gap between valence and conduction bands is very large (≃ 15 eV) as shown in Fig. 4.5. Therefore, a very high electric field is required to push the valence electrons to the conduction band.

Insulators

For this reason, the electrical conductivity of such materials is extremely small and may be regarded as nil under ordinary conditions.

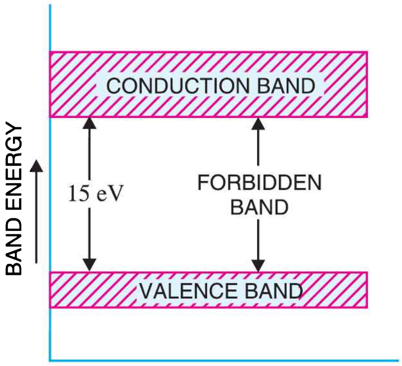


Fig. 4.5

At room temperature, the valence electrons of the insulators do not have enough energy to cross over to the conduction band. However, when the temperature is raised, some of the valence electrons may acquire enough energy to cross over to the conduction band. Hence, the resistance of an insulator decreases with the increase in temperature *i.e.* an insulator has negative temperature coefficient of resistance.

(*ii*) **Conductors.** Conductors (*e.g.* copper, aluminium) are those substances which easily allow the passage of electric current through them. It is because there are a large number of free electrons available in a conductor. In terms of energy band, the valence and conduction bands overlap each other as shown in Fig. 4.6. Due to this overlapping, a slight potential difference across a conductor causes the free electrons to constitute electric current. Thus, the electrical behaviour of conductors can be satisfactorily explained by the band energy theory of materials.

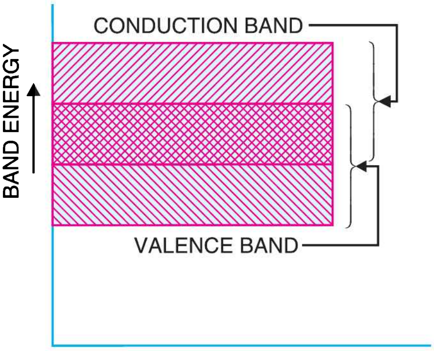


Fig. 4.6

(*iii*) **Semicondutors.** Semiconductors (*e.g.* germanium, silicon etc.) are those substances whose electrical conductivity lies inbetween conductors and insulators. In terms of energy band, the valence band is almost filled and conduction band is almost empty. Further, the energy gap between valence and conduction bands is very small as shown in Fig. 4.7. Therefore, comparatively smaller electric field (smaller than insulators but much greater than conductors) is required to push the electrons from the valence band to the conduction band. In short, a semiconductor has :

(*a*) almost full valence band

(*b*) almost empty conduction band

(*c*) small energy gap ($\simeq$ 1 eV) between valence and conduction bands.

At low temperature, the valence band is completely full and conduction band is completely empty. Therefore, a semiconductor virtually behaves as an insulator at low temperatures. However, even at room temperature, some electrons (about one electron for 10^{10} atoms) cross over to the conduction band, imparting little conductivity to the semiconductor. As the temperature is increased, more valence electrons cross over to the conduction band and the conductivity increases. This shows that electrical conductivity of a semiconductor increases with the rise in temperature *i.e.* a semiconductor has negative temperature co-efficient of resistance.

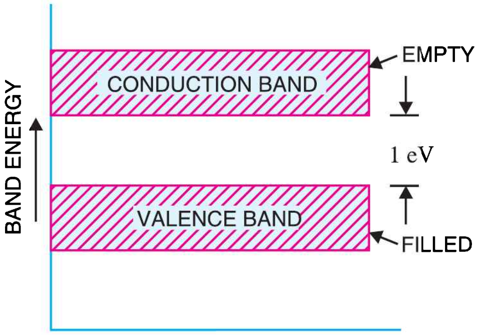
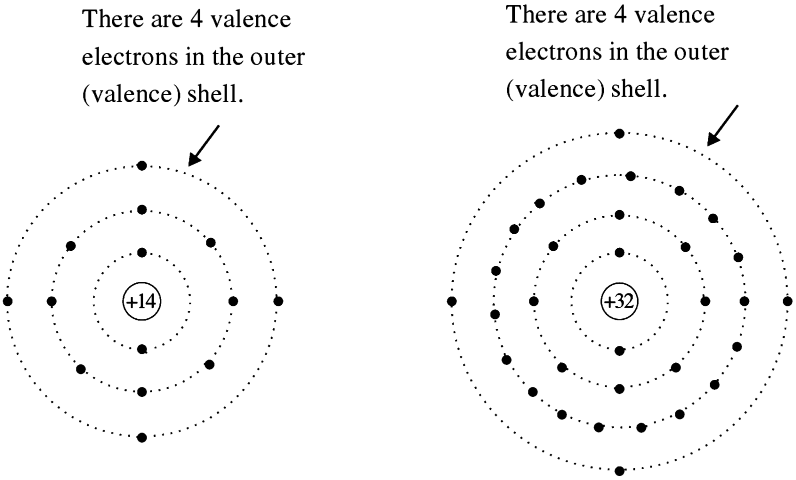


Fig. 4.7

4.6 Silicon

During the infancy of electronic industry, both germanium and silicon were used in the manufacture of semiconductor devices. As the electronic field advanced, it was realised that silicon was superior to germanium in many respects. Since silicon is the most widely used material in the manufacture of semiconductor devices, we shall continue to discuss the properties of this material (as compared to germanium) as and when we get the chance.


There are 4 valence electrons in the outer (valence) shell.
+14
There are 4 valence electrons in the outer (valence) shell.
+32

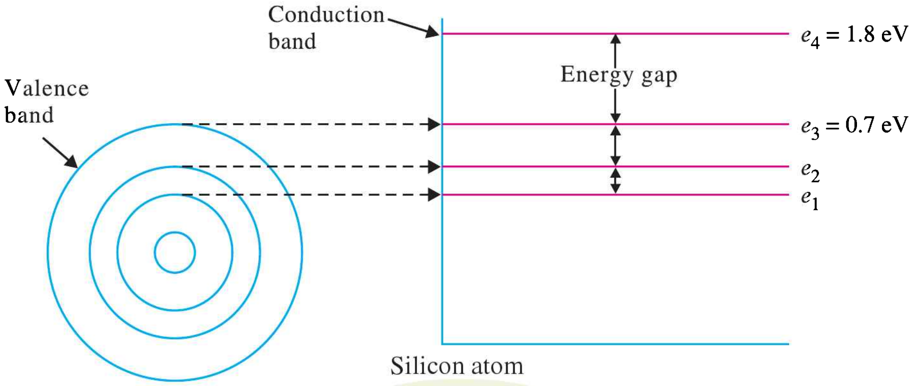
Silicon atom
(*i*)

Germanium atom
(*ii*)

Fig. 4.8

(*i*) Note the atomic structure of germanium and silicon in Fig. 4.8 carefully. The valence electrons in germanium are in the fourth orbit while the valence electrons in silicon are in the third orbit; closer to the nucleus. Therefore, the germanium valence electrons are at higher energy level than those in silicon. This means that germanium valence electrons require smaller amount of additional energy to escape from the atom and become free electron. What is the effect of this property? This property makes germanium more unstable at high temperatures. This is the basic reason why silicon is widely used as semiconductor material.

(*ii*) Fig. 4.9 shows the energy level/band of silicon atom. The atomic number of silicon is 14 so that its 14 electrons are distributed in 3 orbits. Each energy level/band is associated with certain amount of energy and is separated from the adjacent bands by energy gap. ***No electron can exist in the energy gap***. For an electron to jump from one orbit to the next higher orbit, external energy


Conduction band
Valence band
Energy gap
$e_4 = 1.8$ eV
$e_3 = 0.7$ eV
e_2
e_1

Silicon atom

Fig. 4.9

(e.g. heat) equal to the energy difference of the orbits must be supplied. For example, the valence band is shown to have an energy level of 0.7 eV. The conduction band is shown to have an energy level of 1.8 eV. Thus for an electron to jump from the valence band to the conduction band, an energy = 1.8 – 0.7 = 1.1 eV must be supplied. As you will see, the energy band description of substances is very important in understanding many fields of science and engineering including electronics.

MULTIPLE-CHOICE QUESTIONS

1. The electrons in the third orbit of an atom have .... energy than the electrons in the second orbit.
(*i*) more (*ii*) less
(*iii*) the same (*iv*) none of the above

2. When an electron jumps from higher orbit to a lower orbit, it .... energy.
(*i*) absorbs (*ii*) emits
(*iii*) sometimes emits, sometimes absorbs
(*iv*) none of the above

3. Which of the following is quantized according to Bohr's theory of atom ?
(*i*) linear momentum of electron
(*ii*) linear velocity of electron
(*iii*) angular momentum of electron
(*iv*) angular velocity of electron

4. A semiconductor has .... band.
(*i*) almost empty valence
(*ii*) almost empty conduction
(*iii*) almost full conduction
(*iv*) none of the above

5. The electrons in the conduction band are known as ....
(*i*) bound electrons (*ii*) valence electrons
(*iii*) free electrons (*iv*) none of the above

6. In insulators, the energy gap between valence and conduction bands is ....
(*i*) very large (*ii*) zero
(*iii*) very small (*iv*) none of the above

7. In a conductor, the energy gap between valence and conduction bands is ....
(*i*) large (*ii*) very large
(*iii*) very small (*iv*) none of the above

8. According to Bohr's theory of atom, an electron can move in an orbit of ....
(*i*) any radius
(*ii*) certain radius
(*iii*) some range of radii
(*iv*) none of the above

9. In a semiconductor, the energy gap between valence and conduction bands is about ....
(*i*) 15 eV (*ii*) 100 eV
(*iii*) 50 eV (*iv*) 1 eV

10. The energy gap between valence and conduction bands in insulators is about ....
(*i*) 15 eV (*ii*) 1.5 eV
(*iii*) zero (*iv*) 0.5 eV

Answers to Multiple-Choice Questions

1. (*i*) **2.** (*ii*) **3.** (*iii*) **4.** (*ii*) **5.** (*iii*)
6. (*i*) **7.** (*iii*) **8.** (*ii*) **9.** (*iv*) **10.** (*i*)

Chapter Review Topics

1. Explain the salient features of Bohr's atomic model.
2. Explain the concept of energy bands in solids.
3. Describe the valence band, conduction band and forbidden energy gap with the help of energy level diagram.
4. Give the energy band description of conductors, semiconductors and insulators.

Discussion Questions

1. Why is the energy of an electron more in higher orbits ?
2. What is the concept of energy band ?
3. Why do conduction band electrons possess very high energy ?
4. Why are valence electrons of a material so important ?
5. What is the difference between energy level and energy band ?

5

Semiconductor Physics

5.1 Semiconductor
5.2 Bonds in Semiconductors
5.3 Crystals
5.4 Commonly Used Semiconductors
5.5 Energy Band Description of Semiconductors
5.6 Effect of Temperature on Semiconductors
5.7 Hole Current
5.8 Intrinsic Semiconductor
5.9 Extrinsic Semiconductor
5.10 *n*-type Semiconductor
5.11 *p*-type Semiconductor
5.12 Charge on *n*-type and *p*-type Semiconductors
5.13 Majority and Minority Carriers
5.14 *pn* Junction
5.15 Properties of *pn*-Junction
5.16 Applying D.C. Voltage across *pn*-Junction or Biasing a *pn*- Junction
5.17 Current Flow in a Forward Biased *pn*-Junction
5.18 Volt-Ampere Characteristics of *pn* Junction
5.19 Important Terms
5.20 Limitations in the Operating Conditions of *pn*-Junction

INTRODUCTION

Certain substances like germanium, silicon, carbon etc. are neither good conductors like copper nor insulators like glass. In other words, the resistivity of these materials lies inbetween conductors and insulators. Such substances are classified as *semiconductors*. Semiconductors have some useful properties and are being extensively used in electronic circuits. For instance, *transistor*—a semiconductor device is fast replacing bulky vacuum tubes in almost all applications. Transistors are only one of the family of semiconductor devices ; many other semiconductor devices are becoming increasingly popular. In this chapter, we shall focus our attention on the different aspects of semiconductors.

5.1 Semiconductor

It is not easy to define a semiconductor if we want to take into account all its physical characteristics. However, generally, a semiconductor is defined on the basis of electrical conductivity as under :

A **semiconductor** *is a substance which has resistivity (10^{-4} to 0.5 Ωm) inbetween conductors and insulators e.g. germanium, silicon, selenium, carbon etc.*

The reader may wonder, when a semiconductor is neither a good conductor nor an insulator, then why not to classify it as a *resistance material* ? The answer shall be readily available if we study the following table :

S.No.	Substance	Nature	Resistivity
1	Copper	good conductor	1.7×10^{-8} Ω m
2	Germanium	semiconductor	0.6 Ω m
3	Glass	insulator	9×10^{11} Ω m
4	Nichrome	resistance material	10^{-4} Ω m

Comparing the resistivities of above materials, it is apparent that the resistivity of germanium (semiconductor) is quite high as compared to copper (conductor) but it is quite low when compared with glass (insulator). This shows that resistivity of a semiconductor lies inbetween conductors and insulators. However, it will be wrong to consider the semiconductor as a resistance material. For example, nichrome, which is one of the highest resistance material, has resistivity much lower than germanium. This shows that electrically germanium cannot be regarded as a conductor or insulator or a resistance material. This gave such substances like germanium the name of semiconductors.

It is interesting to note that it is not the resistivity alone that decides whether a substance is semiconductor or not. For example, it is just possible to prepare an alloy whose resistivity falls within the range of semiconductors but the alloy cannot be regarded as a semiconductor. In fact, semiconductors have a number of peculiar properties which distinguish them from conductors, insulators and resistance materials.

Properties of Semiconductors

(*i*) The resistivity of a semiconductor is less than an insulator but more than a conductor.

(*ii*) Semiconductors have *negative temperature co-efficient of resistance i.e.* the resistance of a semiconductor decreases with the increase in temperature and *vice-versa*. For example, germanium is actually an insulator at low temperatures but it becomes a good conductor at high temperatures.

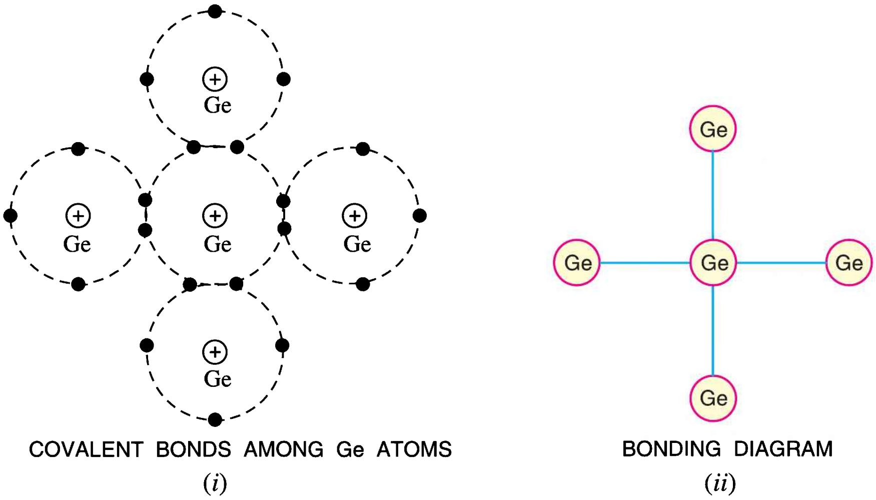
(*iii*) When a suitable metallic impurity (*e.g.* arsenic, gallium etc.) is added to a semiconductor, its current conducting properties change appreciably. This property is most important and is discussed later in detail.

5.2 Bonds in Semiconductors

The atoms of every element are held together by the bonding action of valence electrons. This bonding is due to the fact that it is the tendency of each atom to complete its last orbit by acquiring 8 electrons in it. However, in most of the substances, the last orbit is incomplete *i.e.* the last orbit does not have 8 electrons. This makes the atom active to enter into bargain with other atoms to acquire 8 electrons in the last orbit. To do so, the atom may lose, gain or share valence electrons with other atoms. In semiconductors, bonds are formed by sharing of valence electrons. Such bonds are called *co-valent bonds*. In the formation of a co-valent bond, each atom contributes equal number of valence electrons and the contributed electrons are shared by the atoms engaged in the formation of the bond.

Fig. 5.1 shows the co-valent bonds among germanium atoms. A germanium atom has *4 valence electrons. It is the tendency of each germanium atom to have 8 electrons in the last orbit. To do so, each germanium atom positions itself between four other germanium atoms as shown in Fig. 5.1 (*i*). Each neighbouring atom shares one valence electron with the central atom. In this business of sharing, the central atom completes its last orbit by having 8 electrons revolving around the nucleus. In this way, the central atom sets up co-valent bonds. Fig. 5.1 (*ii*) shows the bonding diagram.

The following points may be noted regarding the co-valent bonds :



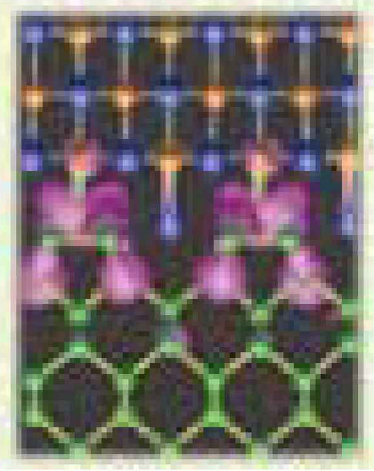
COVALENT BONDS AMONG Ge ATOMS
(*i*)

BONDING DIAGRAM
(*ii*)

Fig. 5.1

(*i*) Co-valent bonds are formed by sharing of valence electrons.

(*ii*) In the formation of co-valent bond, each valence electron of an atom forms direct bond with the valence electron of an adjacent atom. In other words, valence electrons are associated with particular atoms. For this reason, valence electrons in a semiconductor are not free.



Bonds in Semiconductor

5.3 Crystals

A substance in which the atoms or molecules are arranged in an orderly pattern is known as a *crystal*. All semi-conductors have crystalline structure. For example, referring to Fig. 5.1, it is clear that each atom is surrounded by neighbouring atoms in a repetitive manner. Therefore, a piece of germanium is generally called germanium crystal.

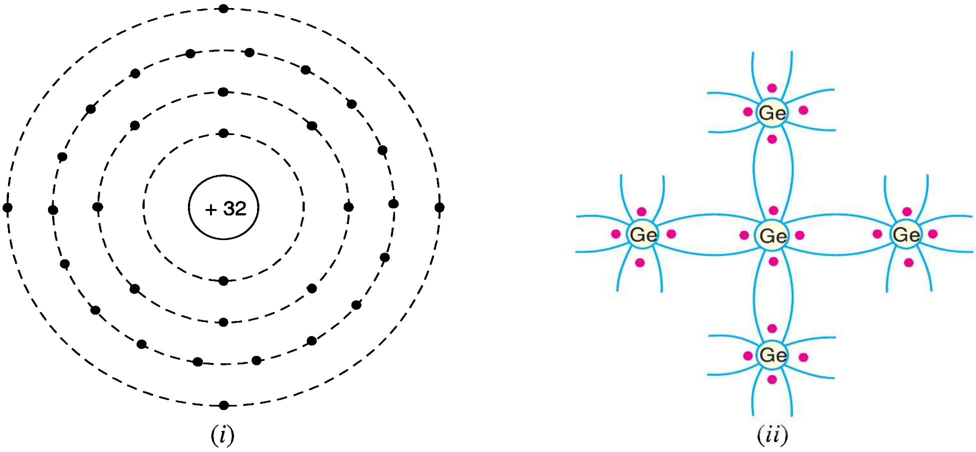
5.4 Commonly Used Semiconductors

There are many semiconductors available, but very few of them have a practical application in electronics. The two most frequently used materials are *germanium* (Ge) and *silicon* (Si). It is because the energy required to break their co-valent bonds (*i.e.* energy required to release an electron from their valence bands) is very small; being about 0.7 eV for germanium and about 1.1 eV for silicon. Therefore, we shall discuss these two semiconductors in detail.

---

* A germanium atom has 32 electrons. First orbit has 2 electrons, second 8 electrons, third 18 electrons and the fourth orbit has 4 electrons.

(*i*) **Germanium.** Germanium has become the model substance among the semiconductors; the main reason being that it can be purified relatively well and crystallised easily. Germanium is an earth element and was discovered in 1886. It is recovered from the ash of certain coals or from the flue dust of zinc smelters. Generally, recovered germanium is in the form of germanium dioxide powder which is then reduced to pure germanium.

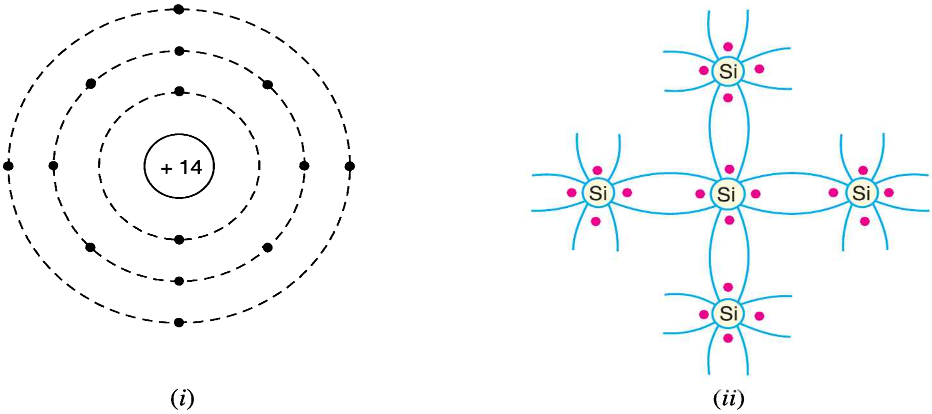


(*i*) (*ii*)

Fig. 5.2

The atomic number of germanium is 32. Therefore, it has 32 protons and 32 electrons. Two electrons are in the first orbit, eight electrons in the second, eighteen electrons in the third and four electrons in the outer or valence orbit [See Fig. 5.2 (*i*)]. It is clear that germanium atom has four valence electrons *i.e.*, it is a tetravalent element. Fig. 5.2 (*ii*) shows how the various germanium atoms are held through co-valent bonds. As the atoms are arranged in an orderly pattern, therefore, germanium has crystalline structure.

(*ii*) **Silicon.** Silicon is an element in most of the common rocks. Actually, sand is silicon dioxide. The silicon compounds are chemically reduced to silicon which is 100% pure for use as a semiconductor.



(*i*) (*ii*)

Fig. 5.3

The atomic number of silicon is 14. Therefore, it has 14 protons and 14 electrons. Two electrons are in the first orbit, eight electrons in the second orbit and four electrons in the third orbit [See Fig. 5.3 (*i*)]. It is clear that silicon atom has four valence electrons *i.e.* it is a tetravalent element. Fig. 5.3 (*ii*) shows how various silicon atoms are held through co-valent bonds. Like germanium, silicon atoms are also arranged in an orderly manner. Therefore, silicon has crystalline structure.

5.5 Energy Band Description of Semiconductors

It has already been discussed that a semiconductor is a substance whose resistivity lies between conductors and insulators. The resistivity is of the order of 10^{-4} to 0.5 ohm metre. However, a semiconductor can be defined much more comprehensively on the basis of energy bands as under :

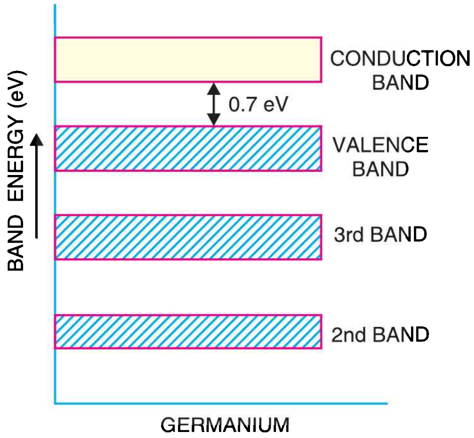


Fig. 5.4

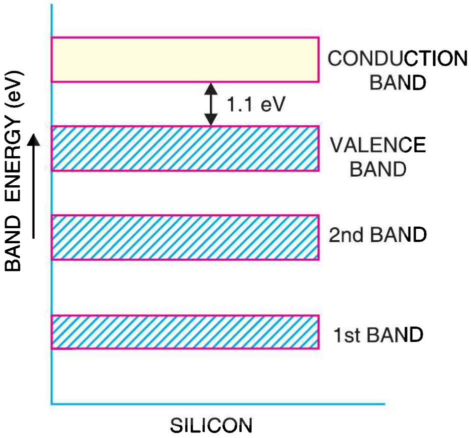


Fig. 5.5

A **semiconductor** *is a substance which has almost filled valence band and nearly empty conduction band with a very small energy gap (≃ 1 eV) separating the two.*

Figs. 5.4 and 5.5 show the energy band diagrams of germanium and silicon respectively. It may be seen that forbidden energy gap is very small; being 1.1 eV for silicon and 0.7 eV for germanium. Therefore, relatively small energy is needed by their valence electrons to cross over to the conduction band. Even at room temperature, some of the valence electrons may acquire sufficient energy to enter into the conduction band and thus become free electrons. However, at this temperature, the number of free electrons available is very *small. Therefore, at room temperature, a piece of germanium or silicon is neither a good conductor nor an insulator. For this reason, such substances are called *semiconductors*.

The energy band description is extremely helpful in understanding the current flow through a semiconductor. Therefore, we shall frequently use this concept in our further discussion.

5.6 Effect of Temperature on Semiconductors

The electrical conductivity of a semiconductor changes appreciably with temperature variations. This is a very important point to keep in mind.

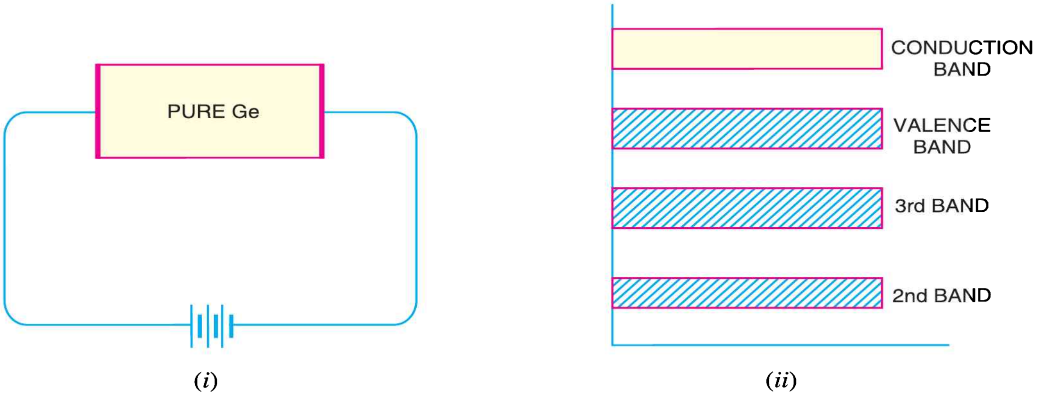
(*i*) At absolute zero. At absolute zero temperature, all the electrons are tightly held by the semiconductor atoms. The inner orbit electrons are bound whereas the valence electrons are engaged in co-valent bonding. At this temperature, the co-valent bonds are very strong and there are no free electrons. Therefore, the semiconductor crystal behaves as a perfect insulator [See Fig. 5.6 (*i*)].

In terms of energy band description, the valence band is filled and there is a large energy gap between valence band and conduction band. Therefore, no valence electron can reach the conduction band to become free electron. It is due to the non-availability of free electrons that a semiconductor behaves as an insulator.

---

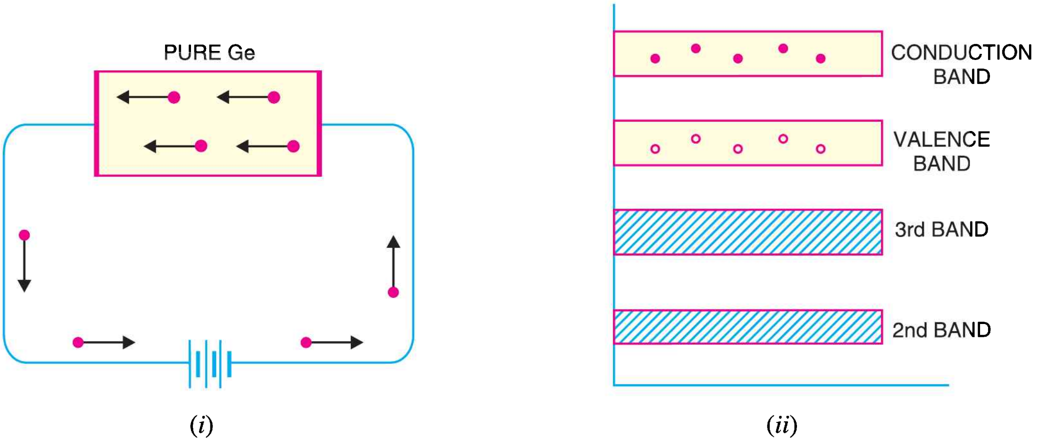
* Out of 10^{10} semiconductor atoms, one atom provides a free electron.

(*ii*) **Above absolute zero.** When the temperature is raised, some of the covalent bonds in the semiconductor break due to the thermal energy supplied. The breaking of bonds sets those electrons *free* which are engaged in the formation of these bonds. The result is that a few free electrons exist in the semiconductor. These free electrons can constitute a tiny electric current if potential difference is applied across the semiconductor crystal [See Fig. 5.7 (*i*)]. *This shows that the resistance of a semiconductor decreases with the rise in temperature i.e.* it has negative temperature coefficient of resistance. It may be added that at room temperature, current through a semiconductor is too small to be of any practical value.



(*i*) (*ii*)

Fig. 5.6



(*i*) (*ii*)

Fig. 5.7

Fig. 5.7 (*ii*) shows the energy band diagram. As the temperature is raised, some of the valence electrons acquire sufficient energy to enter into the conduction band and thus become free electrons. Under the influence of electric field, these free electrons will constitute electric current. It may be noted that each time a valence electron enters into the conduction band, a *hole* is created in the valence band. As we shall see in the next article, holes also contribute to current. In fact, hole current is the most significant concept in semiconductors.

5.7 Hole Current

At room temperature, some of the co-valent bonds in pure semiconductor break, setting up free electrons. Under the influence of electric field, these free electrons constitute electric current. At the same time, another current – the hole current – also flows in the semiconductor. When a covalent bond is broken due to thermal energy, the removal of one electron leaves a vacancy *i.e.* a missing electron in the covalent bond. This missing electron is called a *hole which acts as a positive charge. For one electron set free, one hole is created. Therefore, thermal energy creates *hole-electron pairs*; there being as many holes as the free electrons. The current conduction by holes can be explained as follows :

The hole shows a missing electron. Suppose the valence electron at *L* (See Fig. 5.8) has become free electron due to thermal energy. This creates a hole in the co-valent bond at *L*. The hole is a strong centre of attraction **for the electron. A valence electron (say at *M*) from nearby co-valent bond comes to fill in the hole at *L*. This results in the creation of hole at *M*. Another valence electron (say at *N*) in turn may leave its bond to fill the hole at *M*, thus creating a hole at *N*. Thus the hole having a positive charge has moved from *L* to *N* *i.e.* towards the negative terminal of supply. This constitutes *hole current*.

It may be noted that hole current is due to the movement of ***valence electrons from one co-valent bond to another bond. The reader may wonder why to call it a hole current when the conduction is again by electrons (of course *valence electrons* !). The answer is that the basic reason for current flow is the presence of holes in the co-valent bonds. Therefore, it is more appropriate to consider the current as the movement of holes.

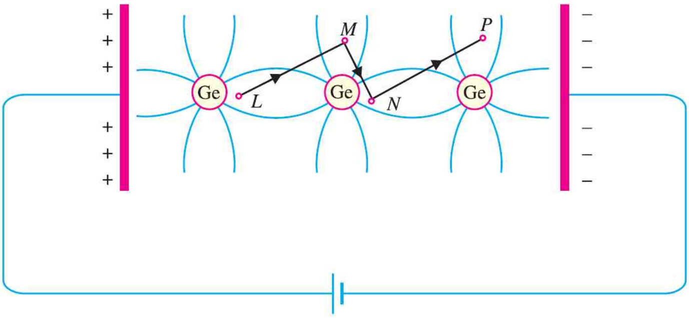


Fig. 5.8

Energy band description. The hole current can be beautifully explained in terms of energy bands. Suppose due to thermal energy, an electron leaves the valence band to enter into the conduction band as shown in Fig. 5.9.

This leaves a vacancy at *L*. Now the valence electron at *M* comes to fill the hole at *L*. The result is that hole disappears at *L* and appears at *M*. Next, the valence electron at *N* moves into the hole at *M*. Consequently, hole is created at *N*. It is clear that valence electrons move along the path *PNML* whereas holes move in the opposite direction *i.e.* along the path *LMNP*.

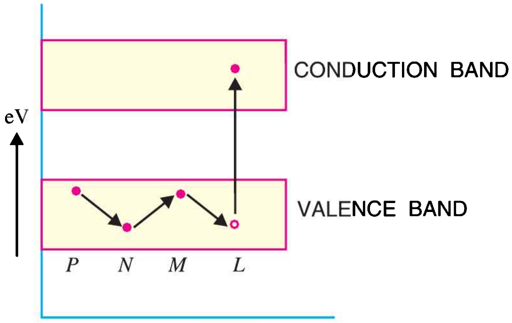


Fig. 5.9

---

* Note that hole acts as a virtual charge, although there is no physical charge on it.

** There is a strong tendency of semiconductor crystal to form co-valent bonds. Therefore, a hole attracts an electron from the neighbouring atom.

*** Unlike the normal current which is by free electrons.

5.8 Intrinsic Semiconductor

A semiconductor in an extremely pure form is known as an **intrinsic semiconductor**.

In an intrinsic semiconductor, even at room temperature, hole-electron pairs are created. When electric field is applied across an intrinsic semiconductor, the current conduction takes place by two processes, namely ; by *free electrons* and *holes* as shown in Fig. 5.10. The free electrons are produced due to the breaking up of some covalent bonds by thermal energy. At the same time, holes are created in the covalent bonds. Under the influence of electric field, conduction through the semiconductor is by both free electrons and holes. Therefore, the total current inside the semiconductor is the sum of currents due to free electrons and holes.

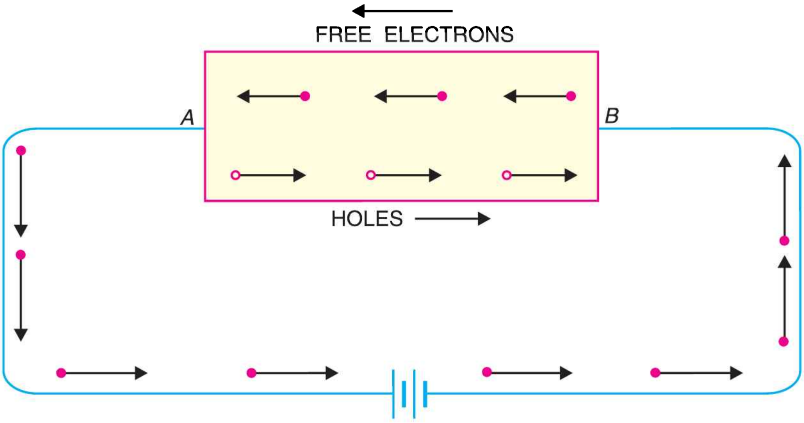


Fig. 5.10

It may be noted that current in the external wires is fully electronic *i.e.* by electrons. What about the holes ? Referring to Fig. 5.10, holes being positively charged move towards the negative terminal of supply. As the holes reach the negative terminal *B*, electrons enter the semiconductor crystal near the terminal and combine with holes, thus cancelling them. At the same time, the loosely held electrons near the positive terminal *A* are attracted away from their atoms into the positive terminal. This creates new holes near the positive terminal which again drift towards the negative terminal.

5.9 Extrinsic Semiconductor

The intrinsic semiconductor has little current conduction capability at room temperature. To be useful in electronic devices, the pure semiconductor must be altered so as to significantly increase its conducting properties. This is achieved by adding a small amount of suitable impurity to a semiconductor. It is then called *impurity* or *extrinsic semiconductor*. The process of adding impurities to a semiconductor is known as *doping*. The amount and type of such impurities have to be closely controlled during the preparation of extrinsic semiconductor. Generally, for 10^8 atoms of semiconductor, one impurity atom is added.

The purpose of adding impurity is to increase either the number of free electrons or holes in the semiconductor crystal. As we shall see, if a pentavalent impurity (having 5 valence electrons) is added to the semiconductor, a large number of free electrons are produced in the semiconductor. On the other hand, addition of trivalent impurity (having 3 valence electrons) creates a large number of holes in the semiconductor crystal. Depending upon the type of impurity added, extrinsic semiconductors are classified into:

(*i*) *n*-type semiconductor (*ii*) *p*-type semiconductor

5.10 *n*-type Semiconductor

When a small amount of pentavalent impurity is added to a pure semiconductor, it is known as **n-type semiconductor.**

The addition of pentavalent impurity provides a large number of free electrons in the semiconductor crystal. Typical examples of pentavalent impurities are *arsenic* (At. No. 33) and *antimony* (At. No. 51). Such impurities which produce *n*-type semiconductor are known as *donor impurities* because they donate or provide free electrons to the semiconductor crystal.

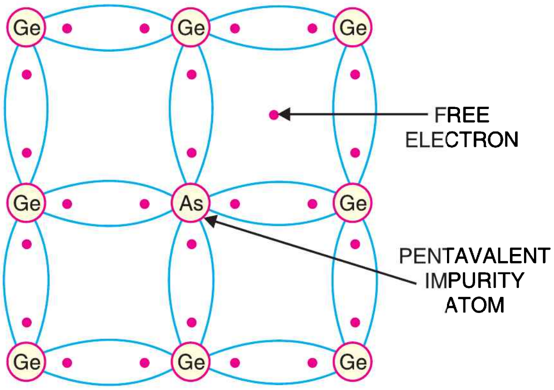


Fig. 5.11

To explain the formation of *n*-type semiconductor, consider a pure germanium crystal. We know that germanium atom has four valence electrons. When a small amount of pentavalent impurity like arsenic is added to germanium crystal, a large number of free electrons become available in the crystal. The reason is simple. Arsenic is pentavalent *i.e.* its atom has five valence electrons. An arsenic atom fits in the germanium crystal in such a way that its four valence electrons form covalent bonds with four germanium atoms. The *fifth* valence electron of arsenic atom finds no place in co-valent bonds and is thus free as shown in Fig. 5.11. Therefore, for each arsenic atom added, one free electron will be available in the germanium crystal. Though each arsenic atom provides one free electron, yet an extremely small amount of arsenic impurity provides enough atoms to supply millions of free electrons.

Fig. 5.12 shows the energy band description of *n*-type semi-conductor. The addition of pentavalent impurity has produced a number of conduction band electrons *i.e.*, free electrons. The four valence electrons of pentavalent atom form covalent bonds with four neighbouring germanium atoms. The fifth left over valence electron of the pentavalent atom cannot be accommodated in the valence band and travels to the conduction band. The following points may be noted carefully :

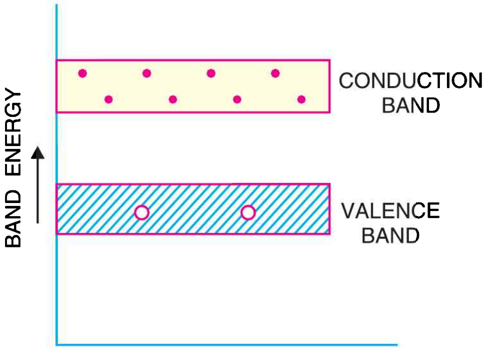


Fig. 5.12

(*i*) Many new free electrons are produced by the addition of pentavalent impurity.

(*ii*) Thermal energy of room temperature still generates a few hole-electron pairs. However, the number of free electrons provided by the pentavalent impurity far exceeds the number of holes. It is due to this predominance of electrons over holes that it is called *n*-type semiconductor (*n* stands for negative).

n-type conductivity. The current conduction in an *n*-type semiconductor is *predominantly* by free electrons *i.e.* negative charges and is called *n-type* or *electron type conductivity*. To understand *n*-type conductivity, refer to Fig. 5.13. When p.d. is applied across the *n*-type semiconductor, the free electrons (donated by impurity) in the crystal will be directed towards the positive terminal, constituting electric current. As the current flow through the crystal is by free electrons which are carriers of negative charge, therefore, this type of conductivity is called negative or *n*-type conductivity. It may be noted that conduction is just as in ordinary metals like copper.

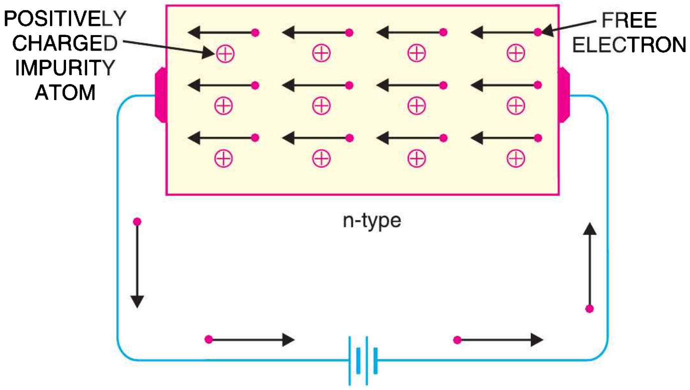


Fig. 5.13

5.11 *p*-type Semiconductor

When a small amount of trivalent impurity is added to a pure semiconductor, it is called **p-type semiconductor.**

The addition of trivalent impurity provides a large number of holes in the semiconductor. Typical examples of trivalent impurities are *gallium* (At. No. 31) and *indium* (At. No. 49). Such impurities which produce *p*-type semiconductor are known as *acceptor impurities* because the holes created can accept the electrons.

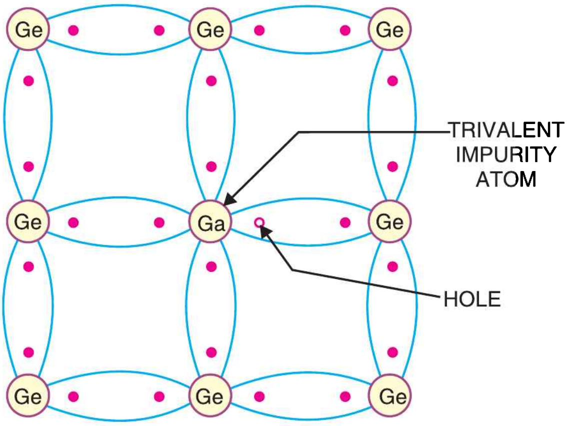


Fig. 5.14

To explain the formation of *p*-type semiconductor, consider a pure germanium crystal. When a small amount of trivalent impurity like gallium is added to germanium crystal, there exists a large number of holes in the crystal. The reason is simple. Gallium is trivalent *i.e.* its atom has three valence electrons. Each atom of gallium fits into the germanium crystal but now only three co-valent bonds can be formed. It is because three valence electrons of gallium atom can form only three single co-valent bonds with three germanium atoms as shown in Fig. 5.14. In the fourth co-valent bond, only germanium atom contributes one valence electron while gallium has no valence electron to contribute as all its three valence electrons are already engaged in the co-valent bonds with neighbouring germanium atoms. In other words, fourth bond is incomplete; being short of one electron. This missing electron is called a *hole*. Therefore, for each gallium atom added, one hole is created. A small amount of gallium provides millions of holes.

Fig. 5.15 shows the energy band description of the *p*-type semiconductor. The addition of trivalent impurity has produced a large number of holes. However, there are a few conduction band electrons due to thermal energy associated with room temperature. But the holes far outnumber the conduction band electrons. It is due to the predominance of holes over free electrons that it is called *p*-type semiconductor (*p* stands for positive).

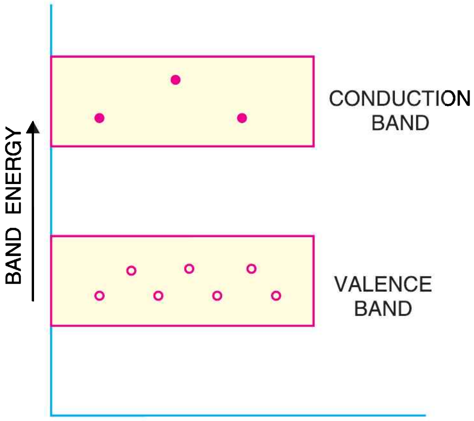


Fig. 5.15

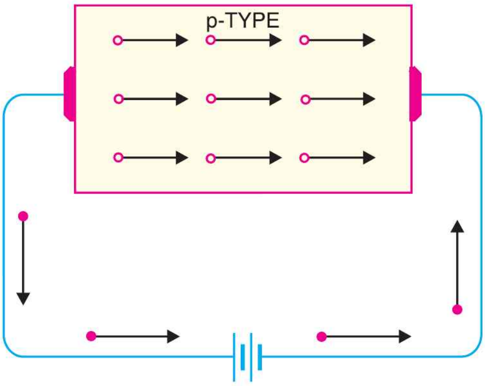


Fig. 5.16

p-type conductivity. The current conduction in p-type semiconductor is predominantly by holes *i.e.* positive charges and is called *p-type* or *hole-type conductivity*. To understand p-type conductivity, refer to Fig. 5.16. When *p.d.* is applied to the p-type semiconductor, the holes (donated by the impurity) are shifted from one co-valent bond to another. As the holes are positively charged, therefore, they are directed towards the negative terminal, constituting what is known as hole current. It may be noted that in p-type conductivity, the valence electrons move from one co-valent bond to another unlike the n-type where current conduction is by free electrons.

5.12 Charge on *n*-type and *p*-type Semiconductors

As discussed before, in n-type semiconductor, current conduction is due to excess of electrons whereas in a p-type semiconductor, conduction is by holes. The reader may think that n-type material has a net negative charge and p-type a net positive charge. But this conclusion is wrong. It is true that n-type semiconductor has excess of electrons but these extra electrons were supplied by the atoms of donor impurity and each atom of donor impurity is electrically neutral. When the impurity atom is added, the term "excess electrons" refers to an excess with regard to the number of electrons needed to fill the co-valent bonds in the semiconductor crystal. The extra electrons are free electrons and increase the conductivity of the semiconductor. The situation with regard to p-type semiconductor is also similar. *It follows, therefore, that n-type as well as p-type semiconductor is electrically neutral.*

5.13 Majority and Minority Carriers

It has already been discussed that due to the effect of impurity, n-type material has a large number of free electrons whereas p-type material has a large number of holes. However, it may be recalled that even at room temperature, some of the co-valent bonds break, thus releasing an equal number of free electrons and holes. An n-type material has its share of electron-hole pairs (released due to breaking of bonds at room temperature) but in addition has a much larger quantity of free electrons due to the effect of impurity. These impurity-caused free electrons are not associated with holes. Consequently, an n-type material has a large number of free electrons and a small number of holes as shown in Fig. 5.17 (*i*). The free electrons in this case are considered *majority carriers* — since the majority portion of current in n-type material is by the flow of free electrons — and the holes are the *minority carriers*.

Similarly, in a p-type material, holes outnumber the free electrons as shown in Fig. 5.17 (*ii*). Therefore, holes are the majority carriers and free electrons are the minority carriers.

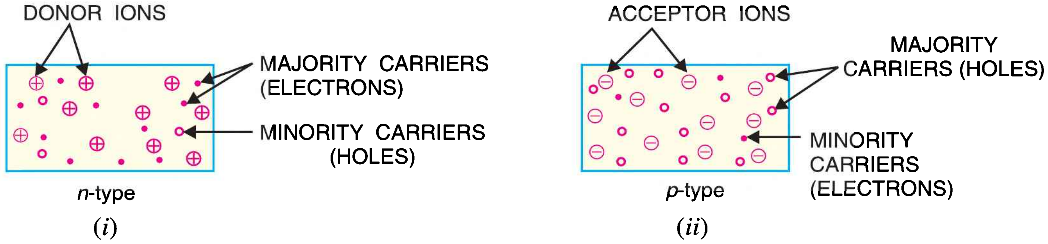

DONOR IONS
MAJORITY CARRIERS (ELECTRONS)
MINORITY CARRIERS (HOLES)
n-type
(i)
ACCEPTOR IONS
MAJORITY CARRIERS (HOLES)
MINORITY CARRIERS (ELECTRONS)
p-type
(ii)

Fig. 5.17

5.14 *pn* Junction

When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called ***pn*** **junction.**

Most semiconductor devices contain one or more *pn* junctions. The *pn* junction is of great importance because it is in effect, the *control element* for semiconductor devices. A thorough knowledge of the formation and properties of *pn* junction can enable the reader to understand the semiconductor devices.

Formation of *pn* junction. In actual practice, the characteristic properties of *pn* junction will not be apparent if a *p*-type block is just brought in contact with *n*-type block. In fact, *pn* junction is fabricated by special techniques. One common method of making *pn* junction is called *alloying*. In this method, a small block of indium (trivalent impurity) is placed on an *n*-type germanium slab as shown in Fig. 5.18 (*i*). The system is then heated to a temperature of about 500°C. The indium and some of the germanium melt to form a small puddle of molten germanium-indium mixture as shown in Fig. 5.18 (*ii*). The temperature is then lowered and puddle begins to solidify. Under proper conditions, the atoms of indium impurity will be suitably adjusted in the germanium slab to form a single crystal. The addition of indium overcomes the excess of electrons in the *n*-type germanium to such an extent that it creates a *p*-type region.

As the process goes on, the remaining molten mixture becomes increasingly rich in indium. When all germanium has been redeposited, the remaining material appears as indium button which is frozen on to the outer surface of the crystallised portion as shown in Fig. 5.18 (*iii*). This button serves as a suitable base for soldering on leads.

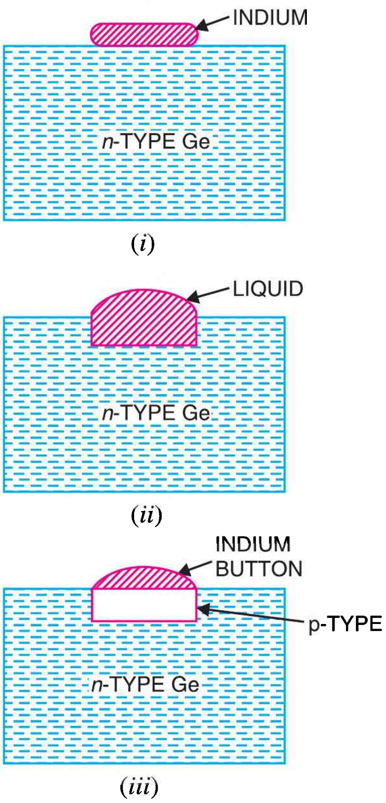
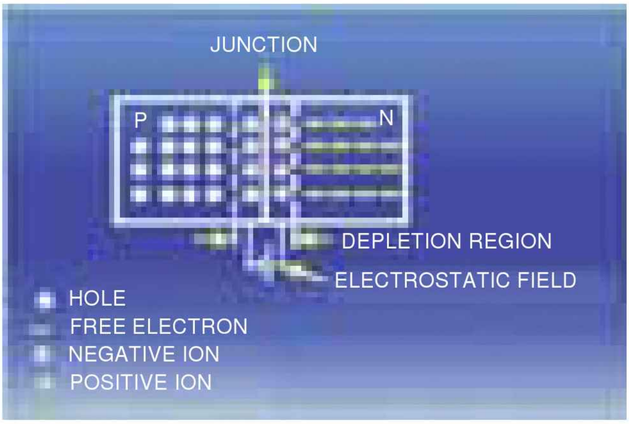
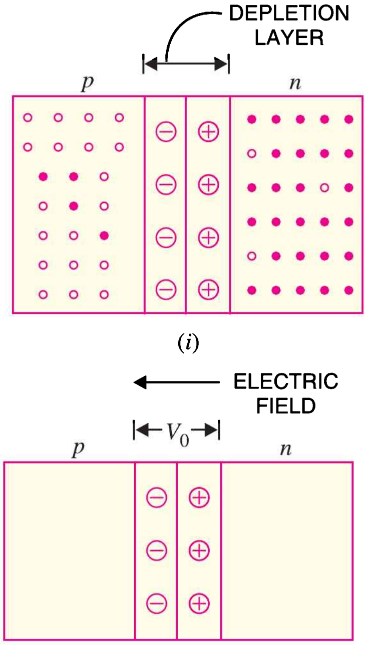

INDIUM
n-TYPE Ge
(i)
LIQUID
n-TYPE Ge
(ii)
INDIUM BUTTON
p-TYPE
n-TYPE Ge
(iii)

Fig. 5.18


JUNCTION
P
N
DEPLETION REGION
ELECTROSTATIC FIELD
HOLE
FREE ELECTRON
NEGATIVE ION
POSITIVE ION

5.15 Properties of *pn* Junction

At the instant of *pn*-junction formation, the free electrons near the junction in the *n* region begin to diffuse across the junction into the *p* region where they combine with holes near the junction. The result is that *n* region loses free electrons as they diffuse into the junction. This creates a layer of positive charges (pentavalent ions) near the junction. As the electrons move across the junction, the *p* region loses holes as the electrons and holes combine. The result is that there is a layer of negative charges (trivalent ions) near the junction. These two layers of positive and negative charges form the *depletion region* (or *depletion layer*). The term depletion is due to the fact that near the junction, the region is depleted (*i.e.* emptied) of *charge carries* (free electrons and holes) due to diffusion across the junction. It may be noted that depletion layer is formed very quickly and is very thin compared to the *n* region and the *p* region. For clarity, the width of the depletion layer is shown exaggerated.



(*i*)

(*ii*)

Fig. 5.19

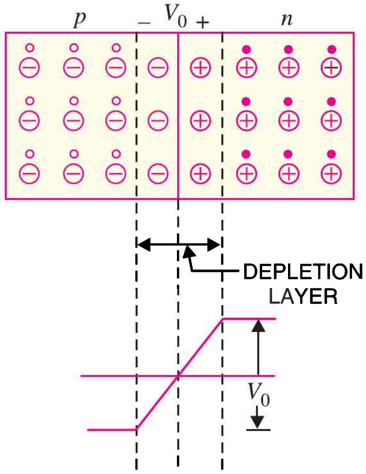


Fig. 5.20

Once *pn* junction is formed and depletion layer created, the diffusion of free electrons stops. In other words, the depletion region acts as a barrier to the further movement of free electrons across the junction. The positive and negative charges set up an electric field. This is shown by a black arrow in Fig. 5.19 (*i*). The electric field is a barrier to the free electrons in the *n*-region. There exists a potential difference across the depletion layer and is called **barrier potential** (V_0). The barrier potential of a *pn* junction depends upon several factors including the type of semiconductor material, the amount of doping and temperature. The typical barrier potential is approximately:

For silicon, $V_0 = 0.7$ V ; For germanium, $V_0 = 0.3$ V

Fig. 5.20 shows the potential (V_0) distribution curve.

5.16 Applying D.C. Voltage Across *pn* Junction or Biasing a pn Junction

In electronics, the term bias refers to the use of d.c. voltage to establish certain operating conditions for an electronic device. In relation to a *pn* junction, there are following two bias conditions :

1. Forward biasing **2. Reverse biasing**

1. Forward biasing. *When external d.c. voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called* **forward biasing.**

To apply forward bias, connect positive terminal of the battery to *p*-type and negative terminal to *n*-type as shown in Fig. 5.21. The applied forward potential establishes an electric field which acts against the field due to potential barrier. Therefore, the resultant field is weakened and the barrier height is reduced at the junction as shown in Fig. 5.21. As potential barrier voltage is very small (0.1 to 0.3 V), therefore, a small forward voltage is sufficient to completely eliminate the barrier. Once the potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero and a low resistance path is established for the entire circuit. Therefore, current flows in the circuit. This is called *forward current*. With forward bias to *pn* junction, the following points are worth noting :

(*i*) The potential barrier is reduced and at some forward voltage (0.1 to 0.3 V), it is eliminated altogether.

(*ii*) The junction offers low resistance (called *forward resistance*, R_f) to current flow.

(*iii*) Current flows in the circuit due to the establishment of low resistance path. The magnitude of current depends upon the applied forward voltage.

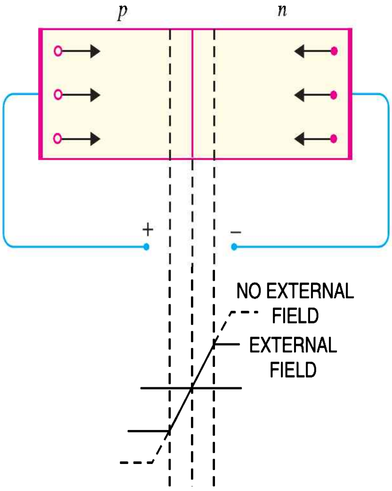


Fig. 5.21

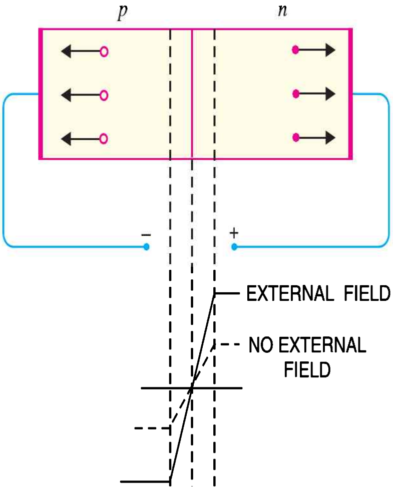


Fig. 5.22

2. Reverse biasing. *When the external d.c. voltage applied to the junction is in such a direction that potential barrier is increased, it is called* **reverse biasing.**

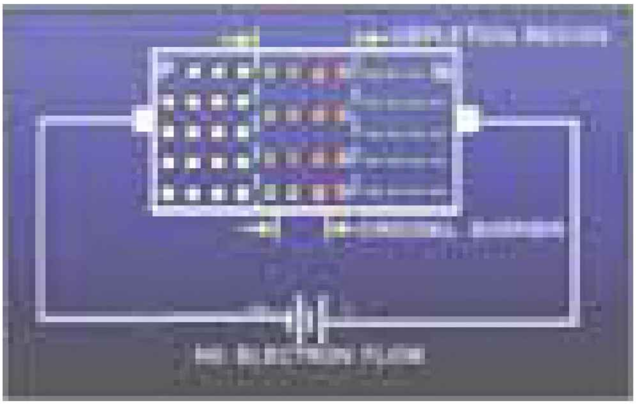
To apply reverse bias, connect negative terminal of the battery to *p*-type and positive terminal to *n*-type as shown in Fig. 5.22. It is clear that applied reverse voltage establishes an electric field which acts in the same direction as the field due to potential barrier. Therefore, the resultant field at the junction is strengthened and the barrier height is increased as shown in Fig. 5.22. The increased potential barrier prevents the flow of charge carriers across the junction. Thus, a high resistance path is established for the entire circuit and hence the current does not flow. With reverse bias to *pn* junction, the following points are worth noting :

(*i*) The potential barrier is increased.

(*ii*) The junction offers very high resistance (called *reverse resistance*, R_r) to current flow.

(*iii*) No current flows in the circuit due to the establishment of high resistance path.

Conclusion. From the above discussion, it follows that with reverse bias to the junction, a high resistance path is established and hence no current flow occurs. On the other hand, with forward bias to the junction, a low resistance path is set up and hence current flows in the circuit.



5.17 Current Flow in a Forward Biased pn Junction

We shall now see how current flows across *pn* junction when it is forward biased. Fig. 5.23 shows a forward biased *pn* junction. Under the influence of forward voltage, the free electrons in *n*-type move *towards the junction, leaving behind positively charged atoms. However, more electrons arrive from the negative battery terminal and enter the *n*-region to take up their places. As the free electrons reach the junction, they become **valence electrons. As valence electrons, they move through the holes in the *p*-region. The valence electrons move towards left in the *p*-region which is equivalent to the holes moving to right. When the valence electrons reach the left end of the crystal, they flow into the positive terminal of the battery.

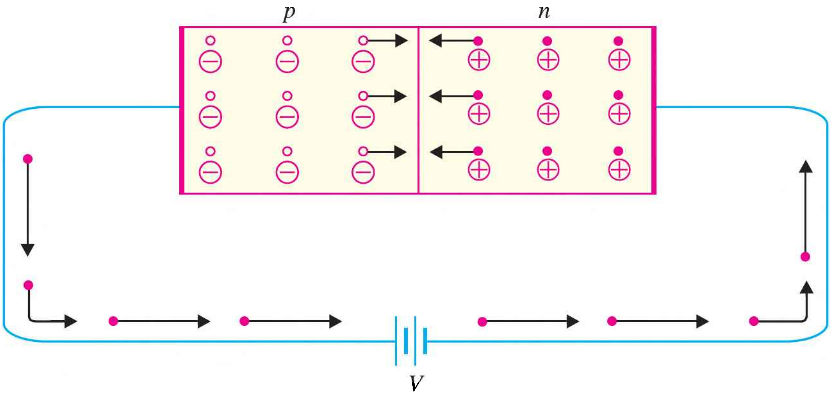


Fig. 5.23

The mechanism of current flow in a forward biased *pn* junction can be summed up as under :

(*i*) The free electrons from the negative terminal continue to pour into the *n*-region while the free electrons in the *n*-region move towards the junction.

(*ii*) The electrons travel through the *n*-region as free-electrons *i.e.* current in *n*-region is by free electrons.

---

* Note that negative terminal of battery is connected to *n*-type. It repels the free electrons in *n*-type towards the junction.

** A hole is in the co-valent bond. When a free electron combines with a hole, it becomes a valence electron.

(iii) When these electrons reach the junction, they combine with holes and become valence electrons.

(iv) The electrons travel through *p*-region as valence electrons *i.e.* current in the *p*-region is by holes.

(v) When these valence electrons reach the left end of crystal, they flow into the positive terminal of the battery.

From the above discussion, it is concluded that in *n*-type region, current is carried by free electrons whereas in *p*-type region, it is carried by holes. However, in the external connecting wires, the current is carried by free electrons.

5.18 Volt-Ampere Characteristics of *pn* Junction

Volt-ampere or *V-I* characteristic of a *pn* junction (also called a *crystal or semiconductor diode*) is the curve between voltage across the junction and the circuit current. Usually, voltage is taken along *x*-axis and current along *y*-axis. Fig. 5.24 shows the *circuit arrangement for determining the *V-I* characteristics of a *pn* junction. The characteristics can be studied under three heads, namely; *zero external voltage*, *forward bias* and *reverse bias*.

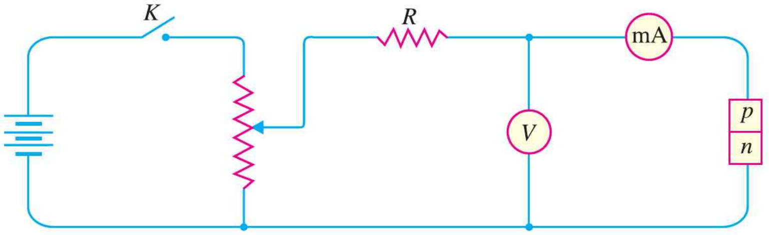


Fig. 5.24

(i) Zero external voltage. When the external voltage is zero, *i.e.* circuit is open at *K*, the potential barrier at the junction does not permit current flow. Therefore, the circuit current is zero as indicated by point *O* in Fig. 5.25.

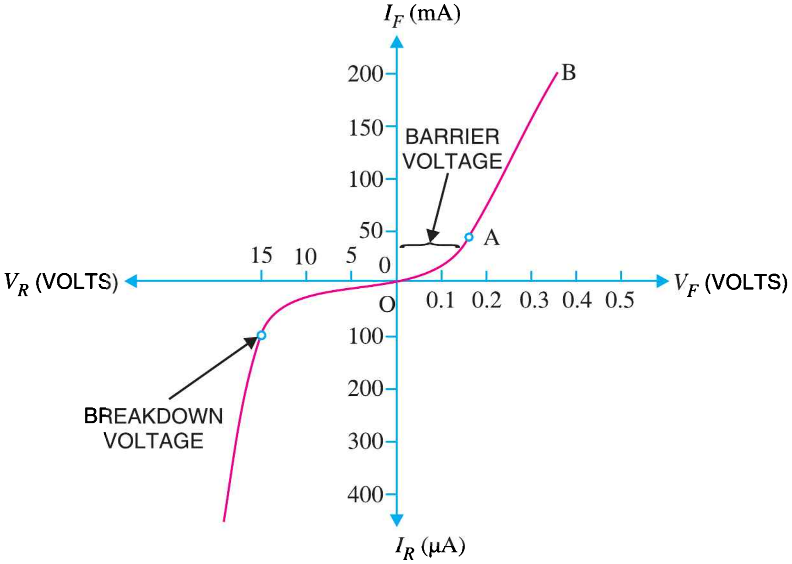


Fig. 5.25

---

* *R* is the current limiting resistance. It prevents the forward current from exceeding the permitted value.

(*ii*) **Forward bias.** With forward bias to the *pn* junction *i.e.* *p*-type connected to positive terminal and *n*-type connected to negative terminal, the potential barrier is reduced. At some forward voltage (0.7 V for Si and 0.3 V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit. From now onwards, the current increases with the increase in forward voltage. Thus, a rising curve *OB* is obtained with forward bias as shown in Fig. 5.25. From the forward characteristic, it is seen that at first (*region OA*),the current increases very slowly and the curve is non-linear. It is because the external applied voltage is used up in overcoming the potential barrier. However, once the external voltage exceeds the potential barrier voltage, the *pn* junction behaves like an ordinary conductor. Therefore, the current rises very sharply with increase in external voltage (*region AB on the curve*). The curve is almost linear.

(*iii*) **Reverse bias.** With reverse bias to the *pn* junction *i.e.* *p*-type connected to negative terminal and *n*-type connected to positive terminal, potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and practically no current flows through the circuit. However, in practice, a very small current (of the order of μ*A*) flows in the circuit with reverse bias as shown in the reverse characteristic. This is called *reverse *saturation current* (I_s) and is due to the minority carriers. It may be recalled that there are a few free electrons in *p*-type material and a few holes in *n*-type material. These undesirable free electrons in *p*-type and holes in *n*-type are called *minority carriers*. As shown in Fig. 5.26, to these minority carriers, the applied reverse bias appears as forward bias. Therefore, a **small current flows in the reverse direction.

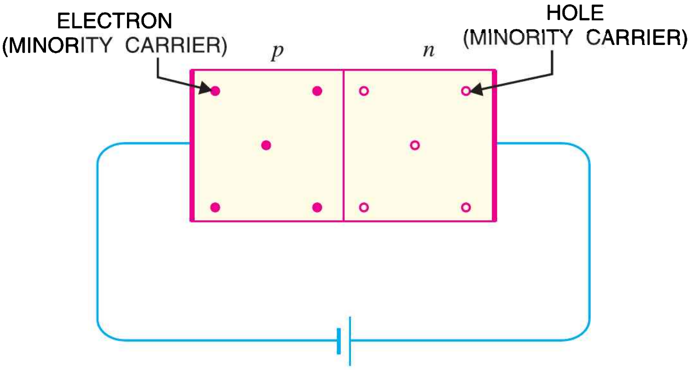


Fig. 5.26

If reverse voltage is increased continuously, the kinetic energy of electrons (minority carriers) may become high enough to knock out electrons from the semiconductor atoms. At this stage *breakdown* of the junction occurs, characterised by a sudden rise of reverse current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

Note. The forward current through a *pn* junction is due to the *majority carriers* produced by the impurity. However, reverse current is due to the *minority carriers* produced due to breaking of some co-valent bonds at room temperature.

5.19 Important Terms

Two important terms often used with *pn* junction (*i.e.* crystal diode) are *breakdown voltage* and *knee voltage*. We shall now explain these two terms in detail.

(*i*) **Breakdown voltage.** *It is the minimum reverse voltage at which pn junction breaks down with sudden rise in reverse current.*

Under normal reverse voltage, a very little reverse current flows through a *pn* junction. However, if the reverse voltage attains a high value, the junction may break down with sudden rise in reverse current. For understanding this point, refer to Fig. 5.27. Even at room temperature, some hole-electron pairs (minority carriers) are produced in the depletion layer as shown in Fig. 5.27 (*i*). With reverse bias, the electrons move towards the positive terminal of supply. At large reverse voltage, these electrons acquire high enough velocities to dislodge valence electrons from semiconductor atoms as shown in Fig. 5.27 (*ii*). The newly liberated electrons in turn free other valence electrons. In this way, we get an *avalanche* of free electrons. Therefore, the *pn* junction conducts a very large reverse current.

---

* The term saturation comes from the fact that it reaches its maximum level quickly and does not significantly change with the increase in reverse voltage.

** Reverse current increases with reverse voltage but can generally be regarded as negligible over the working range of voltages.

Once the breakdown voltage is reached, the high reverse current may damage the junction. Therefore, care should be taken that reverse voltage across a *pn* junction is always less than the breakdown voltage.

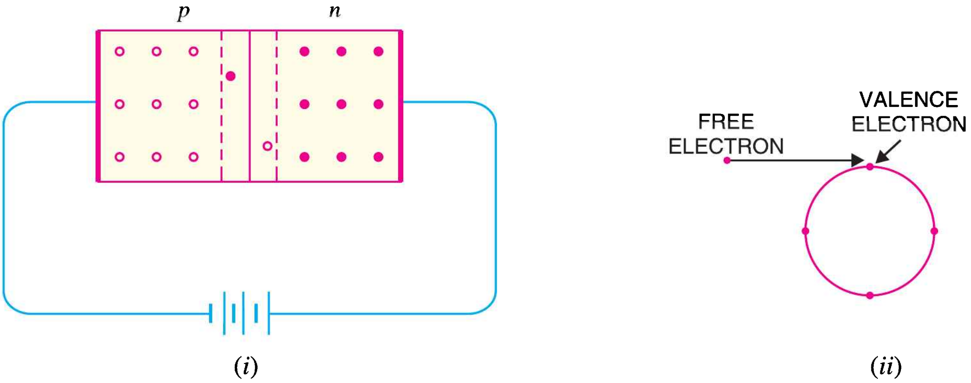


Fig. 5.27

(*ii*) **Knee voltage.** *It is the forward voltage at which the current through the junction starts to increase rapidly.*

When a diode is forward biased, it conducts current very slowly until we overcome the potential barrier. For silicon *pn* junction, potential barrier is 0.7 V whereas it is 0.3 V for germanium junction. It is clear from Fig. 5.28 that knee voltage for silicon diode is 0.7 V and 0.3 V for germanium diode.

Once the applied forward voltage exceeds the knee voltage, the current starts increasing rapidly. It may be added here that in order to get useful current through a *pn* junction, the applied voltage must be more than the knee voltage.

Note. The potential barrier voltage is also known as *turn-on voltage*. This is obtained by taking the straight line portion of the forward characteristic and extending it back to the horizontal axis.

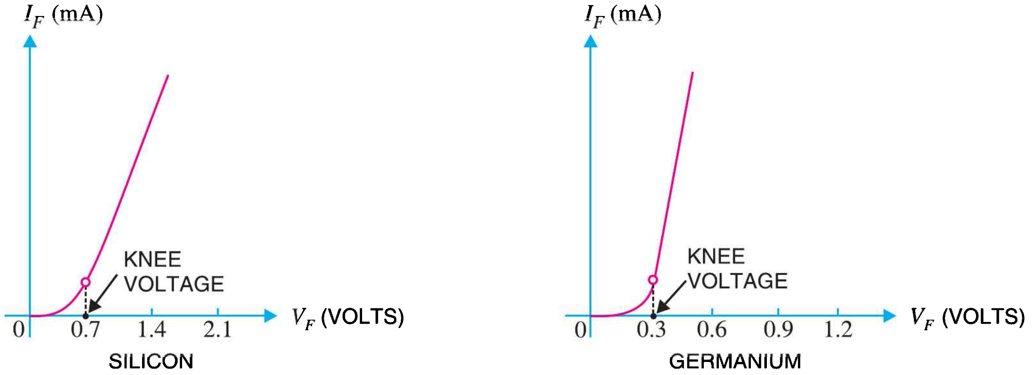


Fig. 5.28

5.20 Limitations in the Operating Conditions of *pn* Junction

Every *pn* junction has limiting values of *maximum forward current, peak inverse voltage* and *maximum power rating*. The *pn* junction will give satisfactory performance if it is operated within these limiting values. However, if these values are exceeded, the *pn* junction may be destroyed due to excessive heat.

(*i*) *Maximum forward current.* It is the highest instantaneous forward current that a *pn* junction can conduct without damage to the junction. Manufacturer's data sheet usually specifies this rating. If the forward current in a *pn* junction is more than this rating, the junction will be destroyed due to overheating.

(*ii*) *Peak inverse voltage (PIV).* It is the maximum reverse voltage that can be applied to the *pn* junction without damage to the junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier service. A *pn* junction *i.e.* a crystal diode is used as a rectifier to change alternating current into direct current. In such applications, care should be taken that reverse voltage across the diode during negative half-cycle of a.c. does not exceed the PIV of diode.

(*iii*) *Maximum power rating.* It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated at the junction is equal to the product of junction current and the voltage across the junction. This is a very important consideration and is invariably specified by the manufacturer in the data sheet.

MULTIPLE-CHOICE QUESTIONS

1. A semiconductor is formed by .... bonds.
(*i*) covalent (*ii*) electrovalent
(*iii*) co-ordinate (*iv*) none of the above

2. A semiconductor has .... temperature coefficient of resistance.
(*i*) positive (*ii*) zero
(*iii*) negative (*iv*) none of the above

3. The most commonly used semiconductor is ....
(*i*) germanium (*ii*) silicon
(*iii*) carbon (*iv*) sulphur

4. A semiconductor has generally .... valence electrons.
(*i*) 2 (*ii*) 3
(*iii*) 6 (*iv*) 4

5. The resistivity of pure germanium under standard conditions is about ....
(*i*) $6 \times 10^4\ \Omega$ cm (*ii*) $60\ \Omega$ cm
(*iii*) $3 \times 10^6\ \Omega$ cm (*iv*) $6 \times 10^{-4}\ \Omega$ cm

6. The resistivity of pure silicon is about ....
(*i*) $100\ \Omega$ cm (*ii*) $6000\ \Omega$ cm
(*iii*) $3 \times 10^5\ \Omega$ cm (*iv*) $1.6 \times 10^{-8}\ \Omega$ cm

7. When a pure semiconductor is heated, its resistance ....
(*i*) goes up (*ii*) goes down
(*iii*) remains the same (*iv*) cannot say

8. The strength of a semiconductor crystal comes from ....
(*i*) forces between nuclei
(*ii*) forces between protons
(*iii*) electron-pair bonds
(*iv*) none of the above

9. When a pentavalent impurity is added to a pure semiconductor, it becomes ....
(*i*) an insulator
(*ii*) an intrinsic semiconductor
(*iii*) *p*-type semiconductor
(*iv*) *n*-type semiconductor

10. Addition of pentavalent impurity to a semiconductor creates many ....
(*i*) free electrons (*ii*) holes
(*iii*) valence electrons
(*iv*) bound electrons

11. A pentavalent impurity has .... valence electrons.
(*i*) 3 (*ii*) 5
(*iii*) 4 (*iv*) 6

12. An *n*-type semiconductor is ....
(*i*) positively charged
(*ii*) negatively charged

(*iii*) electrically neutral
(*iv*) none of the above

13. A trivalent impurity has .... valence electrons.
(*i*) 4 (*ii*) 5
(*iii*) 6 (*iv*) 3

14. Addition of trivalent impurity to a semiconductor creates many ....
(*i*) holes (*ii*) free electrons
(*iii*) valence electrons
(*iv*) bound electrons

15. A hole in a semiconductor is defined as ....
(*i*) a free electron
(*ii*) the incomplete part of an electron pair bond
(*iii*) a free proton
(*iv*) a free neutron

16. The impurity level in an extrinsic semiconductor is about .... of pure semiconductor.
(*i*) 10 atoms for 10^8 atoms
(*ii*) 1 atom for 10^8 atoms
(*iii*) 1 atom for 10^4 atoms
(*iv*) 1 atom for 100 atoms

17. As the doping to a pure semiconductor increases, the bulk resistance of the semiconductor ....
(*i*) remains the same
(*ii*) increases
(*iii*) decreases
(*iv*) none of the above

18. A hole and electron in close proximity would tend to ....
(*i*) repel each other
(*ii*) attract each other
(*iii*) have no effect on each other
(*iv*) none of the above

19. In a semiconductor, current conduction is due ....
(*i*) only to holes
(*ii*) only to free electrons
(*iii*) to holes and free electrons
(*iv*) none of the above

20. The random motion of holes and free electrons due to thermal agitation is called ....
(*i*) diffusion (*ii*) pressure
(*iii*) ionisation (*iv*) none of the above

21. A forward biased *pn* junction has a resistance of the ....
(*i*) order of Ω (*ii*) order of kΩ
(*iii*) order of MΩ (*iv*) none of the above

22. The battery connections required to forward bias a *pn* junction are ....
(*i*) +ve terminal to *p* and –ve terminal to *n*
(*ii*) –ve terminal to *p* and +ve terminal to *n*
(*iii*) –ve terminal to *p* and –ve terminal to *n*
(*iv*) none of the above

23. The barrier voltage at a *pn* junction for germanium is about ....
(*i*) 3.5 V (*ii*) 3V
(*iii*) zero (*iv*) 0.3 V

24. In the depletion region of a *pn* junction, there is a shortage of ....
(*i*) acceptor ions (*ii*) holes and electrons
(*iii*) donor ions (*iv*) none of the above

25. A reverse biased *pn* junction has ....
(*i*) very narrow depletion layer
(*ii*) almost no current
(*iii*) very low resistance
(*iv*) large current flow

26. A *pn* junction acts as a ....
(*i*) controlled switch
(*ii*) bidirectional switch
(*iii*) unidirectional switch
(*iv*) none of the above

27. A reverse biased *pn* junction has resistance of the........
(*i*) order of Ω (*ii*) order of kΩ
(*iii*) order of MΩ (*iv*) none of the above

28. The leakage current across a *pn* junction is due to ....
(*i*) minority carriers
(*ii*) majority carriers
(*iii*) junction capacitance
(*iv*) none of the above

29. When the temperature of an extrinsic semiconductor is increased, the pronounced effect is on ....
(*i*) junction capacitance

(*ii*) minority carriers
(*iii*) majority carriers
(*iv*) none of the above

30. With forward bias to a *pn* junction, the width of depletion layer ....
(*i*) decreases (*ii*) increases
(*iii*) remains the same
(*iv*) none of the above

31. The leakage current in a *pn* junction is of the order of ....
(*i*) A (*ii*) mA
(*iii*) kA (*iv*) μA

32. In an intrinsic semiconductor, the number of free electrons ....
(*i*) equals the number of holes
(*ii*) is greater than the number of holes
(*iii*) is less than the number of holes
(*iv*) none of the above

33. At room temperature, an intrinsic semiconductor has ....
(*i*) many holes only
(*ii*) a few free electrons and holes
(*iii*) many free electrons only
(*iv*) no holes or free electrons

34. At absolute temperature, an intrinsic semiconductor has ....
(*i*) a few free electrons
(*ii*) many holes
(*iii*) many free electrons
(*iv*) no holes or free electrons

35. At room temperature, an intrinsic silicon crystal acts approximately as ....
(*i*) a battery
(*ii*) a conductor
(*iii*) an insulator
(*iv*) a piece of copper wire

Answers to Multiple-Choice Questions

1. (*i*)	**2.** (*iii*)	**3.** (*ii*)	**4.** (*iv*)	**5.** (*ii*)
6. (*ii*)	**7.** (*ii*)	**8.** (*iii*)	**9.** (*iv*)	**10.** (*i*)
11. (*ii*)	**12.** (*iii*)	**13.** (*iv*)	**14.** (*i*)	**15.** (*ii*)
16. (*ii*)	**17.** (*iii*)	**18.** (*ii*)	**19.** (*iii*)	**20.** (*i*)
21. (*i*)	**22.** (*i*)	**23.** (*iv*)	**24.** (*ii*)	**25.** (*ii*)
26. (*iii*)	**27.** (*iii*)	**28.** (*i*)	**29.** (*ii*)	**30.** (*i*)
31. (*iv*)	**32.** (*i*)	**33.** (*ii*)	**34.** (*iv*)	**35.** (*iii*)

Chapter Review Topics

1. What do you understand by a semi-conductor ? Discuss some important properties of semiconductors.
2. Which are the most commonly used semiconductors and why ?
3. Give the energy band description of semiconductors.
4. Discuss the effect of temperature on semiconductors.
5. Give the mechanism of hole current flow in a semiconductor.
6. What do you understand by intrinsic and extrinsic semiconductors ?
7. What is a *pn* junction ? Explain the formation of potential barrier in a *pn* junction.
8. Discuss the behaviour of a *pn* junction under forward and reverse biasing.
9. Draw and explain the *V-I* characteristics of a *pn* junction.
10. Write short notes on the following :
  (*i*) Breakdown voltage
  (*ii*) Knee voltage
  (*iii*) Limitations in the operating conditions of *pn* junction

Discussion Questions

1. Why is a semiconductor an insulator at ordinary temperature ?
2. Why are electron carriers present in *p*-type semiconductor ?
3. Why is silicon preferred to germanium in the manufacture of semiconductor devices ?
4. What is the importance of peak inverse voltage ?

6

Semiconductor Diode

6.1 Semiconductor Diode
6.3 Resistance of Crystal Diode
6.5 Crystal Diode Equivalent Circuits
6.7 Crystal Diode Rectifiers
6.9 Output Frequency of Half-Wave Rectifier
6.11 Full-Wave Rectifier
6.13 Full-Wave Bridge Rectifier
6.15 Efficiency of Full-Wave Rectifier
6.17 Nature of Rectifier Output
6.19 Comparison of Rectifiers
6.21 Types of Filter Circuits
6.23 Half-Wave Voltage Doubler
6.25 Zener Diode
6.27 Zener Diode as Voltage Stabiliser
6.29 Crystal Diodes versus Vacuum Diodes

INTRODUCTION

It has already been discussed in the previous chapter that a *pn* junction conducts current easily when forward biased and practically no current flows when it is reverse biased. This unilateral conduction characteristic of *pn* junction (*i.e.* semiconductor diode) is similar to that of a vacuum diode. Therefore, like a vacuum diode, a semiconductor diode can also accomplish the job of *rectification i.e.* change alternating current to direct current. However, semiconductor diodes have become more *popular as they are smaller in size, cheaper and robust and usually operate with greater efficiency. In this chapter, we shall focus our attention on the circuit performance and applications of semiconductor diodes.

---

* On the other hand, vacuum diodes can withstand high reverse voltages and can operate at fairly high temperatures.

6.1 Semiconductor Diode

A pn junction is known as a **semi-conductor** *or* ***crystal diode**.

The outstanding property of a crystal diode to conduct current in one direction only permits it to be used as a rectifier. A crystal diode is usually represented by the schematic symbol shown in Fig. 6.1. The arrow in the symbol indicates the direction of easier conventional current flow.

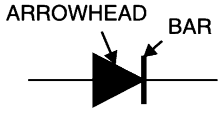
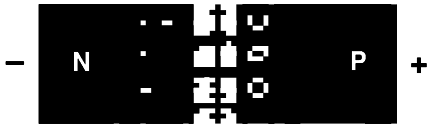


Fig. 6.1



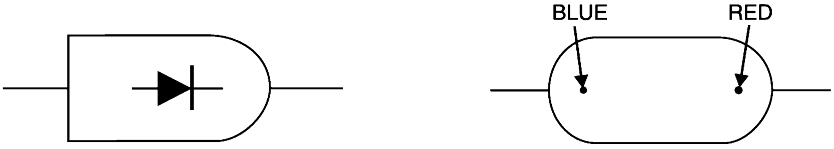
A crystal diode has two terminals. When it is connected in a circuit, one thing to decide is whether the diode is forward or reverse biased. There is an easy rule to ascertain it. If the external circuit is trying to push the conventional current in the direction of arrow, the diode is forward biased. On the other hand, if the conventional current is trying to flow opposite to arrowhead, the diode is reverse biased. Putting in simple words :

(*i*) If *arrowhead* of diode symbol is *positive w.r.t. bar* of the symbol, the diode is forward biased.

(*ii*) If the *arrowhead* of diode symbol is *negative w.r.t. bar*, the diode is reverse biased.

Identification of crystal diode terminals. While using a crystal diode, it is often necessary to know which end is arrowhead and which end is bar. For this purpose, the following methods are available :

(*i*) Some manufacturers actually paint the symbol on the body of the diode *e.g. BY*127, *BY*114 crystal diodes manufactured by *BEL* [See Fig. 6.2 (*i*)].



BY 127
(*i*)

OA 80
(*ii*)

Fig. 6.2

(*ii*) Sometimes, red and blue marks are used on the body of the crystal diode. Red mark denotes arrow whereas blue mark indicates bar *e.g. OA80* crystal diode [See Fig. 6.2 (*ii*)].

6.2 Crystal Diode as a Rectifier

Fig. 6.3 illustrates the rectifying action of a crystal diode. The a.c. input voltage to be rectified, the diode and load R_L are connected in series. The d.c. output is obtained across the load as explained in the following discussion. During the positive half-cycle of a.c. input voltage, the arrowhead becomes positive *w.r.t.* bar. Therefore, diode is forward biased and conducts current in the circuit. The result is that positive half-cycle of input voltage appears across R_L as shown. However, during the negative half-cycle of input a.c. voltage, the diode becomes reverse biased because now the arrowhead is negative *w.r.t.* bar. Therefore, diode does not conduct and no voltage appears across load R_L. The result is that output consists of positive half-cycles of input a.c. voltage while the negative half-cycles are suppressed. In this way, crystal diode has been able to do rectification i.e. change a.c. into d.c. It may be seen that output across R_L is pulsating d.c.

---

* So called because *pn* junction is grown out of a crystal.

It is interesting to see that behaviour of diode is like a *switch*. When the diode is forward biased, it behaves like a closed switch and connects the a.c. supply to the load R_L. However, when the diode is reverse biased, it behaves like an open switch and disconnects the a.c. supply from the load R_L. This switching action of diode permits only the positive half-cycles of input a.c. voltage to appear across R_L.

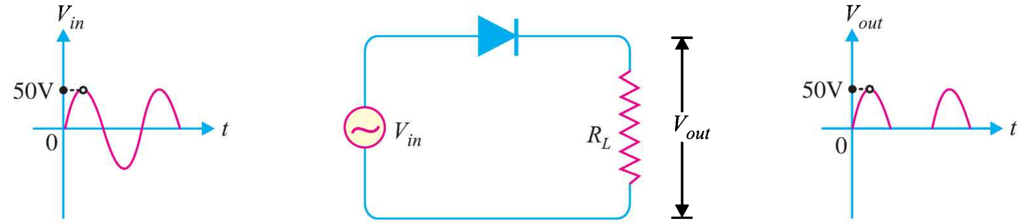
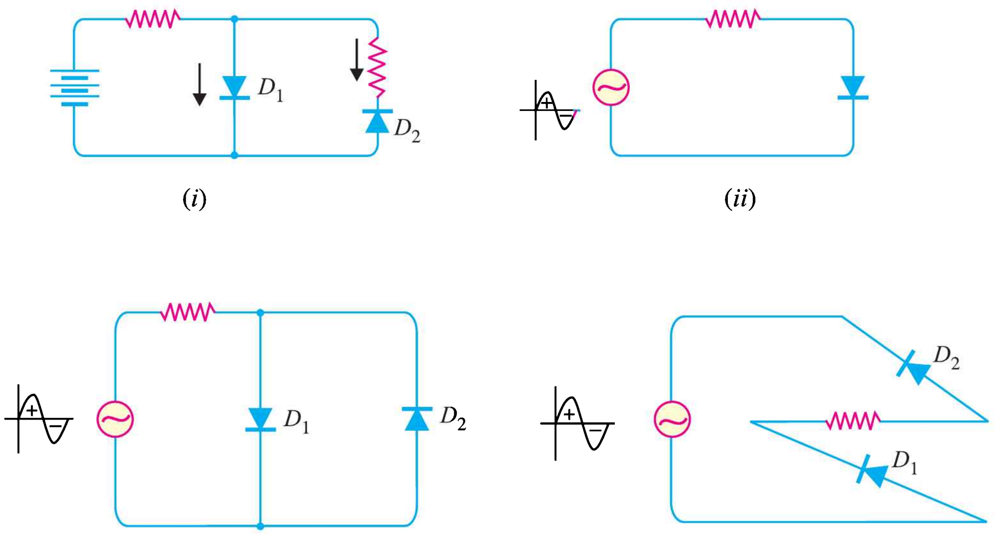


Fig. 6.3

Example 6.1. *In each diode circuit of Fig. 6.4, find whether the diodes are forward or reverse biased.*



(*i*) (*ii*)

(*iii*) (*iv*)

Fig. 6.4

Solution.

(***i***) Refer to Fig. 6.4 (*i*). The conventional current coming out of battery flows in the branch circuits. In diode D_1, the conventional current flows in the direction of arrowhead and hence this diode is forward biased. However, in diode D_2,the conventional current flows opposite to arrowhead and hence this diode is reverse biased.

(***ii***) Refer to Fig. 6.4 (*ii*). During the positive half-cycle of input a.c. voltage, the conventional current flows in the direction of arrowhead and hence diode is forward biased. However, during the negative half-cycle of input a.c. voltage, the diode is reverse biased.

(***iii***) Refer to Fig. 6.4 (*iii*). During the positive half-cycle of input a.c. voltage, conventional current flows in the direction of arrowhead in D_1 but it flows opposite to arrowhead in D_2. Therefore, during positive half-cycle, diode D_1 is forward biased and diode D_2 reverse biased. However, during the negative half-cycle of input a.c. voltage, diode D_2 is forward biased and D_1 is reverse biased.

(*iv*) Refer to Fig. 6.4 (*iv*). During the positive half-cycle of input a.c. voltage, both the diodes are reverse biased. However, during the negative half-cycle of input a.c. voltage, both the diodes are forward biased.

6.3 Resistance of Crystal Diode

It has already been discussed that a forward biased diode conducts easily whereas a reverse biased diode practically conducts no current. It means that *forward resistance* of a diode is quite small as compared with its *reverse resistance.*

1. Forward resistance. The resistance offered by the diode to forward bias is known as *forward resistance.* This resistance is not the same for the flow of direct current as for the changing current. Accordingly; this resistance is of two types, namely; *d.c. forward resistance* and *a.c. forward resistance.*

(*i*) *d.c. forward resistance.* It is the opposition offered by the diode to the direct current. It is measured by the ratio of d.c. voltage across the diode to the resulting d.c. current through it. Thus, referring to the forward characteristic in Fig. 6.5, it is clear that when forward voltage is *OA*, the forward current is *OB.*

$$\therefore \quad \text{d.c. forward resistance, } R_f = \frac{OA}{OB}$$

(*ii*) *a.c. forward resistance.* It is the opposition offered by the diode to the changing forward current. It is measured by the ratio of change in voltage across diode to the resulting change in current through it *i.e.*

$$\text{a.c. forward resistance, } r_f = \frac{\text{Change in voltage across diode}}{\text{Corresponding change in current through diode}}$$

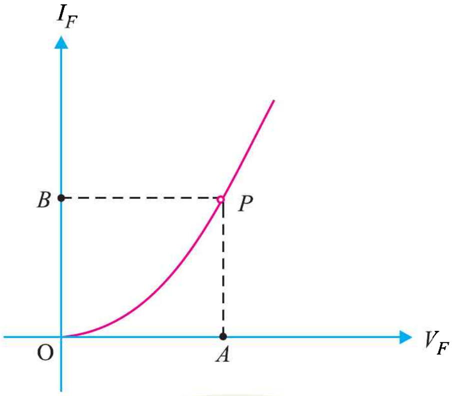


Fig. 6.5

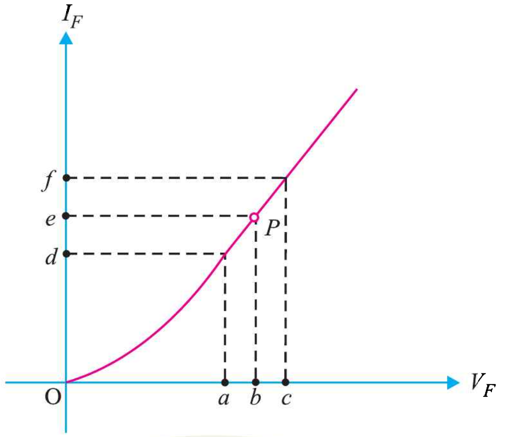


Fig. 6.6

The a.c. forward resistance is more significant as the diodes are generally used with alternating voltages. The a.c. forward resistance can be determined from the forward characteristic as shown in Fig. 6.6. If *P* is the operating point at any instant, then forward voltage is *ob* and forward current is *oe.* To find the a.c. forward resistance, vary the forward voltage on both sides of the operating point equally as shown in Fig. 6.6 where *ab* = *bc*. It is clear from this figure that :

For forward voltage *oa*, circuit current is *od.*

For forward voltage *oc*, circuit current is *of.*

$$\therefore \quad \text{a.c. forward resistance, } r_f = \frac{\text{Change in forward voltage}}{\text{Change in forward current}} = \frac{oc - oa}{of - od} = \frac{ac}{df}$$

It may be mentioned here that forward resistance of a crystal diode is very small, ranging from 1 to 25 Ω.

2. Reverse resistance. The resistance offered by the diode to the reverse bias is known as *reverse resistance*. It can be d.c. reverse resistance or a.c. reverse resistance depending upon whether the reverse bias is direct or changing voltage. Ideally, the reverse resistance of a diode is infinite. However, in practice, the reverse resistance is not infinite because for any value of reverse bias, there does exist a small leakage current. It may be emphasised here that reverse resistance is very large compared to the forward resistance. In germanium diodes, the ratio of reverse to forward resistance is 40000 : 1 while for silicon this ratio is 1000000 : 1.

6.4 Equivalent Circuit of Crystal Diode

It is generally profitable to replace a device or system by its equivalent circuit. An equivalent circuit of a device (*e.g.* crystal diode, transistor etc.) is a combination of electric elements, which when connected in a circuit, acts exactly as does the device when connected in the same circuit. Once the device is replaced by its equivalent circuit, the resulting network can be solved by traditional circuit analysis techniques. We shall now find the equivalent circuit of a crystal diode.

(*i*) ***Approximate Equivalent circuit.** When the forward voltage V_F is applied across a diode, it will not conduct till the potential barrier V_0 at the junction is overcome. When the forward voltage exceeds the potential barrier voltage, the diode starts conducting as shown in Fig. 6.7 (*i*). The forward current I_f flowing through the diode causes a voltage drop in its internal resistance r_f. Therefore, the forward voltage V_F applied across the *actual* diode has to overcome :

(*a*) potential barrier V_0

(*b*) internal drop $I_f r_f$

$$\therefore \quad V_F = V_0 + I_f r_f$$

For a silicon diode, V_0 = 0.7 V whereas for a germanium diode, V_0 = 0.3 V.

Therefore, approximate equivalent circuit for a crystal diode is a switch in series with a battery V_0 and internal resistance r_f as shown in Fig. 6.7 (*ii*). This approximate equivalent circuit of a diode is very helpful in studying the performance of the diode in a circuit.

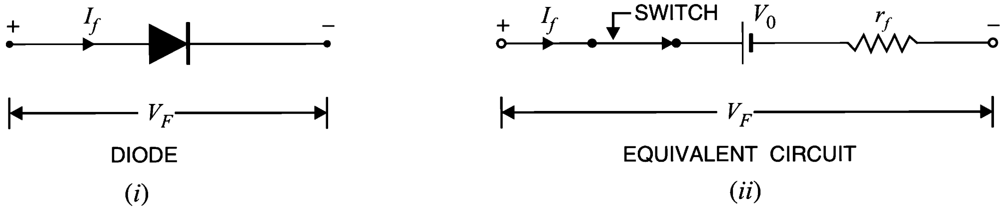


Fig. 6.7

(*ii*) **Simplified Equivalent circuit.** For most applications, the internal resistance r_f of the crystal diode can be ignored in comparison to other elements in the equivalent circuit. The equivalent circuit then reduces to the one shown in Fig. 6.8 (*ii*). This simplified equivalent circuit of the crystal diode is frequently used in diode-circuit analysis.

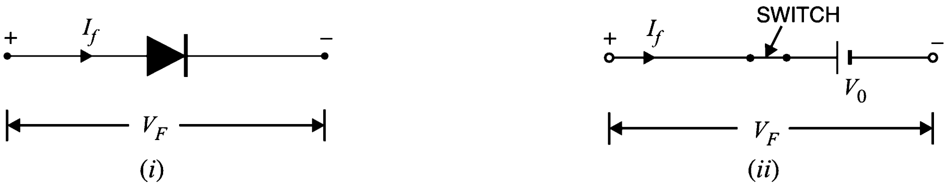


Fig. 6.8

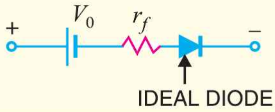
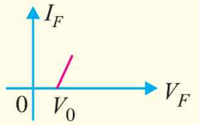
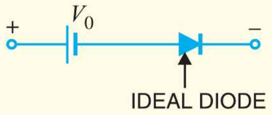
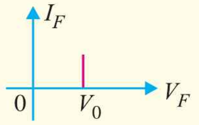
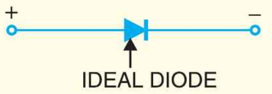
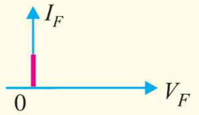
---

* We assume here that *V*/*I* characteristic of crystal diode is linear.

***(iii)* Ideal diode model.** An ideal diode is one which behaves as a perfect conductor when forward biased and as a perfect insulator when reverse biased. Obviously, in such a hypothetical situation, forward resistance $r_f = 0$ and potential barrier V_0 is considered negligible. It may be mentioned here that although ideal diode is never found in practice, yet diode circuit analysis is made on this basis. *Therefore, while discussing diode circuits, the diode will be assumed ideal unless and until stated otherwise.*

6.5 Crystal Diode Equivalent Circuits

It is desirable to sum up the various models of crystal diode equivalent circuit in the tabular form given below:

S.No.	Type	Model	Characteristic
1.	Approximate model		
2.	Simplified model		
3.	Ideal Model		

Example 6.2. *An a.c. voltage of peak value 20 V is connected in series with a silicon diode and load resistance of 500 Ω. If the forward resistance of diode is 10 Ω, find :*

(i) peak current through diode *(ii) peak output voltage*

What will be these values if the diode is assumed to be ideal ?

Solution.

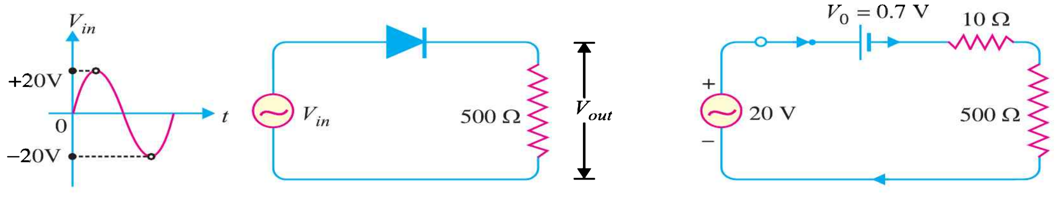
Peak input voltage = 20 V

Forward resistance, r_f = 10 Ω

Load resistance, R_L = 500 Ω

Potential barrier voltage, V_0 = 0.7 V

The diode will conduct during the positive half-cycles of a.c. input voltage only. The equivalent circuit is shown in Fig. 6.9 (*ii*).



(*i*) (*ii*)

Fig. 6.9

(*i*) The peak current through the diode will occur at the instant when the input voltage reaches positive peak *i.e.* $V_{in} = V_F = 20$ V.

$$\therefore \quad V_F = V_0 + (I_f)_{peak}\,[r_f + R_L] \qquad \ldots(i)$$

$$\text{or} \quad (I_f)_{peak} = \frac{V_F - V_0}{r_f + R_L} = \frac{20 - 0.7}{10 + 500} = \frac{19.3}{510}\text{ A} = \mathbf{37.8\ mA}$$

(*ii*) Peak output voltage $= (I_f)_{peak} \times R_L = 37.8\text{ mA} \times 500\ \Omega = \mathbf{18.9\ V}$

Ideal diode. For an ideal diode, put $V_0 = 0$ and $r_f = 0$ in equation (*i*).

$$\therefore \quad V_F = (I_f)_{peak} \times R_L$$

$$\text{or} \quad (I_f)_{peak} = \frac{V_F}{R_L} = \frac{20\text{ V}}{500\ \Omega} = \mathbf{40\ mA}$$

Peak output voltage $= (I_f)_{peak} \times R_L = 40\text{ mA} \times 500\ \Omega = \mathbf{20\ V}$

Comments. It is clear from the above example that output voltage is *nearly* the same whether the actual diode is used or the diode is considered ideal. This is due to the fact that input voltage is quite large as compared with V_0 and voltage drop in r_f. Therefore, nearly the whole input forward voltage appears across the load. For this reason, diode circuit analysis is generally made on the ideal diode basis.

Example 6.3. *Find the current through the diode in the circuit shown in Fig. 6.10 (i). Assume the diode to be ideal.*

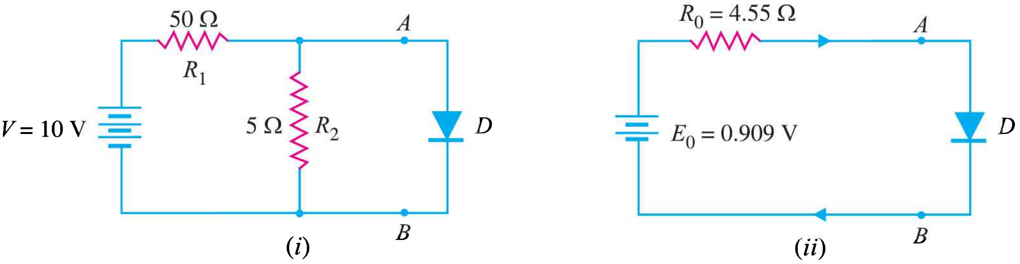


Fig. 6.10

Solution. We shall use Thevenin's theorem to find current in the diode. Referring to Fig. 6.10(*i*),

$$E_0 = \text{Thevenin's voltage}$$

$$= \text{Open circuited voltage across } AB \text{ with diode removed}$$

$$= \frac{R_2}{R_1 + R_2} \times V = \frac{5}{50 + 5} \times 10 = 0.909\text{ V}$$

$$R_0 = \text{Thevenin's resistance}$$

= Resistance at terminals *AB* with diode removed and battery replaced by a short circuit

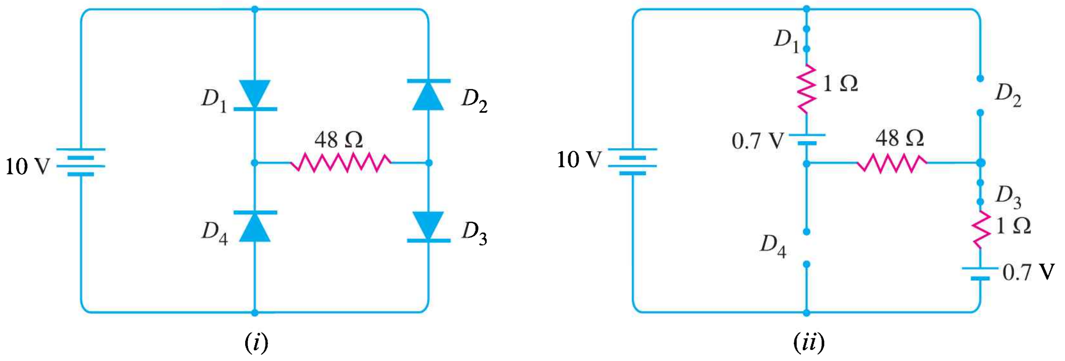
$$= \frac{R_1 R_2}{R_1 + R_2} = \frac{50 \times 5}{50 + 5} = 4.55\ \Omega$$

Fig. 6.10 (*ii*) shows Thevenin's equivalent circuit. Since the diode is ideal, it has zero resistance.

$$\therefore \quad \text{Current through diode} = \frac{E_0}{R_0} = \frac{0.909}{4.55} = 0.2\text{ A} = \mathbf{200\ mA}$$

Example 6.4. *Calculate the current through 48 Ω resistor in the circuit shown in Fig. 6.11 (i). Assume the diodes to be of silicon and forward resistance of each diode is 1 Ω.*

Solution. Diodes D_1 and D_3 are forward biased while diodes D_2 and D_4 are reverse biased. We can, therefore, consider the branches containing diodes D_2 and D_4 as "open". Replacing diodes D_1 and D_3 by their equivalent circuits and making the branches containing diodes D_2 and D_4 open, we get the circuit shown in Fig. 6.11 (*ii*). Note that for a silicon diode, the barrier voltage is 0.7 V.



10 V
D_1
D_2
48 Ω
D_4
D_3
(i)
10 V
D_1
1 Ω
0.7 V
48 Ω
D_2
D_3
1 Ω
0.7 V
D_4
(ii)

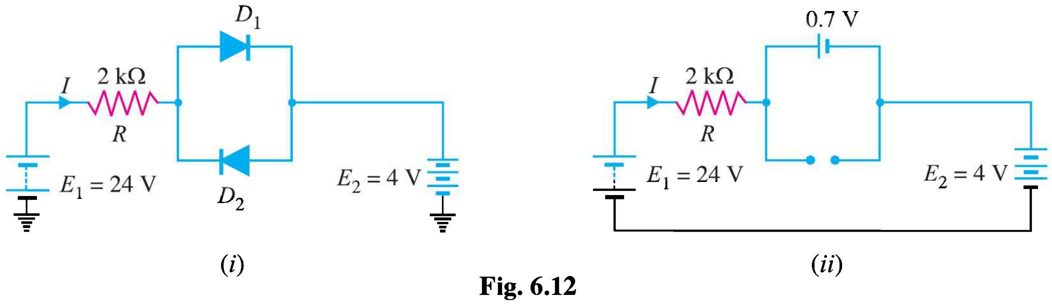
Fig. 6.11

Net circuit voltage = 10 – 0.7 – 0.7 = 8.6 V

Total circuit resistance = 1 + 48 + 1 = 50 Ω

∴ Circuit current = 8.6/50 = 0.172 A = **172 mA**

Example 6.5. *Determine the current I in the circuit shown in Fig. 6.12 (i). Assume the diodes to be of silicon and forward resistance of diodes to be zero.*



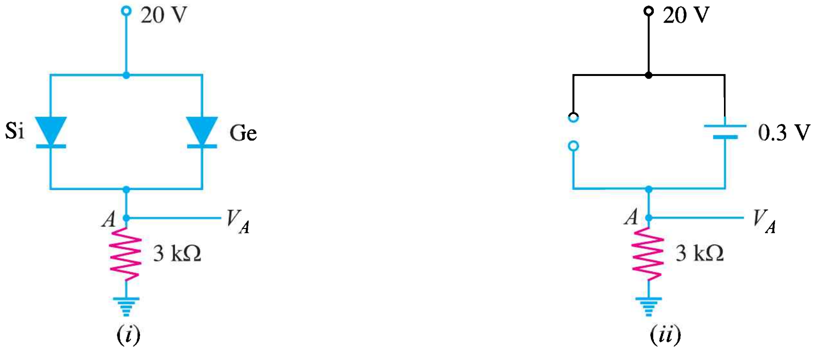
D_1
I
2 kΩ
R
$E_1 = 24$ V
D_2
$E_2 = 4$ V
(i)
0.7 V
I
2 kΩ
R
$E_1 = 24$ V
$E_2 = 4$ V
(ii)

Fig. 6.12

Solution. The conditions of the problem suggest that diode D_1 is forward biased and diode D_2 is reverse biased. We can, therefore, consider the branch containing diode D_2 as open as shown in Fig. 6.12 (*ii*). Further, diode D_1 can be replaced by its simplified equivalent circuit.

$$\therefore \quad I = \frac{E_1 - E_2 - V_0}{R} = \frac{24 - 4 - 0.7}{2\text{ k}\Omega} = \frac{19.3\text{ V}}{2\text{ k}\Omega} = \mathbf{9.65\ mA}$$

Example 6.6. *Find the voltage V_A in the circuit shown in Fig. 6.13 (i). Use simplified model.*



20 V
Si
Ge
A
V_A
3 kΩ
(i)
20 V
0.3 V
A
V_A
3 kΩ
(ii)

Fig. 6.13

Solution. It appears that when the applied voltage is switched on, both the diodes will turn "on". But that is not so. When voltage is applied, germanium diode ($V_0 = 0.3$ V) will turn on first and a level of 0.3 V is maintained across the parallel circuit. The silicon diode never gets the opportunity to have 0.7 V across it and, therefore, remains in open-circuit state as shown in Fig. 6.13 (*ii*).

$$\therefore \quad V_A = 20 - 0.3 = \mathbf{19.7\ V}$$

Example 6.7. *Find V_Q and I_D in the network shown in Fig. 6.14 (i). Use simplified model.*

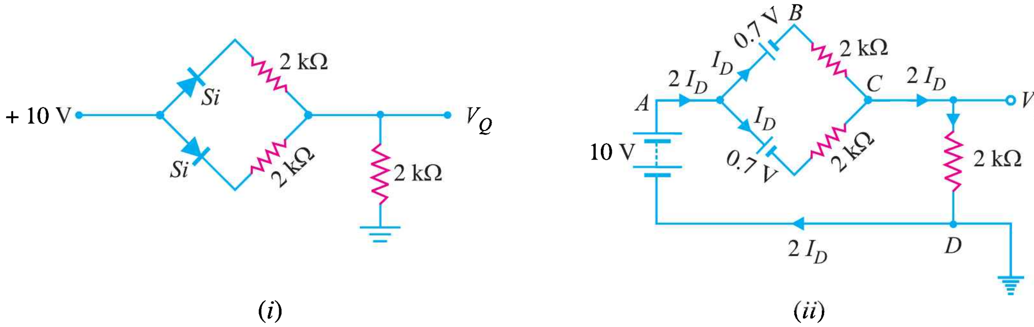
Solution. Replace the diodes by their simplified models. The resulting circuit will be as shown in Fig. 6.14 (*ii*). By symmetry, current in each branch is I_D so that current in branch *CD* is $2I_D$. Applying Kirchhoff's voltage law to the closed circuit *ABCDA*, we have,

$$-0.7 - I_D \times 2 - 2\,I_D \times 2 + 10 = 0 \qquad (I_D \text{ in mA})$$

$$\text{or} \quad 6\,I_D = 9.3$$

$$\therefore \quad I_D = \frac{9.3}{6} = \mathbf{1.55\ mA}$$

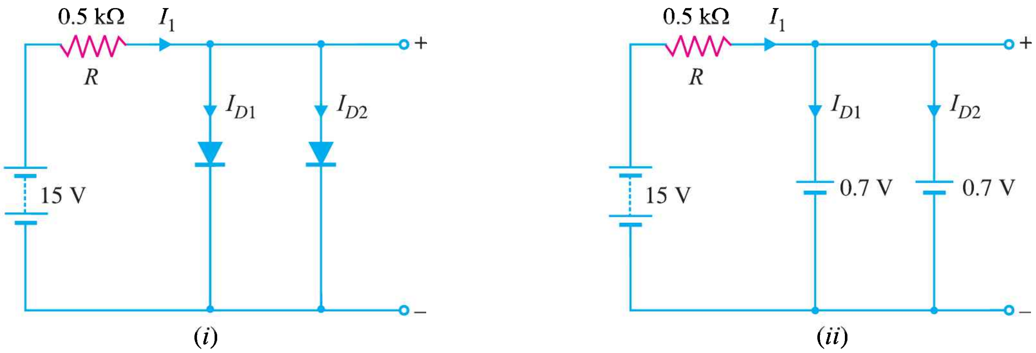
$$\text{Also} \quad V_Q = (2\,I_D) \times 2\text{ k}\Omega = (2 \times 1.55\text{ mA}) \times 2\text{ k}\Omega = \mathbf{6.2\ V}$$



(*i*) (*ii*)

Fig. 6.14

Example 6.8. *Determine current through each diode in the circuit shown in Fig. 6.15 (i). Use simplified model. Assume diodes to be similar.*



(*i*) (*ii*)

Fig. 6.15

Solution. The applied voltage forward biases each diode so that they conduct current in the same direction. Fig. 6.15 (*ii*) shows the equivalent circuit using simplified model. Referring to Fig. 6.15 (*ii*),

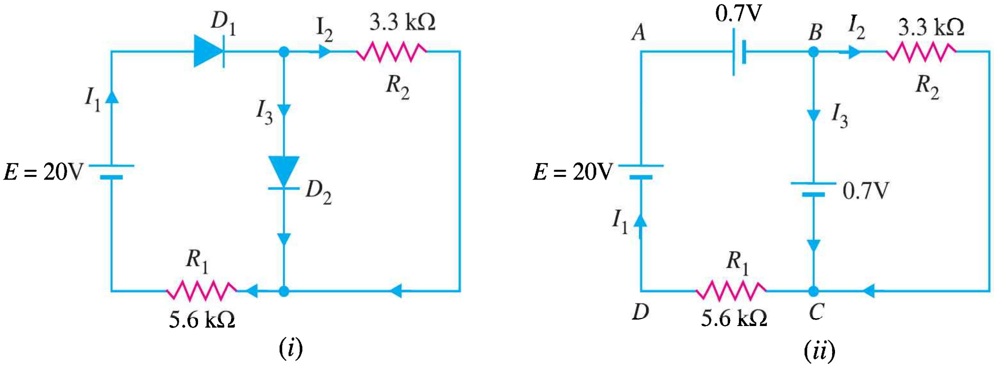
$$I_1 = \frac{\text{Voltage across } R}{R} = \frac{15 - 0.7}{0.5\text{ k}\Omega} = 28.6\text{ mA}$$

Since the diodes are similar, $I_{D1} = I_{D2} = \dfrac{I_1}{2} = \dfrac{28.6}{2} = \mathbf{14.3\ mA}$

Comments. Note the use of placing the diodes in parallel. If the current rating of each diode is

20 mA and a single diode is used in this circuit, a current of 28.6 mA would flow through the diode, thus damaging the device. By placing them in parallel, the current is limited to a safe value of 14.3 mA for the same terminal voltage.

Example 6.9. *Determine the currents I_1, I_2 and I_3 for the network shown in Fig. 6.16(i). Use simplified model for the diodes.*



D_1
I_2
3.3 kΩ
R_2
I_1
I_3
E = 20V
D_2
R_1
5.6 kΩ
(i)
0.7V
A
B
I_2
3.3 kΩ
R_2
I_3
E = 20V
0.7V
I_1
R_1
D
5.6 kΩ
C
(ii)

Fig. 6.16

Solution. An inspection of the circuit shown in Fig. 6.16 (*i*) shows that both diodes D_1 and D_2 are forward biased. Using simplified model for the diodes, the circuit shown in Fig. 6.16 (*i*) becomes the one shown in Fig. 6.16 (*ii*). The voltage across R_2 (= 3.3 k Ω) is 0.7V.

$$\therefore \qquad I_2 = \frac{0.7 \text{ V}}{3.3 \text{ k}\Omega} = \mathbf{0.212 \text{ mA}}$$

Applying Kirchhoff's voltage law to loop *ABCDA* in Fig. 6.16 (*ii*), we have,

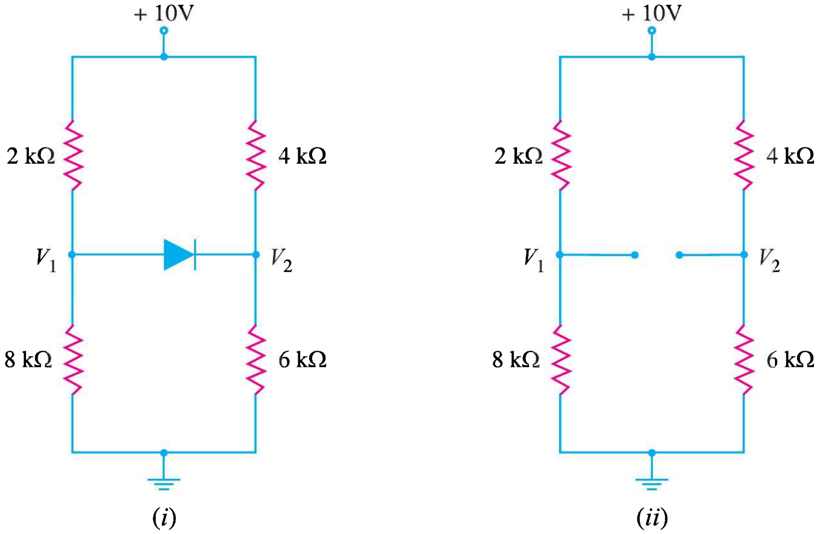
$$-0.7 - 0.7 - I_1 R_1 + 20 = 0$$

$$\therefore \qquad I_1 = \frac{20 - 0.7 - 0.7}{R_1} = \frac{18.6 \text{ V}}{5.6 \text{ k}\Omega} = \mathbf{3.32 \text{ mA}}$$

Now $\qquad I_1 = I_2 + I_3$

$$\therefore \qquad I_3 = I_1 - I_2 = 3.32 - 0.212 = \mathbf{3.108 \text{ mA}}$$

Example 6.10. *Determine if the diode (ideal) in Fig. 6.17 (i) is forward biased or reverse biased.*



+ 10V
2 kΩ
4 kΩ
V_1
V_2
8 kΩ
6 kΩ
(i)
+ 10V
2 kΩ
4 kΩ
V_1
V_2
8 kΩ
6 kΩ
(ii)

Fig. 6.17

Solution. Let us assume that diode in Fig. 6.17 (*i*) is *OFF i.e.* it is reverse biased. The circuit then becomes as shown in Fig. 6.17 (*ii*). Referring to Fig. 6.17 (*ii*), we have,

$$V_1 = \frac{10\text{ V}}{2\text{ k}\Omega + 8\text{ k}\Omega} \times 8\text{ k}\Omega = 8\text{V}$$

$$V_2 = \frac{10\text{ V}}{4\text{ k}\Omega + 6\text{ k}\Omega} \times 6\text{ k}\Omega = 6\text{V}$$

$\therefore$ Voltage across diode $= V_1 - V_2 = 8 - 6 = 2\text{V}$

Now $V_1 - V_2 = 2\text{V}$ is enough voltage to make the diode *forward biased*. Therefore, our initial assumption was wrong.

Example 6.11. *Determine the state of diode for the circuit shown in Fig. 6.18 (i) and find I_D and V_D. Assume simplified model for the diode.*

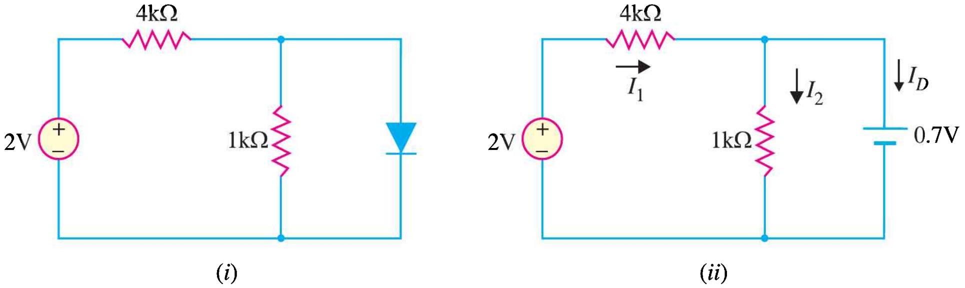


Fig. 6.18

Solution. Let us assume that the diode is *ON*. Therefore, we can replace the diode with a 0.7V battery as shown in Fig. 6.18 (*ii*). Referring to Fig. 6.18 (*ii*), we have,

$$I_1 = \frac{(2 - 0.7)\text{ V}}{4\text{ k}\Omega} = \frac{1.3\text{ V}}{4\text{ k}\Omega} = 0.325\text{ mA}$$

$$I_2 = \frac{0.7\text{ V}}{1\text{ k}\Omega} = 0.7\text{ mA}$$

Now $\quad I_D = I_1 - I_2 = 0.325 - 0.7 = -0.375\text{ mA}$

Since the diode current is negative, the diode must be **OFF** and the true value of diode current is I_D = **0 mA**. Our initial assumption was wrong. In order to analyse the circuit properly, we should replace the diode in Fig. 6.18 (*i*) with an open circuit as shown in Fig. 6.19. The voltage V_D across the diode is

$$V_D = \frac{2\text{ V}}{1\text{ k}\Omega + 4\text{ k}\Omega} \times 1\text{ k}\Omega = \mathbf{0.4V}$$

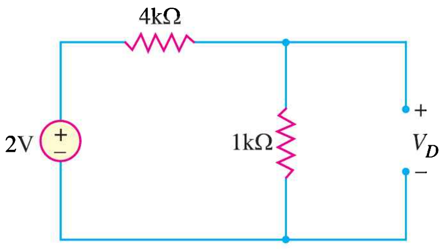


Fig. 6.19

We know that 0.7V is required to turn *ON* the diode. Since V_D is only 0.4V, the answer confirms that the diode is *OFF*.

6.6 Important Terms

While discussing the diode circuits, the reader will generally come across the following terms :

(*i*) **Forward current.** It is the current flowing through a forward biased diode. Every diode has a maximum value of forward current which it can safely carry. If this value is exceeded, the diode may be destroyed due to excessive heat. For this reason, the manufacturers' data sheet specifies the maximum forward current that a diode can handle safely.

(*ii*) **Peak inverse voltage.** *It is the maximum reverse voltage that a diode can withstand without destroying the junction.*

If the reverse voltage across a diode exceeds this value, the reverse current increases sharply and breaks down the junction due to excessive heat. Peak inverse voltage is extremely important when diode is used as a rectifier. In rectifier service, it has to be ensured that reverse voltage across the diode does not exceed its PIV during the negative half-cycle of input a.c. voltage. As a matter of fact, PIV consideration is generally the deciding factor in diode rectifier circuits. The peak inverse voltage may be between 10V and 10 kV depending upon the type of diode.

(*iii*) **Reverse current or leakage current.** It is the current that flows through a reverse biased diode. This current is due to the minority carriers. Under normal operating voltages, the reverse current is quite small. Its value is extremely small (< 1μ A) for silicon diodes but it is appreciable (≃ 100 μA) for germanium diodes.

It may be noted that the reverse current is usually very small as compared with forward current. For example, the forward current for a typical diode might range upto 100 mA while the reverse current might be only a few μA—a ratio of many thousands between forward and reverse currents.

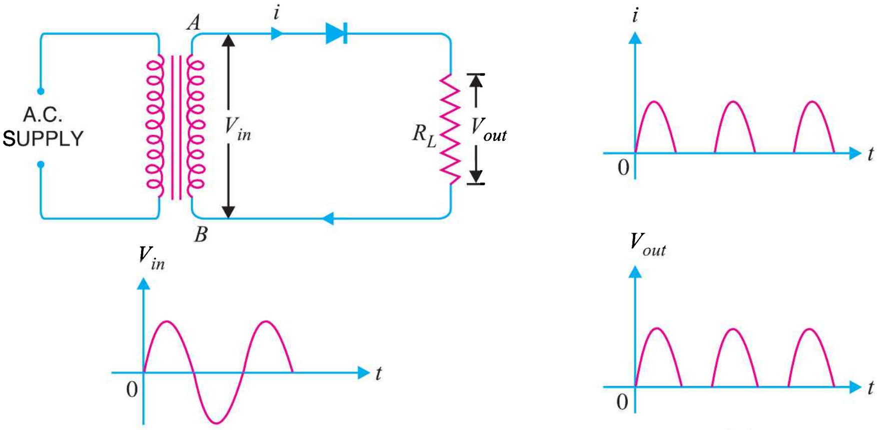
6.7 Crystal Diode Rectifiers

For reasons associated with economics of generation and transmission, the electric power available is usually an a.c. supply. The supply voltage varies sinusoidally and has a frequency of 50 Hz. It is used for lighting, heating and electric motors. But there are many applications (*e.g.* electronic circuits) where d.c. supply is needed. When such a d.c. supply is required, the mains a.c. supply is rectified by using crystal diodes. The following two rectifier circuits can be used :

(*i*) Half-wave rectifier (*ii*) Full-wave rectifier

6.8 Half-Wave Rectifier

In half-wave rectification, the rectifier conducts current only during the positive half-cycles of input a.c. supply. The negative half-cycles of a.c. supply are suppressed *i.e.* during negative half-cycles, no current is conducted and hence no voltage appears across the load. Therefore, current always flows in one direction (*i.e.* d.c.) through the load though after every half-cycle.



(*i*) (*ii*)

Fig. 6.20

Circuit details. Fig. 6.20 shows the circuit where a single crystal diode acts as a half-wave rectifier. The a.c. supply to be rectified is applied in series with the diode and load resistance R_L. Generally, a.c. supply is given through a transformer. The use of transformer permits two advantages. Firstly, it allows us to step up or step down the a.c. input voltage as the situation demands. Secondly, the transformer isolates the rectifier circuit from power line and thus reduces the risk of electric shock.

Operation. The a.c. voltage across the secondary winding AB changes polarities after every half-cycle. During the positive half-cycle of input a.c. voltage, end A becomes positive *w.r.t.* end B. This makes the diode forward biased and hence it conducts current. During the negative half-cycle, end A is negative *w.r.t.* end B. Under this condition, the diode is reverse biased and it conducts no current. Therefore, current flows through the diode during positive half-cycles of input a.c. voltage only ; it is blocked during the negative half-cycles [See Fig. 6.20 (*ii*)]. In this way, current flows through load R_L always in the same direction. Hence d.c. output is obtained across R_L. It may be noted that output across the load is pulsating d.c. These pulsations in the output are further smoothened with the help of *filter circuits* discussed later.

Disadvantages : The main disadvantages of a half-wave rectifier are :

(*i*) The pulsating current in the load contains alternating component whose basic frequency is equal to the supply frequency. Therefore, an elaborate filtering is required to produce steady direct current.

(*ii*) The a.c. supply delivers power only half the time. Therefore, the output is low.

6.9 Output Frequency of Half-Wave Rectifier

The output frequency of a half-wave rectifier is equal to the input frequency (50 Hz). Recall how a complete cycle is defined. A waveform has a complete cycle when it repeats the same wave pattern over a given time. Thus in Fig. 6.21 (*i*), the a.c. input voltage repeats the same wave pattern over 0° – 360°, 360° – 720° and so on. In Fig. 6.21 (*ii*), the output waveform also repeats the same wave pattern over 0° – 360°, 360° – 720° and so on. This means that when input a.c. completes one cycle, the output half-wave rectified wave also completes one cycle. In other words, the output frequency is equal to the input frequency *i.e.*

$$f_{out} = f_{in}$$

For example, if the input frequency of sine wave applied to a half-wave rectifier is 100 Hz, then frequency of the output wave will also be 100 Hz.

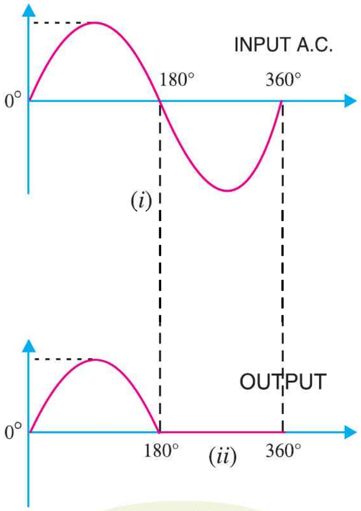


Fig. 6.21

6.10 Efficiency of Half-Wave Rectifier

The ratio of d.c. power output to the applied input a.c. power is known as **rectifier efficiency** *i.e.*

$$\text{Rectifier efficiency, } \eta = \frac{\text{d.c. power output}}{\text{Input a.c. power}}$$

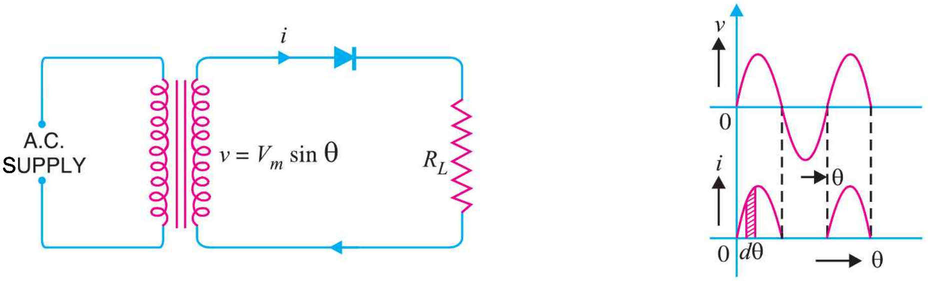


Fig. 6.22

Consider a half-wave rectifier shown in Fig. 6.22. Let $v = V_m \sin\theta$ be the alternating voltage that appears across the secondary winding. Let r_f and R_L be the diode resistance and load resistance respectively. The diode conducts during positive half-cycles of a.c. supply while no current conduction takes place during negative half-cycles.

d.c. power. The output current is pulsating direct current. Therefore, in order to find d.c. power, average current has to be found out.

$$*I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^\pi i\,d\theta = \frac{1}{2\pi}\int_0^\pi \frac{V_m \sin\theta}{r_f + R_L}\,d\theta$$

$$= \frac{V_m}{2\pi(r_f + R_L)}\int_0^\pi \sin\theta\,d\theta = \frac{V_m}{2\pi(r_f + R_L)}[-\cos\theta]_0^\pi$$

$$= \frac{V_m}{2\pi(r_f + R_L)} \times 2 = \frac{V_m}{(r_f + R_L)} \times \frac{1}{\pi}$$

$$= \frac{{}^{**}I_m}{\pi} \qquad \left[\because I_m = \frac{V_m}{(r_f + R_L)}\right]$$

$$\therefore \quad \text{d.c. power, } P_{dc} = I_{dc}^2 \times R_L = \left(\frac{I_m}{\pi}\right)^2 \times R_L \qquad ...(i)$$

a.c. power input : The a.c. power input is given by :

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For a half-wave rectified wave, $I_{rms} = I_m/2$

$$\therefore \quad P_{ac} = \left(\frac{I_m}{2}\right)^2 \times (r_f + R_L) \qquad ...(ii)$$

$$\therefore \quad \text{Rectifier efficiency} = \frac{\text{d.c. output power}}{\text{a.c. input power}} = \frac{(I_m/\pi)^2 \times R_L}{(I_m/2)^2\,(r_f + R_L)}$$

$$= \frac{0.406\,R_L}{r_f + R_L} = \frac{0.406}{1 + \frac{r_f}{R_L}}$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

$\therefore$ Max. rectifier efficiency = 40.6%

This shows that in half-wave rectification, a maximum of 40.6% of a.c. power is converted into d.c. power.

Example 6.12. *The applied input a.c. power to a half-wave rectifier is 100 watts. The d.c. output power obtained is 40 watts.*

(*i*) *What is the rectification efficiency ?*

(*ii*) *What happens to remaining 60 watts ?*

Solution.

$$(i) \quad \text{Rectification efficiency} = \frac{\text{d.c. output power}}{\text{a.c. input power}} = \frac{40}{100} = 0.4 = \mathbf{40\%}$$

(*ii*) 40% efficiency of rectification does not mean that 60% of power is lost in the rectifier circuit. In fact, a crystal diode consumes little power due to its small internal resistance. The 100 W

$$* \quad \text{Average value} = \frac{\text{Area under the curve over a cycle}}{\text{Base}} = \frac{\int_0^\pi i\,d\theta}{2\pi}$$

** It may be remembered that the *area of one-half cycle of a sinusoidal wave* is twice the peak value. Thus in this case, peak value is I_m and, therefore, area of one-half cycle is 2 I_m.

$$\therefore \quad I_{av} = I_{dc} = \frac{2\,I_m}{2\pi} = \frac{I_m}{\pi}$$

a.c. power is contained as 50 watts in positive half-cycles and 50 watts in negative half-cycles. The 50 watts in the negative half-cycles are not supplied at all. Only 50 watts in the positive half-cycles are converted into 40 watts.

$$\therefore \quad \text{Power efficiency} = \frac{40}{50} \times 100 = 80\%$$

Although 100 watts of a.c. power was supplied, the half-wave rectifier accepted only 50 watts and converted it into 40 watts d.c. power. Therefore, it is appropriate to say that efficiency of rectification is 40% and *not* 80% which is power efficiency.

Example 6.13. *An a.c. supply of 230 V is applied to a half-wave rectifier circuit through a transformer of turn ratio 10 : 1. Find* (*i*) *the output d.c. voltage and* (*ii*) *the peak inverse voltage. Assume the diode to be ideal.*

Solution.

Primary to secondary turns is

$$\frac{N_1}{N_2} = 10$$

R.M.S. primary voltage

= 230 V

∴ Max. primary voltage is

$$V_{pm} = (\sqrt{2}) \times \text{r.m.s. primary voltage}$$
$$= (\sqrt{2}) \times 230 = 325.3 \text{ V}$$

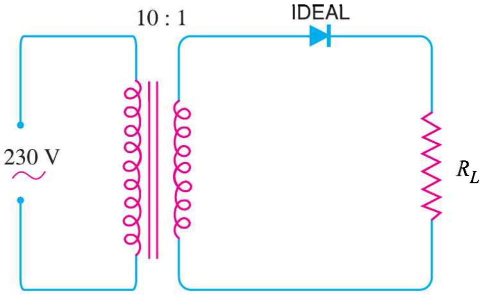


Fig. 6.23

Max. secondary voltage is

$$V_{sm} = V_{pm} \times \frac{N_2}{N_1} = 325.3 \times \frac{1}{10} = 32.53 \text{ V}$$

(*i*)
$$I_{d.c.} = \frac{I_m}{\pi}$$

$$\therefore \quad V_{dc} = \frac{I_m}{\pi} \times R_L = \frac{V_{sm}}{\pi} = \frac{32.53}{\pi} = \mathbf{10.36\ V}$$

(***ii***) During the negative half-cycle of a.c. supply, the diode is reverse biased and hence conducts no current. Therefore, the maximum secondary voltage appears across the diode.

∴ Peak inverse voltage = **32.53 V**

Example 6.14. *A crystal diode having internal resistance $r_f = 20\Omega$ is used for half-wave rectification. If the applied voltage $v = 50 \sin \omega t$ and load resistance $R_L = 800\ \Omega$, find :*

(*i*) I_m, I_{dc}, I_{rms} (*ii*) *a.c. power input and d.c. power output*

(*iii*) *d.c. output voltage* (*iv*) *efficiency of rectification.*

Solution.

$$v = 50 \sin \omega t$$

$$\therefore \quad \text{Maximum voltage, } V_m = 50 \text{ V}$$

(*i*)
$$I_m = \frac{V_m}{r_f + R_L} = \frac{50}{20 + 800} = 0.061 \text{ A} = \mathbf{61\ mA}$$

$$I_{dc} = I_m/\pi = 61/\pi = \mathbf{19.4\ mA}$$

$$I_{rms} = I_m/2 = 61/2 = \mathbf{30.5\ mA}$$

(***ii***)
$$\text{a.c. power input} = (I_{rms})^2 \times (r_f + R_L) = \left(\frac{30.5}{1000}\right)^2 \times (20 + 800) = \mathbf{0.763\ watt}$$

$$\text{d.c. power output} = I_{dc}^2 \times R_L = \left(\frac{19.4}{1000}\right)^2 \times 800 = \mathbf{0.301\ watt}$$

(*iii*) $$\text{d.c. output voltage} = I_{dc} R_L = 19.4 \text{ mA} \times 800\ \Omega = \mathbf{15.52\ volts}$$

(*iv*) $$\text{Efficiency of rectification} = \frac{0.301}{0.763} \times 100 = \mathbf{39.5\%}$$

Example 6.15. *A half-wave rectifier is used to supply 50V d.c. to a resistive load of 800 Ω. The diode has a resistance of 25 Ω. Calculate a.c. voltage required.*

Solution.

Output d.c. voltage, $V_{dc} = 50$ V

Diode resistance, $r_f = 25\ \Omega$

Load resistance, $R_L = 800\ \Omega$

Let V_m be the maximum value of a.c. voltage required.

$$\therefore \qquad V_{dc} = I_{dc} \times R_L$$

$$= \frac{I_m}{\pi} \times R_L = \frac{V_m}{\pi(r_f + R_L)} \times R_L \qquad \left[\because I_m = \frac{V_m}{r_f + R_L}\right]$$

$$\text{or} \qquad 50 = \frac{V_m}{\pi(25 + 800)} \times 800$$

$$\therefore \qquad V_m = \frac{\pi \times 825 \times 50}{800} = \mathbf{162\ V}$$

Hence a.c. voltage of maximum value 162 V is required.

6.11 Full-Wave Rectifier

In full-wave rectification, current flows through the load in the same direction for both half-cycles of input a.c. voltage. This can be achieved with two diodes working alternately. For the positive half-cycle of input voltage, one diode supplies current to the load and for the negative half-cycle, the other diode does so ; current being always in the same direction through the load. Therefore, a full-wave rectifier utilises both half-cycles of input a.c. voltage to produce the d.c. output. The following two circuits are commonly used for full-wave rectification :

(*i*) Centre-tap full-wave rectifier (*ii*) Full-wave bridge rectifier

6.12 Centre-Tap Full-Wave Rectifier

The circuit employs two diodes D_1 and D_2 as shown in Fig. 6.24. A centre tapped secondary winding *AB* is used with two diodes connected so that each uses one half-cycle of input a.c. voltage. In other words, diode D_1 utilises the a.c. voltage appearing across the upper half (*OA*) of secondary winding for rectification while diode D_2 uses the lower half winding *OB*.

Operation. During the positive half-cycle of secondary voltage, the end *A* of the secondary winding becomes positive and end *B* negative. This makes the diode D_1 forward biased and diode D_2 reverse biased. Therefore, diode D_1 conducts while diode D_2 does not. The conventional current flow is through diode D_1, load resistor R_L and the upper half of secondary winding as shown by the dotted arrows. During the negative half-cycle, end *A* of the secondary winding becomes negative and end *B* positive. Therefore, diode D_2 conducts while diode D_1 does not. The conventional current flow is through diode D_2, load R_L and lower half winding as shown by solid arrows. Referring to Fig. 6.24, it may be seen that current in the load R_L is *in the same direction* for both half-cycles of input a.c. voltage. Therefore, d.c. is obtained across the load R_L. Also, the polarities of the d.c. output across the load should be noted.

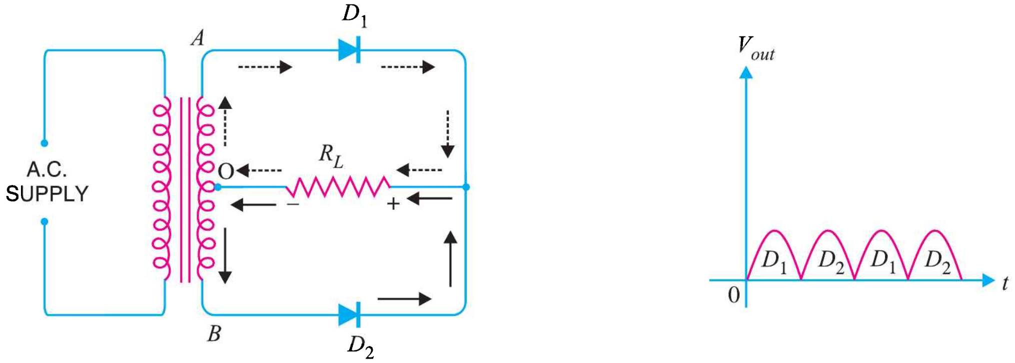

D_1
A
A.C.
SUPPLY
O
R_L
–
+
B
D_2
V_{out}
D_1
D_2
D_1
D_2
0
t

Fig. 6.24

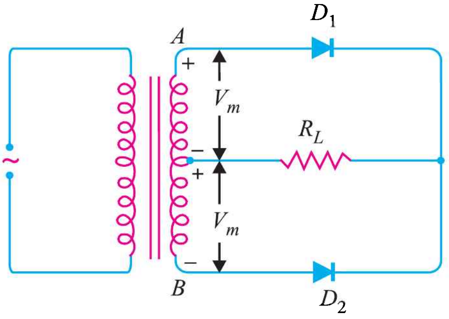

D_1
A
+
V_m
–
+
V_m
–
R_L
B
D_2

Fig. 6.25

Peak inverse voltage. Suppose V_m is the maximum voltage across the half secondary winding. Fig. 6.25 shows the circuit at the instant secondary voltage reaches its maximum value in the positive direction. At this instant, diode D_1 is conducting while diode D_2 is non-conducting. Therefore, whole of the secondary voltage appears across the non-conducting diode. Consequently, the peak inverse voltage is twice the maximum voltage across the half-secondary winding *i.e.*

$$\text{PIV} = 2\,V_m$$

Disadvantages

(*i*) It is difficult to locate the centre tap on the secondary winding.

(*ii*) The d.c. output is small as each diode utilises only one-half of the transformer secondary voltage.

(*iii*) The diodes used must have high peak inverse voltage.

6.13 Full-Wave Bridge Rectifier

The need for a centre tapped power transformer is eliminated in the bridge rectifier. It contains four diodes D_1, D_2, D_3 and D_4 connected to form bridge as shown in Fig. 6.26. The a.c. supply to be rectified is applied to the diagonally opposite ends of the bridge through the transformer. Between other two ends of the bridge, the load resistance R_L is connected.

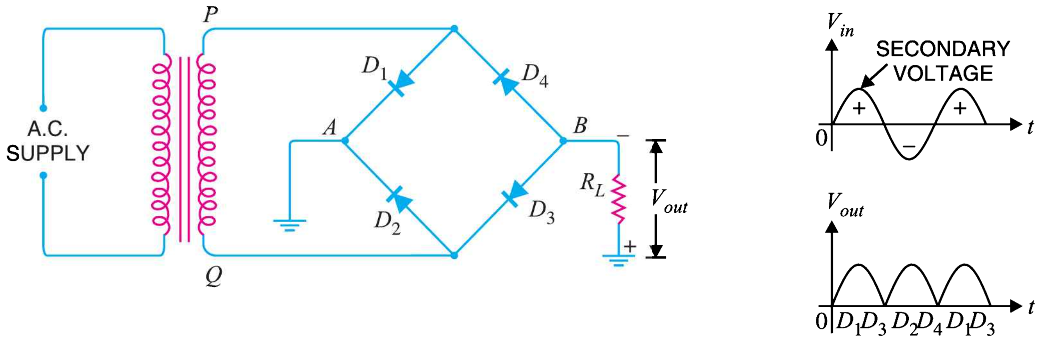

P
A.C.
SUPPLY
Q
D_1
D_4
A
B
D_2
D_3
–
R_L
+
V_{out}
V_{in}
SECONDARY
VOLTAGE
+
–
+
0
t
V_{out}
0
D_1D_3
D_2D_4
D_1D_3
t

Fig. 6.26

Operation. During the positive half-cycle of secondary voltage, the end *P* of the secondary winding becomes positive and end *Q* negative. This makes diodes D_1 and D_3 forward biased while diodes D_2 and D_4 are reverse biased. Therefore, only diodes D_1 and D_3 conduct. These two diodes will be in series through the load R_L as shown in Fig. 6.27 (*i*). The conventional current flow is shown by dotted arrows. It may be seen that current flows from *A* to *B* through the load R_L .

During the negative half-cycle of secondary voltage, end *P* becomes negative and end *Q* positive. This makes diodes D_2 and D_4 forward biased whereas diodes D_1 and D_3 are reverse biased. Therefore, only diodes D_2 and D_4 conduct. These two diodes will be in series through the load R_L as shown in Fig. 6.27 (*ii*). The current flow is shown by the solid arrows. It may be seen that again current flows from *A* to *B* through the load *i.e.* in the same direction as for the positive half-cycle. Therefore, d.c. output is obtained across load R_L.

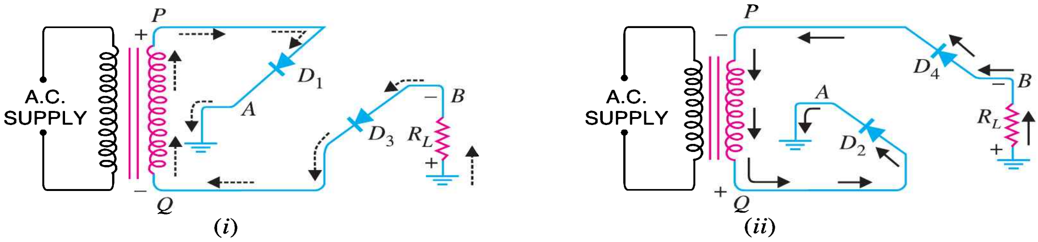


Fig. 6.27

Peak inverse voltage. The peak inverse voltage (PIV) of each diode is equal to the maximum secondary voltage of transformer. Suppose during positive half cycle of input a.c., end *P* of secondary is positive and end *Q* negative. Under such conditions, diodes D_1 and D_3 are forward biased while diodes D_2 and D_4 are reverse biased. Since the diodes are considered ideal, diodes D_1 and D_3 can be replaced by wires as shown in Fig. 6.28 (*i*). This circuit is the same as shown in Fig. 6.28 (*ii*).

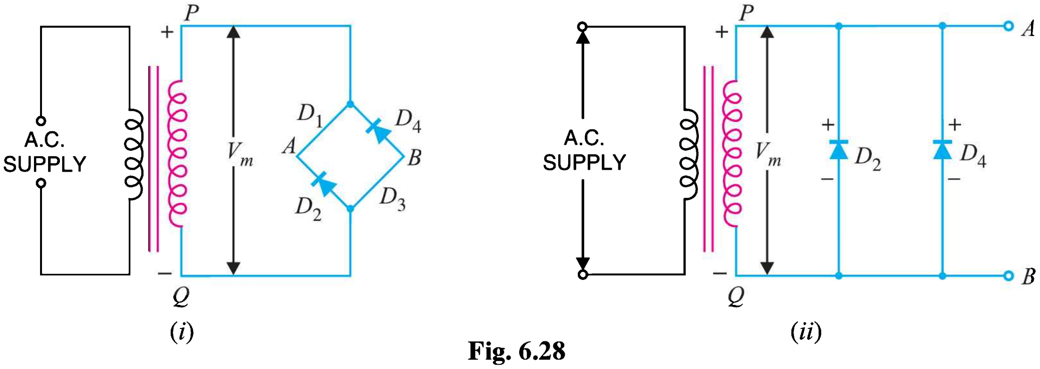


Fig. 6.28

Referring to Fig. 6.28 (*ii*), it is clear that two reverse biased diodes (*i.e.*, D_2 and D_4) and the secondary of transformer are in parallel. Hence PIV of each diode (D_2 and D_4) is equal to the maximum voltage (V_m) across the secondary. Similarly, during the next half cycle, D_2 and D_4 are forward biased while D_1 and D_3 will be reverse biased. It is easy to see that reverse voltage across D_1 and D_3 is equal to V_m.

Advantages

(*i*) The need for centre-tapped transformer is eliminated.

(*ii*) The output is twice that of the centre-tap circuit for the same secondary voltage.

(*iii*) The PIV is one-half that of the centre-tap circuit (for same d.c. output).

Disadvantages

(*i*) It requires four diodes.

(*ii*) As during each half-cycle of a.c. input two diodes that conduct are in series, therefore, voltage drop in the internal resistance of the rectifying unit will be twice as great as in the centre tap circuit. This is objectionable when secondary voltage is small.

6.14 Output Frequency of Full-Wave Rectifier

The output frequency of a full-wave rectifier is double the input frequency. Remember that a wave has a complete cycle when it repeats the same pattern. In Fig. 6.29 (*i*), the input a.c. completes one cycle from 0° – 360°. However, the full-wave rectified wave completes 2 cycles in this period [See Fig. 6.29 (*ii*)]. Therefore, output frequency is twice the input frequency *i.e.*

$$f_{out} = 2 f_{in}$$

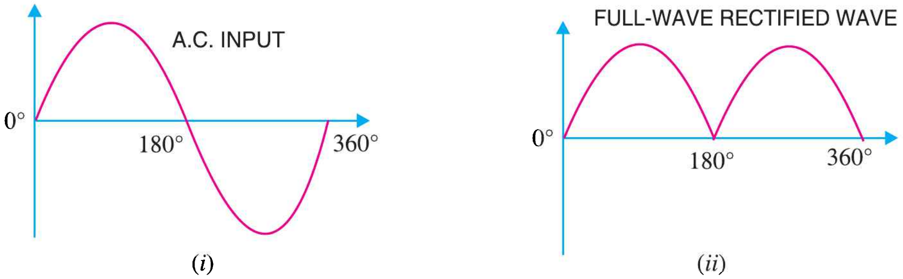


Fig. 6.29

For example, if the input frequency to a full-wave rectifier is 100 Hz, then the output frequency will be 200 Hz.

6.15 Efficiency of Full-Wave Rectifier

Fig. 6.30 shows the process of full-wave rectification. Let $v = V_m \sin \theta$ be the a.c. voltage to be rectified. Let r_f and R_L be the diode resistance and load resistance respectively. Obviously, the rectifier will conduct current through the load in the same direction for both half-cycles of input a.c. voltage. The instantaneous current i is given by :

$$i = \frac{v}{r_f + R_L} = \frac{V_m \sin \theta}{r_f + R_L}$$

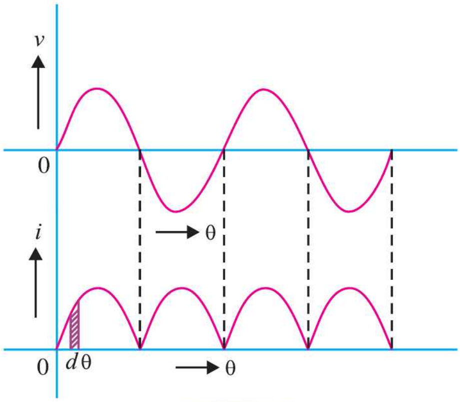


Fig. 6.30

d.c. output power. The output current is pulsating direct current. Therefore, in order to find the d.c. power, average current has to be found out. From the elementary knowledge of electrical engineering,

$$I_{dc} = \frac{2I_m}{\pi}$$

$$\therefore \quad \text{d.c. power output, } P_{dc} = I_{dc}^2 \times R_L = \left(\frac{2I_m}{\pi}\right)^2 \times R_L \qquad ...(i)$$

a.c. input power. The a.c. input power is given by :

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For a full-wave rectified wave, we have,

$$I_{rms} = I_m / \sqrt{2}$$

$$\therefore \quad P_{ac} = \left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L) \qquad ...(ii)$$

∴ Full-wave rectification efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)}$$

$$= \frac{8}{\pi^2} \times \frac{R_L}{(r_f + R_L)} = \frac{0.812\, R_L}{r_f + R_L} = \frac{0.812}{1 + \frac{r_f}{R_L}}$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

∴ Maximum efficiency = 81.2%

This is double the efficiency due to half-wave rectifier. Therefore, a full-wave rectifier is twice as effective as a half-wave rectifier.

Example 6.16. *A full-wave rectifier uses two diodes, the internal resistance of each diode may be assumed constant at 20 Ω. The transformer r.m.s. secondary voltage from centre tap to each end of secondary is 50 V and load resistance is 980 Ω. Find :*

(*i*) *the mean load current* (*ii*) *the r.m.s. value of load current*

Solution.

$$r_f = 20\ \Omega, \quad R_L = 980\ \Omega$$

$$\text{Max. a.c. voltage, } V_m = 50 \times \sqrt{2} = 70.7\ \text{V}$$

$$\text{Max. load current, } I_m = \frac{V_m}{r_f + R_L} = \frac{70.7\ \text{V}}{(20 + 980)\ \Omega} = 70.7\ \text{mA}$$

(*i*) $$\text{Mean load current, } I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 70.7}{\pi} = \mathbf{45\ mA}$$

(*ii*) R.M.S. value of load current is

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{70.7}{\sqrt{2}} = \mathbf{50\ mA}$$

Example 6.17. *In the centre-tap circuit shown in Fig. 6.31, the diodes are assumed to be ideal i.e. having zero internal resistance. Find* :

(*i*) *d.c. output voltage*(*ii*) *peak inverse voltage* (*iii*) *rectification efficiency.*

Solution.

Primary to secondary turns, $N_1/N_2 = 5$

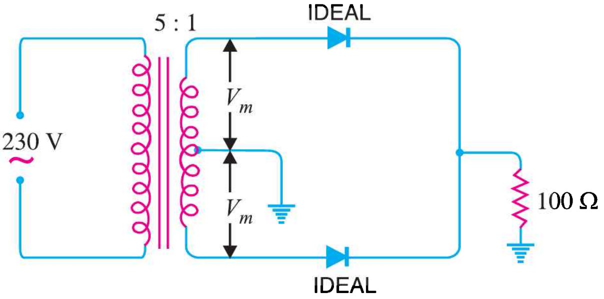


Fig. 6.31

R.M.S. primary voltage = 230 V

∴ R.M.S. secondary voltage

$$= 230 \times (1/5) = 46 \text{ V}$$

Maximum voltage across secondary

$$= 46 \times \sqrt{2} = 65\text{V}$$

Maximum voltage across half secondary winding is

$$V_m = 65/2 = 32.5 \text{ V}$$

(*i*) Average current, I_{dc} = $\dfrac{2V_m}{\pi R_L} = \dfrac{2 \times 32.5}{\pi \times 100} = 0.207 \text{ A}$

∴ d.c. output voltage, $V_{dc} = I_{dc} \times R_L = 0.207 \times 100 = \mathbf{20.7\ V}$

(*ii*) The peak inverse voltage is equal to the maximum secondary voltage, *i.e.*

$$PIV = \mathbf{65\ V}$$

(*iii*) Rectification efficiency $= \dfrac{0.812}{1 + \dfrac{r_f}{R_L}}$

Since $r_f = 0$

∴ Rectification efficiency = **81.2 %**

Example 6.18. *In the bridge type circuit shown in Fig. 6.32, the diodes are assumed to be ideal. Find :* (*i*) *d.c. output voltage* (*ii*) *peak inverse voltage* (*iii*) *output frequency.*
Assume primary to secondary turns to be 4.

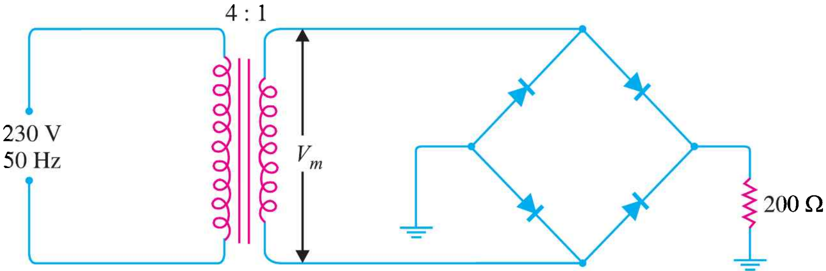


Fig. 6.32

Solution.

Primary/secondary turns, $N_1/N_2 = 4$

R.M.S. primary voltage = 230 V

∴ R.M.S. secondary voltage $= 230\ (N_2/N_1) = 230 \times (1/4) = 57.5 \text{ V}$

Maximum voltage across secondary is

$$V_m = 57.5 \times \sqrt{2} = 81.3 \text{ V}$$

(*i*) Average current, $I_{dc} = \dfrac{2V_m}{\pi R_L} = \dfrac{2 \times 81.3}{\pi \times 200} = 0.26 \text{ A}$

∴ d.c. output voltage, $V_{dc} = I_{dc} \times R_L = 0.26 \times 200 = \mathbf{52\ V}$

(*ii*) The peak inverse voltage is equal to the maximum secondary voltage *i.e.*

$$PIV = \mathbf{81.3\ V}$$

(*iii*) In full-wave rectification, there are two output pulses for each complete cycle of the input a.c. voltage. Therefore, the output frequency is twice that of the a.c. supply frequency *i.e.*

$$f_{out} = 2 \times f_{in} = 2 \times 50 = \mathbf{100\ Hz}$$

Example 6.19. *Fig. 6.33 (i) and Fig. 6.33 (ii) show the centre-tap and bridge type circuits having the same load resistance and transformer turn ratio. The primary of each is connected to 230V, 50 Hz supply.*

(*i*) *Find the d.c. voltage in each case.*

(*ii*) *PIV for each case for the same d.c. output. Assume the diodes to be ideal.*

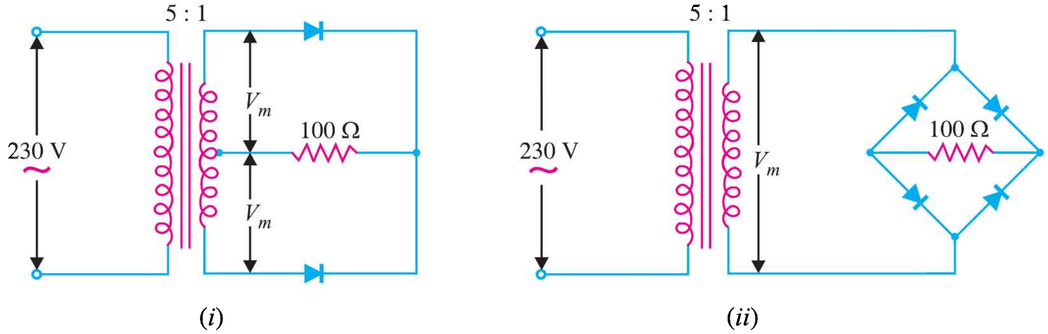


Fig. 6.33

Solution.

(*i*) D.C. output voltage

Centre-tap circuit

$$\text{R.M.S. secondary voltage} = 230 \times 1/5 = 46\text{ V}$$

$$\text{Max. voltage across secondary} = 46 \times \sqrt{2} = 65\text{ V}$$

Max. voltage appearing across half secondary winding is

$$V_m = 65/2 = 32.5\text{ V}$$

$$\text{Average current, } I_{dc} = \frac{2V_m}{\pi R_L}$$

$$\text{D.C. output voltage, } V_{dc} = I_{dc} \times R_L = \frac{2V_m}{\pi R_L} \times R_L$$

$$= \frac{2V_m}{\pi} = \frac{2 \times 32.5}{\pi} = \mathbf{20.7\ V}$$

Bridge Circuit

$$\text{Max. voltage across secondary, } V_m = 65\text{ V}$$

$$\text{D.C. output voltage, } V_{dc} = I_{dc} R_L = \frac{2V_m}{\pi R_L} \times R_L = \frac{2\,V_m}{\pi} = \frac{2 \times 65}{\pi} = \mathbf{41.4\ V}$$

This shows that for the same secondary voltage, the d.c. output voltage of bridge circuit is twice that of the centre-tap circuit.

(*ii*) PIV for same d.c. output voltage

The d.c. output voltage of the two circuits will be the same if V_m (*i.e.* max. voltage utilised by each circuit for conversion into d.c.) is the same. For this to happen, the turn ratio of the transformers should be as shown in Fig. 6.34.

Centre-tap circuit

$$\text{R.M.S. secondary voltage} = 230 \times 1/5 = 46 \text{ V}$$

$$\text{Max. voltage across secondary} = 46 \times \sqrt{2} = 65 \text{ V}$$

Max. voltage across half secondary winding is

$$V_m = 65/2 = 32.5 \text{ V}$$

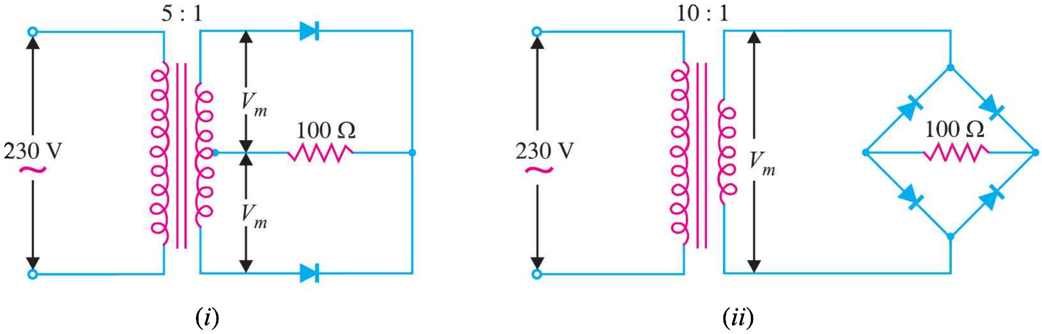


Fig. 6.34

$$\therefore \quad PIV = 2\,V_m = 2 \times 32.5 = \mathbf{65\ V}$$

Bridge type circuit

$$\text{R.M.S. secondary voltage} = 230 \times 1/10 = 23 \text{ V}$$

$$\text{Max. voltage across secondary, } V_m = 23 \times \sqrt{2} = 32.5 \text{ V}$$

$$\therefore \quad PIV = V_m = \mathbf{32.5\ V}$$

This shows that for the same d.c. output voltage, *PIV* of bridge circuit is half that of centre-tap circuit. This is a distinct advantage of bridge circuit.

Example 6.20. *The four diodes used in a bridge rectifier circuit have forward resistances which may be considered constant at 1Ω and infinite reverse resistance. The alternating supply voltage is 240 V r.m.s. and load resistance is 480 Ω. Calculate (i) mean load current and (ii) power dissipated in each diode.*

Solution.

$$\text{Max. a.c. voltage, } V_m = 240 \times \sqrt{2} \text{ V}$$

(*i*) At any instant in the bridge rectifier, two diodes in series are conducting. Therefore, total circuit resistance = 2 $r_f + R_L$.

$$\text{Max. load current, } I_m = \frac{V_m}{2\,r_f + R_L} = \frac{240 \times \sqrt{2}}{2 \times 1 + 480} = 0.7 \text{ A}$$

$$\therefore \quad \text{Mean load current, } I_{dc} = \frac{2\,I_m}{\pi} = \frac{2 \times 0.7}{\pi} = \mathbf{0.45\ A}$$

(*ii*) Since each diode conducts only half a cycle, diode r.m.s. current is :

$$I_{r.m.s.} = I_m/2 = 0.7/2 = 0.35 \text{ A}$$

$$\text{Power dissipated in each diode} = I^2_{r.m.s.} \times r_f = (0.35)^2 \times 1 = \mathbf{0.123\ W}$$

Example 6.21. *The bridge rectifier shown in Fig. 6.35 uses silicon diodes. Find (i) d.c. output* *voltage (ii) d.c. output current. Use simplified model for the diodes.*

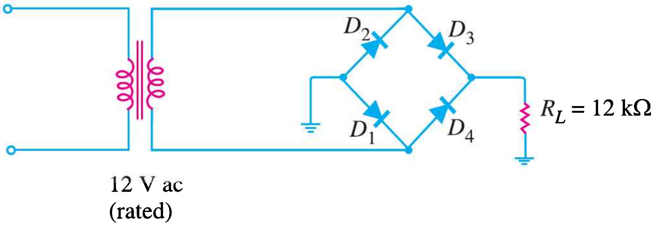


Fig. 6.35

Solution. The conditions of the problem suggest that the a.c voltage across transformer secondary is 12V r.m.s.

∴ Peak secondary voltage is

$$V_{s\,(pk)} = 12 \times \sqrt{2} = 16.97 \text{ V}$$

(*i*) At any instant in the bridge rectifier, two diodes in series are conducting.

∴ Peak output voltage is

$$V_{out\,(pk)} = 16.97 - 2\,(0.7) = 15.57 \text{ V}$$

∴ Average (or d.c.) output voltage is

$$V_{av} = V_{dc} = \frac{2\,V_{out\,(pk)}}{\pi} = \frac{2 \times 15.57}{\pi} = \mathbf{9.91V}$$

(*ii*) Average (or d.c.) output current is

$$I_{av} = \frac{V_{av}}{R_L} = \frac{9.91\text{V}}{12 \text{ k}\Omega} = \mathbf{825.8\ \mu A}$$

6.16 Faults in Centre-Tap Full-Wave Rectifier

The faults in a centre-tap full-wave rectifier may occur in the transformer or rectifier diodes. Fig. 6.36 shows the circuit of a centre-tap full-wave rectifier. A fuse is connected in the primary of the transformer for protection purposes.

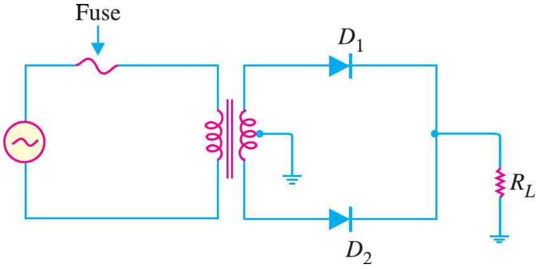


Fig. 6.36

We can divide the rectifier faults into two classes viz.

1. Faults in transformer **2.** Faults in rectifier diodes

1. Faults in Transformer. The transformer in a rectifier circuit can develop the following faults :

(*i*) A shorted primary or secondary winding.

(*ii*) An open primary or secondary winding.

(*iii*) A short between the primary or secondary winding and the transformer frame.

(*i*) In most cases, a **shorted primary** or **shorted secondary** will cause the fuse in the primary to blow. If the fuse does not blow, the d.c. output from the rectifier will be extremely low and the transformer itself will be very hot.

(*ii*) When the **primary** or **secondary winding of the transformer opens**, the output from the rectifier will drop to zero. In this case, the primary fuse will not blow. If you believe that either transformer winding is open, a simple resistance check will verify your doubt. If either winding reads a very high resistance, the winding is open.

(*iii*) If **either winding shorts to the transformer casing**, the primary fuse will blow. This fault can be checked by measuring the resistances from the winding leads to the transformer casing. A low resistance measurement indicates that a winding-to-case short exists.

2. Faults in Rectifier Diodes. If a fault occurs in a rectifier diode, the circuit conditions will indicate the type of fault.

(*i*) If **one diode in the centre-tap full-wave rectifier is shorted**, the primary fuse will blow. The reason is simple. Suppose diode D_2 in Fig. 6.36 is shorted. Then diode D_2 will behave as a wire. When diode D_1 is forward biased, the transformer secondary will be shorted through D_1. This will cause excessive current to flow in the secondary (and hence in the primary), causing the primary fuse to blow.

(*ii*) If **one diode in the centre-tap full-wave rectifier opens**, the output from the rectifier will resemble the output from a half-wave rectifier. The remedy is to replace the diode.

Bridge Rectifier Faults. The transformer faults and their remedies for bridge rectifier circuits are the same as for centre-tap full-wave rectifier. Again symptoms for shorted and open diodes in the bridge rectifier are the same as those for the centre-tap circuit. In the case of bridge circuit, you simply have more diodes that need to be tested.

6.17 Nature of Rectifier Output

It has already been discussed that the output of a rectifier is pulsating d.c. as shown in Fig. 6.37. In fact, if such a waveform is carefully analysed, it will be found that it contains a d.c. component and an a.c. component. The a.c. component is responsible for the *pulsations in the wave. The reader may wonder how a pulsating d.c. voltage can have an a.c. component when the voltage never becomes negative. The answer is that any wave which varies in a regular manner has an a.c. component.

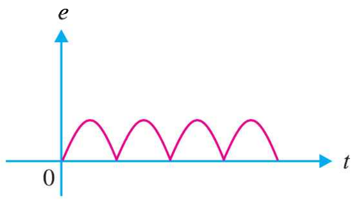
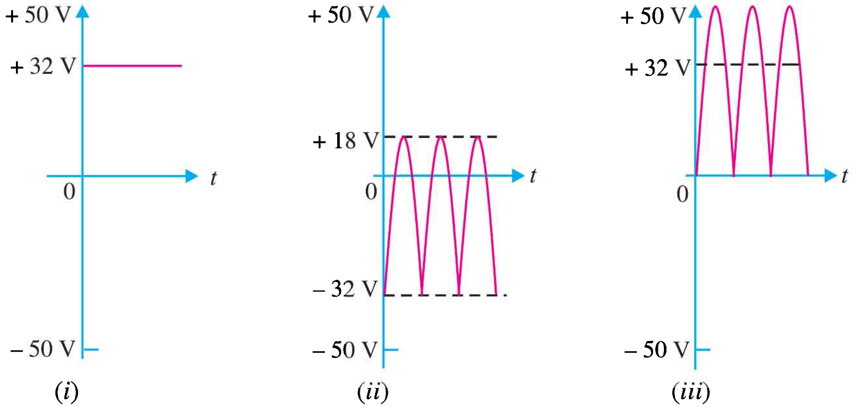


Fig. 6.37



(*i*) (*ii*) (*iii*)

Fig. 6.38

---

* Means changing output voltage.

Rectifier

The fact that a pulsating d.c. contains both d.c. and a.c. components can be beautifully illustrated by referring to Fig. 6.38. Fig. 6.38 (*i*) shows a pure d.c. component, whereas Fig. 6.38 (*ii*) shows the *a.c. component. If these two waves are added together, the resulting wave will be as shown in Fig. 6.38 (*iii*). It is clear that the wave shown in Fig. 6.38 (*iii*) never becomes negative, although it contains both a.c. and d.c. components. The striking resemblance between the rectifier output wave shown in Fig. 6.37 and the wave shown in Fig. 6.38 (*iii*) may be noted.

It follows, therefore, that a pulsating output of a rectifier contains a d.c. component and an a.c. component.

6.18 Ripple Factor

The output of a rectifier consists of a d.c. component and an a.c. component (also known as *ripple*). The a.c. component is undesirable and accounts for the pulsations in the rectifier output. The effectiveness of a rectifier depends upon the magnitude of a.c. component in the output ; the smaller this component, the more effective is the rectifier.

The ratio of r.m.s. value of a.c. component to the d.c. component in the rectifier output is known as **ripple factor** *i.e.*

$$\text{Ripple factor} = \frac{\text{r.m.s. value of a.c component}}{\text{value of d.c. component}} = \frac{I_{ac}}{I_{dc}}$$

Therefore, ripple factor is very important in deciding the effectiveness of a rectifier. The smaller the ripple factor, the lesser the effective a.c. component and hence more effective is the rectifier.

Mathematical analysis. The output current of a rectifier contains d.c. as well as a.c. component. The undesired a.c. component has a frequency of 100 Hz (*i.e.* double the supply frequency 50 Hz) and is called the *ripple* (See Fig. 6.39). It is a fluctuation superimposed on the d.c. component.

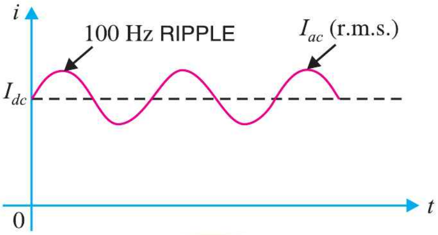


Fig. 6.39

By definition, the effective (*i.e.* r.m.s.) value of total load current is given by :

$$I_{rms} = \sqrt{I_{dc}^2 + I_{ac}^2}$$

or $$I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

Dividing throughout by I_{dc}, we get,

$$\frac{I_{ac}}{I_{dc}} = \frac{1}{I_{dc}}\sqrt{I_{rms}^2 - I_{dc}^2}$$

But I_{ac}/I_{dc} is the ripple factor.

$$\therefore \quad \text{Ripple factor} = \frac{1}{I_{dc}}\sqrt{I_{rms}^2 - I_{dc}^2} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

(*i*) **For half-wave rectification.** In half-wave rectification,

$$I_{rms} = I_m/2 \quad ; \quad I_{dc} = I_m/\pi$$

---

* Although the a.c. component is not a sine-wave, yet it is alternating one.

$$\therefore \qquad \text{Ripple factor} = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = 1.21$$

It is clear that a.c. component exceeds the d.c. component in the output of a half-wave rectifier. This results in greater pulsations in the output. Therefore, half-wave rectifier is ineffective for conversion of a.c. into d.c.

(*ii*) **For full-wave rectification.** In full-wave rectification,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad ; \quad I_{dc} = \frac{2\,I_m}{\pi}$$

$$\therefore \qquad \text{Ripple factor} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2\,I_m/\pi}\right)^2 - 1} = 0.48$$

$$i.e. \qquad \frac{\text{effective a.c. component}}{\text{d.c. component}} = 0.48$$

This shows that in the output of a full-wave rectifier, the d.c. component is more than the a.c. component. Consequently, the pulsations in the output will be less than in half-wave rectifier. For this reason, full-wave rectification is invariably used for conversion of a.c. into d.c.

Example 6.22. *A power supply A delivers 10 V dc with a ripple of 0.5 V r.m.s. while the power supply B delivers 25 V dc with a ripple of 1 mV r.m.s. Which is better power supply ?*

Solution. The lower the ripple factor of a power supply, the better it is.

For power supply A

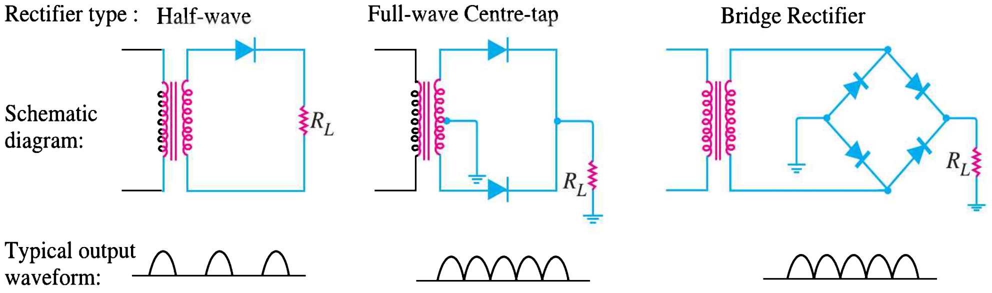
$$\text{Ripple factor} = \frac{V_{ac(r.m.s.)}}{V_{dc}} = \frac{0.5}{10} \times 100 = 5\%$$

For power supply B

$$\text{Ripple factor} = \frac{V_{ac(r.m.s.)}}{V_{dc}} = \frac{0.001}{25} \times 100 = 0.004\%$$

Clearly, power supply *B* is better.

6.19 Comparison of Rectifiers



S. No.	Particulars	Half-wave	Centre-tap	Bridge type
1	No. of diodes	1	2	4
2	Transformer necessary	no	yes	no
3	Max. efficiency	40.6%	81.2%	81.2%
4	Ripple factor	1.21	0.48	0.48
5	Output frequency	f_{in}	$2f_{in}$	$2f_{in}$
6	Peak inverse voltage	V_m	$2\,V_m$	V_m

A comparison among the three rectifier circuits must be made very judiciously. Although bridge circuit has some disadvantages, it is the best circuit from the viewpoint of overall performance. When cost of the transformer is the main consideration in a rectifier assembly, we invariably use the bridge circuit. This is particularly true for large rectifiers which have a low-voltage and a high-current rating.

6.20 Filter Circuits

Generally, a rectifier is required to produce pure d.c. supply for using at various places in the electronic circuits. However, the output of a rectifier has pulsating *character *i.e.* it contains a.c. and d.c. components. The a.c. component is undesirable and must be kept away from the load. To do so, a *filter circuit* is used which removes (or *filters out*) the a.c. component and allows only the d.c. component to reach the load.

A **filter circuit** *is a device which removes the a.c. component of rectifier output but allows the d.c. component to reach the load.*

Obviously, a filter circuit should be installed between the rectifier and the load as shown in Fig. 6.40. A filter circuit is generally a combination of inductors (L) and capacitors (C). The filtering action of L and C depends upon the basic electrical principles. A capacitor passes a.c. readily but does not **pass d.c. at all. On the other hand, an inductor †opposes a.c. but allows d.c. to pass through it. It then becomes clear that suitable network of L and C can effectively remove the a.c. component, allowing the d.c. component to reach the load.

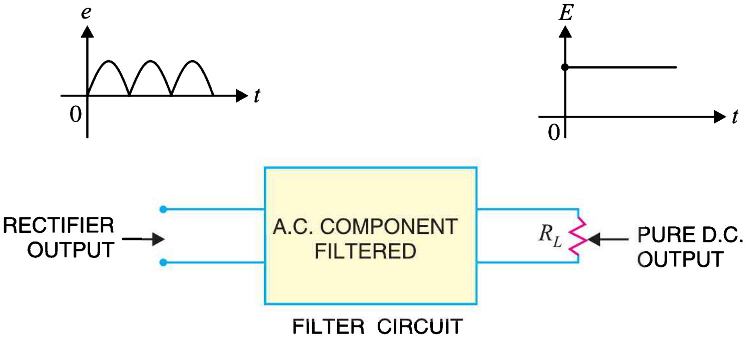


Fig. 6.40

6.21 Types of Filter Circuits

The most commonly used filter circuits are *capacitor filter*, *choke input filter* and *capacitor input filter or π-filter*. We shall discuss these filters in turn.

(*i*) **Capacitor filter.** Fig. 6.41 (*ii*) shows a typical capacitor filter circuit. It consists of a capacitor C placed across the rectifier output in parallel with load R_L. The pulsating direct voltage of the rectifier is applied across the capacitor. As the rectifier voltage increases, it charges the capacitor and also supplies current to the load. At the end of quarter cycle [Point A in Fig. 6.41 (*iii*)], the

---

* If such a d.c. is applied in an electronic circuit, it will produce a *hum.*

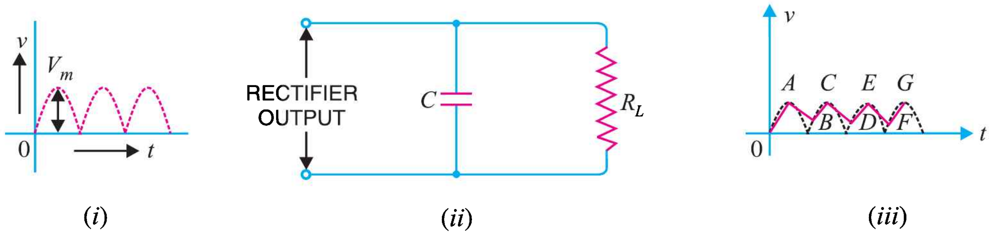
** A capacitor offers infinite reactance to d.c. For d.c., $f = 0$.

$$\therefore \quad X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 0 \times C} = \infty$$

Hence, a capacitor does not allow d.c. to pass through it.

† We know $X_L = 2\pi fL$. For d.c., $f = 0$ and, therefore, $X_L = 0$. Hence inductor passes d.c. quite readily. For a.c., it offers opposition and drops a part of it.

capacitor is charged to the peak value V_m of the rectifier voltage. Now, the rectifier voltage starts to decrease. As this occurs, the capacitor discharges through the load and voltage across it (*i.e.* across parallel combination of *R-C*) decreases as shown by the line *AB* in Fig. 6.41 (*iii*). The voltage across load will decrease only slightly because immediately the next voltage peak comes and recharges the capacitor. This process is repeated again and again and the output voltage waveform becomes *ABCDEFG*. It may be seen that very little ripple is left in the output. Moreover, output voltage is higher as it remains substantially near the peak value of rectifier output voltage.



(*i*) (*ii*) (*iii*)

Fig. 6.41

The capacitor filter circuit is extremely popular because of its low cost, small size, little weight and good characteristics. For small load currents (say upto 50 mA), this type of filter is preferred. It is commonly used in transistor radio battery eliminators.

(*ii*) **Choke input filter.** Fig. 6.42 shows a typical choke input filter circuit. It consists of a *choke *L* connected in series with the rectifier output and a filter capacitor *C* across the load. Only a single filter section is shown, but several identical sections are often used to reduce the pulsations as effectively as possible.

The pulsating output of the rectifier is applied across terminals 1 and 2 of the filter circuit. As discussed before, the pulsating output of rectifier contains a.c. and d.c. components. The choke offers high opposition to the passage of a.c. component but negligible opposition to the d.c. component. The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at terminal 3.

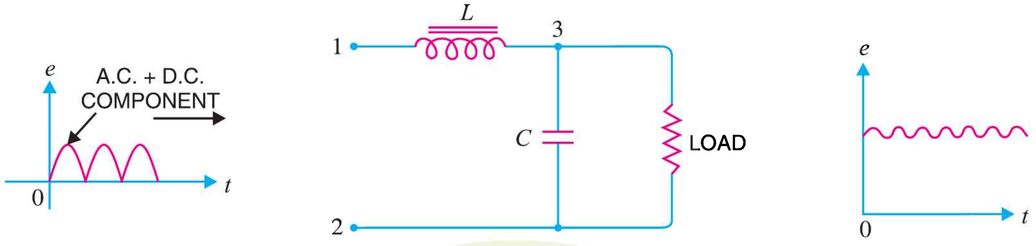


Fig. 6.42

At terminal 3, the rectifier output contains d.c. component and the remaining part of a.c. component which has managed to pass through the choke. Now, the low reactance of filter capacitor bypasses the a.c. component but prevents the d.c. component to flow through it. Therefore, only d.c. component reaches the load. In this way, the filter circuit has filtered out the a.c. component from the rectifier output, allowing d.c. component to reach the load.

(*iii*) **Capacitor input filter** *or* **π-filter.** Fig. 6.43 shows a typical capacitor input filter or **π-filter. It consists of a filter capacitor C_1 connected across the rectifier output, a choke *L* in series and another filter capacitor C_2 connected across the load. Only one filter section is shown but several identical sections are often used to improve the smoothing action.

---

* The shorthand name of inductor coil is choke.

** The shape of the circuit diagram of this filter circuit appears like Greek letter π (pi) and hence the name π-filter.

The pulsating output from the rectifier is applied across the input terminals (*i.e.* terminals 1 and 2) of the filter. The filtering action of the three components *viz* C_1, L and C_2 of this filter is described below :

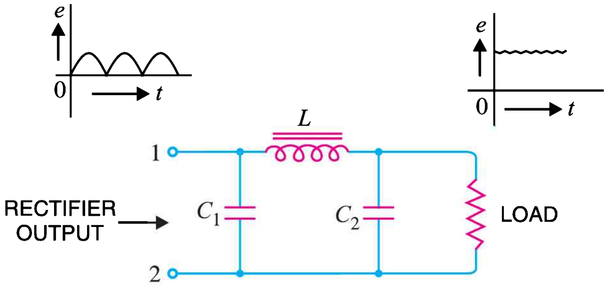


Fig. 6.43

(*a*) The *filter capacitor* C_1 offers low reactance to a.c. component of rectifier output while it offers infinite reactance to the d.c. component. Therefore, capacitor C_1 bypasses an appreciable amount of a.c. component while the d.c. component continues its journey to the choke L.

(*b*) The *choke* L offers high reactance to the a.c. component but it offers almost zero reactance to the d.c. component. Therefore, it allows the d.c. component to flow through it, while the *unbypassed a.c. component is blocked.

(*c*) The *filter capacitor* C_2 bypasses the a.c. component which the choke has failed to block. Therefore, only d.c. component appears across the load and that is what we desire.

Example 6.23. *For the circuit shown in Fig. 6.44, find the output d.c. voltage.*

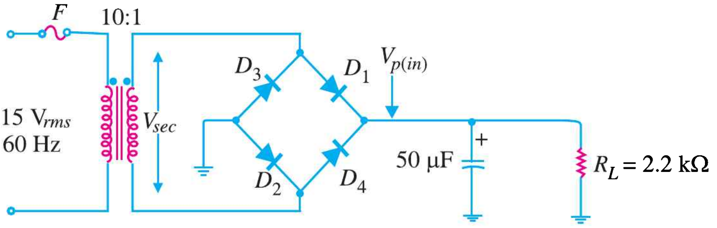


Fig. 6.44

Solution. It can be proved that output d.c. voltage is given by :

$$V_{dc} = V_{p(in)}\left(1 - \frac{1}{2f\,R_L C}\right)$$

Here $V_{p(in)}$ = Peak rectified full-wave voltage applied to the filter

f = Output frequency

Peak primary voltage, $V_{p(prim)} = \sqrt{2} \times 115 = 163\text{V}$

Peak secondary voltage, $V_{p(sec)} = \left(\frac{1}{10}\right) \times 163 = 16.3\text{V}$

Peak full-wave rectified voltage at the filter input is

$$V_{p\,(in)} = V_{p\,(sec)} - 2\times 0.7 = 16.3 - 1.4 = 14.9\text{V}$$

For full-wave rectification, $f = 2\ f_{in} = 2\times 60 = 120$ Hz

Now $$\frac{1}{2f\,R_L C} = \frac{1}{2\times 120\times(2.2\times 10^3)\times(50\times 10^{-6})} = 0.038$$

---

* That part of a.c. component which could not be bypassed by capacitor C_1.

$$\therefore \quad V_{dc} = V_{p(in)}\left(1 - \frac{1}{2f\ R_L C}\right) = 14.9\ (1 - 0.038) = \mathbf{14.3V}$$

Example 6.24. *The choke of Fig. 6.45 has a d.c. resistance of 25 Ω. What is the d.c. voltage if the full-wave signal into the choke has a peak value of 25.7 V ?*

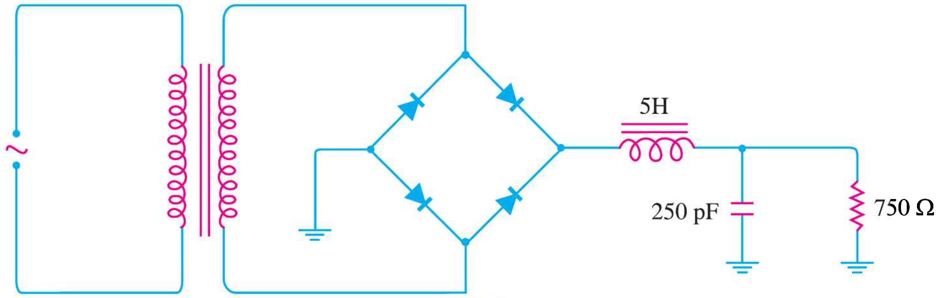


Fig. 6.45

Solution. The output of a full-wave rectifier has a d.c. component and an a.c. component. Due to the presence of a.c. component, the rectifier output has a pulsating character as shown in Fig. 6.46. The maximum value of the pulsating output is V_m and d.c. component is $V'_{dc} = 2\ V_m/\pi$.

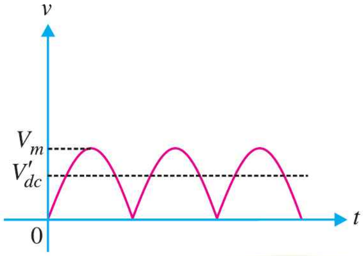


Fig. 6.46

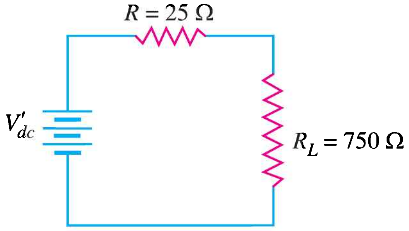


Fig. 6.47

For d.c. component V'_{dc}, the choke resistance is in series with the load as shown in Fig. 6.47.

$$\therefore \quad \text{Voltage across load, } V_{dc} = \frac{V'_{dc}}{R + R_L} \times R_L$$

$$\text{In our example, } V'_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 25.7}{\pi} = 16.4\ \text{V}$$

$$\therefore \quad \text{Voltage across load, } V_{dc} = \frac{V'_{dc}}{R + R_L} \times R_L = \frac{16.4}{25 + 750} \times 750 = \mathbf{15.9\ V}$$

The voltage across the load is 15.9 V dc *plus* a small ripple.

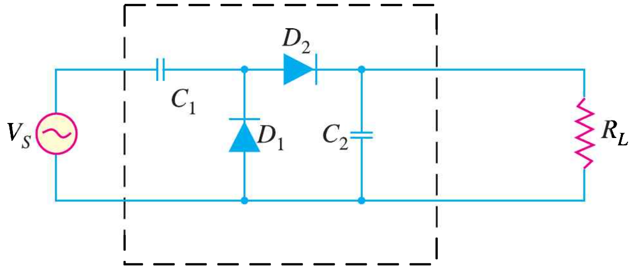
6.22 Voltage Multipliers

With a diode, we can build a rectifier to produce a d.c. voltage that is nearly equal to the peak value of input a.c. voltage. We can also use diodes and capacitors to build a circuit that will provide a *d.c output* that is multiple of the *peak input a.c. voltage*. Such a circuit is called a voltage multiplier. For example, a *voltage doubler* will provide a d.c. output that is *twice* the peak input a.c. voltage, a *voltage tripler* will provide a d.c. output that is three times the peak input a.c. voltage and so on.

While voltage multipliers provide d.c. output that is much greater than the peak input a.c. voltage, there is no power amplification and law of conservation of energy holds good. When a voltage multiplier *increases* the peak input voltage by a factor *n*, the peak input current is *decreased* by approximately the same factor. Thus the actual power output from a voltage multiplier will *never* be greater than the input power. In fact, there are losses in the circuit (e.g. in diodes, capacitors etc.) so that the output power will actually be *less than* the input power.

6.23 Half-Wave Voltage Doubler

A half-wave voltage doubler consists of two diodes and two capacitors connected in a manner as shown in Fig. 6.48. It will be shown that if the peak input a.c. voltage is $V_{S(pk)}$, the d.c. output voltage will be 2 $V_{S\,(pk)}$ provided the diodes are ideal (this assumption is fairly reasonable). The basic idea in a voltage multiplier is to charge each capacitor to the peak input a.c. voltage and to arrange the capacitors so that their stored voltages will add.

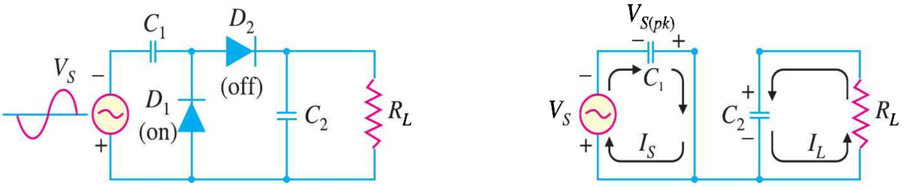


Half-wave voltage doubler

Fig. 6.48

Circuit action. We now discuss the working of a half-wave voltage doubler.

(*i*) During the negative half-cycle of a.c. input voltage [See Fig. 6.49 (*i*)], diode D_1 is forward biased and diode D_2 is reverse biased [See Fig. 6.49 (*i*)]. Therefore, diode D_1 can be represented by a *short* and diode D_2 as an *open*. The equivalent circuit then becomes as shown in Fig. 6.49 (*ii*).

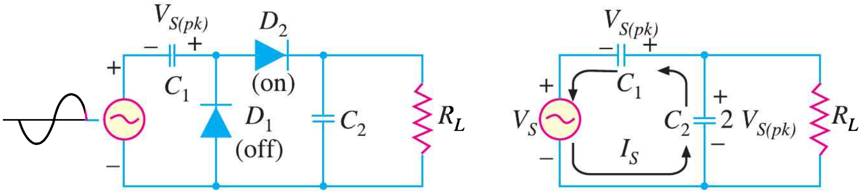


(*i*) (*ii*)

Fig. 6.49

As you can see [See Fig.6.49 (*ii*)], C_1 will charge until voltage across it becomes equal to peak value of source voltage [$V_{S\,(pk)}$]. At the same time, C_2 will be in the process of discharging through the load R_L (The source of this charge on C_2 will be explained in a moment). *Note that in all figures electron flow is shown.*

(*ii*) When the polarity of the input a.c. voltage reverses (*i.e.* during positive half-cycle), the circuit conditions become as shown in Fig. 6.50 (*i*). Now D_1 is reverse biased and D_2 is forward biased and the equivalent circuit becomes as shown in Fig. 6.50 (*ii*).



(*i*) (*ii*)

Fig. 6.50

Referring to Fig. 6.50 (*ii*), it is easy to see that C_1 (charged to $V_{S\,(pk)}$)and the source voltage (V_S) now act as *series-aiding* voltage sources. Thus C_2 will be charged to the sum of the series peak voltages *i.e.* 2 $V_{S(pk)}$.

(*iii*) When V_S returns to its original polarity (*i.e.* negative half-cycle), D_2 is again turned off (*i.e.* reverse biased). With D_2 turned off, the only discharge path for C_2 is through the load resistance R_L. The time constant (= $R_L\,C_2$) of this circuit is so adjusted that C_2 has little time to lose any of its charge before the input polarity reverses again. During the positive half-cycle, D_2 is turned on and C_2 recharges until voltage across it is again equal to 2 $V_{S\,(pk)}$.

$\therefore$ D.C. output voltage, $V_{dc} = 2\ V_{S\,(pk)}$

Since C_2 barely discharges between input cycles, the output waveform of the half-wave voltage doubler closely resembles that of a filtered half-wave rectifier. Fig. 6.51 shows the input and output waveforms for a half-wave voltage doubler.

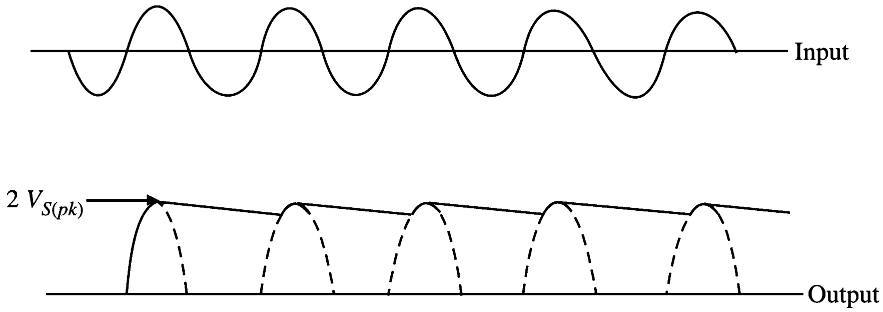


Fig. 6.51

The voltage multipliers have the disadvantage of poor voltage regulation. This means that d.c. output voltage drops considerably as the load current increases. Large filter capacitors are needed to help maintain the output voltage.

6.24 Voltage Stabilisation

A rectifier with an appropriate filter serves as a good source of d.c. output. However, the major disadvantage of such a power supply is that the output voltage changes with the variations in the input voltage or load. Thus, if the input voltage increases, the d.c. output voltage of the rectifier also increases. Similarly, if the load current increases, the output voltage falls due to the voltage drop in the rectifying element, filter chokes, transformer winding etc. In many electronic applications, it is desired that the output voltage should remain constant regardless of the variations in the input voltage or load. In order to ensure this, a voltage stabilising device, called voltage stabiliser is used. Several stabilising circuits have been designed but only *zener diode* as a voltage stabiliser will be discussed.

6.25 Zener Diode

It has already been discussed that when the reverse bias on a crystal diode is increased, a critical voltage, called *breakdown voltage* is reached where the reverse current increases sharply to a high value. The breakdown region is the knee of the reverse characteristic as shown in Fig. 6.52. The satisfactory explanation of this breakdown of the junction was first given by the American scientist *C.* Zener. Therefore, the breakdown voltage is sometimes called *zener voltage* and the sudden increase in current is known as zener current.

The breakdown or zener voltage depends upon the amount of doping. If the diode is heavily doped, depletion layer will be thin and consequently the breakdown of the junction will occur at a lower reverse voltage. On the other hand, a lightly doped diode has a higher breakdown voltage. When an ordinary crystal diode is properly doped so that it has a sharp breakdown voltage, it is called

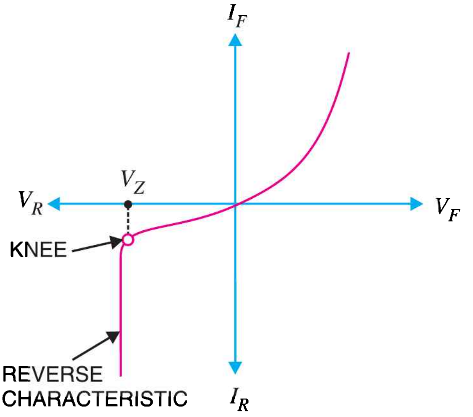


Fig. 6.52

a zener diode.

A properly doped crystal diode which has a sharp breakdown voltage is known as a **zener diode.**

Fig. 6.53 shows the symbol of a zener diode. It may be seen that it is just like an ordinary diode except that the bar is turned into *z*-shape. The following points may be noted about the zener diode:

(*i*) A zener diode is like an ordinary diode except that it is properly doped so as to have a sharp breakdown voltage.

(*ii*) A zener diode is always reverse connected *i.e.* it is always reverse biased.

(*iii*) A zener diode has sharp breakdown voltage, called zener voltage V_Z.

(*iv*) When forward biased, its characteristics are just those of ordinary diode.

(*v*) The zener diode is not immediately burnt just because it has entered the *breakdown region. As long as the external circuit connected to the diode limits the diode current to less than *burn out* value, the diode will not burn out.

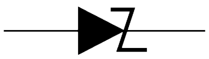
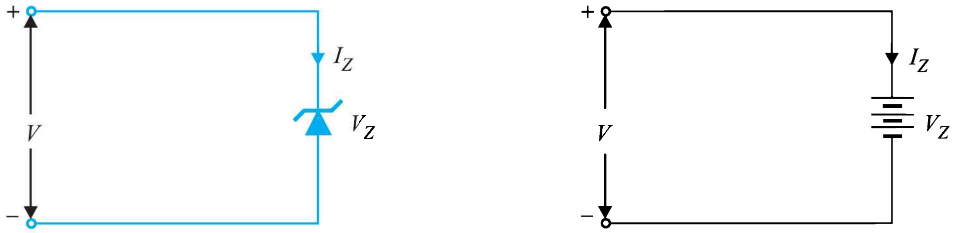


Fig. 6.53

6.26 Equivalent Circuit of Zener Diode

The analysis of circuits using zener diodes can be made quite easily by replacing the zener diode by its equivalent circuit.

(*i*) **"On" state.** When reverse voltage across a zener diode is equal to or more than break down voltage V_Z, the current increases very sharply. In this region, the curve is almost vertical. It means that voltage across zener diode is constant at V_Z even though the current through it changes. Therefore, in the breakdown region, an **ideal zener diode can be represented by a battery of voltage V_Z as shown in Fig. 6.54 (*ii*). Under such conditions, the zener diode is said to be in the "ON" state.



(*i*) $V \geq V_Z$

(*ii*) Equivalent circuit of zener for ''on'' state

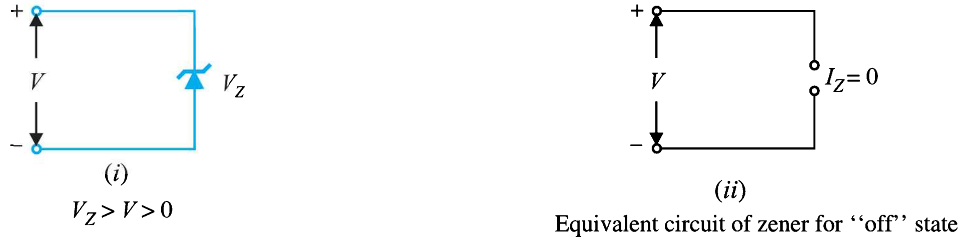
Fig. 6.54

(*ii*) **"OFF" state.** When the reverse voltage across the zener diode is less than V_Z but greater than 0 V, the zener diode is in the "OFF" state. Under such conditions, the zener diode can be represented by an open-circuit as shown in Fig. 6.55 (*ii*).

---

* The current is limited only by both external resistance and the power dissipation of zener diode.

** This assumption is fairly reasonable as the impedance of zener diode is quite small in the breakdown region.



(*i*)
$V_Z > V > 0$

(*ii*)
Equivalent circuit of zener for ''off'' state

Fig. 6.55

6.27 Zener Diode as Voltage Stabiliser

A zener diode can be used as a voltage regulator to provide a constant voltage from a source whose voltage may vary over sufficient range. The circuit arrangement is shown in Fig. 6.56 (*i*). The zener diode of zener voltage V_Z is reverse connected across the load R_L across which constant output is desired. The series resistance R absorbs the output voltage fluctuations so as to maintain constant voltage across the load. It may be noted that the zener will maintain a constant voltage V_Z (= E_0) across the load so long as the input voltage does not fall below V_Z.

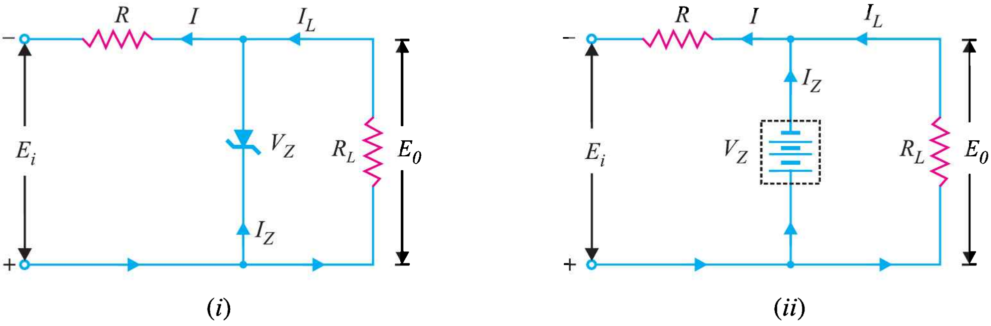


Fig. 6.56

When the circuit is properly designed, the load voltage E_0 remains essentially constant (equal to V_Z) even though the input voltage E_i and load resistance R_L may vary over a wide range.

(*i*) Suppose the input voltage increases. Since the zener is in the breakdown region, the zener diode is equivalent to a battery V_Z as shown in Fig. 6.56 (*ii*). It is clear that output voltage remains constant at V_Z (= E_0). The excess voltage is dropped across the series resistance R. This will cause an increase in the value of total current I. The zener will conduct the increase of current in I while the load current remains constant. Hence, output voltage E_0 remains constant irrespective of the changes in the input voltage E_i.

(*ii*) Now suppose that input voltage is constant but the load resistance R_L decreases. This will cause an increase in load current. The extra current cannot come from the source because drop in R (and hence source current I) will not change as the zener is within its regulating range. The additional load current will come from a decrease in zener current I_Z. Consequently, the output voltage stays at constant value.

$$\text{Voltage drop across } R = E_i - E_0$$
$$\text{Current through } R, I = I_Z + I_L$$

Applying Ohm's law, we have,

$$R = \frac{E_i - E_0}{I_Z + I_L}$$

6.28 Solving Zener Diode Circuits

The analysis of zener diode circuits is quite similar to that applied to the analysis of semiconductor diodes. The first step is to determine the state of zener diode *i.e.*, whether the zener is in the "on" state or "off" state. Next, the zener is replaced by its appropriate model. Finally, the unknown quantities are determined from the resulting circuit.

1. E_i and R_L fixed. This is the simplest case and is shown in Fig. 6.57 (*i*). Here the applied voltage E_i as well as load R_L is fixed. The first step is to find the state of zener diode. This can be determined by removing the zener from the circuit and calculating the voltage V across the resulting open-circuit as shown in Fig. 6.57 (*ii*).

$$V = E_0 = \frac{R_L E_i}{R + R_L}$$

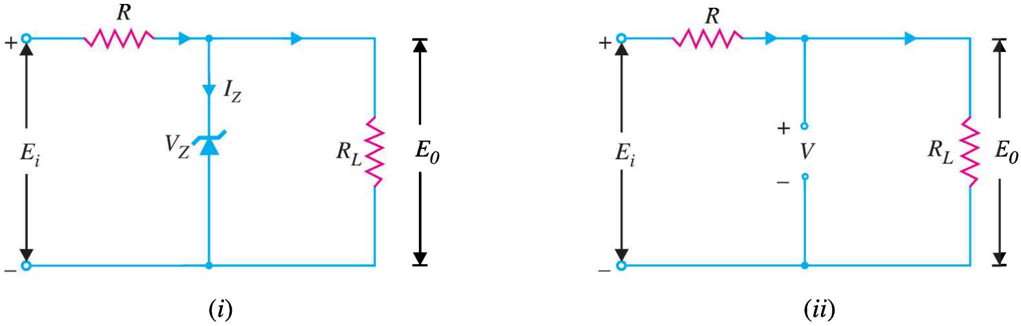


Fig. 6.57

If $V \geq V_Z$, the zener diode is in the "on" state and its equivalent model can be substituted as shown in Fig. 6.58 (*i*). If $V < V_Z$, the diode is in the "off" state as shown in Fig. 6.58 (*ii*).

(*i*) **On state.** Referring to circuit shown in Fig. 6.58 (*i*),

$$E_0 = V_Z$$

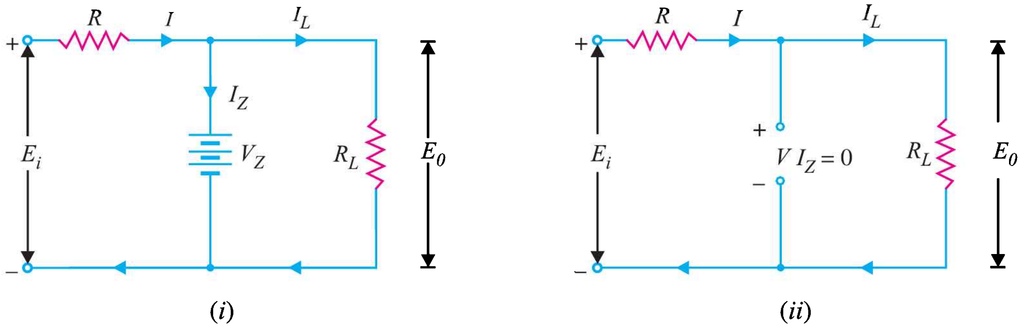


Fig. 6.58

$$I_Z = I - I_L \quad \text{where } I_L = \frac{E_0}{R_L} \text{ and } I = \frac{E_i - E_0}{R}$$

Power dissipated in zener, $P_Z = V_Z I_Z$

(*ii*) **Off state.** Referring to the circuit shown in Fig. 6.58 (*ii*),

$$I = I_L \quad \text{and} \quad I_Z = 0$$

$$V_R = E_i - E_0 \quad \text{and} \quad V = E_0 \quad (V < V_Z)$$

$$\therefore \quad P_Z = V I_Z = V(0) = 0$$

2. Fixed $\mathbf{E_i}$ and Variable $\mathbf{R_L}$. This case is shown in Fig. 6.59. Here the applied voltage (E_i) is fixed while load resistance R_L (and hence load current I_L) changes. Note that there is a definite range of R_L values (and hence I_L values) which will ensure the zener diode to be in "on" state. Let us calculate that range of values.

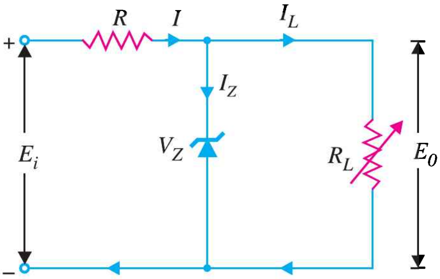


Fig. 6.59

(*i*) **$\mathbf{R_{Lmin}}$ and $\mathbf{I_{Lmax}}$.** Once the zener is in the "on" state, load voltage E_0 (= V_Z) is constant. As a result, when load resistance is minimum (*i.e.*, R_{Lmin}), load current will be maximum ($I_L = E_0/R_L$). In order to find the minimum load resistance that will turn the zener on, we simply calculate the value of R_L that will result in $E_0 = V_Z$ *i.e.*,

$$E_0 = V_Z = \frac{{}^*R_L E_i}{R + R_L}$$

$$\therefore \quad R_{Lmin} = \frac{R V_Z}{E_i - V_Z} \quad \ldots(i)$$

This is the minimum value of load resistance that will ensure that zener is in the "on" state. Any value of load resistance less than this value will result in a voltage E_0 across the load less than V_Z and the zener will be in the "off" state.

Clearly ; $$I_{Lmax} = \frac{E_0}{R_{Lmin}} = \frac{V_Z}{R_{Lmin}}$$

(*ii*) **$\mathbf{I_{Lmin}}$ and $\mathbf{R_{Lmax}}$.** It is easy to see that when load resistance is maximum, load current is minimum.

Now, Zener current, $I_Z = I - I_L$

When the zener is in the "on" state, I remains **fixed. This means that when I_L is maximum, I_Z will be minimum. On the other hand, when I_L is minimum, I_Z is maximum. If the maximum current that a zener can carry safely is †I_{ZM}, then,

---

* If you remove the zener in the circuit shown in Fig. 6.59, then voltage V across the open-circuit is

$$V = \frac{R_L E_i}{R + R_L}$$

The zener will be turned on when $V = V_Z$.

** Voltage across R, $V_R = E_i - E_0$ and $I = V_R/R$. As E_i and E_0 are fixed, I remains the same.

† Max. power dissipation in zener, $P_{ZM} = V_Z I_{ZM}$

$$I_{Lmin} = I - I_{ZM}$$

and
$$R_{Lmax} = \frac{E_0}{I_{Lmin}} = \frac{V_Z}{I_{Lmin}}$$

If the load resistance exceeds this limiting value, the current through zener will exceed I_{ZM} and the device may burn out.

3. Fixed R_L and Variable E_i. This case is shown in Fig. 6.60. Here the load resistance R_L is fixed while the applied voltage (E_i) changes. Note that there is a definite range of E_i values that will ensure that zener diode is in the "on" state. Let us calculate that range of values.

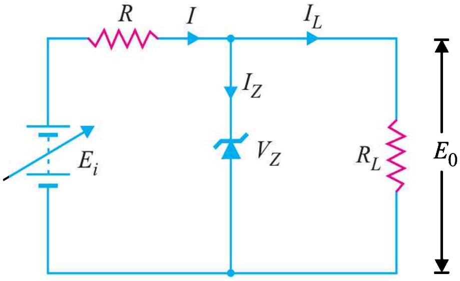


Fig. 6.60

(i)* E$_i$ *(min). To determine the minimum applied voltage that will turn the zener on, simply calculate the value of E_i that will result in load voltage $E_0 = V_Z$ *i.e.*,

$$E_0 = V_Z = \frac{R_L\,E_i}{R + R_L}$$

$$\therefore \quad E_{i\,(min)} = \frac{(R + R_L)\,V_Z}{R_L}$$

(ii)* E$_i$ *(max)

Now, current through R, $I = I_Z + I_L$

Since I_L $(= E_0/R_L = V_Z/R_L)$ is fixed, the value of I will be maximum when zener current is maximum *i.e.*,

$$I_{max} = I_{ZM} + I_L$$

Now
$$E_i = I\,R + E_0$$

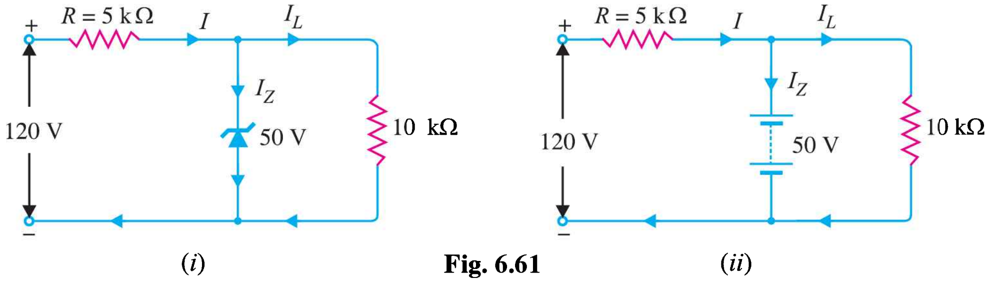
Since E_0 $(= V_Z)$ is constant, the input voltage will be maximum when I is maximum.

$$\therefore \quad E_{i\,(max)} = I_{max}\,R + V_Z$$

Example 6.25. *For the circuit shown in Fig. 6.61 (i), find :*

(i) the output voltage *(ii) the voltage drop across series resistance*

(iii) the current through zener diode.



(*i*) **Fig. 6.61** (*ii*)

Solution. If you remove the zener diode in Fig. 6.61 (*i*), the voltage V across the open-circuit is given by :

$$V = \frac{R_L\, E_i}{R + R_L} = \frac{10 \times 120}{5 + 10} = 80 \text{ V}$$

Since voltage across zener diode is greater than V_Z (= 50 V), the zener is in the "on" state. It can, therefore, be represented by a battery of 50 V as shown in Fig. 6.61 (*ii*).

(*i*) Referring to Fig. 6.61 (*ii*),

Output voltage $= V_Z = \mathbf{50\ V}$

(*ii*) Voltage drop across R = Input voltage $- V_Z = 120 - 50 = \mathbf{70\ V}$

(*iii*) Load current, $I_L = V_Z/R_L = 50 \text{ V}/10 \text{ k}\Omega = 5 \text{ mA}$

$$\text{Current through } R,\ I = \frac{70 \text{ V}}{5 \text{ k}\Omega} = 14 \text{ mA}$$

Applying Kirchhoff's first law, $I = I_L + I_Z$

∴ Zener current, $I_Z = I - I_L = 14 - 5 = \mathbf{9\ mA}$

Example 6.26. *For the circuit shown in Fig. 6.62 (i), find the maximum and minimum values of zener diode current.*

Solution. The first step is to determine the state of the zener diode. It is easy to see that for the given range of voltages (80 – 120 V), the voltage across the zener is greater than V_Z (= 50 V). Hence the zener diode will be in the "on" state for this range of applied voltages. Consequently, it can be replaced by a battery of 50 V as shown in Fig. 6.62 (*ii*).

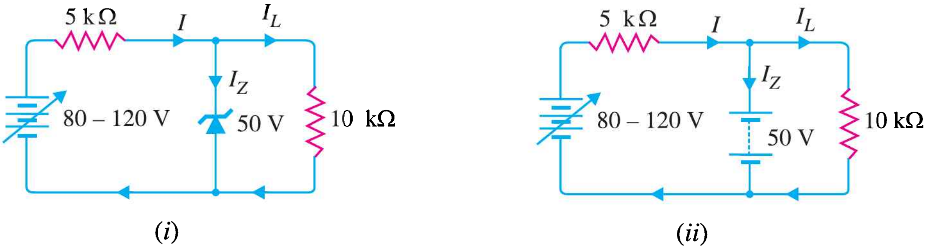


Fig. 6.62

Maximum zener current. The zener will conduct *maximum current when the input voltage is maximum *i.e.* 120 V. Under such conditions :

Voltage across 5 kΩ = 120 – 50 = 70 V

$$\text{Current through 5 k}\Omega,\ I = \frac{70 \text{ V}}{5 \text{ k}\Omega} = 14 \text{ mA}$$

$$\text{Load current, } I_L = \frac{50 \text{ V}}{10 \text{ k}\Omega} = 5 \text{ mA}$$

Applying Kirchhoff's first law, $I = I_L + I_Z$

∴ Zener current, $I_Z = I - I_L = 14 - 5 = \mathbf{9\ mA}$

---

* $I_Z = I - I_L$. Since I_L (= V_Z/R_L) is fixed, I_Z will be maximum when I is maximum.

Now, $I = \frac{E_i - E_0}{R} = \frac{E_i - V_Z}{R}$. Since V_Z (= E_0) and R are fixed, I will be maximum when E_i is maximum and *vice-versa*.

Minimum Zener current. The zener will conduct minimum current when the input voltage is minimum *i.e.* 80 V. Under such conditions, we have,

$$\text{Voltage across } 5\ \text{k}\Omega = 80 - 50 = 30\ \text{V}$$

$$\text{Current through } 5\ \text{k}\Omega,\ I = \frac{30\ \text{V}}{5\ \text{k}\Omega} = 6\ \text{mA}$$

$$\text{Load current, } I_L = 5\ \text{mA}$$

$$\therefore \quad \text{Zener current, } I_Z = I - I_L = 6 - 5 = \mathbf{1\ mA}$$

Example 6.27. *A 7.2 V zener is used in the circuit shown in Fig. 6.63 and the load current is to vary from 12 to 100 mA. Find the value of series resistance R to maintain a voltage of 7.2 V across the load. The input voltage is constant at 12V and the minimum zener current is 10 mA.*

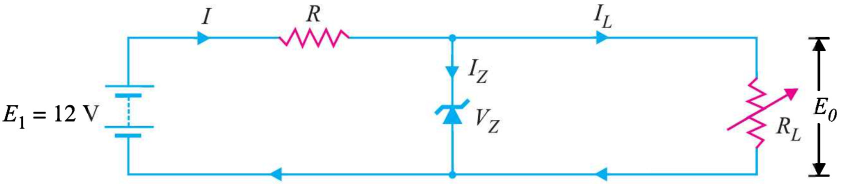


Fig. 6.63

Solution.

$$E_i = 12\ \text{V}; \quad V_Z = 7.2\ \text{V}$$

$$R = \frac{E_i - E_0}{I_Z + I_L}$$

The voltage across R is to remain constant at 12 – 7.2 = 4.8 V as the load current changes from 12 to 100 mA. The minimum zener current will occur when the load current is maximum.

$$\therefore \quad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{12\ \text{V} - 7.2\ \text{V}}{(10 + 100)\ \text{mA}} = \frac{4.8\ \text{V}}{110\ \text{mA}} = \mathbf{43.5\ \Omega}$$

If $R = 43.5\ \Omega$ is inserted in the circuit, the output voltage will remain constant over the regulating range. As the load current I_L decreases, the zener current I_Z will increase to such a value that $I_Z + I_L$ = 110 mA. Note that if load resistance is open-circuited, then $I_L = 0$ and zener current becomes 110 mA.

Example 6.28. *The zener diode shown in Fig. 6.64 has V_Z = 18 V. The voltage across the load stays at 18 V as long as I_Z is maintained between 200 mA and 2 A. Find the value of series resistance R so that E_0 remains 18 V while input voltage E_i is free to vary between 22 V to 28V.*

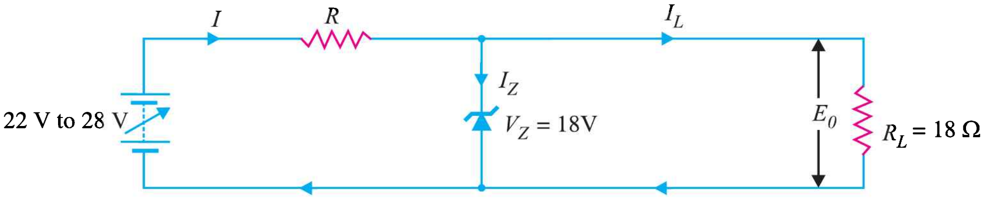


Fig. 6.64

Solution. The zener current will be minimum (*i.e.* 200 mA) when the input voltage is minimum (*i.e.* 22 V). The load current stays at constant value $I_L = V_Z / R_L$ = 18 V/18 Ω = 1 A = 1000 mA.

$$\therefore \quad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{(22 - 18)\ \text{V}}{(200 + 1000)\ \text{mA}} = \frac{4\ \text{V}}{1200\ \text{mA}} = \mathbf{3.33\ \Omega}$$

Example 6.29. *A 10-V zener diode is used to regulate the voltage across a variable load resistor [See fig. 6.65]. The input voltage varies between 13 V and 16 V and the load current varies between 10 mA and 85 mA. The minimum zener current is 15 mA. Calculate the value of series resistance R.*

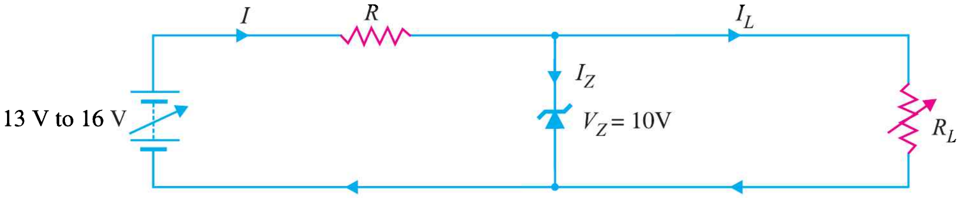


Fig. 6.65

Solution. The zener will conduct minimum current (*i.e.* 15 mA) when input voltage is minimum (*i.e.* 13 V).

$$\therefore \qquad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{(13-10)\text{ V}}{(15+85)\text{ mA}} = \frac{3\text{ V}}{100\text{ mA}} = \mathbf{30\ \Omega}$$

Example 6.30. *The circuit of Fig. 6.66 uses two zener diodes, each rated at 15 V, 200 mA. If the circuit is connected to a 45-volt unregulated supply, determine :*

(i) The regulated output voltage *(ii) The value of series resistance R*

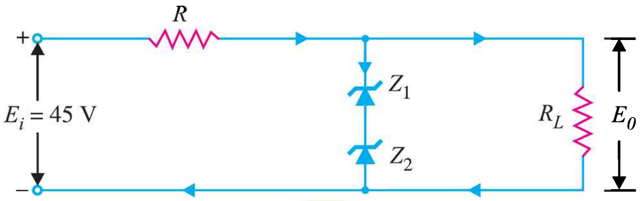


Fig. 6.66

Solution. When the desired regulated output voltage is higher than the rated voltage of the zener, two or more zeners are connected in series as shown in Fig. 6.66. However, in such circuits, care must be taken to select those zeners that have the same current rating.

Current rating of each zener, I_Z = 200 mA

Voltage rating of each zener, V_Z = 15 V

Input voltage, E_i = 45 V

(*i*) Regulated output voltage, E_0 = 15 + 15 = **30 V**

(*ii*) Series resistance, $R = \frac{E_i - E_0}{I_Z} = \frac{45-30}{200\text{ mA}} = \frac{15\text{ V}}{200\text{ mA}} = \mathbf{75\ \Omega}$

Example 6.31. *What value of series resistance is required when three 10-watt, 10-volt, 1000 mA zener diodes are connected in series to obtain a 30-volt regulated output from a 45 volt d.c. power source ?*

Solution. Fig. 6.67 shows the desired circuit. The worst case is at no load because then zeners carry the maximum current.

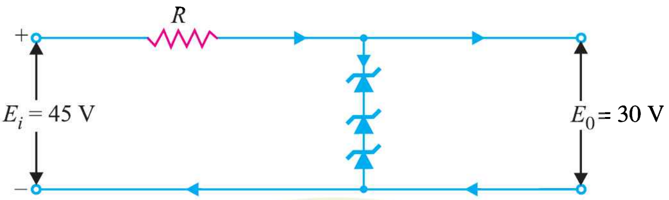


Fig. 6.67

Voltage rating of each zener, $V_Z = 10\text{ V}$

Current rating of each zener, $I_Z = 1000\text{ mA}$

Input unregulated voltage, $E_i = 45\text{ V}$

Regulated output voltage, $E_0 = 10 + 10 + 10 = 30\text{ V}$

Let R ohms be the required series resistance.

$$\text{Voltage across } R = E_i - E_0 = 45 - 30 = 15\text{ V}$$

$$\therefore \quad R = \frac{E_i - E_0}{I_Z} = \frac{15\text{ V}}{1000\text{ mA}} = \mathbf{15\ \Omega}$$

Example 6.32. *Over what range of input voltage will the zener circuit shown in Fig. 6.68 maintain 30 V across 2000 Ω load, assuming that series resistance R = 200 Ω and zener current rating is 25 mA ?*

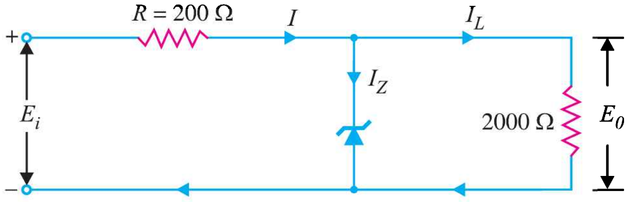


Fig. 6.68

Solution. The minimum input voltage required will be when $I_Z = 0$. Under this condition,

$$I_L = I = \frac{30\text{ V}}{2000\ \Omega} = 15\text{ mA}$$

$$\therefore \quad \text{Minimum input voltage} = 30 + IR = 30 + 15\text{ mA} \times 200\ \Omega$$

$$= 30 + 3 = \mathbf{33\ V}$$

The maximum input voltage required will be when $I_Z = 25$ mA. Under this condition,

$$I = I_L + I_Z = 15 + 25 = 40\text{ mA}$$

$$\therefore \quad \text{Max. input voltage} = 30 + IR$$

$$= 30 + 40\text{ mA} \times 200\ \Omega$$

$$= 30 + 8 = \mathbf{38\ V}$$

Therefore, the input voltage range over which the circuit will maintain 30 V across the load is **33 V to 38 V.**

Example 6.33. *In the circuit shown in Fig. 6.69, the voltage across the load is to be maintained at 12 V as load current varies from 0 to 200 mA. Design the regulator. Also find the maximum wattage rating of zener diode.*

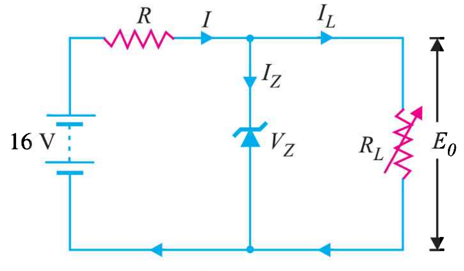


Fig. 6.69

Solution. By designing the regulator here means to find the values of V_Z and R. Since the load voltage is to be maintained at 12 V, we will use a zener diode of zener voltage 12 V *i.e.*,

$$V_Z = \mathbf{12\ V}$$

The voltage across R is to remain constant at 16 – 12 = 4 V as the load current changes from 0 to 200 mA. The minimum zener current will occur when the load current is maximum.

$$\therefore \quad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{16 - 12}{(0 + 200)\text{ mA}} = \frac{4\text{ V}}{200\text{ mA}} = \mathbf{20\ \Omega}$$

Maximum power rating of zener is

$$P_{ZM} = V_Z I_{ZM} = (12\text{ V})(200\text{ mA}) = \mathbf{2.4\ W}$$

Example. 6.34. *Fig. 6.70 shows the basic zener diode circuits. What will be the circuit behaviour if the zener is (i) working properly (ii) shorted (iii) open-circuited?*

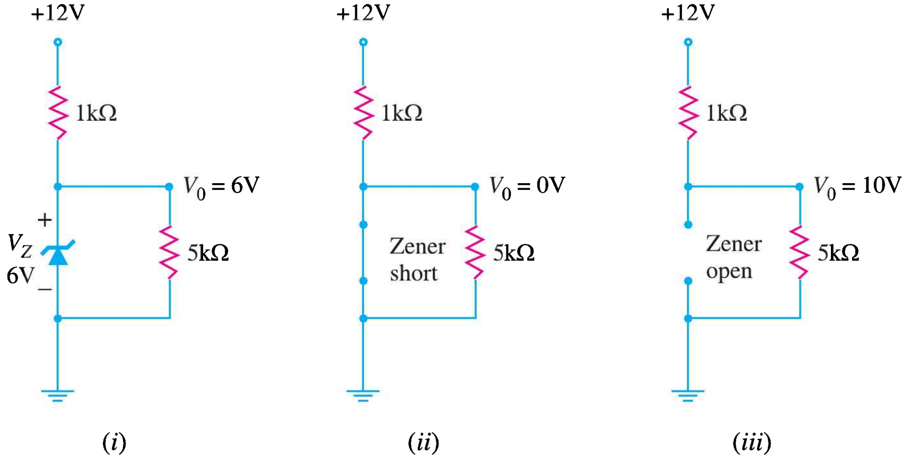


Fig. 6.70

Solution. Zener diodes cannot be tested individually with a multimeter. It is because multimeters usually do not have enough input voltage to put the zener into breakdown region.

(*i*) If the zener diode is working properly, the voltage V_0 across the load (= 5 kΩ) will be nearly 6V [See Fig. 6.70 (*i*)].

(*ii*) If the zener diode is short [See Fig. 6.70 (*ii*)], you will measure V_0 as 0V. The same problem could also be caused by a shorted load resistor (= 5kΩ) or an opened source resistor (= 1 kΩ). The only way to tell which device has failed is to remove the resistors and check them with an ohmmeter. If the resistors are good, then zener diode is bad.

(*iii*) If the zener diode is open-circuited, the voltage V_0 across the load (= 5 kΩ) will be 10V.

Example 6.35. *Fig. 6.71 shows regulated power supply using a zener diode. What will be the circuit behaviour if (i) filter capacitor shorts (ii) filter capacitor opens?*

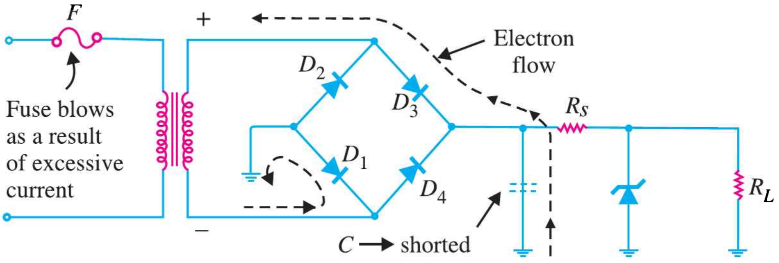


Fig. 6.71

Solution. The common faults in a zener voltage regulator are shorted filter capacitor or opened filter capacitor.

(*i*) **When filter capacitor shorts.** When the filter capacitor shorts, the primary fuse will blow. The reason for this is illustrated in Fig. 6.71. When the filter capacitor shorts, it shorts out the load resistance R_L. This has the same effect as wiring the two sides of the bridge together (See Fig. 6.71).

If you trace from the high side of the bridge to the low side, you will see that the only resistance across the secondary of the transformer is the forward resistance of the two *ON* diodes. This effectively shorts out the transformer secondary. The result is that excessive current flows in the secondary and hence in the primary. Consequently, the primary fuse will blow.

(*ii*) **When filter capacitor opens.** When the filter capacitor opens, it will cause the ripple in the power supply output to increase drastically. At the same time, the d.c. output voltage will show a significant drop. Since an open filter capacitor is the only fault that will cause *both* of these symptoms, no further testing is necessary. If both symptoms appear, replace the filter capacitor.

6.29 Crystal Diodes versus Vacuum Diodes

Semiconductor diodes (or crystal diodes) have a number of advantages and disadvantages as compared to their electron-tube counterparts (*i.e.*, vacuum diodes).

Advantages :

(*i*) They are smaller, more rugged and have a longer life.

(*ii*) They are simpler and inherently cheaper.

(*iii*) They require no filament power. As a result, they produce less heat than the equivalent vacuum diodes.

Disadvantages :

(*i*) They are extremely heat sensitive. Even a slight rise in temperature increases the current appreciably. Should the temperature *exceed the rated value of the diode, the increased flow of current may produce enough heat to ruin the *pn* junction. On the other hand, vacuum diodes function normally over a wide range of temperature changes.

It may be noted that silicon is better than germanium as a semiconductor material. Whereas a germanium diode should not be operated at temperatures higher than 80°C, silicon diodes may operate safely at temperatures upto about 200°C.

(*ii*) They can handle small currents and low inverse voltages as compared to vacuum diodes.

(*iii*) They cannot stand an overload even for a short period. Any slight overload, even a transient pulse, may permanently damage the crystal diode. On the other hand, vacuum diodes can stand an overload for a short period and when the overload is removed, the tube will generally recover.

MULTIPLE-CHOICE QUESTIONS

1. A crystal diode has ....
(*i*) one *pn* junction
(*ii*) two *pn* junctions
(*iii*) three *pn* junctions
(*iv*) none of the above

2. A crystal diode has forward resistance of the order of ....
(*i*) kΩ (*ii*) Ω
(*iii*) MΩ (*iv*) none of the above

3. If the arrow of crystal diode symbol is positive w.r.t. bar, then diode is .... biased.
(*i*) forward
(*ii*) reverse
(*iii*) either forward or reverse
(*iv*) none of the above

4. The reverse current in a diode is of the order of ....
(*i*) kA (*ii*) mA
(*iii*) μA (*iv*) A

5. The forward voltage drop across a silicon diode is about ....

---

* Even when soldering the leads of a crystal diode, care must be taken not to permit heat from the soldering device to reach the crystal diode.

(*i*) 2.5 V (*ii*) 3 V
(*iii*) 10 V (*iv*) 0.7 V

6. A crystal diode is used as ....
(*i*) an amplifier (*ii*) a rectifier
(*iii*) an oscillator (*iv*) a voltage regulator

7. The d.c. resistance of a crystal diode is .... its a.c. resistance.
(*i*) the same as (*ii*) more than
(*iii*) less than (*iv*) none of the above

8. An ideal crystal diode is one which behaves as a perfect .... when forward biased.
(*i*) conductor
(*ii*) insulator
(*iii*) resistance material
(*iv*) none of the above

9. The ratio of reverse resistance and forward resistance of a germanium crystal diode is about ....
(*i*) 1 : 1 (*ii*) 100 : 1
(*iii*) 1000 : 1 (*iv*) 40000 : 1

10. The leakage current in a crystal diode is due to ....
(*i*) minority carriers
(*ii*) majority carriers
(*iii*) junction capacitance
(*iv*) none of the above

11. If the temperature of a crystal diode increases, then leakage current ....
(*i*) remains the same
(*ii*) decreases
(*iii*) increases
(*iv*) becomes zero

12. The PIV rating of a crystal diode is .... that of equivalent vacuum diode.
(*i*) the same as (*ii*) lower than
(*iii*) more than (*iv*) none of the above

13. If the doping level of a crystal diode is increased, the breakdown voltage ....
(*i*) remains the same
(*ii*) is increased
(*iii*) is decreased
(*iv*) none of the above

14. The knee voltage of a crystal diode is approximately equal to ....
(*i*) applied voltage
(*ii*) breakdown voltage
(*iii*) forward voltage
(*iv*) barrier potential

15. When the graph between current through and voltage across a device is a straight line, the device is referred to as ....
(*i*) linear (*ii*) active
(*iii*) nonlinear (*iv*) passive

16. When the crystal diode current is large, the bias is ....
(*i*) forward (*ii*) inverse
(*iii*) poor (*iv*) reverse

17. A crystal diode is a .... device.
(*i*) non-linear (*ii*) bilateral
(*iii*) linear (*iv*) none of the above

18. A crystal diode utilises .... characteristic for rectification.
(*i*) reverse (*ii*) forward
(*iii*) forward or reverse
(*iv*) none of the above

19. When a crystal diode is used as a rectifier, the most important consideration is ....
(*i*) forward characteristic
(*ii*) doping level
(*iii*) reverse characteristic
(*iv*) PIV rating

20. If the doping level in a crystal diode is increased, the width of depletion layer ....
(*i*) remains the same
(*ii*) is decreased
(*iii*) is increased
(*iv*) none of the above

21. A zener diode has ....
(*i*) one *pn* junction
(*ii*) two *pn* junctions
(*iii*) three *pn* junctions
(*iv*) none of the above

22. A zener diode is used as ....
(*i*) an amplifier (*ii*) a voltage regulator
(*iii*) a rectifier (*iv*) a multivibrator

23. The doping level in a zener diode is .... that of a crystal diode.

(*i*) the same as (*ii*) less than
(*iii*) more than (*iv*) none of the above

24. A zener diode is always .... connected.
(*i*) reverse
(*ii*) forward
(*iii*) either reverse or forward
(*iv*) none of the above

25. A zener diode utilises .... characteristic for its operation.
(*i*) forward
(*ii*) reverse
(*iii*) both forward and reverse
(*iv*) none of the above

26. In the breakdown region, a zener diode behaves like a .... source.
(*i*) constant voltage
(*ii*) constant current
(*iii*) constant resistance
(*iv*) none of the above

27. A zener diode is destroyed if it ....
(*i*) is forward biased
(*ii*) is reverse biased
(*iii*) carries more than rated current
(*iv*) none of the above

28. A series resistance is connected in the zener circuit to ....
(*i*) properly reverse bias the zener
(*ii*) protect the zener
(*iii*) properly forward bias the zener
(*iv*) none of the above

29. A zener diode is .... device.
(*i*) a non-linear (*ii*) a linear
(*iii*) an amplifying (*iv*) none of the above

30. A zener diode has .... breakdown voltage.
(*i*) undefined (*ii*) sharp
(*iii*) zero (*iv*) none of the above

31. .... rectifier has the lowest forward resistance.
(*i*) solid state (*ii*) vacuum tube
(*iii*) gas tube (*iv*) none of the above

32. Mains a.c. power is converted into d.c. power for ....
(*i*) lighting purposes
(*ii*) heaters
(*iii*) using in electronic equipment
(*iv*) none of the above

33. The disadvantage of a half-wave rectifier is that the ....
(*i*) components are expensive
(*ii*) diodes must have a higher power rating
(*iii*) output is difficult to filter
(*iv*) none of the above

34. If the a.c. input to a half-wave rectifier has an r.m.s. value of $400/\sqrt{2}$ volts, then diode PIV rating is ....
(*i*) $400/\sqrt{2}$ V (*ii*) 400 V
(*iii*) $400 \times \sqrt{2}$ V (*iv*) none of the above

35. The ripple factor of a half-wave rectifier is ....
(*i*) 2 (*ii*) 1.21
(*iii*) 2.5 (*iv*) 0.48

36. There is a need of transformer for ....
(*i*) half-wave rectifier
(*ii*) centre-tap full-wave rectifier
(*iii*) bridge full-wave rectifier
(*iv*) none of the above

37. The *PIV* rating of each diode in a bridge rectifier is .... that of the equivalent centre-tap rectifier.
(*i*) one-half (*ii*) the same as
(*iii*) twice (*iv*) four times

38. For the same secondary voltage, the output voltage from a centre-tap rectifier is .... than that of bridge rectifier.
(*i*) twice (*ii*) thrice
(*iii*) four times (*iv*) one-half

39. If the PIV rating of a diode is exceeded, ...
(*i*) the diode conducts poorly
(*ii*) the diode is destroyed
(*iii*) the diode behaves as zener diode
(*iv*) none of the above

40. A 10 V power supply would use .... as filter capacitor.
(*i*) paper capacitor (*ii*) mica capacitor
(*iii*) electrolytic capacitor
(*iv*) air capacitor

41. A 1000 V power supply would use .... as a filter capacitor.

(*i*) paper capacitor
(*ii*) air capacitor
(*iii*) mica capacitor
(*iv*) electrolytic capacitor

42. The ...... filter circuit results in the best voltage regulation.

(*i*) choke input
(*ii*) capacitor input
(*iii*) resistance input
(*iv*) none of the above

43. A half-wave rectifier has an input voltage of 240 V r.m.s. If the step-down transformer has a turns ratio of 8 : 1, what is the peak load voltage ? Ignore diode drop.

(*i*) 27.5 V (*ii*) 86.5 V
(*iii*) 30 V (*iv*) 42.5 V

44. The maximum efficiency of a half-wave rectifier is ....

(*i*) 40.6% (*ii*) 81.2%
(*iii*) 50% (*iv*) 25%

45. The most widely used rectifier is ....

(*i*) half-wave rectifier
(*ii*) centre-tap full-wave rectifier
(*iii*) bridge full-wave rectifier
(*iv*) none of the above

Answers to Multiple-Choice Questions

1.	(*i*)	**2.**	(*ii*)	**3.**	(*i*)	**4.**	(*iii*)	**5.**	(*iv*)
6.	(*ii*)	**7.**	(*iii*)	**8.**	(*i*)	**9.**	(*iv*)	**10.**	(*i*)
11.	(*iii*)	**12.**	(*ii*)	**13.**	(*iii*)	**14.**	(*iv*)	**15.**	(*i*)
16.	(*i*)	**17.**	(*i*)	**18.**	(*ii*)	**19.**	(*iv*)	**20.**	(*iii*)
21.	(*i*)	**22.**	(*ii*)	**23.**	(*iii*)	**24.**	(*i*)	**25.**	(*ii*)
26.	(*i*)	**27.**	(*iii*)	**28.**	(*ii*)	**29.**	(*i*)	**30.**	(*ii*)
31.	(*i*)	**32.**	(*iii*)	**33.**	(*iii*)	**34.**	(*ii*)	**35.**	(*iv*)
36.	(*ii*)	**37.**	(*i*)	**38.**	(*iv*)	**39.**	(*ii*)	**40.**	(*iii*)
41.	(*i*)	**42.**	(*i*)	**43.**	(*iv*)	**44.**	(*i*)	**45.**	(*iii*)

Chapter Review Topics

1. What is a crystal diode ? Explain its rectifying action.
2. Draw the graphic symbol of crystal diode and explain its significance. How the polarities of crystal diode are identified ?
3. What do you understand by the d.c. and a.c. resistance of a crystal diode ? How will you determine them from the *V-I* characteristic of a crystal diode ?
4. Draw the equivalent circuit of a crystal diode.
5. Discuss the importance of peak inverse voltage in rectifier service.
6. Describe a half-wave rectifier using a crystal diode.
7. Derive an expression for the efficiency of a half-wave rectifier.
8. With a neat sketch, explain the working of (*i*) Centre-tap full-wave rectifier (*ii*) Full-wave bridge rectifier.
9. Derive an expression for the efficiency for a full-wave rectifier.
10. Write a short note about the nature of rectifier output.
11. What is a ripple factor ? What is its value for a half-wave and full-wave rectifier ?
12. Describe the action of the following filter circuits : (*i*) capacitor filter (*ii*) choke input filter (*iii*) capacitor input filter.
13. What is a zener diode ? Draw the equivalent circuit of an ideal zener in the breakdown region.
14. Explain how zener diode maintains constant voltage across the load.

Problems

1. What is the current in the circuit in Fig. 6.72 ? Assume the diode to be ideal. **[10 mA]**

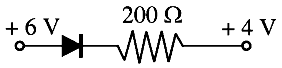


Fig. 6.72

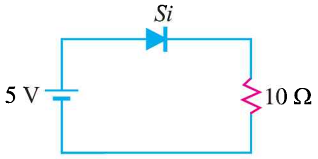


Fig. 6.73

2. Using equivalent circuit, determine the current in the circuit shown in Fig. 6.73. Assume the forward resistance of the diode to be 2 Ω. **[358 mA]**
3. Find the voltage V_A and current I in the circuit shown in Fig. 6.74. Use simplified model. **[14 V; 2 mA]**
4. Determine the magnitude of V_A in the circuit shown in Fig. 6.75. **[9.5 V]**
5. A half-wave rectifier uses a transformer of turn ratio 4 : 1. If the primary voltage is 240 V (r.m.s.), find (*i*) d.c. output voltage (*ii*) peak inverse voltage. Assume the diode to be ideal. **[(*i*) 27 V (*ii*) 85 V]**

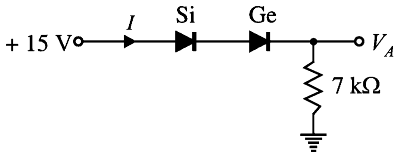


Fig. 6.74

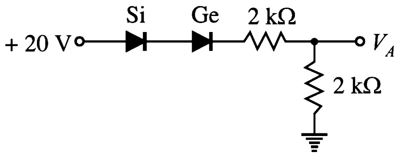


Fig. 6.75

6. A half-wave rectifier uses a transformer of turn ratio 2 : 1. The load resistance is 500 Ω. If the primary voltage (r.m.s.) is 240 V, find (*i*) d.c. output voltage (*ii*) peak inverse voltage. **[(*i*) 54 V (*ii*) 170 V]**

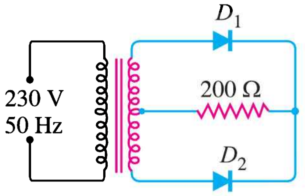


Fig. 6.76

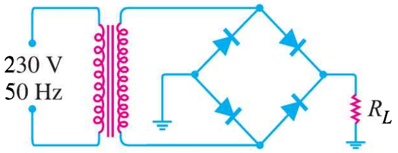
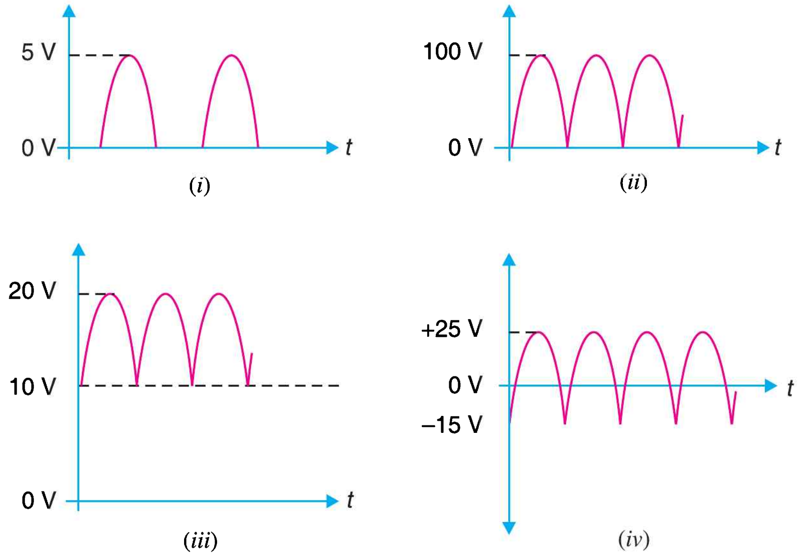


Fig. 6.77

7. In Fig. 6.76, the maximum voltage across half of secondary winding is 50 V. Find (*i*) the average load voltage (*ii*) peak inverse voltage (*iii*) output frequency. Assume the diodes to be ideal. **[(*i*) 31.8 V (*ii*) 100 V (*iii*) 100 Hz]**
8. In Fig. 6.77, the maximum secondary voltage is 136 V. Find (*i*) the d.c. load voltage (*ii*) peak inverse voltage (*iii*) output frequency. **[(*i*) 86.6 V (*ii*) 136 V (*iii*) 100 Hz]**
9. A semiconductor diode having ideal forward and reverse characteristics is used in a half-wave rectifier circuit supplying a resistive load of 1000 Ω. If the r.m.s. value of the sinusoidal supply voltage is 250 V, determine (*i*) the r.m.s. diode current and (*ii*) power dissipated in the load. **[(*i*) 177 mA (*ii*) 31.3W]**
10. The four semiconductor diodes used in a bridge rectifier circuit have forward resistance which can be considered constant at 0.1Ω and infinite reverse resistance. They supply a mean current of 10 A to a resistive load from a sinusoidally varying alternating supply of 20V r.m.s. Determine the resistance of the load and the efficiency of the circuit. **[1.6Ω ; 72%]**
11. Find the average value of each voltage in Fig. 6.78. **[(*i*) 1.59 V (*ii*) 63.7 V (*iii*) 16.4 V (*iv*) 10.5 V]**



(*i*) (*ii*) (*iii*) (*iv*)

Fig. 6.78

12. Calculate the peak voltage across each half of a centre-tapped transformer used in a full-wave rectifier that has an average output voltage of 110V. **[173V]**
13. What PIV rating is required for the diodes in a bridge rectifier that produces an average output voltage of 50V? **[78.5 V]**
14. In the circuit shown in Fig. 6.79, is zener diode in the on or off state ? **[Off]**

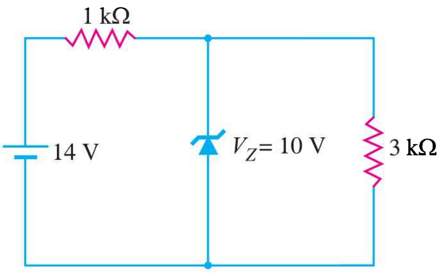


Fig. 6.79

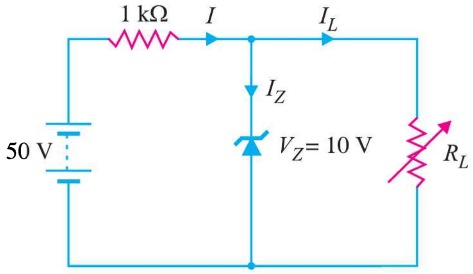


Fig. 6.80

15. In the circuit shown in Fig. 6.80, determine the range of R_L that will result in a constant voltage of 10 V across R_L. **[250 Ω to 1.25 kΩ]**

Discussion Questions

1. Why are diodes not operated in the breakdown region in rectifier service ?
2. Why do we use transformers in rectifier service ?
3. Why is *PIV* important in rectifier service ?
4. Why is zener diode used as a voltage regulator ?
5. Why is capacitor input filter preferred to choke input filter ?

7

Special-Purpose Diodes

7.1 Zener Diode
7.2 Light-Emitting Diode (LED)
7.3 LED Voltage and Current
7.4 Advantages of LED
7.5 Multicolour LEDs
7.6 Applications of LEDs
7.7 Photo-diode
7.8 Photo-diode operation
7.9 Characteristics of Photo-diode
7.10 Applications of photo-diodes
7.11 Optoisolator
7.12 Tunnel Diode
7.13 Tunnel Diode Oscillator
7.14 Varactor Diode
7.15 Application of Varactor Diode
7.16 Shockley Diode

INTRODUCTION

The most common application of diodes is rectification. The rectifier diodes are used in power supplies to convert a.c. voltage into d.c. voltage. But rectification is not all that a diode can do. A number of specific types of diodes are manufactured for specific applications in this fast developing world. Some of the more common special-purpose diodes are (*i*) Zener diode (*ii*) Light-emitting diode (LED) (*iii*) Photo-diode (*iv*) Tunnel diode (*v*) Varactor diode and (*vi*) Shockley diode.

7.1 Zener Diode

A zener diode is a special type of diode that is designed to operate in the reverse breakdown region. An ordinary diode operated in this region will usually be destroyed due to excessive current. This is not the case for the zener diode.

A zener diode is heavily doped to reduce the reverse breakdown voltage. This causes a very thin depletion layer. As a result, a zener diode has a sharp reverse breakdown voltage V_Z. This is clear from the reverse characteristic of zener diode shown in Fig. 7.1. Note that the reverse characteristic drops in an almost vertical manner at reverse voltage V_Z. As the curve reveals, two things happen when V_Z is reached :

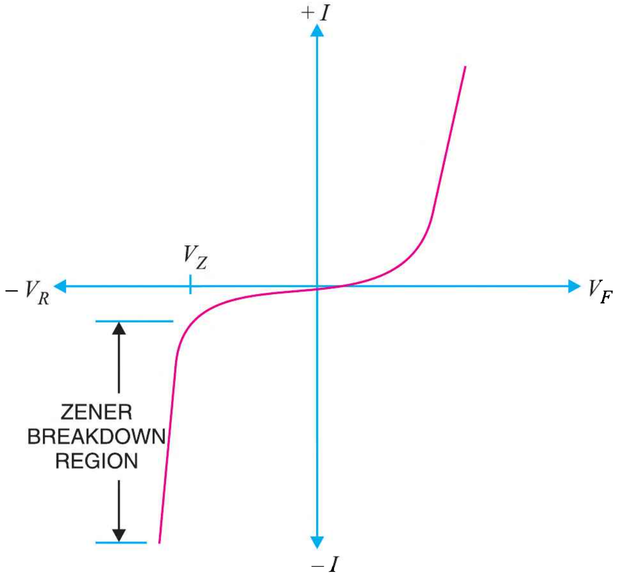


Fig. 7.1

(*i*) The diode current increases rapidly.

(*ii*) The reverse voltage V_Z across the diode remains almost constant.

In other words, *the zener diode operated in this region will have a relatively constant voltage across it, regardless of the value of current through the device.* This permits the zener diode to be used as a *voltage regulator.* For detailed discussion on zener diode, the reader may refer to chapter 6 of this book.

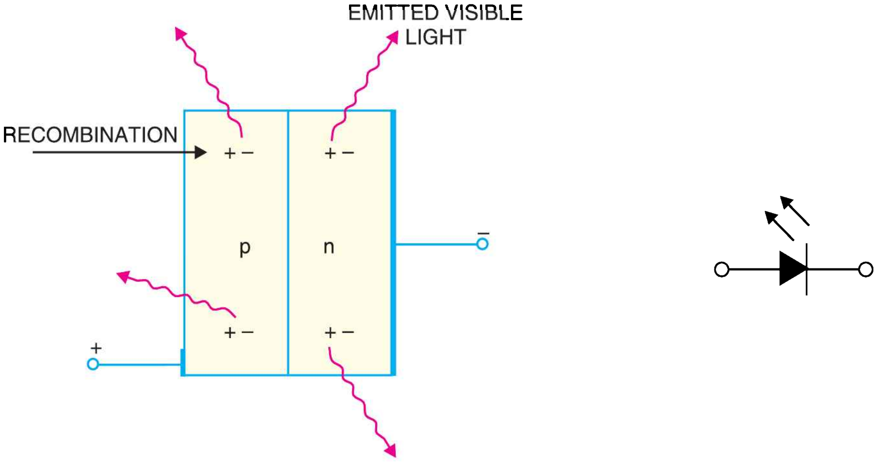
7.2 Light-Emitting Diode (LED)

A **light-emitting diode (LED)** *is a diode that gives off visible light when forward biased.*

Light-emitting diodes are not made from silicon or germanium but are made by using elements like gallium, phosphorus and arsenic. By varying the quantities of these elements, it is possible to produce light of different wavelengths with colours that include red, green, yellow and blue. For example, when a LED is manufactured using gallium arsenide, it will produce a red light. If the LED is made with gallium phosphide, it will produce a green light.

Light-emitting diode

Theory. When light-emitting diode (LED) is forward biased as shown in Fig. 7.2 (*i*), the electrons from the *n*-type material cross the *pn* junction and recombine with holes in the *p*-type material. Recall that these free electrons are in the conduction band and at a higher energy level than the holes in the valence band. When recombination takes place, the recombining electrons release energy in the form of heat and light. In germanium and silicon diodes, almost the entire energy is given up in the form of heat and emitted light is insignificant. However, in materials like gallium arsenide, the number of photons of light energy is sufficient to produce quite intense visible light.



(*i*) (*ii*)

Fig. 7.2

Fig. 7.2 (*ii*) shows the schematic symbol for a LED. The arrows are shown as pointing away from the diode, indicating that light is being emitted by the device when forward biased. Although LEDs are available in several colours (red, green, yellow and orange are the most common), the schematic symbol is the same for all LEDs. There is nothing in the symbol to indicate the colour of a particular LED. Fig. 7.3 shows the graph between radiated light and the forward current of the LED. It is clear from the graph that the intensity of radiated light is directly proportional to the forward current of LED.

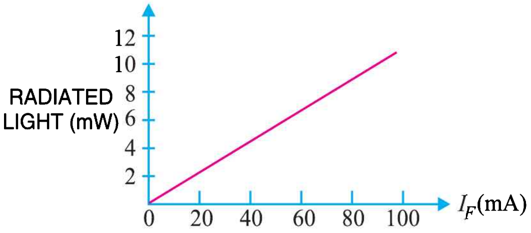


Fig. 7.3

7.3 LED Voltage and Current

The forward voltage ratings of most LEDs is from 1V to 3V and forward current ratings range from 20 mA to 100 mA. In order that current through the LED does not exceed the safe value, a resistor R_S is connected in series with it as shown in Fig. 7.4. The input voltage is V_S and the voltage across LED is V_D.

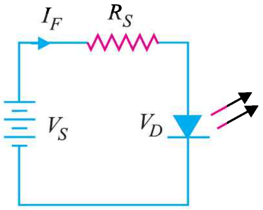


Fig. 7.4

$\therefore$ Voltage across $R_S = V_S - V_D$

$\therefore$ Circuit current, $I_F = \dfrac{V_S - V_D}{R_S}$

Example 7.1. *What value of series resistor is required to limit the current through a LED to 20 mA with a forward voltage drop of 1.6 V when connected to a 10V supply ?*

Solution.

Series resistor, $R_S = \dfrac{V_S - V_D}{I_F}$

Here $V_S = 10\text{ V}; \quad V_D = 1.6\text{ V}; \quad I_F = 20\text{ mA} = 20 \times 10^{-3}\text{ A}$

$$\therefore \qquad R_S = \frac{10 - 1.6}{20 \times 10^{-3}} = \mathbf{420\ \Omega}$$

Note that resistor R_S is also called *current-limiting resistor.*

Example 7.2. *What is current through the LED in the circuit shown in Fig. 7.5 ? Assume that voltage drop across the LED is 2 V.*

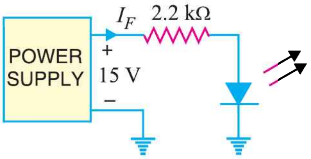


Fig. 7.5

Solution.

$$\text{Current through LED, } I_F = \frac{V_S - V_D}{R_S}$$

Here V_S = 15 V; V_D = 2 V; R_S = 2.2 kΩ = 2.2×10^3 Ω

$$\therefore \qquad I_F = \frac{15 - 2}{2.2 \times 10^3} = 5.91 \times 10^{-3}\ \text{A} = \mathbf{5.91\ mA}$$

7.4 Advantages of LED

The light-emitting diode (LED) is a solid-state light source. LEDs have replaced incandescent lamps in many applications because they have the following advantages :

(*i*) Low voltage

(*ii*) Longer life (more than 20 years)

(*iii*) Fast on-off switching

Protecting LED against reverse bias. The LEDs have low reverse voltage ratings. For example, a typical LED may have a maximum reverse voltage rating of 3V. This means that if a reverse voltage greater than 3 V is applied to the LED, the LED may be destroyed. Therefore, one must be careful not to use LEDs with a high level of reverse bias. One way to protect a LED is to connect a rectifier diode in parallel with LED as shown in Fig. 7.6. If reverse voltage greater than the reverse voltage rating of LED is accidentally applied, the rectifier diode will be turned on. This protects the LED from damage.

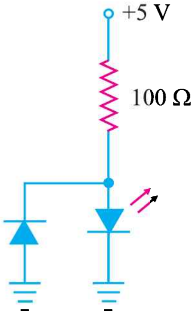
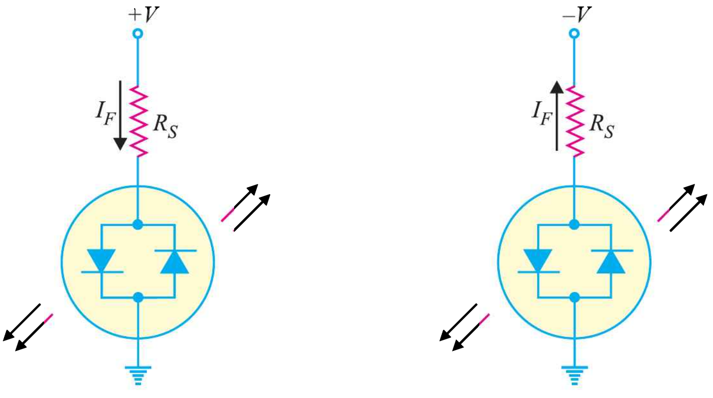


Fig. 7.6

7.5 Multicolour LEDs

A LED that emits one colour when forward biased and another colour when reverse biased is called a **multicolour LED.**

One commonly used schematic symbol for these LEDs is shown in Fig. 7.7. Multicolour LEDs



(*i*) (*ii*)

Fig. 7.7

actually contain two *pn* junctions that are connected in *reverse-parallel i.e.* they are in parallel with anode of one being connected to the cathode of the other. If positive potential is applied to the top terminal as shown in Fig. 7.7 (*i*), the *pn* junction on the **left** will light. Note that the device current passes through the left *pn* junction. If the polarity of the voltage source is reversed as shown in Fig. 7.7 (*ii*), the *pn* junction on the **right** will light. Note that the direction of device current has reversed and is now passing through the right *pn* junction.

Multicolour LEDs are typically *red* when biased in one direction and *green* when biased in the other. If a multicolour LED is switched fast enough between two polarities, the LED will produce a *third* colour. A red/green LED will produce a *yellow* light when rapidly switched back and forth between biasing polarities.

7.6 Applications of LEDs

The LED is a low-power device. The power rating of a LED is of the order of milliwatts. This means that it is useful as an indicator but not good for illumination. Probably the two most common applications for visible LEDs are (*i*) as a power indicator (*ii*) seven-segment display.

(*i*) **As a power indicator.** A LED can be used to indicate whether the power is on or not. Fig. 7.8 shows the simple use of the LED as a power indicator. When the switch S is closed, power is applied to the load. At the same time current also flows through the LED which lights, indicating power is on. The resistor R_S in series with the LED ensures that current rating of the LED is not exceeded.

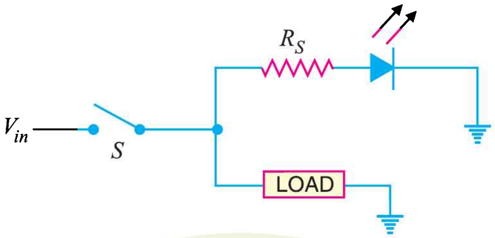


Fig. 7.8

(*ii*) **Seven-segment display.** LEDs are often grouped to form seven-segment display. Fig. 7.9 (*i*) shows the front of a seven segment display. It contains seven LEDs (*A, B, C, D, E, F* and *G*) shaped in a figure of *8. Each LED is called a **segment. If a particular LED is forward biased, that LED or segment will light and produces a bar of light. By forward biasing various combinations of seven LEDs, it is possible to display any number from 0 to 9. For example, if LEDs *A, B, C, D* and *G* are lit (by forward biasing them), the display will show the number 3. Similarly, if LEDs *C, D, E, F, A* and *G* are lit, the display will show the number *6*. To get the number 0, all segments except *G* are lit.

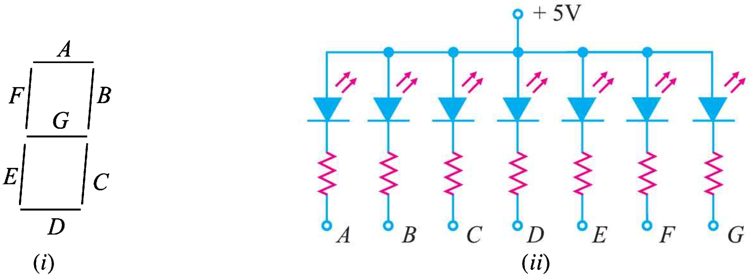


Fig. 7.9

Fig. 7.9 (*ii*) shows the schematic diagram of seven-segment display. External series resistors are included to limit currents to safe levels. Note that the anodes of all seven LEDs are connected to a common positive voltage source of +5 V. This arrangement is known as **common-anode type*. In order to light a particular LED, say *A*, we ground the point *A* in Fig. 7.9 (*ii*). It forward biases the LED *A* which will be lit.

---

* Note that LEDs *A, B, C, D, E* and *F* are arranged clockwise from the top with LED *G* in the middle.

** Each LED is called a segment because it forms part of the character being displayed.

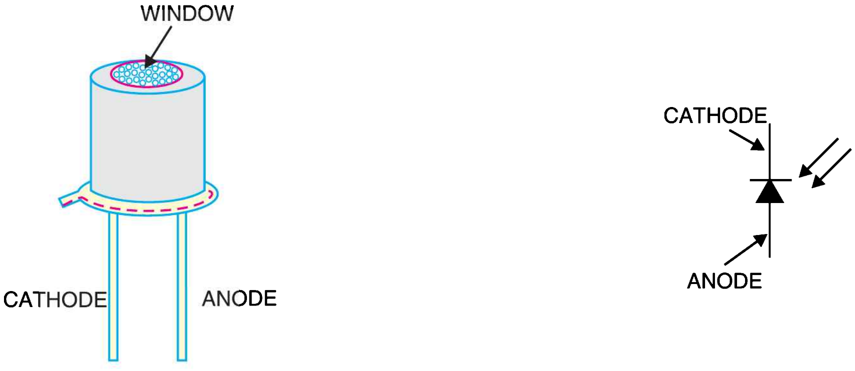
7.7 Photo-diode

A **photo-diode** *is a reverse-biased silicon or germanium pn junction in which reverse current increases when the junction is exposed to light.*

The reverse current in a photo-diode is directly proportional to the intensity of light falling on its *pn* junction. This means that greater the intensity of light falling on the *pn* junction of photo-diode, the greater will be the reverse current.

Principle. When a rectifier diode is reverse biased, it has a very small reverse leakage current. The same is true for a photo-diode. The reverse current is produced by thermally generated electron-hole pairs which are swept across the junction by the electric field created by the reverse voltage. In a rectifier diode, the reverse current increases with temperature due to an increase in the number of electron-hole pairs. *A photo-diode differs from a rectifier diode in that when its pn junction is exposed to light, the reverse current increases with the increase in light intensity and vice-versa.* This is explained as follows. When light (photons) falls on the ***pn* junction, the energy is imparted by the photons to the atoms in the junction. This will create more free electrons (and more holes). These additional free electrons will increase the reverse current. As the intensity of light incident on the *pn* junction increases, the reverse current also increases. In other words, as the incident light intensity increases, the resistance of the device (photo-diode) ***decreases.

Photo-diode package. Fig. 7.10 (*i*) shows a typical photo-diode package. It consists of a *pn* junction mounted on an insulated substrate and sealed inside a metal case. A glass window is mounted on top of the case to allow light to enter and strike the *pn* junction. The two leads extending from the case are labelled anode and cathode. The cathode is typically identified by a tab extending from the side of the case.



(*i*) (*ii*)

Fig. 7.10

Fig. 7.10 (*ii*) shows the schematic symbol of a photo-diode. The inward arrows represent the incoming light.

---

* Also available is the *common-cathode type* where all cathodes are connected together.

** This is true only if the light energy is applied at the junction. If it is applied to the crystal at some distance from the junction, the free electrons and holes will recombine (thus neutralising each other) before they can join the flow of reverse current.

*** It is for this reason that semiconductor devices such as diodes and transistors are usually enclosed in opaque case to protect them from light. Those diodes or transistors which are used for light-detecting, on the other hand, must be encased in transparent plastic or glass so that light may fall on them.

7.8 Photo-diode Operation

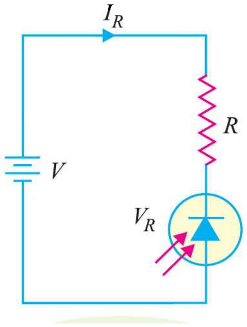


Fig. 7.11

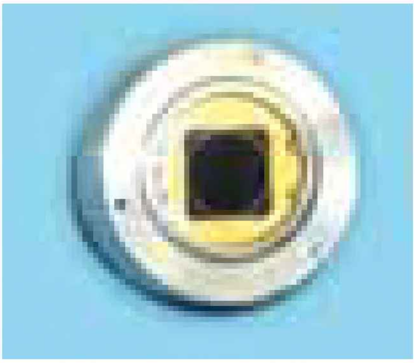
Fig. 7.11 shows the basic photo-diode circuit. The circuit has reverse-biased photo-diode, resistor *R* and d.c. supply. The operation of the photo-diode is as under :

(*i*) When no light is incident on the *pn* junction of photo-diode, the reverse current I_r is extremely small. This is called **dark current.**

The resistance of photo-diode with no incident light is called *dark resistance* (R_R).

$$\text{Dark resistance of photo-diode, } R_R = \frac{V_R}{\text{Dark current}}$$

(*ii*) When light is incident on the *pn* junction of the photo-diode, there is a transfer of energy from the incident light (photons) to the atoms in the junction. This will create more free electrons (and more holes). These additional free electrons will increase the reverse current.



Calibrated Photo-Diode

(*iii*) As the intensity of light increases, the reverse current I_R goes on increasing till it becomes maximum. This is called **saturation current.**

7.9 Characteristics of Photo-diode

There are two important characteristics of photo-diode.

(*i*) **Reverse current-Illumination curve.** Fig. 7.12 shows the graph between reverse current (I_R) and illumination (E) of a photo-diode. The reverse current is shown on the vertical axis and is measured in μA. The illumination is indicated on the horizontal axis and is measured in mW/cm^2. Note that graph is a straight line passing through the origin.

$\therefore \quad I_R = mE$

where $\quad m$ = slope of the straight line

The quantity *m* is called the *sensitivity* of the photo-diode.

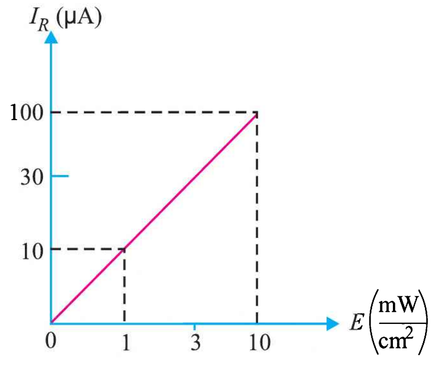


Fig. 7.12

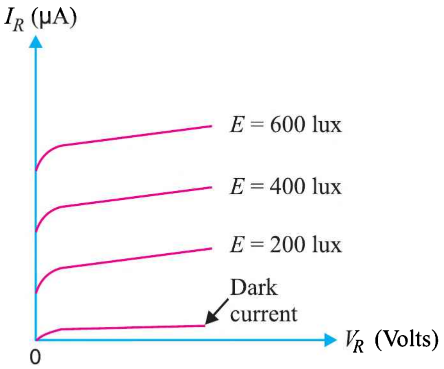


Fig. 7.13

(*ii*) **Reverse voltage-Reverse current curve.** Fig. 7.13 shows the graph between reverse current (I_R) and reverse voltage (V_R) for various illumination levels. It is clear that for a given reverse-biased voltage V_R, the reverse current I_R increases as the illumination (E) on the *pn* junction of photo-diode is increased.

7.10 Applications of Photo-diodes

There are a large number of applications of photo-diodes. However, we shall give two applications of photo-diodes by way of illustration.

(*i*) **Alarm circuit using photo-diode.** Fig. 7.14 shows the use of photo-diode in an alarm system. Light from a light source is allowed to fall on a photo-diode fitted in the doorway. The reverse current I_R will continue to flow so long as the light beam is not broken. If a person passes through the door, light beam is broken and the reverse current drops to the dark current level. As a result, an alarm is sounded.

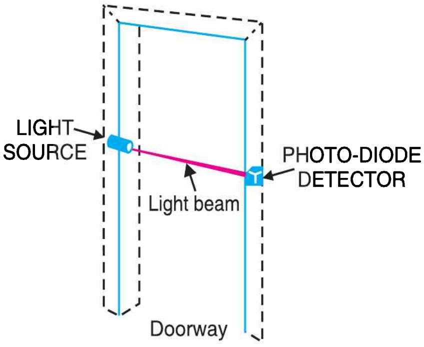


Fig. 7.14

(*ii*) **Counter circuit using photo-diode.** A photo-diode may be used to count items on a conveyor belt. Fig. 7.15 shows a photo-diode circuit used in a system that counts objects as they pass by on a conveyor. In this circuit, a source of light sends a concentrated beam of light across a conveyor to a photo-diode. As the object passes, the light beam is broken, I_R drops to the dark current level and the count is increased by one.

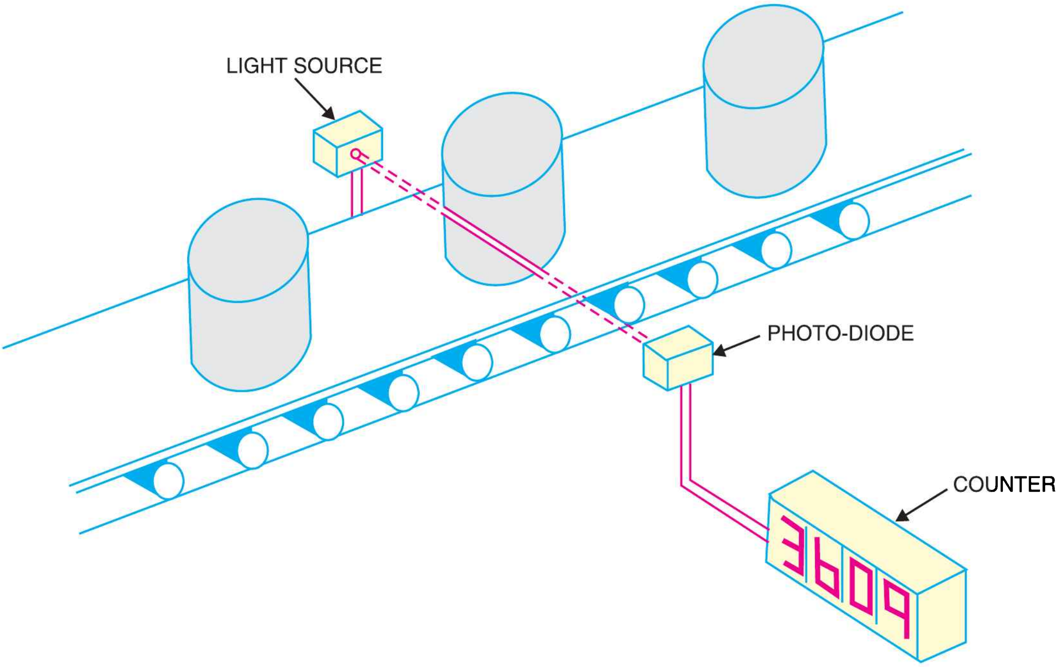


Fig. 7.15

Example 7.3. *From the reverse current-Illumination curve for a photo-diode shown in Fig. 7.16, determine the dark resistance. Assume a reverse-biased voltage of 10 V.*

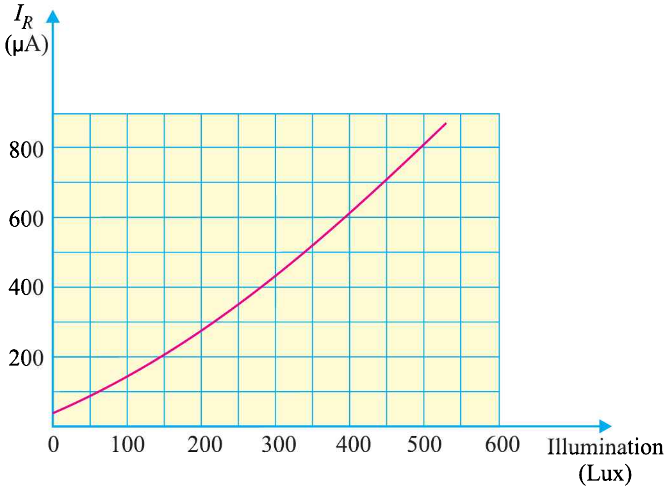


Fig. 7.16

Solution.

The current that flows when the incident light is removed from the photo-diode is called *dark current*. The resistance of a photo-diode corresponding to dark current is called *dark resistance*. From the curve shown in Fig. 7.16, it is clear that for zero illumination, the reverse current is 50 μA.

$$\therefore \quad \text{Dark current, } I_r = 50\ \mu\text{A} = 50 \times 10^{-6}\ \text{A}$$

$$\text{Reverse voltage, } V_R = 10\ \text{V}$$

$$\therefore \quad \text{Dark resistance, } R_R = \frac{V_R}{I_r} = \frac{10}{50 \times 10^{-6}} = 200 \times 10^3\ \Omega = \mathbf{200\ k\Omega}$$

Example 7.4. *A photo-diode is exposed to light with an illumination of 2.5 mW/cm^2. If the sensitivity of the photo-diode for the given conditions is 37.4 μA/mW/cm^2, find the reverse current through the device.*

Solution.

$$\text{Reverse current} = \text{Sensitivity} \times \text{Illumination}$$

or

$$I_R = m \times E = 37.4 \times 2.5 = \mathbf{93.5\ \mu A}$$

7.11 Optoisolator

An ***optoisolator*** *(also called optocoupler) is a device that uses light to couple a signal from its input (a photoemitter e.g., a LED) to its output (a photodetector e.g., a photo-diode).*

Fig. 7.17 shows a LED-photo diode optoisolator. The LED is on the left and the photo-diode is on the right. The arrangement shown in Fig. 7.17 is referred to as *optocoupling* because the output from the LED circuit is coupled via light to the photo-diode circuit. When the LED is energised, current flows through the LED. The light from the LED hits the photo diode and sets up a reverse current through resistor R_2. The voltage across the photo-diode is given by :

$$V_{out} = V_{SS} - I R_2$$

The output voltage depends on how large the reverse current is. If we vary the LED supply, the amount of light changes and this causes the photo diode current to change. As a result, V_{out} changes. The key advantage of an optoisolator is the electrical isolation between the input and output circuits; the only contact between the input and output circuits is the stream of light.

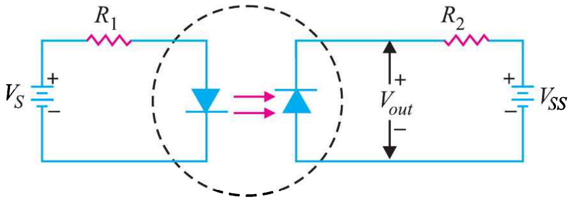


Fig. 7.17

7.12 Tunnel Diode

A **tunnel diode** *is a pn junction that exhibits negative resistance between two values of forward voltage (i.e., between peak-point voltage and valley-point voltage).*

A conventional diode exhibits *positive resistance when it is forward biased or reverse biased. However, if a semiconductor junction diode is heavily doped with impurities, it exhibits negative resistance (*i.e.* current decreases as the voltage is increased) in certain regions in the forward direction. Such a diode is called *tunnel diode.*

Theory. The tunnel diode is basically a *pn* junction with heavy doping of *p*-type and *n*-type semiconductor materials. In fact, a tunnel diode is doped approximately 1000 times as heavily as a conventional diode. This heavy doping results in a large number of majority carriers. Because of the large number of carriers, most are not used during the initial recombination that produces the depletion layer. As a result, the *depletion layer is very narrow.* In comparison with conventional diode, the depletion layer of a tunnel diode is 100 times narrower. The operation of a tunnel diode depends upon the *tunneling effect* and hence the name.

Tunneling effect. The heavy doping provides a large number of majority carriers. Because of the large number of carriers, there is much drift activity in *p* and *n* sections. This causes many valence electrons to have their energy levels raised closer to the conduction region. Therefore, it takes only a very small applied forward voltage to cause conduction.

The movement of valence electrons from the valence energy band to the conduction band with little or no applied forward voltage is called **tunneling.** *Valence electrons seem to tunnel through the forbidden energy band.*

As the forward voltage is first *increased,* the diode current rises rapidly due to tunneling effect. Soon the tunneling effect is reduced and current flow starts to *decrease* as the forward voltage across the diode is increased. The tunnel diode is said to have entered the negative resistance region. As the voltage is further increased, the tunneling effect plays less and less part until a valley-point is reached. From now onwards, the tunnel diode behaves as ordinary diode *i.e.*, diode current increases with the increase in forward voltage.

V-I Characteristic. Fig. 7.18 (*i*) shows the V-I characteristic of a typical tunnel diode.

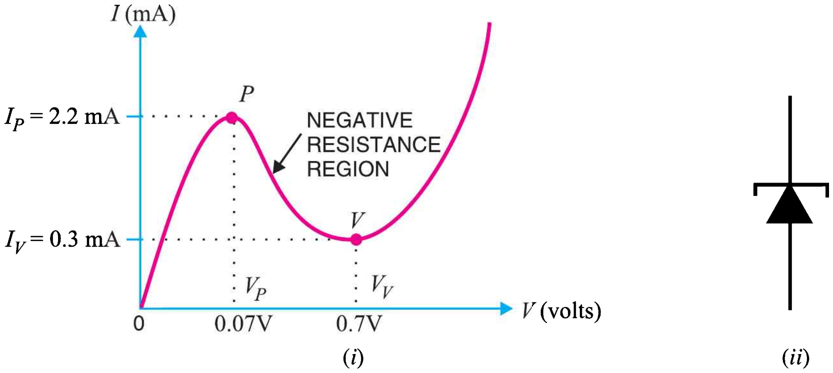
(*i*) As the forward voltage across the tunnel diode is increased from zero, electrons from the *n*-region "tunnel" through the potential barrier to the *p*-region. As the forward voltage increases, the diode current also increases until the *peak-point P* is reached. The diode current has now reached peak current I_P (= 2.2 mA) at about peak-point voltage V_P (= 0.07 V). Until now the diode has exhibited positive resistance.

(*ii*) As the voltage is increased beyond V_P, the tunneling action starts decreasing and the diode current decreases as the forward voltage is increased until *valley-point V* is reached at valley-point voltage V_V (= 0.7V). In the region between peak-point and valley-point (*i.e.*, between points *P* and

---

* If current flowing through a circuit or device increases as the applied voltage is increased, we say that the circuit or device has positive resistance.

V), the diode exhibits negative resistance *i.e.*, as the forward bias is increased, the current decreases. This suggests that tunnel diode, when operated in the negative resistance region, can be used as an oscillator or a switch.



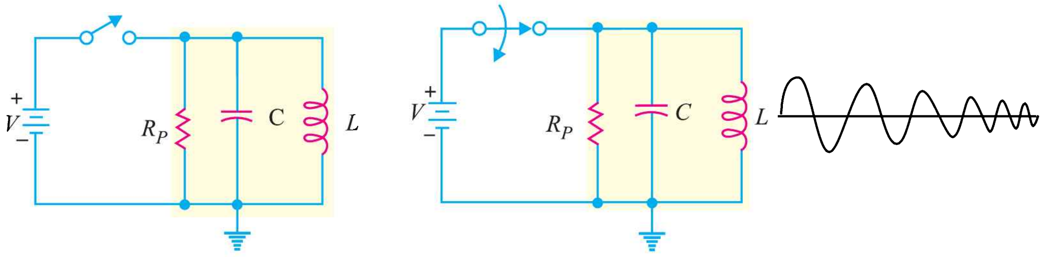
(*i*) (*ii*)

Fig. 7.18

(***iii***) When forward bias is increased beyond valley-point voltage V_V (= 0.7 V), the tunnel diode behaves as a normal diode. In other words, from point V onwards, the diode current increases with the increase in forward voltage *i.e.*, the diode exhibits positive resistance once again. Fig. 7.18. (*ii*) shows the symbol of tunnel diode. It may be noted that a tunnel diode has a high reverse current but operation under this condition is not generally used.

7.13 Tunnel Diode Oscillator

A tunnel diode is always operated in the negative resistance region. When operated in this region, it works very well in an oscillator. Fig. 7.19 (*i*) shows a parallel resonant circuit. Note that R_P is the parallel equivalent of the series winding resistance of the coil. When the tank circuit is set into oscillations by applying voltage as shown in Fig. 7.19. (*ii*), damped oscillations are produced. It is because energy is lost in the resistance R_P of the tank circuit.



(*i*) (*ii*)

Fig. 7.19

If a tunnel diode is placed in series with the tank circuit and biased at the centre of the negative-resistance portion of its characteristic as shown in Fig. 7.20, undamped oscillations are produced at the output. It is because the negative-resistance characteristic of the tunnel diode counteracts the positive-resistance characteristic of the tank circuit.

The circuit shown in Fig. 7.20 is called *tunnel diode oscillator* or *negative resistance oscillator.* The negative resistance oscillator has one major drawback. While the circuit works very well at extreme high frequencies (upper mega hertz range), it cannot be used efficiently at low frequencies. Low-frequency oscillators generally use transistors.

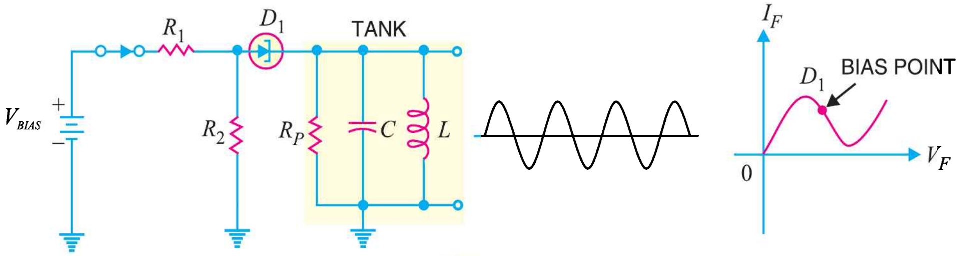
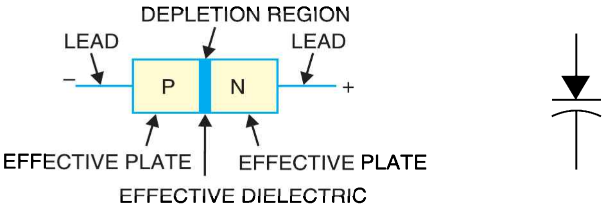


Fig. 7.20

7.14 Varactor Diode

A junction diode which acts as a variable capacitor under changing reverse bias is known as a ***varactor diode.***

When a *pn* junction is formed, depletion layer is created in the junction area. Since there are no charge carriers within the depletion zone, the zone acts as an insulator. The *p*-type material with holes (considered positive) as majority carriers and *n*-type material with electrons (–ve charge) as majority carriers act as charged plates. Thus the diode may be considered as a capacitor with *n*-region and *p*-region forming oppositely charged plates and with depletion zone between them acting as a dielectric. This is illustrated in Fig. 7.21 (*i*). A varactor diode is specially constructed to have high capacitance under reverse bias. Fig. 7.21 (*ii*) shows the symbol of varactor diode. The values of capacitance of varactor diodes are in the picofarad (10^{-12} F) range.



(*i*) (*ii*)

Fig. 7.21

Theory. For normal operation, a *varactor diode is always *reverse biased.* The capacitance of varactor diode is found as :

$$C_T = \varepsilon \frac{A}{W_d}$$

where C_T = Total capacitance of the junction

ε = Permittivity of the semiconductor material

A = Cross-sectional area of the junction

W_d = Width of the depletion layer

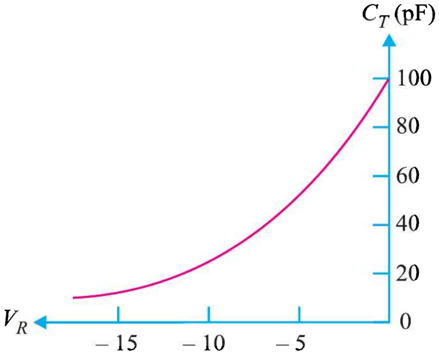


Fig. 7.22

When reverse voltage across a varactor diode is increased, the width W_d of the depletion layer increases. Therefore, the total junction capacitance C_T of the junction decreases. On the other hand, if the reverse voltage across the diode is lowered, the width W_d of the depletion layer decreases. Consequently, the total junction capacitance C_T increases.

---

* A forward biased varactor diode would serve no useful purpose.

Fig. 7.22 shows the curve between reverse bias voltage V_R across varactor diode and total junction capacitance C_T. Note that C_T can be changed simply by changing the voltage V_R. For this reason, a varactor diode is sometimes called **voltage-controlled capacitor.**

7.15 Application of Varactor Diode

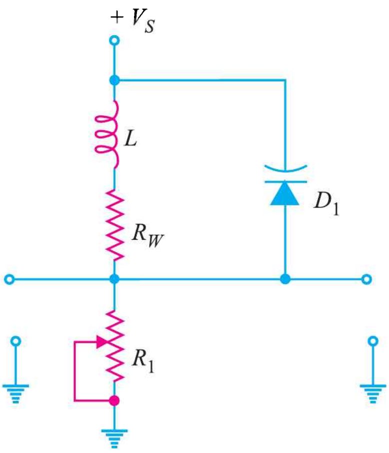


Fig. 7.23

We have discussed that we can increase or decrease the junction capacitance of varactor diode simply by changing the reverse bias on the diode. This makes a varactor diode ideal for use in circuits that require voltage-controlled tuning. Fig. 7.23 shows the use of varactor diode in a tuned circuit. Note that the capacitance of the varactor is in *parallel* with the inductor. The varactor and the inductor form a parallel *LC* circuit. *For normal operation, a varactor diode is always operated under reverse bias.* In fact, this condition is met in the circuit shown in Fig. 7.23. The resistance R_W in the circuit is the *winding resistance* of the inductor. This winding resistance is in series with the potentiometer R_1. Thus R_1 and R_W form a voltage divider that is used to determine the amount of reverse bias across the varactor diode D_1 and therefore its capacitance. By adjusting the setting of R_1, we can vary the diode capacitance. This, in turn, varies the resonant frequency of the *LC* circuit. The resonant frequency f_r of the *LC* circuit is given by;

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

If the amount of varactor reverse bias is *decreased,* the value of *C* of the varactor *increases.* The increase in *C* will cause the resonant frequency of the circuit to *decrease.* Thus, *a decrease in reverse bias causes a decrease in resonant frequency and vice-versa.*

Example 7.5. *The LC tank circuit shown in Fig. 7.23 has a 1 mH inductor. The varactor has capacitance of 100 pF when reverse bias is 5V d.c. Determine the resonant frequency of the circuit for this reverse bias.*

Solution.

$$\text{Resonant frequency, } f_r = \frac{1}{2\pi\sqrt{LC}}$$

Here, $L = 1\text{mH} = 1 \times 10^{-3}$ H; $C = 100$ pF $= 100 \times 10^{-12}$ F

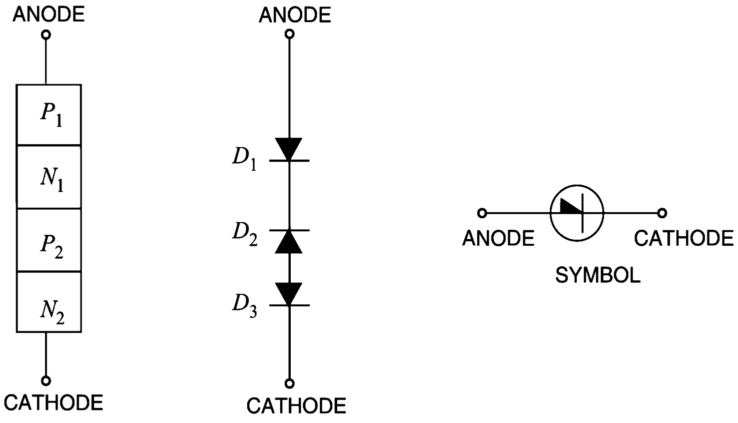
$$\therefore \quad f_r = \frac{1}{2\pi\sqrt{1\times10^{-3}\times100\times10^{-12}}} = 503.3 \times 10^3 \text{ Hz} = \mathbf{503.3\ kHz}$$

7.16 Shockley Diode

Named after its inventor, a Shockley diode is a *PNPN* device having two terminals as shown in Fig. 7.24 (*i*). This *device acts as a switch and consists of four alternate *P*-type and *N*-type layers in a single crystal. The various layers are labelled as P_1, N_1, P_2 and N_2 for identification. Since a *P*-region adjacent to an N-region may be considered a junction diode, the Shockley diode is equivalent to three junction diodes connected in series as shown in Fig. 7.24 (*ii*). The symbol of Shockley diode is shown in Fig. 7.24 (*iii*).

---

* Note that if we remove the gate terminal of an SCR, the resulting device is Shockley diode.



(*i*) (*ii*) (*iii*)

Fig. 7.24

Working

(*i*) When Shockley diode is forward biased (*i.e.*, anode is positive w.r.t. cathode), diodes D_1 and D_3 would be forward-biased while diode D_2 would be reverse-biased. Since diode D_2 offers very high resistance (being reverse biased) and the three diodes are in series, the Shockley diode presents a very high resistance. As the *forward voltage increases, the reverse bias across D_2 is also increased. At some forward voltage (called *breakover voltage* V_{BO}), reverse breakdown of D_2 occurs. Since this breakdown results in reduced resistance, the Shockley diode presents a very low resistance. From now onwards, the Shockley diode behaves as a conventional forward-biased diode; the forward current being determined by the applied voltage and external load resistance. This behaviour of Shockley diode is indicated on its *V-I* characteristic in Fig. 7.25.

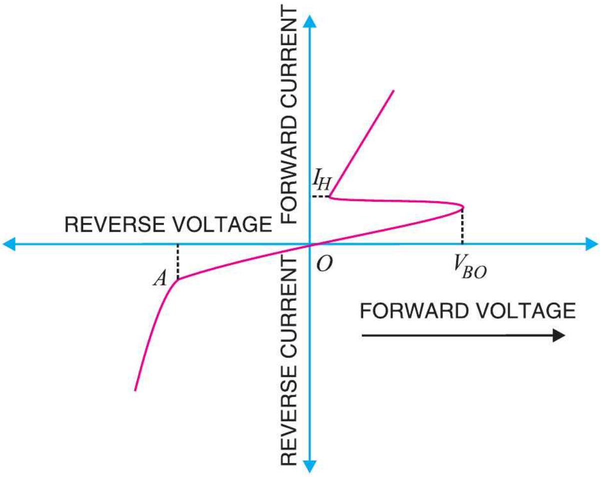


Fig. 7.25

(*ii*) When Shockley diode is reverse biased (*i.e.*, anode is negative *w.r.t.* cathode), diodes D_1 and D_3 would be reverse-biased while diode D_2 would be forward-biased. If reverse voltage is increased sufficiently, the reverse voltage breakdown (point *A* in Fig. 7.25) of Shockley diode is reached. At this point, diodes D_1 and D_3 would go into reverse-voltage breakdown, the reverse current flowing through them would rise rapidly and the heat produced by this current flow could ruin the entire device. For this reason, *Shockley diode should never be operated with a reverse voltage sufficient to reach the reverse-voltage breakdown point.*

---

* Since D_1 and D_3 offer very low resistance (being forward biased), the entire applied voltage appears as reverse voltage across D_2.

Conclusion. The above discussion reveals that Shockley diode behaves like a switch. So long as the forward voltage is less than breakover voltage, Shockley diode offers very high resistance (*i.e.*, switch is open) and practically conducts no current. At voltages above the break-over value, Shockley diode presents a very low resistance (*i.e.* switch is closed) and Shockley diode conducts heavily. It may be noted that Shockley diode is also known as *PNPN diode* or *four layer diode* or *reverse-blocking diode thyristor.*

Note. Once Shockley diode is turned ON (*i.e.*, it starts conducting), the only way to turn it OFF is to reduce the applied voltage to such a value so that current flowing through Shockley diode drops below its *holding current* (I_H) *value*. Diode D_2 then comes out of its reverse-breakdown state and its high-resistance value is restored. This, in turn, causes the entire Shockley diode to revert to its high-resistance (switch open) state.

MULTIPLE-CHOICE QUESTIONS

1. Zener diodes are used primarily as
(*i*) amplifiers (*ii*) voltage regulators
(*iii*) rectifiers (*iv*) oscillators

2. A *pn* junction that radiates energy as light instead of as heat is called a
(*i*) LED (*ii*) photo-diode
(*iii*) photocell (*iv*) Zener diode

3. The capacitance of a varactor diode increases when reverse voltage across it
(*i*) decreases (*ii*) increases
(*iii*) breaks down (*iv*) stores charge

4. To display the digit 8 in a seven-segment indicator
(*i*) C must be lighted
(*ii*) G must be off
(*iii*) F must be on
(*iv*) All segments must be lighted

5. A photo-diode is normally
(*i*) forward-biased
(*ii*) reverse-biased
(*iii*) Neither forward nor reverse biased
(*iv*) Emitting light

6. When the reverse voltage increases, the junction capacitance
(*i*) decreases (*ii*) stays the same
(*iii*) increases (*iv*) has more bandwidth

7. The device associated with voltage-controlled capacitance is a
(*i*) LED (*ii*) photo-diode
(*iii*) varactor diode (*iv*) Zener diode

8. The varactor is usually
(*i*) forward-biased
(*ii*) reverse-biased
(*iii*) unbiased
(*iv*) in the breakdown region

9. When the light increases, the reverse current in a photo-diode
(*i*) increases (*ii*) decreases
(*iii*) is unaffected (*iv*) none of the above

10. To display the digit 0 in a seven segment display
(*i*) A must be lighted
(*ii*) F must be off
(*iii*) G must be on
(*iv*) all segments except G should be lighted

Answers to Multiple-Choice Questions

1. (*ii*) **2.** (*i*) **3.** (*i*) **4.** (*iv*) **5.** (*ii*)
6. (*i*) **7.** (*iii*) **8.** (*ii*) **9.** (*i*) **10.** (*iv*)

Chapter Review Topics

1. What is a LED ?
2. Explain the working of a LED.
3. Give two applications of LEDs.
4. Why do LEDs need series current-limiting resistors ?
5. How does LED differ from an ordinary diode ?
6. What is a photo-diode ?
7. How does photo-diode work ?
8. Give two applications of photo-diodes.
9. What is an optoisolator ?
10. What is a tunnel diode ?
11. Explain the V-I characteristics of a tunnel diode.
12. Explain the working of tunnel diode oscillator.
13. What is a varactor diode ?
14. Explain the working of varactor diode.
15. Give one application of varactor diode.
16. Explain the working of Shockley diode.

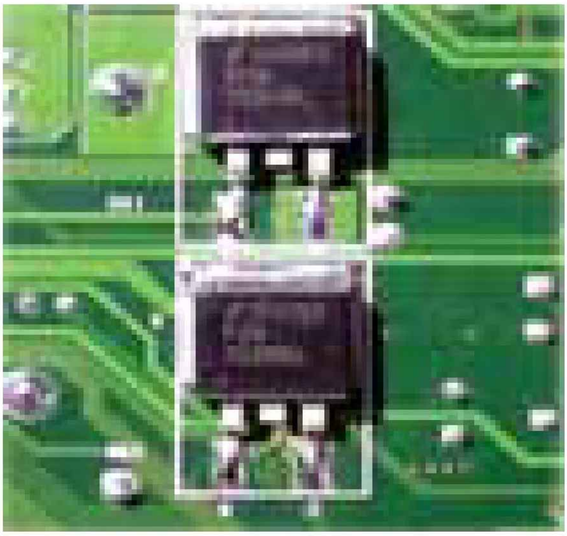
Discussion Questions

1. Why is LED not made of silicon or germanium ?
2. Where do we use seven-segment display ?
3. How do we protect LED from large reverse voltage ?
4. How does photo-diode differ from an ordinary diode ?
5. What is dark resistance of photo-diode ?
6. What do you mean by the sensitivity of photo-diode ?
7. What is the use of optoisolator ?
8. How does the width of depletion layer change the capacitance of a varactor ?

8

Transistors

8.1 Transistor
8.3 Some Facts about the Transistor
8.5 Transistor Symbols
8.7 Transistor Connections
8.9 Characteristics of Common Base Connection
8.11 Measurement of Leakage Current
8.13 Common Collector Connection
8.15 Commonly Used Transistor Connection
8.17 Transistor Load Line Analysis
8.19 Practical Way of Drawing CE Circuit
8.21 Performance of Transistor Amplifier
8.23 Power Rating of Transistor
8.25 Semiconductor Devices Numbering System
8.27 Transistor Testing
8.29 Transistors Versus Vacuum Tubes



INTRODUCTION

When a third doped element is added to a crystal diode in such a way that two *pn* junctions are formed, the resulting device is known as a *transistor*. The transistor—an entirely new type of electronic device—is capable of achieving amplification of weak signals in a fashion comparable and often superior to that realised by vacuum tubes. Transistors are far smaller than vacuum tubes, have no filament and hence need no heating power and may be operated in any position. They are mechanically strong, have practically unlimited life and can do some jobs better than vacuum tubes.

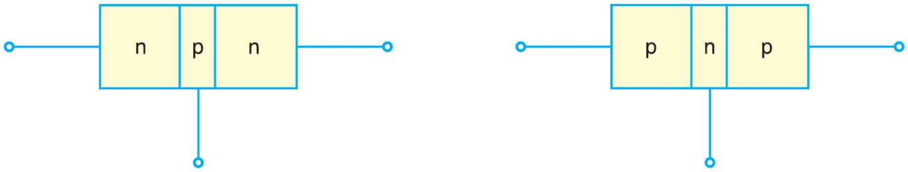
Invented in 1948 by J. Bardeen and W.H. Brattain of Bell Telephone Laboratories, U.S.A.; transistor has now become the heart of most electronic applications. Though transistor is only slightly more than 58 years old, yet it is fast replacing vacuum tubes in almost all applications. In this chapter, we shall focus our attention on the various aspects of transistors and their increasing applications in the fast developing electronics industry.

8.1 Transistor

A **transistor** *consists of two pn junctions formed by *sandwiching either p-type or n-type semiconductor between a pair of opposite types.* Accordingly ; there are two types of transistors, namely;

(*i*) *n-p-n* transistor (*ii*) *p-n-p* transistor

An *n-p-n* transistor is composed of two *n*-type semiconductors separated by a thin section of *p*-type as shown in Fig. 8.1 (*i*). However, a *p-n-p* transistor is formed by two *p*-sections separated by a thin section of *n*-type as shown in Fig. 8.1 (*ii*).



(*i*) (*ii*)

Fig. 8.1

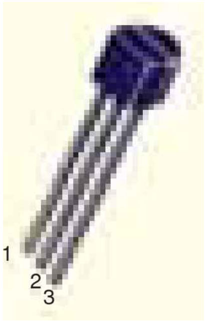
In each type of transistor, the following points may be noted :

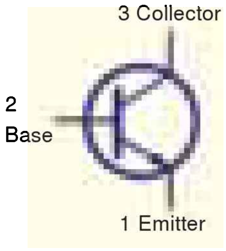
(*i*) These are two *pn* junctions. Therefore, a transistor may be regarded as a combination of two diodes connected back to back.

(*ii*) There are three terminals, one taken from each type of semiconductor.

(*iii*) The middle section is a very thin layer. This is the most important factor in the function of a transistor.

Origin of the name "Transistor". When new devices are invented, scientists often try to devise a name that will appropriately describe the device. A transistor has two *pn* junctions. As discussed later, one junction is forward biased and the other is reverse biased. The forward biased junction has a low resistance path whereas a reverse biased junction has a high resistance path. The weak signal is introduced in the low resistance circuit and output is taken from the high resistance circuit. Therefore, a transistor *transfers* a signal from a low resistance to high resistance. The prefix 'trans' means the signal transfer property of the device while 'istor' classifies it as a solid element in the same general family with resistors.





---

* In practice, these three blocks *p, n, p* are grown out of the same crystal by adding corresponding impurities in turn.

8.2 Naming the Transistor Terminals

A transistor (*pnp* or *npn*) has three sections of doped semiconductors. The section on one side is the *emitter* and the section on the opposite side is the *collector*. The middle section is called the *base* and forms two junctions between the emitter and collector.

(*i*) **Emitter.** The section on one side that supplies charge carriers (electrons or holes) is called the *emitter*. *The emitter is always forward biased w.r.t. base* so that it can supply a large number of *majority carriers. In Fig. 8.2 (*i*), the emitter (*p*-type) of *pnp* transistor is forward biased and supplies hole charges to its junction with the base. Similarly, in Fig. 8.2 (*ii*), the emitter (*n*-type) of *npn* transistor has a forward bias and supplies free electrons to its junction with the base.

(*ii*) **Collector.** The section on the other side that collects the charges is called the *collector*. *The collector is always reverse biased*. Its function is to remove charges from its junction with the base. In Fig. 8.2 (*i*), the collector (*p*-type) of *pnp* transistor has a reverse bias and receives hole charges that flow in the output circuit. Similarly, in Fig. 8.2 (*ii*), the collector (*n*-type) of *npn* transistor has reverse bias and receives electrons.

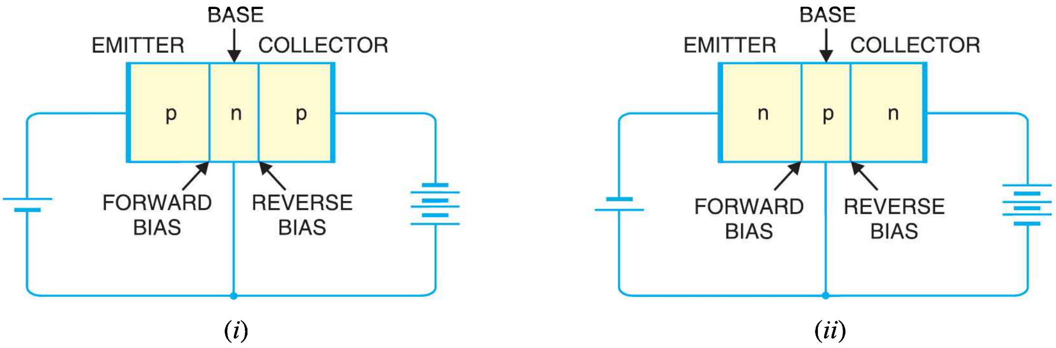


Fig. 8.2

(*iii*) **Base.** The middle section which forms two *pn*-junctions between the emitter and collector is called the *base*. The base-emitter junction is forward biased, allowing low resistance for the emitter circuit. The base-collector junction is reverse biased and provides high resistance in the collector circuit.

8.3 Some Facts about the Transistor

Before discussing transistor action, it is important that the reader may keep in mind the following facts about the transistor :

(*i*) The transistor has three regions, namely ; *emitter*, *base* and *collector*. The base is much thinner than the emitter while **collector is wider than both as shown in Fig. 8.3. However, for the sake of convenience, it is customary to show emitter and collector to be of equal size.

(*ii*) The emitter is heavily doped so that it can inject a large number of charge carriers (electrons or holes) into the base. The base is lightly doped and very thin ; it passes most of the emitter injected charge carriers to the collector. The collector is moderately doped.

---

* Holes if emitter is *p*-type and electrons if the emitter is *n*-type.

** During transistor operation, much heat is produced at the collector junction. The collector is made larger to dissipate the heat.

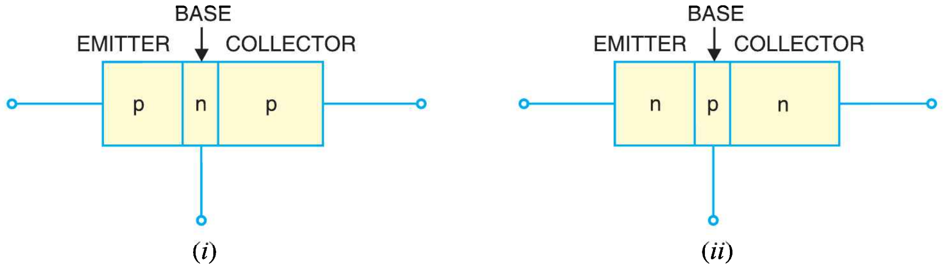


Fig. 8.3

(iii) The transistor has two *pn* junctions *i.e.* it is like two diodes. The junction between emitter and base may be called *emitter-base diode* or simply the *emitter diode*. The junction between the base and collector may be called *collector-base diode* or simply *collector diode*.

(iv) The emitter diode is always forward biased whereas collector diode is always reverse biased.

(v) The resistance of emitter diode (forward biased) is very small as compared to collector diode (reverse biased). Therefore, forward bias applied to the emitter diode is generally very small whereas reverse bias on the collector diode is much higher.

8.4 Transistor Action

The emitter-base junction of a transistor is forward biased whereas collector-base junction is reverse biased. If for a moment, we ignore the presence of emitter-base junction, then *practically** no current would flow in the collector circuit because of the reverse bias. However, if the emitter-base junction is also present, then forward bias on it causes the emitter current to flow. It is seen that this emitter current almost entirely flows in the collector circuit. Therefore, the current in the collector circuit depends upon the emitter current. If the emitter current is zero, then collector current is nearly zero. However, if the emitter current is 1mA, then collector current is also about 1mA. This is precisely what happens in a transistor. We shall now discuss this transistor action for ***npn*** and ***pnp*** transistors.

(i) **Working of npn transistor.** Fig. 8.4 shows the *npn* transistor with forward bias to emitter-base junction and reverse bias to collector-base junction. The forward bias causes the electrons in the *n*-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons flow through the *p*-type base, they tend to combine with holes. As the base is lightly doped and very thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base** current I_B. The remainder (***more than 95%) cross over into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flows in the collector circuit. It is clear that emitter current is the sum of collector and base currents *i.e.*

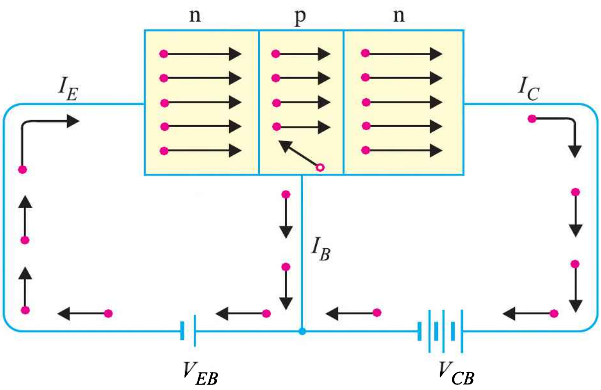
$$I_E = I_B + I_C$$

---

* In actual practice, a very little current (a few μA) would flow in the collector circuit. This is called collector cut off current and is due to minority carriers.

** The electrons which combine with holes become valence electrons. Then as valence electrons, they flow down through holes and into the external base lead. This constitutes base current I_B.

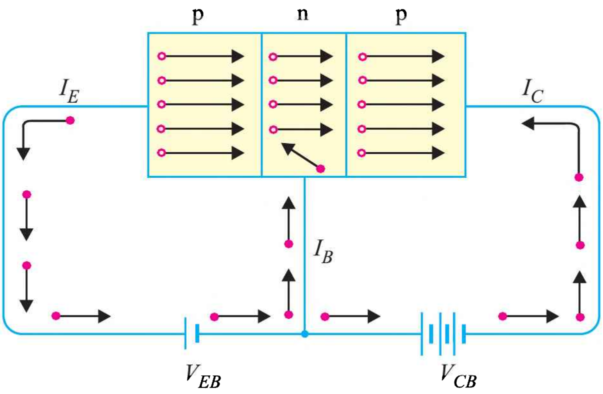
*** The reasons that most of the electrons from emitter continue their journey through the base to collector to form collector current are : (*i*) The base is lightly doped and very thin. Therefore, there are a few holes which find enough time to combine with electrons. (*ii*) The reverse bias on collector is quite high and exerts attractive forces on these electrons.



Basic connection of *npn* transistor

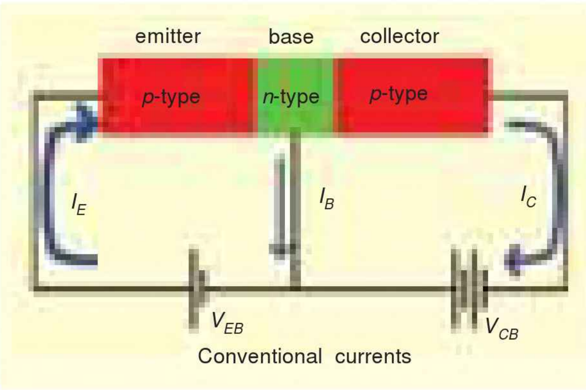
Fig. 8.4

(*ii*) **Working of pnp transistor.** Fig. 8.5 shows the basic connection of a *pnp* transistor. The forward bias causes the holes in the *p*-type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes cross into *n*-type base, they tend to combine with the electrons. As the base is lightly doped and very thin, therefore, only a few holes (less than 5%) combine with the electrons. The remainder (more than 95%) cross into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flows in the collector circuit. It may be noted that current conduction within *pnp* transistor is by holes. However, in the external connecting wires, the current is still by electrons.



Basic connection of *pnp* transistor

Fig. 8.5

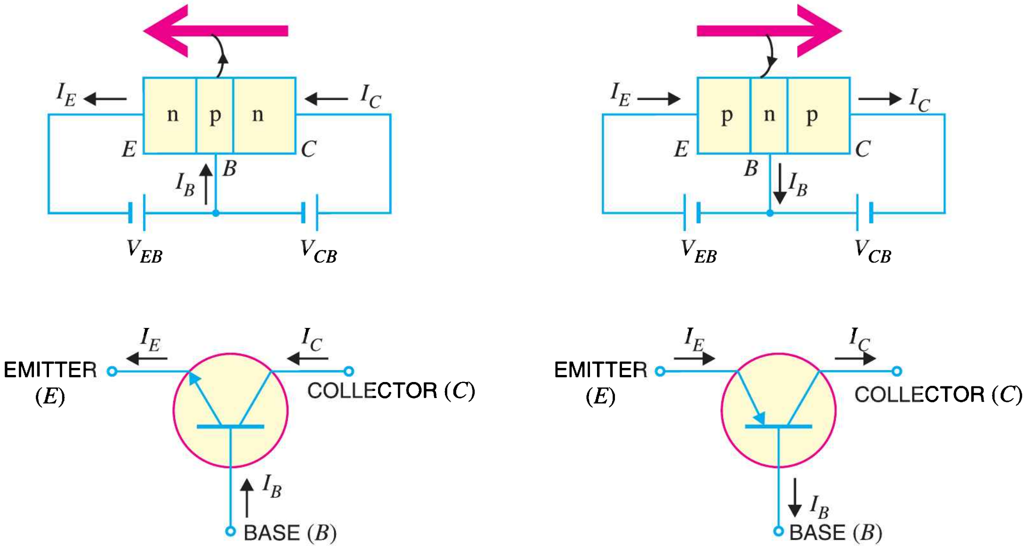


Importance of transistor action. The input circuit (*i.e.* emitter-base junction) has low resistance because of forward bias whereas output circuit (*i.e.* collector-base junction) has high resistance due to reverse bias. As we have seen, the input emitter current almost entirely flows in the collector circuit. Therefore, a transistor transfers the input signal current from a low-resistance circuit to a high-resistance circuit. This is the key factor responsible for the amplifying capability of the transistor. We shall discuss the amplifying property of transistor later in this chapter.

Note. There are two basic transistor types : the **bipolar junction transistor** (*BJT*) and **field-effect transistor** (*FET*). As we shall see, these two transistor types differ in both their operating characteristics and their internal construction. **Note that when we use the term transistor, it means bipolar junction transistor (*BJT*).** The term comes from the fact that in a bipolar transistor, there are *two* types of charge carriers (*viz*. electrons and holes) that play part in conductions. Note that bi means two and polar refers to polarities. The field-effect transistor is simply referred to as *FET*.

8.5 Transistor Symbols

In the earlier diagrams, the transistors have been shown in diagrammatic form. However, for the sake of convenience, the transistors are represented by schematic diagrams. The symbols used for *npn* and *pnp* transistors are shown in Fig. 8.6.



(*i*) (*ii*)

Fig. 8.6

Note that emitter is shown by an arrow which indicates the direction of conventional current flow with forward bias. For *npn* connection, it is clear that conventional current flows out of the emitter as indicated by the outgoing arrow in Fig. 8.6 (*i*). Similarly, for *pnp* connection, the conventional current flows into the emitter as indicated by inward arrow in Fig. 8.6 (*ii*).

8.6 Transistor Circuit as an Amplifier

A transistor raises the strength of a weak signal and thus acts as an amplifier. Fig. 8.7 shows the basic circuit of a transistor amplifier. The weak signal is applied between emitter-base junction and output is taken across the load R_C connected in the collector circuit. In order to achieve faithful amplification, the input circuit should always remain forward biased. To do so, a d.c. voltage V_{EE} is applied in the input circuit in addition to the signal as

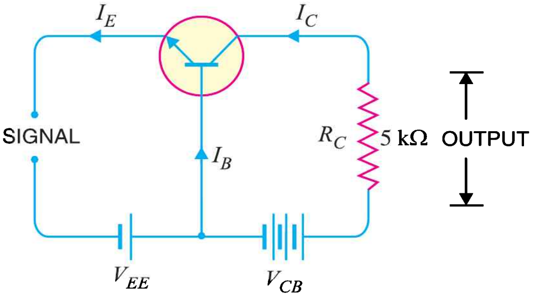


Fig. 8.7

shown. This d.c. voltage is known as bias voltage and its magnitude is such that it always keeps the input circuit forward biased regardless of the polarity of the signal.

As the input circuit has low resistance, therefore, a small change in signal voltage causes an appreciable change in emitter current. This causes almost the *same change in collector current due to transistor action. The collector current flowing through a high load resistance R_C produces a large voltage across it. Thus, a weak signal applied in the input circuit appears in the amplified form in the collector circuit. It is in this way that a transistor acts as an amplifier.

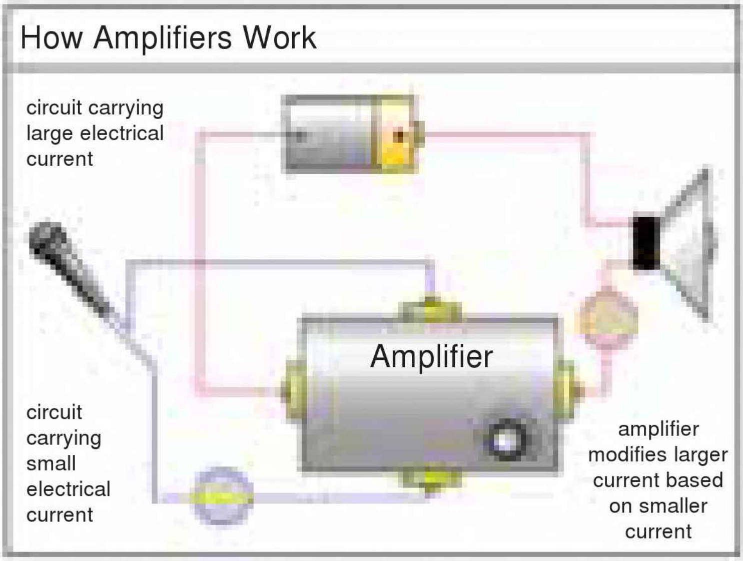

How Amplifiers Work
circuit carrying large electrical current
circuit carrying small electrical current
Amplifier
amplifier modifies larger current based on smaller current

Illustration. The action of a transistor as an amplifier can be made more illustrative if we consider typical circuit values. Suppose collector load resistance R_C = 5 kΩ. Let us further assume that a change of 0.1V in signal voltage produces a change of 1 mA in emitter current. Obviously, the change in collector current would also be approximately 1 mA. This collector current flowing through collector load R_C would produce a voltage = 5 kΩ × 1 mA = 5 V. Thus, a change of 0.1 V in the signal has caused a change of 5 V in the output circuit. In other words, the transistor has been able to raise the voltage level of the signal from 0.1 V to 5 V *i.e.* voltage amplification is 50.

Example 8.1. *A common base transistor amplifier has an input resistance of 20 Ω and output resistance of 100 kΩ. The collector load is 1 kΩ. If a signal of 500 mV is applied between emitter and base, find the voltage amplification. Assume α_{ac} to be nearly one.*

Solution. **Fig. 8.8 shows the conditions of the problem. Note that output resistance is very high as compared to input resistance. This is not surprising because input junction (base to emitter) of the transistor is forward biased while the output junction (base to collector) is reverse biased.

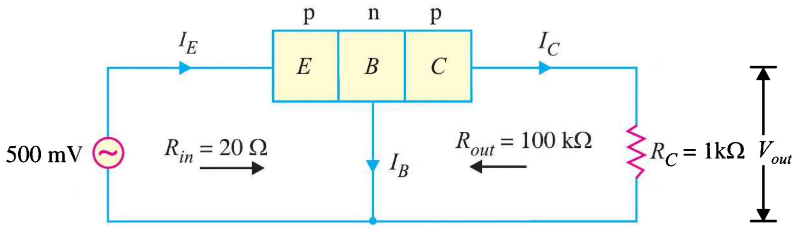


Fig. 8.8

---

[*] The reason is as follows. The collector-base junction is reverse biased and has a very high resistance of the order of mega ohms. Thus collector-base voltage has little effect on the collector current. This means that a large resistance R_C can be inserted in series with collector without disturbing the collector current relation to the emitter current *viz.* $I_C = \alpha I_E + I_{CBO}$. Therefore, collector current variations caused by a small base-emitter voltage fluctuations result in voltage changes in R_C that are quite high—often hundreds of times larger than the emitter-base voltage.

[**] The d.c. biasing is omitted in the figure because our interest is limited to amplification.

Input current, $I_E = \frac{\text{Signal}}{R_{in}} = \frac{500\text{ mV}}{20\ \Omega} = 25$ mA. Since α_{ac} is nearly 1, output current, $I_C = I_E =$ 25 mA.

$$\text{Output voltage, } V_{out} = I_C R_C = 25\text{ mA} \times 1\text{ k}\Omega = 25\text{ V}$$

$$\therefore \quad \text{Voltage amplification, } A_v = \frac{V_{out}}{\text{signal}} = \frac{25\,V}{500\,mV} = \mathbf{50}$$

Comments. The reader may note that basic amplifying action is produced by transferring a current from a *low-resistance* to a *high-resistance* circuit. Consequently, the name transistor is given to the device by combining the two terms given in magenta letters below :

Transfer + Res**istor** ⟶ **Transistor**

8.7 Transistor Connections

There are three leads in a transistor *viz.*, emitter, base and collector terminals. However, when a transistor is to be connected in a circuit, we require four terminals; two for the input and two for the output. This difficulty is overcome by making one terminal of the transistor common to both input and output terminals. The input is fed between this common terminal and one of the other two terminals. The output is obtained between the common terminal and the remaining terminal. Accordingly; a transistor can be connected in a circuit in the following three ways :

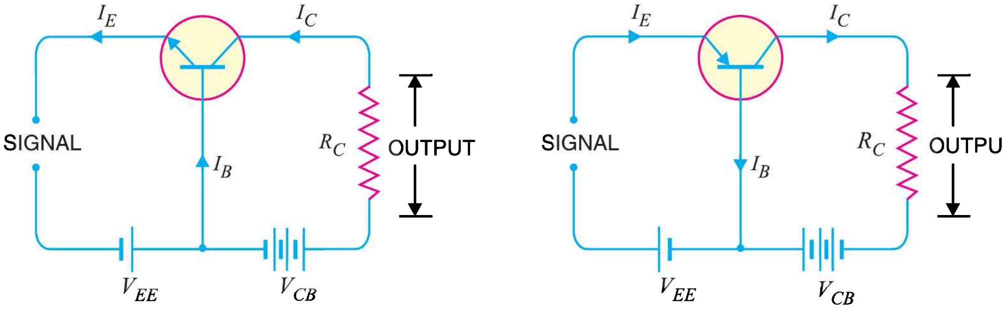
(*i*) common base connection (*ii*) common emitter connection

(*iii*) common collector connection

Each circuit connection has specific advantages and disadvantages. It may be noted here that regardless of circuit connection, the emitter is always biased in the forward direction, while the collector always has a reverse bias.

8.8 Common Base Connection

In this circuit arrangement, input is applied between emitter and base and output is taken from collector and base. Here, base of the transistor is common to both input and output circuits and hence the name common base connection. In Fig. 8.9 (*i*), a common base *npn* transistor circuit is shown whereas Fig. 8.9 (*ii*) shows the common base *pnp* transistor circuit.



(*i*) (*ii*)

Fig. 8.9

1. Current amplification factor (α). It is the ratio of output current to input current. In a common base connection, the input current is the emitter current I_E and output current is the collector current I_C.

The ratio of change in collector current to the change in emitter current at constant collector-base voltage V_{CB} is known as **current amplification factor** *i.e.*

$$*\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{CB}$$

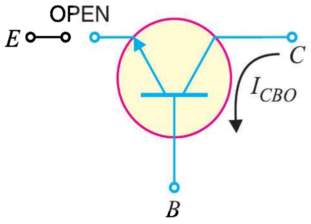


Fig. 8.10

It is clear that current amplification factor is less than **unity. This value can be increased (but not more than unity) by decreasing the base current. This is achieved by making the base thin and doping it lightly. Practical values of α in commercial transistors range from 0.9 to 0.99.

2. Expression for collector current. The whole of emitter current does not reach the collector. It is because a small percentage of it, as a result of electron-hole combinations occurring in base area, gives rise to base current. Moreover, as the collector-base junction is reverse biased, therefore, some leakage current flows due to minority carriers. It follows, therefore, that total collector current consists of :

(*i*) That part of emitter current which reaches the collector terminal *i.e.* ***αI_E.

(*ii*) The leakage current $I_{leakage}$. This current is due to the movement of minority carriers across base-collector junction on account of it being reverse biased. This is generally much smaller than αI_E.

$$\therefore \quad \text{Total collector current, } I_C = \alpha I_E + I_{leakage}$$

It is clear that if $I_E = 0$ (*i.e.*, emitter circuit is open), a small leakage current still flows in the collector circuit. This $I_{leakage}$ is abbreviated as I_{CBO}, meaning collector-base current with emitter open. The I_{CBO} is indicated in Fig. 8.10.

$$\therefore \quad I_C = \alpha I_E + I_{CBO} \quad \text{...}(i)$$

$$\text{Now} \quad I_E = I_C + I_B$$

$$\therefore \quad I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$\text{or} \quad I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$\text{or} \quad I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha} \quad \text{...}(ii)$$

Relation (*i*) or (*ii*) can be used to find I_C. It is further clear from these relations that the collector current of a transistor can be controlled by either the emitter or base current.

Fig. 8.11 shows the concept of I_{CBO}. In *CB* configuration, a small collector current flows even when the emitter current is zero. This is the leakage collector current (*i.e.* the collector current when emitter is open) and is denoted by I_{CBO}. When the emitter voltage V_{EE} is also applied, the various currents are as shown in Fig. 8.11 (*ii*).

Note. Owing to improved construction techniques, the magnitude of I_{CBO} for general-purpose and low-powered transistors (especially silicon transistors) is usually very small and may be neglected in calculations. However, for high power applications, it will appear in microampere range. Further, I_{CBO} is very much temperature dependent; it increases rapidly with the increase in temperature. Therefore, at higher temperatures, I_{CBO} plays an important role and must be taken care of in calculations.

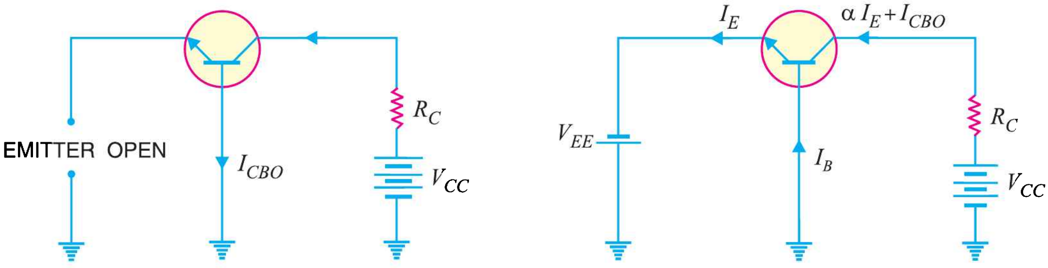
---

* If only d.c. values are considered, then $\alpha = I_C/I_E$.

** At first sight, it might seem that since there is no current gain, no voltage or power amplification could be possible with this arrangement. However, it may be recalled that output circuit resistance is much higher than the input circuit resistance. Therefore, it does give rise to voltage and power gain.

*** $$\alpha = \frac{I_C}{I_E} \quad \therefore \quad I_C = \alpha I_E$$

In other words, αI_E part of emitter current reaches the collector terminal.



(*i*) (*ii*)

Fig. 8.11

Example 8.2. *In a common base connection, $I_E = 1mA$, $I_C = 0.95mA$. Calculate the value of I_B.*

Solution. Using the relation, $I_E = I_B + I_C$

or $1 = I_B + 0.95$

$\therefore$ $I_B = 1 - 0.95 = \mathbf{0.05\ mA}$

Example 8.3. *In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.*

Solution. Here, $\alpha = 0.9, \quad I_E = 1$ mA

Now $\alpha = \dfrac{I_C}{I_E}$

or $I_C = \alpha I_E = 0.9 \times 1 = 0.9$ mA

Also $I_E = I_B + I_C$

$\therefore$ Base current, $I_B = I_E - I_C = 1 - 0.9 = \mathbf{0.1\ mA}$

Example 8.4. *In a common base connection, $I_C = 0.95$ mA and $I_B = 0.05$ mA. Find the value of α.*

Solution. We know $I_E = I_B + I_C = 0.05 + 0.95 = 1$ mA

$\therefore$ Current amplification factor, $\alpha = \dfrac{I_C}{I_E} = \dfrac{0.95}{1} = \mathbf{0.95}$

Example 8.5. *In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 μA. Find the total collector current. Given that $\alpha = 0.92$.*

Solution. Here, $I_E = 1$ mA, $\alpha = 0.92$, $I_{CBO} = 50\ \mu$A

$$\begin{aligned} \therefore \quad \text{Total collector current, } I_C &= \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3} \\ &= 0.92 + 0.05 = \mathbf{0.97\ mA} \end{aligned}$$

Example 8.6. *In a common base connection, $\alpha = 0.95$. The voltage drop across 2 kΩ resistance which is connected in the collector is 2V. Find the base current.*

Solution. Fig. 8.12 shows the required common base connection. The voltage drop across R_C (= 2 kΩ) is 2V.

$\therefore$ $I_C = 2\text{ V}/2\text{ k}\Omega = 1$ mA

Now $\alpha = I_C/I_E$

$$\therefore \quad I_E = \frac{I_C}{\alpha} = \frac{1}{0.95} = 1.05 \text{ mA}$$

Using the relation, $I_E = I_B + I_C$

$$\therefore \quad I_B = I_E - I_C = 1.05 - 1$$

$$= \mathbf{0.05\ mA}$$

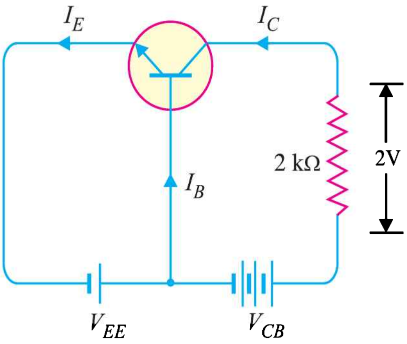


Fig. 8.12

Example 8.7. *For the common base circuit shown in Fig. 8.13, determine I_C and V_{CB}. Assume the transistor to be of silicon.*

Solution. Since the transistor is of silicon, $V_{BE} = 0.7$V. Applying Kirchhoff's voltage law to the emitter-side loop, we get,

$$V_{EE} = I_E R_E + V_{BE}$$

$$\text{or} \quad I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{8V - 0.7V}{1.5 \text{ k}\Omega} = 4.87 \text{ mA}$$

$$\therefore \quad I_C \simeq I_E = \mathbf{4.87\ mA}$$

Applying Kirchhoff's voltage law to the collector-side loop, we have,

$$V_{CC} = I_C R_C + V_{CB}$$

$$\therefore \quad V_{CB} = V_{CC} - I_C R_C$$

$$= 18 \text{ V} - 4.87 \text{ mA} \times 1.2 \text{ k}\Omega = \mathbf{12.16\ V}$$

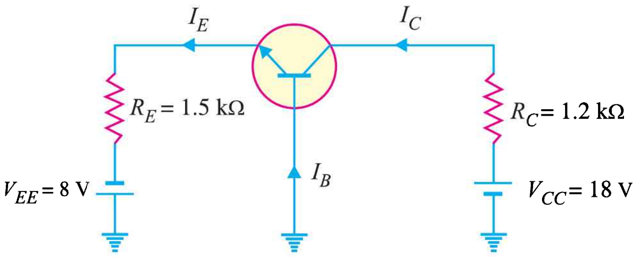


Fig. 8.13

8.9 Characteristics of Common Base Connection

The complete electrical behaviour of a transistor can be described by stating the interrelation of the various currents and voltages. These relationships can be conveniently displayed graphically and the curves thus obtained are known as the characteristics of transistor. The most important characteristics of common base connection are *input characteristics* and *output characteristics.*

1. Input characteristic. It is the curve between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}. The emitter current is generally taken along *y*-axis and emitter-base voltage along *x*-axis. Fig. 8.14 shows the input characteristics of a typical transistor in *CB* arrangement . The following points may be noted from these characteristics :

(*i*) The emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. It means that input resistance is very small.

(*ii*) The emitter current is almost independent of collector-base voltage V_{CB}. This leads to the conclusion that emitter current (and hence collector current) is almost independent of collector voltage.

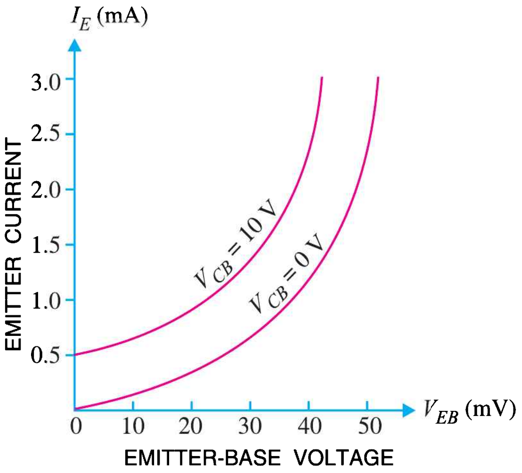


Fig. 8.14

Input resistance. It is the ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}) *i.e.*

$$\text{Input resistance, } r_i = \frac{\Delta V_{BE}}{\Delta I_E} \text{ at constant } V_{CB}$$

In fact, input resistance is the opposition offered to the signal current. As a very small V_{EB} is sufficient to produce a large flow of emitter current I_E, therefore, input resistance is quite small, of the order of a few ohms.

2. Output characteristic. It is the curve between collector current I_C and collector-base voltage V_{CB} at *constant emitter current I_E. Generally, collector current is taken along *y*-axis and collector-base voltage along *x*-axis. Fig. 8.15 shows the output characteristics of a typical transistor in *CB* arrangement.

The following points may be noted from the characteristics :

(*i*) The collector current I_C varies with V_{CB} only at very low voltages (< 1 V). The transistor is *never* operated in this region.

(*ii*) When the value of V_{CB} is raised above 1 – 2 V, the collector current becomes constant as indicated by straight horizontal curves. It means that now I_C is independent of V_{CB} and depends upon I_E only. This is consistent with the theory that the emitter current flows *almost* entirely to the collector terminal. The transistor is *always* operated in this region.

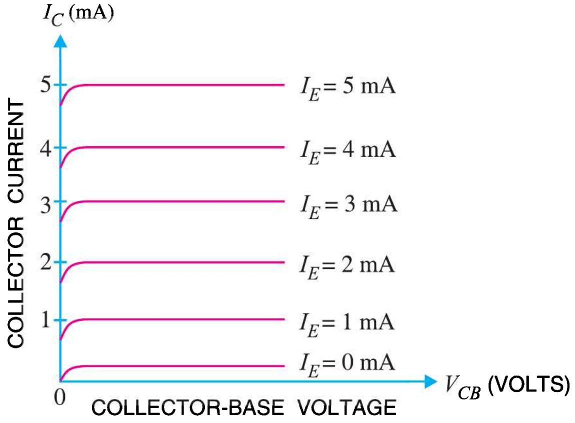


Fig. 8.15

(*iii*) A very large change in collector-base voltage produces only a tiny change in collector current. This means that output resistance is very high.

Output resistance. It is the ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current *i.e.*

$$\text{Output resistance, } r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

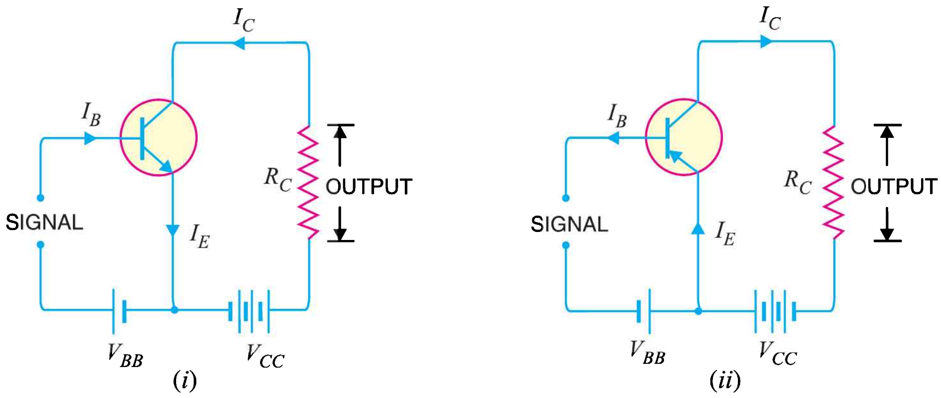
The output resistance of *CB* circuit is very high, of the order of several tens of kilo-ohms. This is not surprising because the collector current changes very slightly with the change in V_{CB}.

8.10 Common Emitter Connection

In this circuit arrangement, input is applied between base and emitter and output is taken from the collector and emitter. Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter connection. Fig. 8.16 (*i*) shows common emitter ***npn*** transistor circuit whereas Fig. 8.16 (*ii*) shows common emitter *pnp* transistor circuit.

---

* I_E has to be kept constant because any change in I_E will produce corresponding change in I_C. Here, we are interested to see how V_{CB} influences I_C.



(*i*) (*ii*)

Fig. 8.16

1. Base current amplification factor (β). In common emitter connection, input current is I_B and output current is I_C.

The ratio of change in collector current (ΔI_C) *to the change in base current* (ΔI_B) *is known as* **base current amplification factor** *i.e.*

$$\beta^* = \frac{\Delta I_C}{\Delta I_B}$$

In almost any transistor, less than 5% of emitter current flows as the base current. Therefore, the value of β is generally greater than 20. Usually, its value ranges from 20 to 500. This type of connection is frequently used as it gives appreciable current gain as well as voltage gain.

Relation between β and α. A simple relation exists between β and α. This can be derived as follows :

$$\beta = \frac{\Delta I_C}{\Delta I_B} \qquad ...(i)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad ...(ii)$$

Now $\quad I_E = I_B + I_C$

or $\quad \Delta I_E = \Delta I_B + \Delta I_C$

or $\quad \Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of ΔI_B in exp. (*i*), we get,

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} \qquad ...(iii)$$

Dividing the numerator and denominator of R.H.S. of exp. (*iii*) by ΔI_E, we get,

$$\beta = \frac{\Delta I_C / \Delta I_E}{\dfrac{\Delta I_E}{\Delta I_E} - \dfrac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1-\alpha} \qquad \left[\because \ \alpha = \frac{\Delta I_C}{\Delta I_E}\right]$$

$$\therefore \qquad \beta = \frac{\alpha}{1-\alpha}$$

It is clear that as α approaches unity, β approaches infinity. In other words, the current gain in common emitter connection is very high. It is due to this reason that this circuit arrangement is used in about 90 to 95 percent of all transistor applications.

---

* If d.c. values are considered, $\beta = I_C/I_B$.

2. Expression for collector current. In common emitter circuit, I_B is the input current and I_C is the output current.

We know $$I_E = I_B + I_C \qquad \text{...}(i)$$

and $$I_C = \alpha I_E + I_{CBO} \qquad \text{...}(ii)$$

From exp. (*ii*), we get, $$I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$$

or $$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

or $$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \qquad \text{...}(iii)$$

From exp. (*iii*), it is apparent that if $I_B = 0$ (*i.e.* base circuit is open), the collector current will be the current to the emitter. This is abbreviated as I_{CEO}, meaning collector-emitter current with base open.

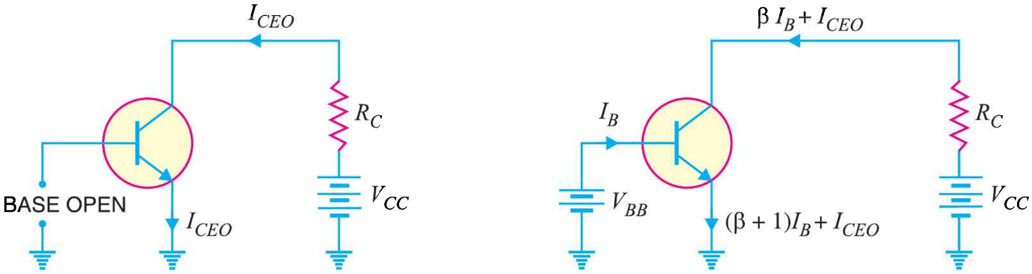
$$\therefore \qquad I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

Substituting the value of $\frac{1}{1-\alpha} I_{CBO} = I_{CEO}$ in exp. (*iii*), we get,

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$

or $$I_C = \beta I_B + I_{CEO} \qquad \left(\because \beta = \frac{\alpha}{1-\alpha}\right)$$

Concept of I_{CEO}. In *CE* configuration, a small collector current flows even when the base current is zero [See Fig. 8.17 (*i*)]. This is the collector cut off current (*i.e.* the collector current that flows when base is open) and is denoted by I_{CEO}. The value of I_{CEO} is much larger than I_{CBO}.



(*i*) (*ii*)

Fig. 8.17

When the base voltage is applied as shown in Fig. 8.17 (*ii*), then the various currents are :

Base current = I_B

Collector current = $\beta I_B + I_{CEO}$

Emitter current = Collector current + Base current

$$= (\beta I_B + I_{CEO}) + I_B = (\beta + 1) I_B + I_{CEO}$$

It may be noted here that :

$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO} = (\beta + 1) I_{CBO} \qquad \left[\because \frac{1}{1-\alpha} = \beta + 1\right]$$

8.11. Measurement of Leakage Current

A very small leakage current flows in all transistor circuits. However, in most cases, it is quite small and can be neglected.

(*i*) **Circuit for I_{CEO} test.** Fig. 8.18 shows the circuit for measuring I_{CEO}. Since base is open

($I_B = 0$), the transistor is in cut off. Ideally, $I_C = 0$ but actually there is a small current from collector to emitter due to minority carriers. It is called I_{CEO} (collector-to-emitter current with base open). This current is usually in the nA range for silicon. A faulty transistor will often have excessive leakage current.

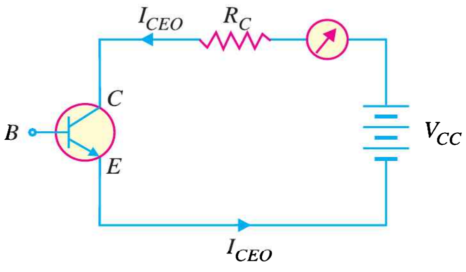


Fig. 8.18

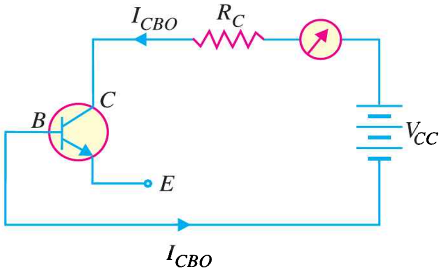


Fig. 8.19

(*ii*) Circuit for I_{CBO} test. Fig. 8.19 shows the circuit for measuring I_{CBO}. Since the emitter is open ($I_E = 0$), there is a small current from collector to base. This is called I_{CBO} (collector-to-base current with emitter open). This current is due to the movement of minority carriers across base-collector junction. The value of I_{CBO} is also small. If in measurement, I_{CBO} is excessive, then there is a possibility that collector-base is shorted.

Example 8.8. *Find the value of β if (i) α = 0.9 (ii) α = 0.98 (iii) α = 0.99.*

Solution. (*i*)

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.9}{1-0.9} = \mathbf{9}$$

(*ii*)

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = \mathbf{49}$$

(*iii*)

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = \mathbf{99}$$

Example 8.9. *Calculate I_E in a transistor for which β = 50 and I_B = 20 μA.*

Solution. Here $\beta = 50,\quad I_B = 20\mu\text{A} = 0.02\text{ mA}$

Now
$$\beta = \frac{I_C}{I_B}$$

$$\therefore \quad I_C = \beta I_B = 50 \times 0.02 = 1\text{ mA}$$

Using the relation, $I_E = I_B + I_C = 0.02 + 1 = \mathbf{1.02\ mA}$

Example 8.10. *Find the α rating of the transistor shown in Fig. 8.20. Hence determine the value of I_C using both α and β rating of the transistor.*

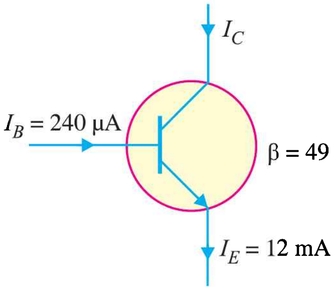


Fig. 8.20

Solution. Fig. 8.20 shows the conditions of the problem.

$$\alpha = \frac{\beta}{1+\beta} = \frac{49}{1+49} = \mathbf{0.98}$$

The value of I_C can be found by using either α or β rating as under :

$$I_C = \alpha I_E = 0.98\ (12\text{ mA}) = \mathbf{11.76\ mA}$$

Also $I_C = \beta I_B = 49\ (240\ \mu\text{A}) = \mathbf{11.76\ mA}$

Example 8.11. *For a transistor, β = 45 and voltage drop across 1kΩ which is connected in the collector circuit is 1 volt. Find the base current for common emitter connection.*

Solution. Fig. 8.21 shows the required common emitter connection. The voltage drop across R_C (= 1 kΩ) is 1volt.

$$\therefore \quad I_C = \frac{1\,V}{1\,k\Omega} = 1 \text{ mA}$$

$$\text{Now} \quad \beta = \frac{I_C}{I_B}$$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{1}{45} = \mathbf{0.022\ mA}$$

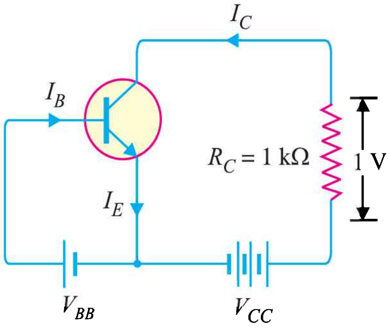


Fig. 8.21

Example 8.12. *A transistor is connected in common emitter (CE) configuration in which collector supply is 8V and the voltage drop across resistance R_C connected in the collector circuit is 0.5V. The value of R_C = 800 Ω. If α = 0.96, determine :*

(i) collector-emitter voltage

(ii) base current

Solution. Fig. 8.22 shows the required common emitter connection with various values.

(*i*) Collector-emitter voltage,

$$V_{CE} = V_{CC} - 0.5 = 8 - 0.5 = \mathbf{7.5\ V}$$

(*ii*) The voltage drop across R_C (= 800 Ω) is 0.5 V.

$$\therefore \quad I_C = \frac{0.5\text{ V}}{800\ \Omega} = \frac{5}{8}\text{ mA} = 0.625 \text{ mA}$$

$$\text{Now} \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24$$

$$\therefore \quad \text{Base current, } I_B = \frac{I_C}{\beta} = \frac{0.625}{24} = \mathbf{0.026\ mA}$$

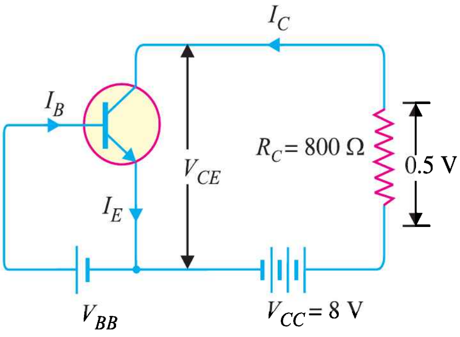
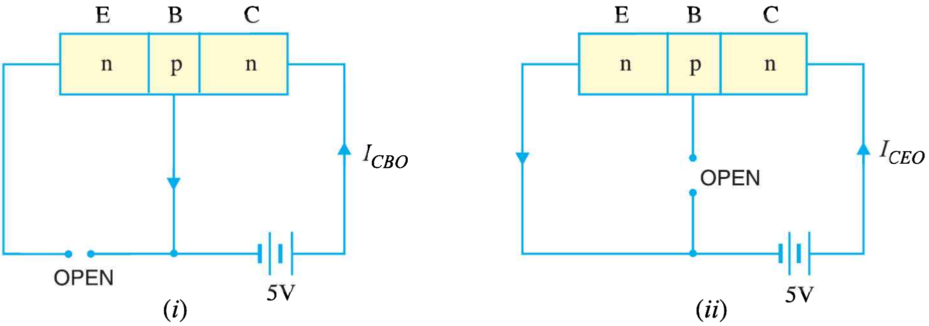


Fig. 8.22

Example 8.13. *An n-p-n transistor at room temperature has its emitter disconnected. A voltage of 5V is applied between collector and base. With collector positive, a current of 0.2 μA flows. When the base is disconnected and the same voltage is applied between collector and emitter, the current is found to be 20 μA. Find α, I_E and I_B when collector current is 1mA.*



(*i*) (*ii*)

Fig. 8.23

Solution. When the emitter circuit is open [See Fig. 8.23 (*i*)], the collector-base junction is reverse biased. A small leakage current I_{CBO} flows due to minority carriers.

$\therefore \quad I_{CBO} = 0.2\ \mu A$ ...*given*

When base is open [See Fig. 8.23 (*ii*)], a small leakage current I_{CEO} flows due to minority carriers.

$\therefore \quad I_{CEO} = 20\ \mu A$ . . . *given*

We know $\quad I_{CEO} = \dfrac{I_{CBO}}{1-\alpha}$

or $\quad 20 = \dfrac{0.2}{1-\alpha}$

$\therefore \quad \alpha = \mathbf{0.99}$

Now $\quad I_C = \alpha I_E + I_{CBO}$

Here $\quad I_C = 1\text{mA} = 1000\ \mu A\ ;\ \alpha = 0.99\ ;\ I_{CBO} = 0.2\ \mu A$

$\therefore \quad 1000 = 0.99 \times I_E + 0.2$

or $\quad I_E = \dfrac{1000 - 0.2}{0.99} = \mathbf{1010\ \mu A}$

and $\quad I_B = I_E - I_C = 1010 - 1000 = \mathbf{10\ \mu A}$

Example 8.14. *The collector leakage current in a transistor is 300 μA in CE arrangement. If now the transistor is connected in CB arrangement, what will be the leakage current? Given that β = 120.*

Solution. $\quad I_{CEO} = 300\ \mu A$

$$\beta = 120\ ;\ \alpha = \frac{\beta}{\beta+1} = \frac{120}{120+1} = 0.992$$

Now, $\quad I_{CEO} = \dfrac{I_{CBO}}{1-\alpha}$

$\therefore \quad I_{CBO} = (1-\alpha)\, I_{CEO} = (1 - 0.992) \times 300 = \mathbf{2.4\ \mu A}$

Note that leakage current in *CE* arrangement (*i.e.* I_{CEO}) is much more than in *CB* arrangement (*i.e.* I_{CBO}).

Example 8.15. *For a certain transistor,* $I_B = 20\ \mu A$; $I_C = 2\ mA$ *and* $\beta = 80$. *Calculate* I_{CBO}.

Solution.

$\quad I_C = \beta I_B + I_{CEO}$

or $\quad 2 = 80 \times 0.02 + I_{CEO}$

$\therefore \quad I_{CEO} = 2 - 80 \times 0.02 = 0.4\ \text{mA}$

Now $\quad \alpha = \dfrac{\beta}{\beta+1} = \dfrac{80}{80+1} = 0.988$

$\therefore \quad I_{CBO} = (1-\alpha)\, I_{CEO} = (1 - 0.988) \times 0.4 = \mathbf{0.0048\ mA}$

Example 8.16. *Using diagrams, explain the correctness of the relation* $I_{CEO} = (\beta + 1)\, I_{CBO}$.

Solution. The leakage current I_{CBO} is the current that flows through the base-collector junction when emitter is open as shown is Fig. 8.24. When the transistor is in *CE* arrangement, the *base current (*i.e.* I_{CBO}) is multiplied by β in the collector as shown in Fig. 8.25.

$\therefore \quad I_{CEO} = I_{CBO} + \beta I_{CBO} = (\beta + 1)\, I_{CBO}$

---

* The current I_{CBO} is amplified because it is forced to flow across the base-emitter junction.

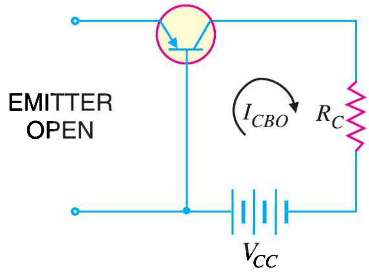

EMITTER
OPEN
I_{CBO}
R_C
V_{CC}

Fig. 8.24

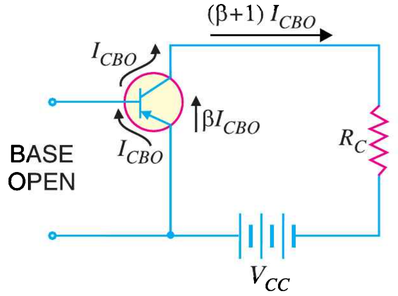
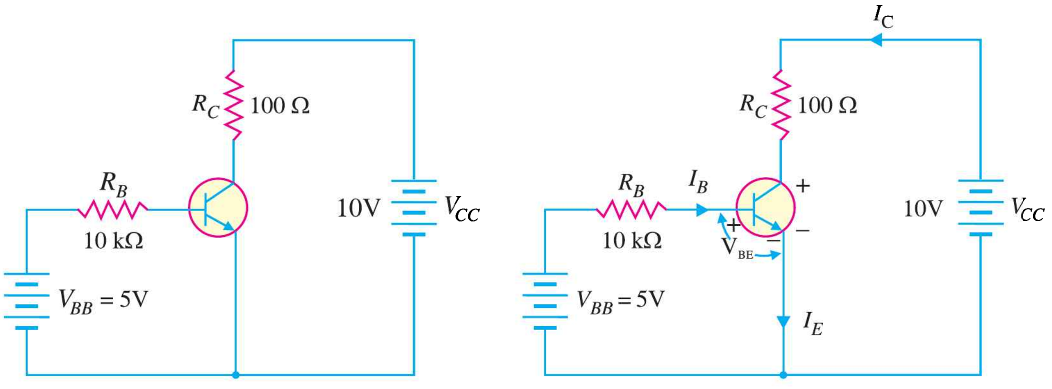

$(\beta+1)\ I_{CBO}$
I_{CBO}
βI_{CBO}
BASE
OPEN
I_{CBO}
R_C
V_{CC}

Fig. 8.25

Example 8.17 *Determine V_{CB} in the transistor * circuit shown in Fig. 8.26 (i). The transistor is of silicon and has $\beta = 150$.*


R_C
100 Ω
R_B
10 kΩ
10V
V_{CC}
$V_{BB} = 5V$
I_C
R_C
100 Ω
R_B
I_B
10 kΩ
+
−
+
−
V_{BE}
10V
V_{CC}
$V_{BB} = 5V$
I_E

(*i*) (*ii*)

Fig. 8.26

Solution. Fig. 8.26 (*i*) shows the transistor circuit while Fig. 8.26 (*ii*) shows the various currents and voltages along with polarities.

Applying Kirchhoff's voltage law to base-emitter loop, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

or $$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{10\ k\Omega} = 430\ \mu A$$

∴ $$I_C = \beta I_B = (150)(430\ \mu A) = 64.5\ mA$$

Now $$V_{CE} = V_{CC} - I_C R_C$$

$$= 10V - (64.5\ mA)\ (100\Omega) = 10V - 6.45V = 3.55V$$

We know that : $$V_{CE} = V_{CB} + V_{BE}$$

∴ $$V_{CB} = V_{CE} - V_{BE} = 3.55 - 0.7 = \mathbf{2.85V}$$

Example 8.18. *In a transistor, $I_B = 68\ \mu A$, $I_E = 30\ mA$ and $\beta = 440$. Determine the α rating of the transistor. Then determine the value of I_C using both the α rating and β rating of the transistor.*

Solution.

$$\alpha = \frac{\beta}{\beta+1} = \frac{440}{440+1} = \mathbf{0.9977}$$

---

* The resistor R_B controls the base current I_B and hence collector current I_C ($= \beta I_B$). If R_B is increased, the base current (I_B) decreases and hence collector current (I_C) will decrease and vice-versa.

$$I_C = \alpha I_E = (0.9977)\,(30 \text{ mA}) = \mathbf{29.93\ mA}$$

Also $$I_C = \beta I_B = (440)\,(68\ \mu\text{A}) = \mathbf{29.93\ mA}$$

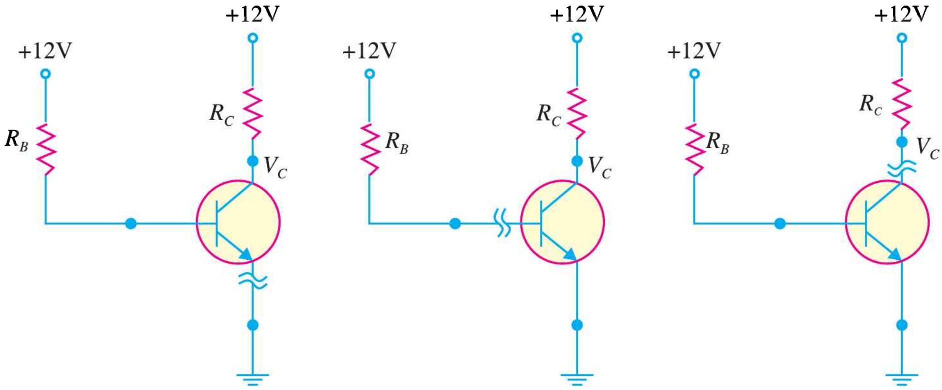
Example 8.19. *A transistor has the following ratings : $I_{C\,(max)}$ = 500 mA and β_{max} = 300. Determine the maximum allowable value of I_B for the device.*

Solution.

$$I_{B\,(max)} = \frac{I_{C\,(max)}}{\beta_{max}} = \frac{500 \text{ mA}}{300} = \mathbf{1.67\ mA}$$

For this transistor, if the base current is allowed to exceed 1.67 mA, the collector current will exceed its maximum rating of 500 mA and the transistor will probably be destroyed.

Example 8.20. *Fig. 8.27 shows the open circuit failures in a transistor. What will be the circuit behaviour in each case ?*



(*i*) (*ii*) (*iii*)

Fig. 8.27

Solution. *Fig 8.27 shows the open circuit failures in a transistor. We shall discuss the circuit behaviour in each case.

(*i*) **Open emitter.** Fig. 8.27 (*i*) shows an open emitter failure in a transistor. Since the collector diode is not forward biased, it is *OFF* and there can be neither collector current nor base current. Therefore, there will be no voltage drops across either resistor and the voltage at the base and at the collector leads of the transistor will be 12V.

(*ii*) **Open-base.** Fig. 8.27 (*ii*) shows an open base failure in a transistor. Since the base is open, there can be no base current so that the transistor is in *cut-off*. Therefore, all the transistor currents are 0A. In this case, the base and collector voltages will both be at 12V.

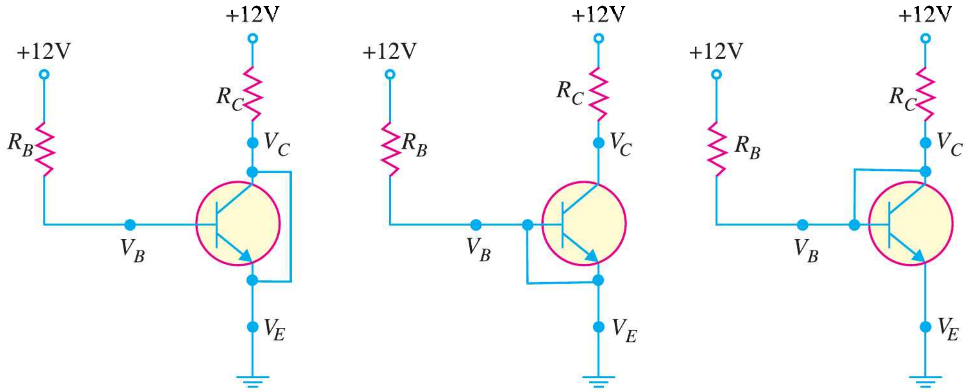
Note. It may be noted that an open failure at either the base or emitter will produce similar results.

(*iii*) **Open collector.** Fig. 8.27 (*iii*) shows an open collector failure in a transistor. In this case, the emitter diode is still *ON*, so we expect to see 0.7V at the base. However, we will see 12V at the collector because there is no collector current.

Example 8.21. *Fig. 8.28 shows the short circuit failures in a transistor. What will be the circuit behaviour in each case ?*

---

* The collector resistor R_C controls the collector voltage $V_C (= V_{CC} - I_C R_C)$. When R_C increases, V_C decreases and vice-versa.



(*i*) (*ii*) (*iii*)

Fig. 8.28

Solution. Fig. 8.28 shows the short circuit failures in a transistor. We shall discuss the circuit behaviour in each case.

(*i*) **Collector-emitter short.** Fig. 8.28 (*i*) shows a short between collector and emitter. The emitter diode is still forward biased, so we expect to see 0.7V at the base. Since the collector is shorted to the emitter, $V_C = V_E = 0$V.

(*ii*) **Base -emitter short.** Fig 8.28 (*ii*) shows a short between base and emitter. Since the base is now directly connected to ground, $V_B = 0$. Therefore, the current through R_B will be diverted to ground and there is no current to forward bias the emitter diode. As a result, the transistor will be *cut-off* and there is no collector current. So we will expect the collector voltage to be 12V.

(*iii*) **Collector-base short.** Fig. 8.28 (*iii*) shows a short between the collector and the base. In this case, the emitter diode is still forward biased so $V_B = 0.7$V. Now, however, because the collector is shorted to the base, $V_C = V_B = 0.7$V.

Note. The collector-emitter short is probably the most common type of fault in a transistor. It is because the collector current (I_C) and collector-emitter voltage (V_{CE}) are responsible for the major part of the power dissipation in the transistor. As we shall see (See Art. 8.23), the power dissipation in a transistor is mainly due to I_C and V_{CE} (*i.e.* $P_D = V_{CE} I_C$). Therefore, the transistor chip between the collector and the emitter is most likely to melt first.

8.12 Characteristics of Common Emitter Connection

The important characteristics of this circuit arrangement are the *input characteristics* and *output characteristics*.

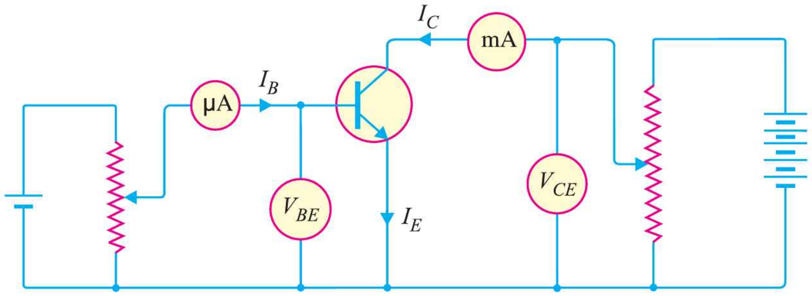


Fig. 8.29

1. Input characteristic. *It is the curve between base current* I_B *and base-emitter voltage* V_{BE} *at constant collector-emitter voltage* V_{CE}.

The input characteristics of a *CE* connection can be determined by the circuit shown in Fig. 8.29. Keeping V_{CE} constant (say at 10 V), note the base current I_B for various values of V_{BE}. Then plot the readings obtained on the graph, taking I_B along *y*-axis and V_{BE} along *x*-axis. This gives the input characteristic at V_{CE} = 10V as shown in Fig. 8.30. Following a similar procedure, a family of input characteristics can be drawn. The following points may be noted from the characteristics :

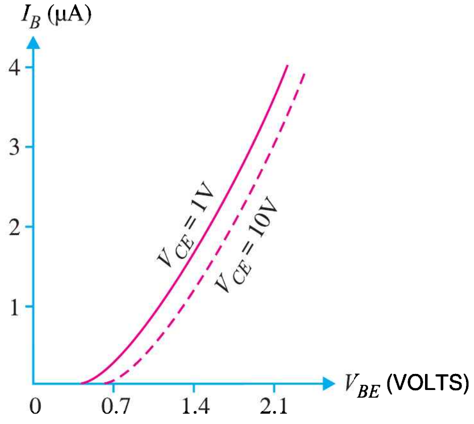


Fig. 8.30

(*i*) The characteristic resembles that of a forward biased diode curve. This is expected since the base-emitter section of transistor is a diode and it is forward biased.

(*ii*) As compared to *CB* arrangement, I_B increases less rapidly with V_{BE}. Therefore, input resistance of a *CE* circuit is higher than that of *CB* circuit.

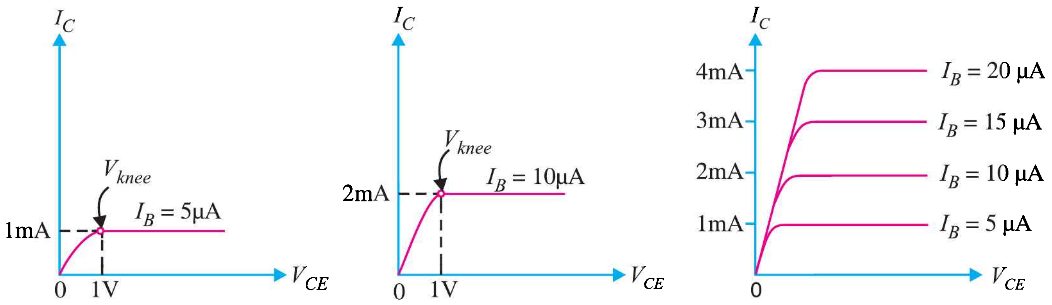
Input resistance. It is the ratio of change in base-emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant V_{CE} *i.e.*

$$\text{Input resistance,} \quad r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

The value of input resistance for a *CE* circuit is of the order of a few hundred ohms.

2. Output characteristic. *It is the curve between collector current* I_C *and collector-emitter voltage* V_{CE} *at constant base current* I_B.

The output characteristics of a *CE* circuit can be drawn with the help of the circuit shown in Fig. 8.29. Keeping the base current I_B fixed at some value say, 5 μA, note the collector current I_C for various values of V_{CE}. Then plot the readings on a graph, taking I_C along *y*-axis and V_{CE} along *x*-axis. This gives the output characteristic at I_B = 5 μA as shown in Fig. 8.31 (*i*). The test can be repeated for I_B = 10 μA to obtain the new output characteristic as shown in Fig. 8.31 (*ii*). Following similar procedure, a family of output characteristics can be drawn as shown in Fig. 8.31 (*iii*).



(*i*) (*ii*) (*iii*)

Fig. 8.31

The following points may be noted from the characteristics:

(*i*) The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V only. After this, collector current becomes *almost* constant and independent of V_{CE}. This value of V_{CE} upto which collector current I_C changes with V_{CE} is called the *knee voltage* (V_{knee}). *The transistors are always operated in the region above knee voltage.*

(*ii*) Above knee voltage, I_C is almost constant. However, a small increase in I_C with increasing V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority carriers before electron-hole combinations occur in the base area.

(*iii*) For any value of V_{CE} above knee voltage, the collector current I_C is approximately equal to $\beta \times I_B$.

Output resistance. It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B *i.e.*

$$\text{Output resistance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

It may be noted that whereas the output characteristics of *CB* circuit are horizontal, they have noticeable slope for the *CE* circuit. Therefore, the output resistance of a *CE* circuit is less than that of *CB* circuit. Its value is of the order of 50 kΩ.

8.13 Common Collector Connection

In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and collector. Here, collector of the transistor is common to both input and output circuits and hence the name common collector connection. Fig. 8.32 (*i*) shows common collector ***npn*** transistor circuit whereas Fig. 8.32 (*ii*) shows common collector ***pnp*** circuit.

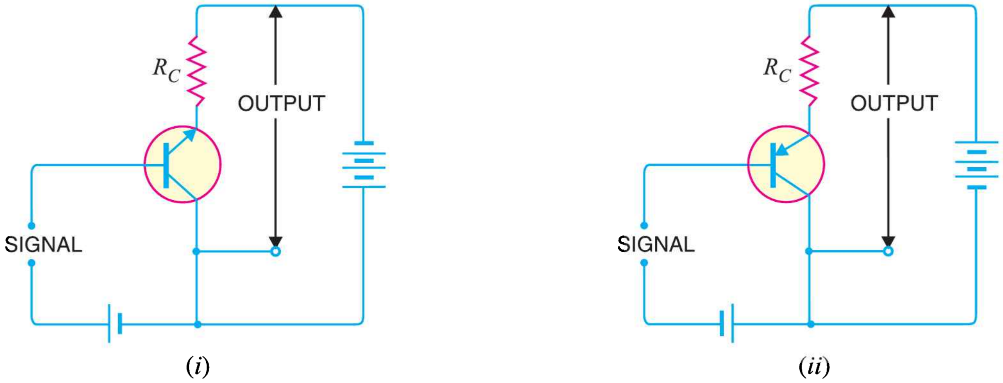


Fig. 8.32

(*i*) **Current amplification factor γ.** In common collector circuit, input current is the base current I_B and output current is the emitter current I_E. Therefore, current amplification in this circuit arrangement can be defined as under :

The ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as **current amplification factor** *in common collector (CC) arrangement i.e.*

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

This circuit provides about the same current gain as the common emitter circuit as $\Delta I_E \simeq \Delta I_C$. However, its voltage gain is always less than 1.

Relation between γ and α

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \quad \text{...}(i)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{...}(ii)$$

Now $$I_E = I_B + I_C$$

or $$\Delta I_E = \Delta I_B + \Delta I_C$$

or $$\Delta I_B = \Delta I_E - \Delta I_C$$

Substituting the value of ΔI_B in exp. (*i*), we get,

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator of R.H.S. by ΔI_E, we get,

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha} \qquad \left(\because \alpha = \frac{\Delta I_C}{\Delta I_E}\right)$$

$$\therefore \quad \gamma = \frac{1}{1-\alpha}$$

(*ii*) Expression for collector current

We know $$I_C = \alpha I_E + I_{CBO} \qquad \text{(See Art. 8.8)}$$

Also $$I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$$

$$\therefore \quad I_E (1 - \alpha) = I_B + I_{CBO}$$

or $$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

or $$I_C \simeq I_E = {}^*(\beta + 1) I_B + (\beta + 1) I_{CBO}$$

(*iii*) Applications. The common collector circuit has very high input resistance (about 750 kΩ) and very low output resistance (about 25 Ω). Due to this reason, the voltage gain provided by this circuit is always less than 1. Therefore, this circuit arrangement is seldom used for amplification. However, due to relatively high input resistance and low output resistance, this circuit is primarily used for impedance matching *i.e.* for driving a low impedance load from a high impedance source.

8.14 Comparison of Transistor Connections

The comparison of various characteristics of the three connections is given below in the tabular form.

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

The following points are worth noting about transistor arrangements :

---

* $\beta = \frac{\alpha}{1-\alpha} \quad \therefore \quad \beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{1}{1-\alpha}$

***(i)* CB Circuit.** The input resistance (r_i) of *CB* circuit is low because I_E is high. The output resistance (r_o) is high because of reverse voltage at the collector. It has no current gain ($\alpha < 1$) but voltage gain can be high. The *CB* circuit is seldom used. The only advantage of *CB* circuit is that it provides good stability against increase in temperature.

***(ii)* CE Circuit.** The input resistance (r_i) of a *CE* circuit is high because of small I_B. Therefore, r_i for a *CE* circuit is much higher than that of *CB* circuit. The output resistance (r_o) of *CE* circuit is smaller than that of *CB* circuit. The current gain of *CE* circuit is large because I_C is much larger than I_B. The voltage gain of *CE* circuit is larger than that of *CB* circuit. The *CE* circuit is generally used because it has the best combination of voltage gain and current gain. The disadvantage of *CE* circuit is that the leakage current is amplified in the circuit, but bias stabilisation methods can be used.

***(iii)* CC Circuit.** The input resistance (r_i) and output resistance (r_o) of *CC* circuit are respectively high and low as compared to other circuits. There is no voltage gain ($A_v < 1$) in a *CC* circuit. This circuit is often used for impedance matching.

8.15 Commonly Used Transistor Connection

Out of the three transistor connections, the common emitter circuit is the most efficient. It is used in about 90 to 95 per cent of all transistor applications. The main reasons for the widespread use of this circuit arrangement are :

***(i)* High current gain.** In a common emitter connection, I_C is the output current and I_B is the input current. In this circuit arrangement, collector current is given by :

$$I_C = \beta I_B + I_{CEO}$$

As the value of β is very large, therefore, the output current I_C is much more than the input current I_B. Hence, the current gain in *CE* arrangement is very high. It may range from 20 to 500.

***(ii)* High voltage and power gain.** Due to high current gain, the common emitter circuit has the highest voltage and power gain of three transistor connections. This is the major reason for using the transistor in this circuit arrangement.

***(iii)* Moderate output to input impedance ratio.** In a common emitter circuit, the ratio of output impedance to input impedance is small (about 50). This makes this circuit arrangement an ideal one for coupling between various transistor stages. However, in other connections, the ratio of output impedance to input impedance is very large and hence coupling becomes highly inefficient due to gross mismatching.

8.16 Transistor as an Amplifier in *CE* Arrangement

Fig. 8.33 shows the common emitter ***npn*** amplifier circuit. Note that a battery V_{BB} is connected in the input circuit in addition to the signal voltage. This d.c. voltage is known as *bias voltage* and its magnitude is such that it always keeps the emitter-base junction forward *biased regardless of the polarity of the signal source.

Operation. During the positive half-cycle of the **signal, the forward bias across the emitter-base junction is increased. Therefore, more electrons flow from the emitter to the collector *via* the base. This causes an increase in collector current. The increased collector current produces a greater voltage drop across the collector load resistance R_C. However, during the negative half-cycle of the signal, the forward bias across emitter-base junction is decreased. Therefore, collector current decreases. This results in the decreased output voltage (in the opposite direction). Hence, an amplified output is obtained across the load.

---

* If d.c. bias voltage is not provided, then during negative half-cycle of the signal, the emitter-base junction will be reverse biased. This will upset the transistor action.

** Throughout the book, we shall use sine wave signals because these are convenient for testing amplifiers. But it must be realised that signals (*e.g.* speech, music etc.) with which we work are generally complex having little resemblance to a sine wave. However, fourier series analysis tells us that such complex signals may be expressed as a sum of sine waves of various frequencies.

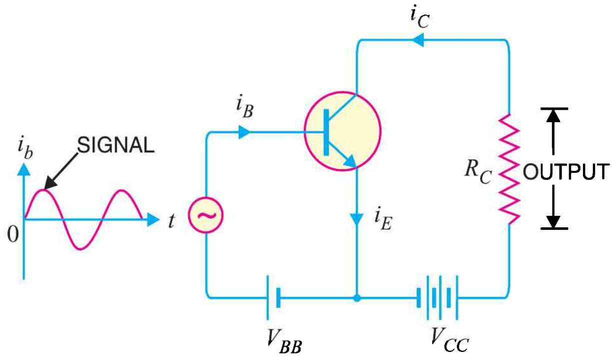


Fig. 8.33

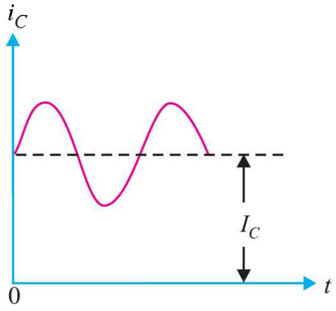


Fig. 8.34

Analysis of collector currents. When no signal is applied, the input circuit is forward biased by the battery V_{BB}. Therefore, a d.c. collector current I_C flows in the collector circuit. This is called *zero signal collector current*. When the signal voltage is applied, the forward bias on the emitter-base junction increases or decreases depending upon whether the signal is positive or negative. During the positive half-cycle of the signal, the forward bias on emitter-base junction is increased, causing total collector current i_C to increase. Reverse will happen for the negative half-cycle of the signal.

Fig. 8.34 shows the graph of total collector current i_C versus time. From the graph, it is clear that total collector current consists of two components, namely ;

(*i*) The d.c. collector current I_C (zero signal collector current) due to bias battery V_{BB}. This is the current that flows in the collector in the absence of signal.

(*ii*) The a.c. collector current i_c due to signal.

∴ Total collector current, $i_C = i_c + I_C$

The useful output is the voltage drop across collector load R_C due to the a.c. component i_c. The purpose of zero signal collector current is to ensure that the emitter-base junction is forward biased at all times. The table below gives the symbols usually employed for currents and voltages in transistor applications.

S. No.	Particular	Instantaneous a.c.	d.c.	Total
1.	Emitter current	i_e	I_E	i_E
2.	Collector current	i_c	I_C	i_C
3.	Base current	i_b	I_B	i_B
4.	Collector-emitter voltage	v_{ce}	V_{CE}	v_{CE}
5.	Emitter-base voltage	v_{eb}	V_{EB}	v_{EB}

8.17 Transistor Load Line Analysis

In the transistor circuit analysis, it is generally required to determine the collector current for various collector-emitter voltages. One of the methods can be used to plot the output characteristics and determine the collector current at any desired collector-emitter voltage. However, a more convenient method, known as *load line method* can be used to solve such problems. As explained later in this section, this method is quite easy and is frequently used in the analysis of transistor applications.

d.c. load line. Consider a common emitter *npn* transistor circuit shown in Fig. 8.35 (*i*) where no signal is applied. Therefore, d.c. conditions prevail in the circuit. The output characteristics of this circuit are shown in Fig. 8.35 (*ii*).

The value of collector-emitter voltage V_{CE} at any time is given by ;

$$V_{CE} = V_{CC} - I_C R_C \qquad ...(i)$$

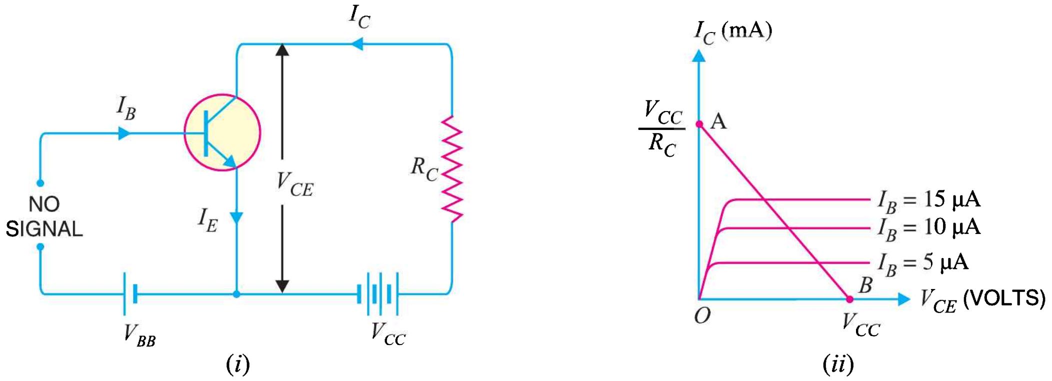


Fig. 8.35

As V_{CC} and R_C are fixed values, therefore, it is a first degree equation and can be represented by a straight line on the output characteristics. This is known as *d.c. load line* and determines the locus of $V_{CE} - I_C$ points for any given value of R_C. To add load line, we need two end points of the straight line. These two points can be located as under :

(*i*) When the collector current $I_C = 0$, then collector-emitter voltage is maximum and is equal to V_{CC} *i.e.*

$$\text{Max. } V_{CE} = V_{CC} - I_C R_C$$
$$= V_{CC} \qquad (\because I_C = 0)$$

This gives the first point B ($OB = V_{CC}$) on the collector-emitter voltage axis as shown in Fig. 8.35 (*ii*).

(*ii*) When collector-emitter voltage $V_{CE} = 0$, the collector current is maximum and is equal to V_{CC}/R_C *i.e.*

$$V_{CE} = V_{CC} - I_C R_C$$

or
$$0 = V_{CC} - I_C R_C$$

$\therefore$
$$\text{Max. } I_C = V_{CC}/R_C$$

This gives the second point A ($OA = V_{CC}/R_C$) on the collector current axis as shown in Fig. 8.35 (*ii*). By joining these two points, d.c. *load line AB is constructed.

Importance. The current (I_C) and voltage (V_{CE}) conditions in the transistor circuit are represented by some point on the output characteristics. The same information can be obtained from the load line. Thus when I_C is maximum (= V_{CC}/R_C), then $V_{CE} = 0$ as shown in Fig. 8.36. If $I_C = 0$, then V_{CE} is maximum

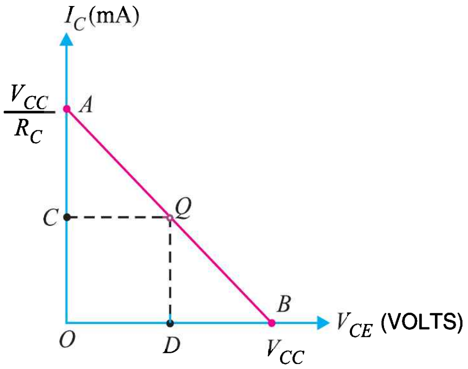


Fig. 8.36

---

* **Why load line ?** The resistance R_C connected to the device is called load or load resistance for the circuit and, therefore, the line we have just constructed is called the load line.

and is equal to V_{CC}. For any other value of collector current say OC, the collector-emitter voltage V_{CE} = OD. It follows, therefore, that load line gives a far more convenient and direct solution to the problem.

Note. If we plot the load line on the output characteristic of the transistor, we can investigate the behaviour of the transistor amplifier. It is because we have the transistor output current and voltage specified in the form of load line equation and the transistor behaviour itself specified implicitly by the output characteristics.

8.18 Operating Point

The zero signal values of I_C *and* V_{CE} *are known as the* **operating point**.

It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied. It is also called quiescent (silent) point or *Q-point* because it is the point on $I_C - V_{CE}$ characteristic when the transistor is silent *i.e.* in the absence of the signal.

Suppose in the absence of signal, the base current is 5 μA. Then I_C and V_{CE} conditions in the circuit must be represented by some point on I_B = 5 μA characteristic. But I_C and V_{CE} conditions in the circuit should also be represented by some point on the d.c. load line AB. The point Q where the load line and the characteristic intersect is the only point which satisfies both these conditions. Therefore, the point Q describes the actual state of affairs in the circuit in the zero signal conditions and is called the operating point. Referring to Fig. 8.37, for I_B = 5 μA, the zero signal values are :

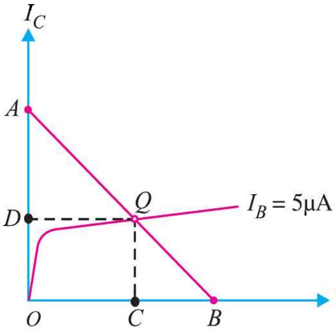


Fig. 8.37

$$V_{CE} = OC \text{ volts}$$
$$I_C = OD \text{ mA}$$

It follows, therefore, that the zero signal values of I_C and V_{CE} (*i.e.* operating point) are determined by the point where d.c. load line intersects the proper base current curve.

Example 8.22. *For the circuit shown in Fig. 8.38 (i), draw the d.c. load line.*

Solution. The collector-emitter voltage V_{CE} is given by ;

$$V_{CE} = V_{CC} - I_C R_C \quad \text{...}(i)$$

When I_C = 0, then,

$$V_{CE} = V_{CC} = 12.5 \text{ V}$$

This locates the point B of the load line on the collector-emitter voltage axis.

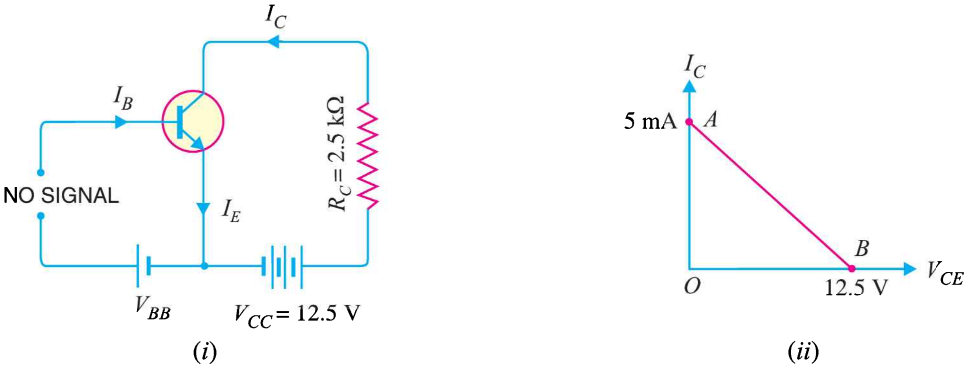


Fig. 8.38

When $V_{CE} = 0$, then,

$$I_C = V_{CC}/R_C = 12.5 \text{ V}/2.5 \text{ k}\Omega = 5 \text{ mA}$$

This locates the point *A* of the load line on the collector current axis. By joining these two points, we get the d.c. load line *AB* as shown in Fig. 8.38 (*ii*).

Example 8.23. *In the circuit diagram shown in Fig. 8.39 (i), if V_{CC} = 12V and R_C = 6 kΩ, draw the d.c. load line. What will be the Q point if zero signal base current is 20μA and β = 50 ?*

Solution. The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$, $V_{CE} = V_{CC} = 12$ V. This locates the point *B* of the load line. When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 12 \text{ V}/6 \text{ k}\Omega = 2$ mA. This locates the point *A* of the load line. By joining these two points, load line *AB* is constructed as shown in Fig. 8.39 (*ii*).

Zero signal base current, I_B = 20 μA = 0.02 mA

Current amplification factor, β = 50

∴ Zero signal collector current, $I_C = \beta I_B = 50 \times 0.02 = 1$ mA

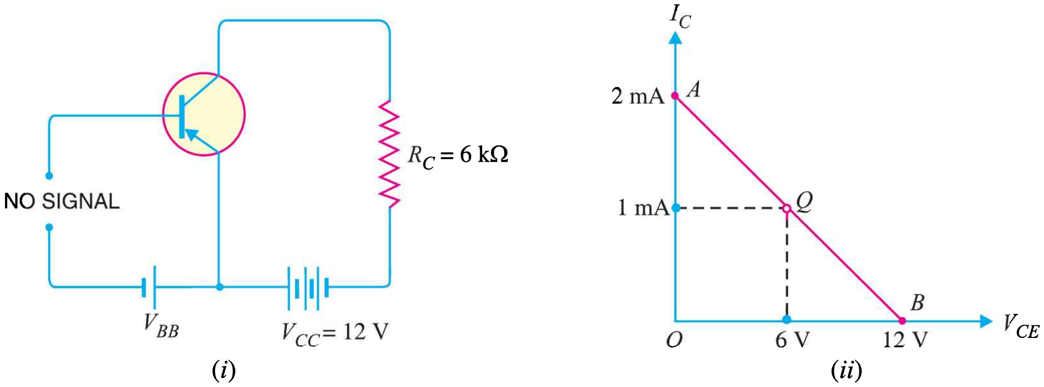


Fig. 8.39

Zero signal collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 12 - 1 \text{ mA} \times 6 \text{ k}\Omega = 6 \text{ V}$$

∴ Operating point is **6 V, 1 mA**.

Fig. 8.39 (*ii*) shows the *Q* point. Its co-ordinates are I_C = 1 mA and V_{CE} = 6 V.

Example 8.24. *In a transistor circuit, collector load is 4 kΩ whereas quiescent current (zero signal collector current) is 1mA.*

(i) What is the operating point if V_{CC} = 10 V ?

(ii) What will be the operating point if R_C = 5 kΩ ?

Solution. V_{CC} = 10 V, I_C = 1 mA

(*i*) When collector load R_C = 4 kΩ, then,

$$V_{CE} = V_{CC} - I_C R_C = 10 - 1 \text{ mA} \times 4 \text{ k}\Omega = 10 - 4 = 6 \text{ V}$$

∴ Operating point is **6 V, 1 mA**.

(*ii*) When collector load R_C = 5 kΩ, then,

$$V_{CE} = V_{CC} - I_C R_C = 10 - 1 \text{ mA} \times 5 \text{ k}\Omega = 10 - 5 = 5 \text{ V}$$

∴ Operating point is **5 V, 1 mA**.

Example 8.25. *Determine the Q point of the transistor circuit shown in Fig. 8.40. Also draw the d.c. load line. Given β = 200 and V_{BE} = 0.7V.*

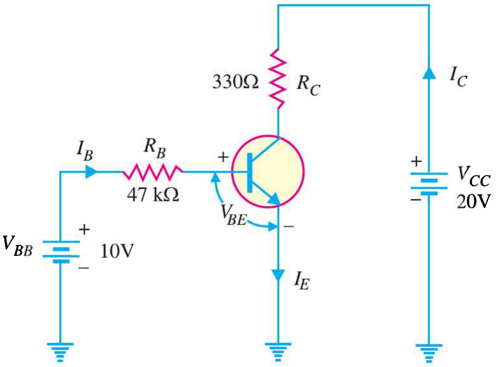


Fig 8.40

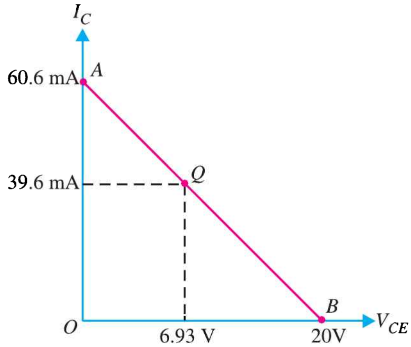


Fig. 8.41

Solution. The presence of resistor R_B in the base circuit should not disturb you because we can apply Kirchhoff's voltage law to find the value of I_B and hence I_C (= βI_B). Referring to Fig. 8.40 and applying Kirchhoff's voltage law to base-emitter loop, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\therefore \qquad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10V - 0.7V}{47\ k\Omega} = 198\ \mu A$$

Now $\qquad I_C = \beta I_B = (200)(198\ \mu A) = 39.6$ mA

Also $\qquad V_{CE} = V_{CC} - I_C R_C = 20V - (39.6mA)(330\ \Omega) = 20V - 13.07V = 6.93V$

Therefore, the Q-point is I_C = **39.6 mA** and V_{CE} = **6.93V.**

D.C. load line. In order to draw the d.c. load line, we need two end points.

$$V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$, $V_{CE} = V_{CC} = 20V$. This locates the point *B* of the load line on the collector-emitter voltage axis as shown in Fig. 8.41. When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 20V/330\Omega = 60.6$ mA. This locates the point *A* of the load line on the collector current axis. By joining these two points, d.c. load line *AB* is constructed as shown in Fig. 8.41.

Example 8.26. *Determine the Q point of the transistor circuit shown in *Fig. 8.42. Also draw the d.c. load line. Given $\beta = 100$ and $V_{BE} = 0.7V$.*

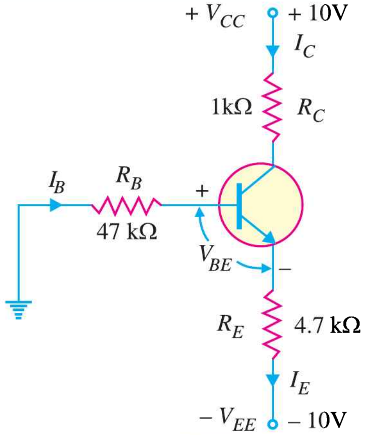


Fig. 8.42

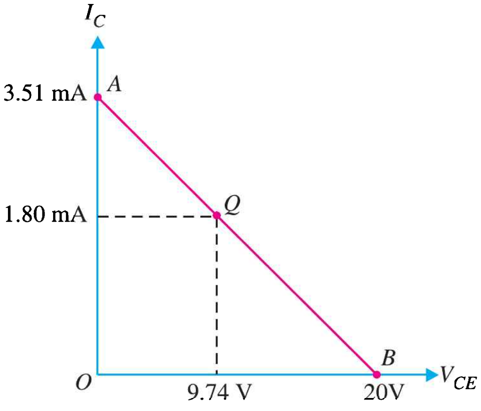


Fig. 8.43

---

* The presence of two power supplies has an effect on the baisc equations for I_C and V_{CE} used for single power supply (*i.e.* V_{CC}). Normally, the two supply voltages will be equal. For example, if V_{CC} = + 10V (d.c.), then V_{EE} = – 10 V (d.c.).

Solution. The transistor circuit shown in Fig. 8.42 may look complex but we can easily apply Kirchhoff's voltage law to find the various voltages and currents in the * circuit.

Applying Kirchhoff's voltage law to the base-emitter loop, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0 \quad \text{or} \quad V_{EE} = I_B R_B + I_E R_E + V_{BE}$$

Now $I_C = \beta I_B$ and $I_C \simeq I_E$. $\therefore$ $I_B = I_E/\beta$. Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $$I_E\left(\frac{R_B}{\beta} + R_E\right) = V_{EE} - V_{BE} \quad \text{or} \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, $$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{10\text{V} - 0.7\text{V}}{4.7\text{ k}\Omega + 47\text{ k}\Omega/100} = \frac{9.3\text{ V}}{5.17\text{ k}\Omega} = 1.8\text{ mA}$$

Applying Kirchhoff's voltage law to the collector side, we have,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C(R_C + R_E) \qquad (\because I_E \simeq I_C)$$

$$= 10\text{V} + 10\text{V} - 1.8\text{ mA}\,(1\text{ k}\Omega + 4.7\text{ k}\Omega) = 9.74\text{V}$$

Therefore, the operating point of the circuit is I_C = **1.8 mA** and V_{CE} = **9.74V.**

D.C. load line. The d.c. load line can be constructed as under :

$$V_{CE} = V_{CC} + V_{EE} - I_C(R_C + R_E)$$

When $I_C = 0$; $V_{CE} = V_{CC} + V_{EE} = 10\text{V} + 10\text{V} = 20\text{V}$. This locates the first point B (OB = 20V) of the load line on the collector-emitter voltage axis. When $V_{CE} = 0$,

$$I_C = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{10V + 10V}{1\,k\Omega + 4.7\,k\Omega} = \frac{20V}{5.7\,k\Omega} = 3.51\text{ mA}$$

This locates the second point A (OA = 3.51 mA) of the load line on the collector current axis. By joining points A and B, d.c. load line AB is constructed as shown in Fig. 8.43.

Example 8.27. *In the above example, find (i) emitter voltage w.r.t. ground (ii) base voltage w.r.t. ground (iii) collector voltage w.r.t. ground.*

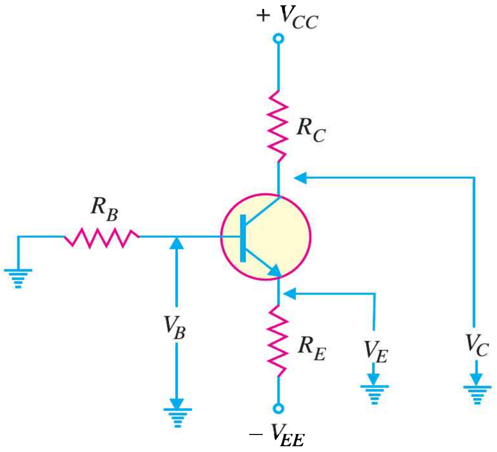


Fig. 8.44

---

* The emitter resistor R_E provides stabilisation of Q-point (See Art. 9.12).

Solution. Refer to Fig. 8.44.

(*i*) The emitter voltage w.r.t. ground is

$$V_E = -V_{EE} + I_E R_E = -10\text{V} + 1.8\text{ mA} \times 4.7\text{ k}\Omega = \mathbf{-1.54V}$$

(*ii*) The base voltage w.r.t. ground is

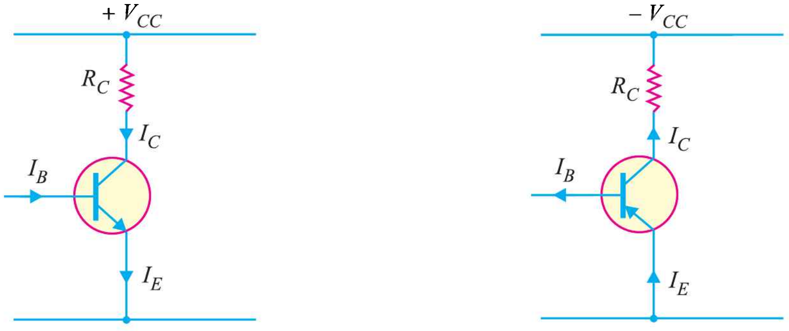
$$V_B = V_E + V_{BE} = 10\text{V} + 0.7\text{V} = \mathbf{10.7V}$$

(*iii*) The collector voltage w.r.t. ground is

$$V_C = V_{CC} - I_C R_C = 10\text{V} - 1.8\text{ mA} \times 1\text{ k}\Omega = \mathbf{8.2V}$$

8.19 Practical Way of Drawing CE Circuit

The common emitter circuits drawn so far can be shown in another convenient way. Fig. 8.45 shows the practical way of drawing *CE* circuit. In Fig. 8.45 (*i*), the practical way of drawing common emitter *npn* circuit is shown. Similarly, Fig. 8.45 (*ii*) shows the practical way of drawing common emitter *pnp* circuit. In our further discussion, we shall often use this scheme of presentation.



(*i*) (*ii*)

Fig. 8.45

8.20 Output from Transistor Amplifier

A transistor raises the strength of a weak signal and thus acts as an amplifier. Fig. 8.46 shows the common emitter amplifier. There are two ways of taking output from this transistor connection. The output can be taken either across R_C or across terminals 1 and 2. In either case, the magnitude of output is the same. This is clear from the following discussion :

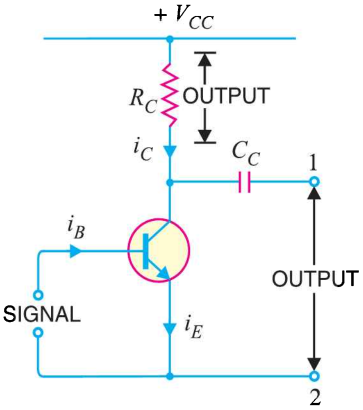


Fig. 8.46

(*i*) **First method.** We can take the output directly by putting a load resistance R_C in the collector circuit *i.e.*

Output = voltage across R_C = $i_c R_C$ ...(*i*)

This method of taking output from collector load is used only in single stage of amplification.

(*ii*) **Second method.** The output can also be taken across terminals 1 and 2 *i.e.* from collector and emitter end of supply.

Output = Voltage across terminals 1 and 2

= $V_{CC} - i_c R_C$

As V_{CC} is a direct voltage and cannot pass through capacitor C_C, therefore, only varying voltage $i_c R_C$ will appear across terminals 1 and 2.

∴ Output = $-i_c R_C$ ...(*ii*)

From exps. (*i*) and (*ii*), it is clear that magnitude of output is the same whether we take output across collector load or terminals 1 and 2. The minus sign in exp. (*ii*) simply indicates the phase reversal. The second method of taking output is used in multistages of amplification.

8.21 Performance of Transistor Amplifier

The performance of a transistor amplifier depends upon input resistance, output resistance, effective collector load, current gain, voltage gain and power gain. As *common emitter connection* is universally adopted, therefore, we shall explain these terms with reference to this mode of connection.

(*i*) Input resistance. *It is the ratio of small change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage i.e.*

$$\text{Input resistance, } R_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

The value of input resistance is quite small because the input circuit is always forward biased. It ranges from 500 Ω for small low powered transistors to as low as 5 Ω for high powered transistors. In fact, input resistance is the opposition offered by the base-emitter junction to the signal flow. Fig. 8.47 shows the general form of an amplifier. The input voltage V_{BE} causes an input current I_B.

$$\therefore \quad \text{Input resistance, } R_i = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{V_{BE}}{I_B}$$

Thus if the input resistance of an amplifier is 500 Ω and the signal voltage at any instant is 1 V, then,

$$\text{Base current, } i_b = \frac{1\,V}{500\,\Omega} = 2\text{ mA}$$

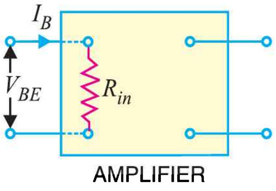


Fig. 8.47

(*ii*) Output resistance. *It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current i.e.*

$$\text{Output resistance, } R_O = \frac{\Delta V_{CE}}{\Delta I_C}$$

The output characteristics reveal that collector current changes very slightly with the change in collector-emitter voltage. Therefore, output resistance of a transistor amplifier is very high– of the order of several hundred kilo-ohms. The physical explanation of high output resistance is that collector-base junction is reverse biased.

(*iii*) Effective collector load. *It is the total load as seen by the a.c. collector current.*

In case of single stage amplifiers, the effective collector load is a parallel combination of R_C and R_O as shown in Fig. 8.48 (*i*).

$$\text{Effective collector load, } R_{AC} = R_C \parallel R_O$$

$$= \frac{R_C \times R_O}{R_C + R_O} = {}^*R_C$$

It follows, therefore, that for a single stage amplifier, effective load is equal to collector load R_C.

However, in a multistage amplifier (*i.e.* having more than one amplification stage), the input resistance R_i of the next stage also comes into picture as shown in Fig. 8.48 (*ii*). Therefore, effective collector load becomes parallel combination of R_C, R_O and R_i *i.e.*

$$\text{Effective collector load, } R_{AC} = R_C \parallel R_O \parallel R_i$$

---

* As output resistance R_O is several times R_C, therefore, R_C can be neglected as compared to R_O.

$$R_{AC} = \frac{R_C \times R_O}{R_O} = R_C$$

$$= {}^*R_C \parallel R_i = \frac{R_C\,R_i}{R_C + R_i}$$

As input resistance R_i is quite small (25 Ω to 500 Ω), therefore, effective load is reduced.

(*iv*) **Current gain.** *It is the ratio of change in collector current* (ΔI_C) *to the change in base current* (ΔI_B) *i.e.*

$$\text{Current gain, } \beta = \frac{\Delta I_C}{\Delta I_B}$$

The value of β ranges from 20 to 500. The current gain indicates that input current becomes β times in the collector circuit.

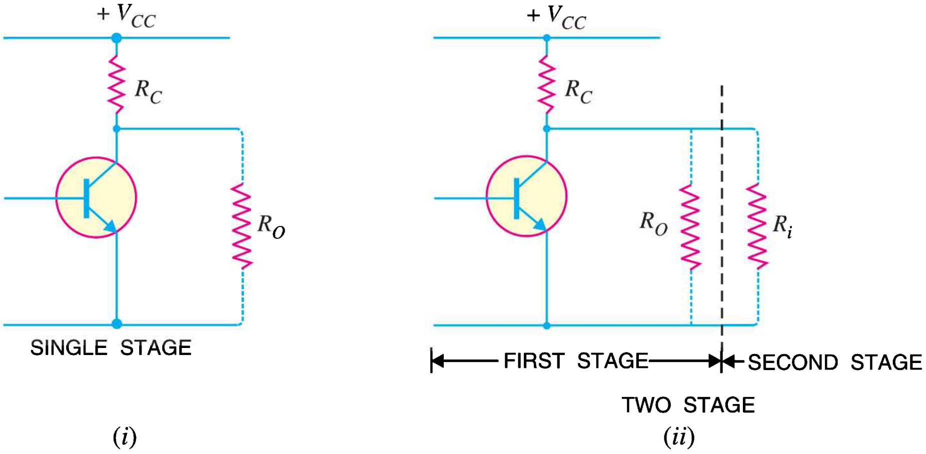


Fig. 8.48

(*v*) **Voltage gain.** *It is the ratio of change in output voltage* (ΔV_{CE}) *to the change in input voltage* (ΔV_{BE}) *i.e.*

$$\begin{aligned}\text{Voltage gain, } A_v &= \frac{\Delta V_{CE}}{\Delta V_{BE}}\\ &= \frac{\text{Change in output current} \times \text{effective load}}{\text{Change in input current} \times \text{input resistance}}\\ &= \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i} = \frac{\Delta I_C}{\Delta I_B} \times \frac{R_{AC}}{R_i} = \beta \times \frac{R_{AC}}{R_i}\end{aligned}$$

For single stage, $R_{AC} = R_C$. However, for multistage, $R_{AC} = \frac{R_C \times R_i}{R_C + R_i}$ where R_i is the input resistance of the next stage.

(*vi*) **Power gain.** *It is the ratio of output signal power to the input signal power i.e.*

$$\begin{aligned}\text{Power gain, } A_p &= \frac{(\Delta I_C)^2 \times R_{AC}}{(\Delta I_B)^2 \times R_i} = \left(\frac{\Delta I_C}{\Delta I_B}\right) \times \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i}\\ &= \text{Current gain} \times \text{Voltage gain}\end{aligned}$$

Example 8.28. *A change of 200 mV in base-emitter voltage causes a change of 100 μA in the base current. Find the input resistance of the transistor.*

Solution. Change in base-emitter voltage is

---

* $R_C \parallel R_O = R_C$ as already explained.

$\Delta V_{BE} = 200 \text{ mV}$

Change in base current, $\Delta I_B = 100 \ \mu\text{A}$

$\therefore$ Input resistance, $R_i = \dfrac{\Delta V_{BE}}{\Delta I_B} = \dfrac{200 \text{ mV}}{100 \ \mu \text{ A}} = \mathbf{2 \ k\Omega}$

Example 8.29. *If the collector current changes from 2 mA to 3mA in a transistor when collector-emitter voltage is increased from 2V to 10V, what is the output resistance ?*

Solution. Change in collector-emitter voltage is

$\Delta V_{CE} = 10 - 2 = 8 \text{ V}$

Change in collector current is $\Delta I_C = 3 - 2 = 1 \text{ mA}$

$\therefore$ Output resistance, $R_O = \dfrac{\Delta V_{CE}}{\Delta I_C} = \dfrac{8 \text{ V}}{1 \text{ mA}} = \mathbf{8 \ k\Omega}$

Example 8.30. *For a single stage transistor amplifier, the collector load is $R_C = 2k\Omega$ and the input resistance $R_i = 1k\Omega$. If the current gain is 50, calculate the voltage gain of the amplifier.*

Solution. Collector load, $R_C = 2 \text{ k}\Omega$

Input resistance, $R_i = 1 \text{ k}\Omega$

Current gain, $\beta = 50$

$\therefore$ Voltage gain, $A_v = \beta \times \dfrac{R_{AC}}{R_i} = \beta \times \dfrac{R_C}{R_i}$ [$\because$ For single stage, $R_{AC} = R_C$]

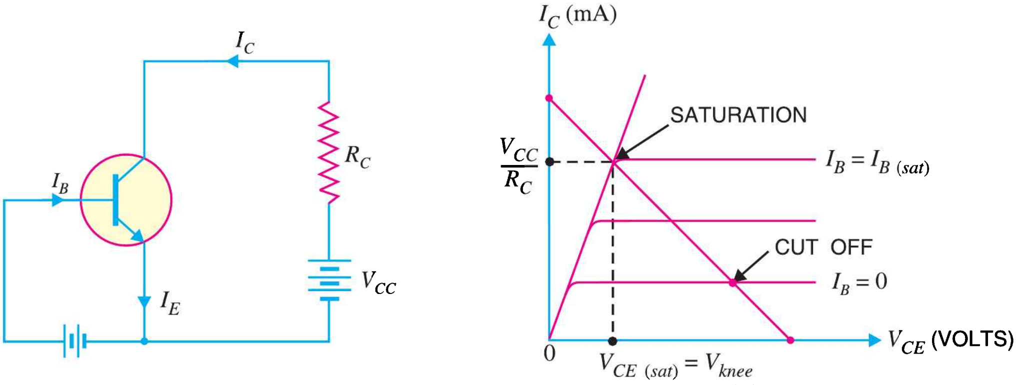
$= 50 \times (2/1) = \mathbf{100}$

8.22 Cut off and Saturation Points

Fig. 8.49 (*i*) shows *CE* transistor circuit while Fig. 8.49 (*ii*) shows the output characteristcs along with the d.c. load line.

(*i*) Cut off. The point where the load line intersects the $I_B = 0$ curve is known as *cut off.* At this point, $I_B = 0$ and only small collector current (*i.e.* collector leakage current I_{CEO}) exists. At cut off, the base-emitter junction no longer remains forward biased and normal transistor action is lost. The collector-emitter voltage is nearly equal to V_{CC} *i.e.*

$$V_{CE\,(cut\ off)} = V_{CC}$$



(*i*) (*ii*)

Fig. 8.49

(*ii*) Saturation. The point where the load line intersects the $I_B = I_{B(sat)}$ curve is called *saturation.* At this point, the base current is maximum and so is the collector current. At saturation, collector-base junction no longer remains reverse biased and normal transistor action is lost.

$$I_{C\,(sat)} \simeq \frac{V_{CC}}{R_C}\,; \quad V_{CE} = V_{CE(sat)} = V_{knee}$$

If base current is greater than $I_{B(sat)}$, then collector current cannot increase because collector-base junction is no longer reverse-biased.

(*iii*) **Active region.** The region between cut off and saturation is known as *active region.* In the active region, collector-base junction remains reverse biased while base-emitter junction remains forward biased. Consequently, the transistor will function normally in this region.

Note. We provide biasing to the transistor to ensure that it operates in the active region. The reader may find the detailed discussion on transistor biasing in the next chapter.

Summary. A transistor has two *pn* junctions *i.e.*, it is like two diodes. The junction between base and emitter may be called *emitter diode.* The junction between base and collector may be called *collector diode.* We have seen above that transistor can act in one of the three states : **cut-off, saturated** and **active**. The state of a transistor is entirely determined by the states of the emitter diode and collector diode [See Fig. 8.50]. The relations between the diode states and the transistor states are :

CUT-OFF : Emitter diode and collector diode are **OFF.**

ACTIVE : Emitter diode is **ON** and collector diode is **OFF.**

SATURATED : Emitter diode and collector diode are **ON.**

In the **active state**, collector current [See Fig 8.51 (*i*)] is β times the base current (*i.e.* $I_C = \beta I_B$). If the transistor is **cut-off,** there is no base current, so there is no collector or emitter current. That is collector emitter pathway is open [See Fig. 8.51 (*ii*)]. In **saturation**, the collector and emitter are, in effect, shorted together. That is the transistor behaves as though a switch has been closed between the collector and emitter [See Fig. 8.51 (*iii*)].

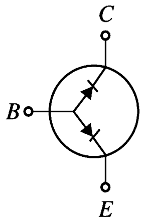
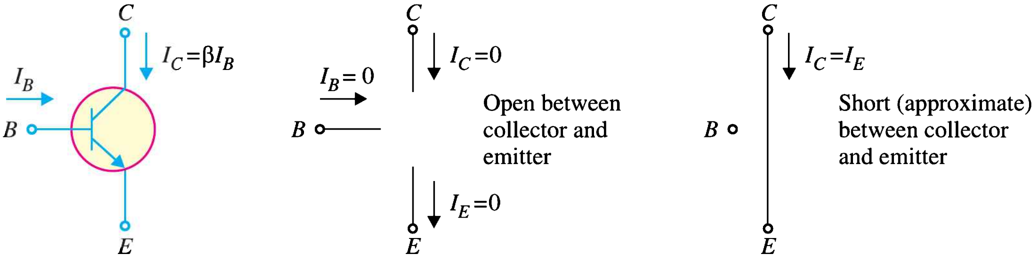


Fig. 8.50


C
$I_C = \beta I_B$
I_B
B
E
C
$I_C = 0$
$I_B = 0$
B
Open between collector and emitter
$I_E = 0$
E
C
$I_C = I_E$
B
Short (approximate) between collector and emitter
E

(*i*) ACTIVE (*ii*) CUT-OFF (*iii*) SATURATED

Fig. 8.51

Note. When the transistor is in the active state, $I_C = \beta I_B$. Therefore, a transistor acts as an amplifier when operating in the active state. Amplification means *linear amplification.* In fact, small signal amplifiers are the most common *linear devices.*

Example 8.31. *Find* $I_{C(sat)}$ *and* $V_{CE(cut\ off)}$ *for the circuit shown in Fig. 8.52 (i).*

Solution. As we decrease R_B, base current and hence collector current increases. The increased collector current causes a greater voltage drop across R_C ; this decreases the collector-emitter voltage. Eventually at some value of R_B, V_{CE} decreases to V_{knee}. At this point, collector-base junction is no longer reverse biased and transistor action is lost. Consequently, further increase in collector current is not possible. The transistor conducts maximum collector current ; we say the transistor is saturated.

$$I_{C(sat)} = \frac{V_{CC} - {}^{*}V_{knee}}{R_C} = \frac{V_{CC}}{R_C} = \frac{20\,V}{1\,k\Omega} = \mathbf{20mA}$$

---

* V_{knee} is about 0.5 V for Ge transistor and about 1V for Si transistor. Consequently, V_{knee} can be neglected as compared to V_{CC} (= 20 V in this case).

As we increase R_B, base current and hence collector current decreases. This decreases the voltage drop across R_C. This increases the collector-emitter voltage. Eventually, when $I_B = 0$, the emitter-base junction is no longer forward biased and transistor action is lost. Consequently, further increase in V_{CE} is not possible. In fact, V_{CE} now equals to V_{CC}.

$$V_{CE(cut\text{-}off)} = V_{CC} = \mathbf{20\ V}$$

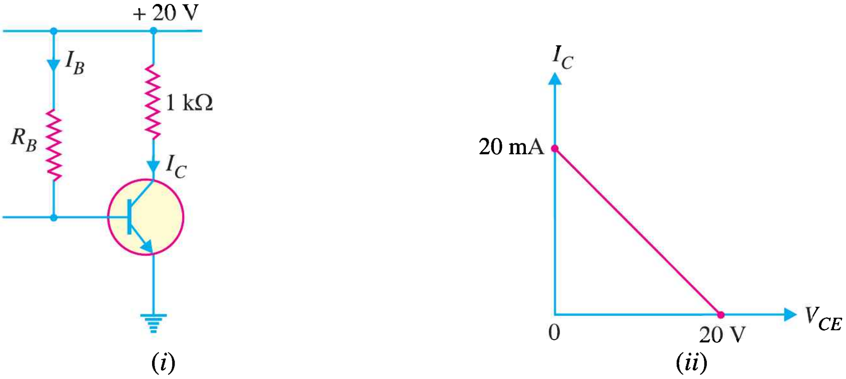


Fig. 8.52

Figure 8.52 (*ii*) shows the saturation and cut off points. Incidentally, they are end points of the d.c. load line.

Note. The exact value of $V_{CE(cut\text{-}off)} = V_{CC} - I_{CEO} R_C$. Since the collector leakage current I_{CEO} is very small, we can neglect $I_{CEO} R_C$ as compared to V_{CC}.

Example 8.32. *Determine the values of $V_{CE\,(off)}$ and $I_{C\,(sat)}$ for the circuit shown in Fig. 8.53.*

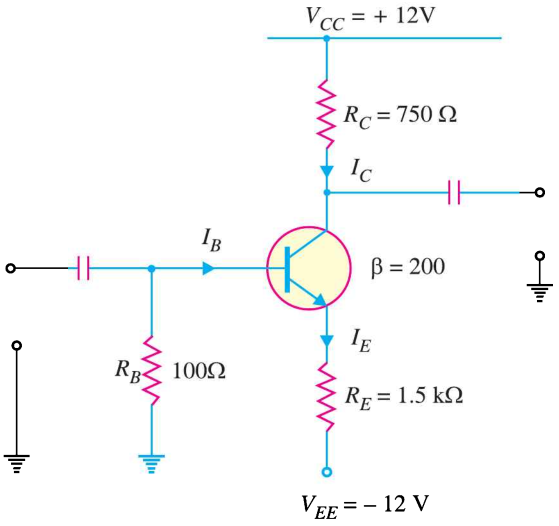


Fig. 8.53

Solution. Applying Kirchhoff's voltage law to the collector side of the circuit in Fig. 8.53, we have,

$$V_{CC} - I_C R_C - V_{CE} - {}^*I_C R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E) \quad \text{... }(i)$$

---

* Voltage across $R_E = I_E R_E$. Since $I_E \simeq I_C$, voltage across $R_E = I_C R_E$.

We have $V_{CE\,(off)}$ when $I_C = 0$. Therefore, putting $I_C = 0$ in eq. (*i*), we have,

$$V_{CE\,(off)} = V_{CC} + V_{EE} = 12 + 12 = \mathbf{24V}$$

We have $I_{C\,(sat)}$ when $V_{CE} = 0$.

$$\therefore \quad I_{C\,(sat)} = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{(12+12)\,V}{(750+1500)\,\Omega} = \mathbf{10.67\ mA}$$

Example 8.33. *Determine whether or not the transistor in Fig. 8.54 is in stauration. Assume $V_{knee} = 0.2V$.*

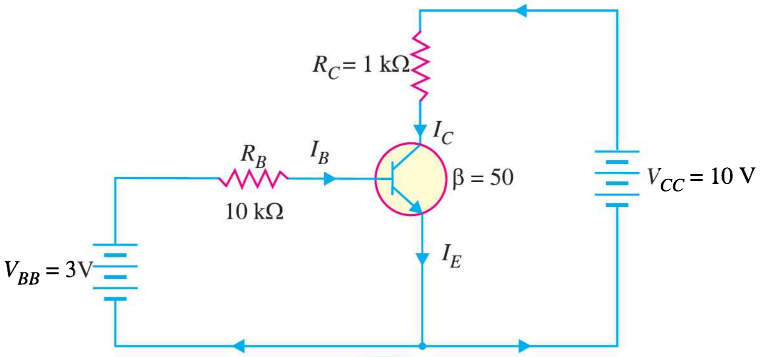


Fig. 8.54

Solution.

$$I_{C\,(sat)} = \frac{V_{CC} - V_{knee}}{R_C} = \frac{10\,V - 0.2\,V}{1\,k\Omega} = \frac{9.8\,V}{1\,k\Omega} = 9.8\text{ mA}$$

Now we shall see if I_B is large enough to produce $I_{C\,(sat)}$.

$$\text{Now} \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3V - 0.7V}{10\,k\Omega} = \frac{2.3\,V}{10\,k\Omega} = 0.23\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 50 \times 0.23 = 11.5\text{ mA}$$

This shows that with specified β, this base current (= 0.23 mA) is capable of producing I_C greater than $I_{C\,(sat)}$. Therefore, the transistor is **saturated.** In fact, the collector current value of 11. 5 mA is never reached. If the base current value corresponding to $I_{C\,(sat)}$ is increased, the collector current remains at the saturated value (= 9.8 mA).

Example 8.34. *Is the transistor in Fig. 8.55 operating in saturated state ?*

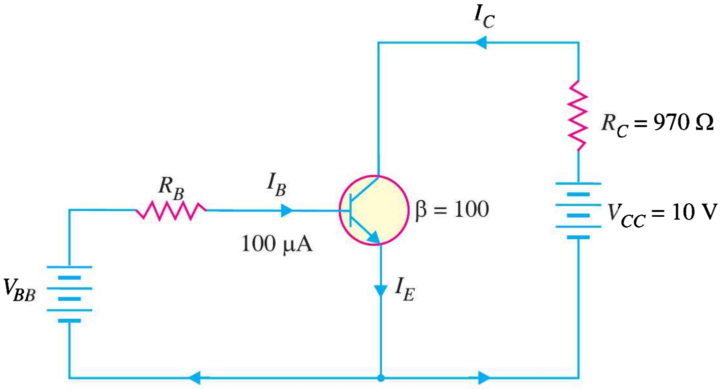


Fig. 8.55

Solution.

$$I_C = \beta I_B = (100)(100\ \mu A) = 10\ mA$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 10V - (10\ mA)(970\Omega) = 0.3V$$

Let us relate the values found to the transistor shown in Fig. 8.56. As you can see, the value of V_{BE} is 0.95V and the value of $V_{CE} = 0.3V$. This leaves V_{CB} of 0.65V (Note that $V_{CE} = V_{CB} + V_{BE}$). In this case, collector – base junction (*i.e.*, collector diode) is forward biased as is the emitter-base junction (*i.e.*, emitter diode). Therefore, the transistor is operating in the **saturation region.**

Note. When the transistor is in the saturated state, the base current and collector current are independent of each other. The base current is still (and always is) found only from the base circuit. The collector current is found apporximately by closing the imaginary switch between the collector and the emitter in the collector circuit.

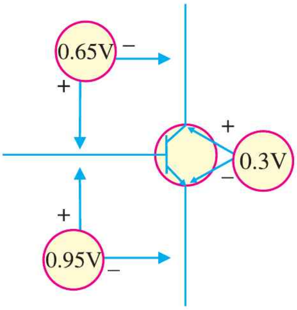


Fig. 8.56

Example 8.35. *For the circuit in Fig. 8.57, find the base supply voltage (V_{BB}) that just puts the transistor into saturation. Assume $\beta = 200$.*

Solution. When transistor first goes into saturation, we can assume that the collector shorts to the emitter (*i.e.* $V_{CE} = 0$) but the collector current is still β times the base current.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - 0}{R_C}$$

$$= \frac{10V - 0}{2\ k\Omega} = 5\ mA$$

The base current I_B corresponding to $I_{C\ (sat)}$ (=5 mA) is

$$I_B = \frac{I_{C\ (sat)}}{\beta} = \frac{5\ mA}{200} = 0.025\ mA$$

Applying Kirchhoff's voltage law to the base circuit, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

or $$V_{BB} = V_{BE} + I_B R_B$$

$$= 0.7V + 0.025\ mA \times 50\ k\Omega = 0.7 + 1.25 = 1.95V$$

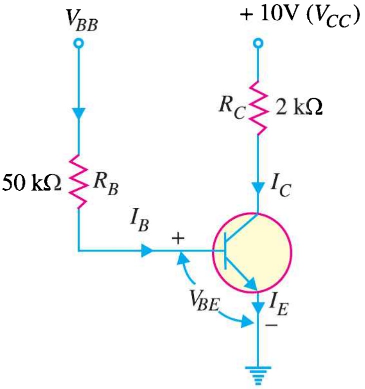


Fig. 8.57

Therefore, for **$V_{BB} \geq 1.95$,** the transistor will be in *saturation.*

Example. 8.36. *Determine the state of the transistor in Fig. 8.58 for the following values of collector resistor* :

(i) $R_C = 2\ k\Omega$ *(ii)* $R_C = 4\ k\Omega$ *(iii)* $R_C = 8\ k\Omega$

Solution. Since I_E does not depend on the value of the collector resistor R_C, the emitter current (I_E) is the same for all three parts.

Emitter voltage, $V_E = V_B - V_{BE} = V_{BB} - V_{BE}$

$$= 2.7V - 0.7\ V = 2V$$

Also $$I_E = \frac{V_E}{R_E} = \frac{2V}{1\ k\Omega} = 2\ mA$$

(i) **When $R_C = 2$ kΩ.** Suppose the transistor is active.

$\therefore \quad I_C = I_E = 2\ mA$

$\therefore \quad I_B = I_C/\beta = 2\ mA/100 = 0.02\ mA$

Collector voltage, $V_C = V_{CC} - I_C R_C$

$= 10V - 2\,mA \times 2\,k\Omega = 10V - 4V = 6V$

Since V_C (= 6V) is greater than V_E (= 2V), the transistor is **active.** Therefore, our assumption that transistor is active is correct.

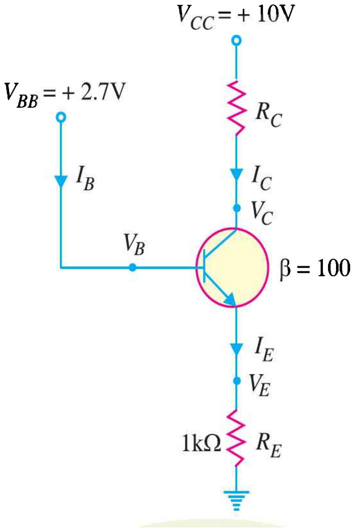


Fig. 8.58

(ii) **When R_C = 4 kΩ.** Suppose the transistor is active.

∴ I_C = 2mA and I_B = 0.02 mA ... as found above

Collector voltage, $V_C = V_{CC} - I_C R_C$

$= 10V - 2\,mA \times 4\,k\Omega = 10V - 8V = 2V$

Since $V_C = V_E$, the transistor is just at the edge of **saturation.** We know that at the edge of saturation, the relation between the transistor currents is the same as in the **active state.** Both answers are correct.

(iii) **When R_C = 8 kΩ.** Suppose the transistor is active.

∴ I_C = 2mA ; I_B = 0.02 mA ... as found earlier.

Collector voltage, $V_C = V_{CC} - I_C R_C$

$= 10V - 2\,mA \times 8\,k\Omega = 10V - 16V = -6V$

Since $V_C < V_E$, the transistor is **saturated** and our assumption is not correct.

Example 8.37. *In the circuit shown in Fig. 8.59, V_{BB} is set equal to the following values :*

(i) V_{BB} = 0.5V (ii) V_{BB} = 1.5V (iii) V_{BB} = 3V

Determine the state of the transistor for each value of the base supply voltage V_{BB}.

Solution. The state of the transistor also depends on the base supply voltage V_{BB}.

(i) **For V_{BB} = 0.5V**

Because the base voltage V_B (= V_{BB} = 0.5V) is less than 0.7V, the transistor is **cut-off.**

(ii) **For V_{BB} = 1.5V**

The base voltage V_B controls the emitter voltage V_E which controls the emitter current I_E.

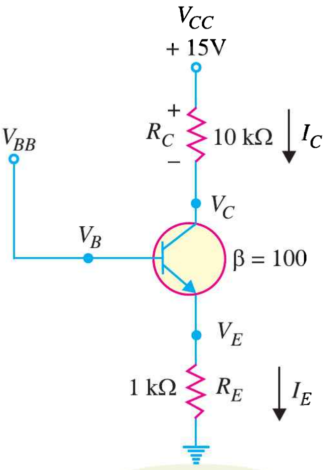


Fig. 8.59

Now $V_E = V_B - 0.7V = 1.5V - 0.7V = 0.8V$

$$\therefore \quad I_E = \frac{V_E}{R_E} = \frac{0.8V}{1\,k\Omega} = 0.8\text{ mA}$$

If the transistor is active, we have,

$I_C = I_E$ = 0.8 mA and $I_B = I_C/\beta$ = 0.8/100 = 0.008 mA

∴ Collector voltage, $V_C = V_{CC} - I_C R_C$

$= 15V - 0.8\,mA \times 10\,k\Omega = 15V - 8V = 7V$

Since $V_C > V_E$, the transistor is **active** and our assumption is correct.

(iii) **For V_{BB} = 3V**

$V_E = V_B - 0.7V = 3V - 0.7V = 2.3V$

$$\therefore \quad I_E = \frac{V_E}{R_E} = \frac{2.3V}{1\,k\Omega} = 2.3\text{ mA}$$

Assuming the transistor is active, we have,

$$I_C = I_E = 2.3 \text{ mA} \quad ; \quad I_B = I_C/\beta = 2.3/100 = 0.023 \text{ mA}$$

Collector voltage, $V_C = V_{CC} - I_C R_C$

$= 15\text{V} - 2.3 \text{ mA} \times 10 \text{ k}\Omega = 15\text{V} - 23\text{V} = -8\text{V}$

Since $V_C < V_E$, the transistor is **saturated** and our assumption is not correct.

8.23 Power Rating of Transistor

The maximum power that a transistor can handle without destruction is known as **power rating** *of the transistor.*

When a transistor is in operation, almost all the power is dissipated at the reverse biased *collector-base junction. The power rating (or maximum power dissipation) is given by :

$$P_{D\,(max)} = \text{Collector current} \times \text{Collector-base voltage}$$

$$= I_C \times V_{CB}$$

$$\therefore \quad P_{D\,(max)} = I_C \times V_{CE}$$

$$[\because V_{CE} = V_{CB} + V_{BE}. \text{ Since } V_{BE} \text{ is very small, } V_{CB} \simeq V_{CE}]$$

While connecting transistor in a circuit, it should be ensured that its power rating is not exceeded otherwise the transistor may be destroyed due to excessive heat. For example, suppose the power rating (or maximum power dissipation) of a transistor is 300 mW. If the collector current is 30 mA, then maximum V_{CE} allowed is given by ;

$$P_{D\,(max)} = I_C \times V_{CE\,(max)}$$

or $\quad 300 \text{ mW} = 30 \text{ mA} \times V_{CE\,(max)}$

or $\quad V_{CE\,(max)} = \dfrac{300 \text{ mW}}{30 \text{ mA}} = 10\text{V}$

This means that for $I_C = 30$ mA, the maximum V_{CE} allowed is 10V. If V_{CE} exceeds this value, the transistor will be destroyed due to excessive heat.

Maximum power dissipation curve. For **power transistors, it is sometimes necessary to draw maximum power dissipation curve on the output characteristics. To draw this curve, we should know the power rating (*i.e.* maximum power dissipation) of the transistor. Suppose the power rating of a transistor is 30 mW.

$$P_{D\,(max)} = V_{CE} \times I_C$$

or $\quad 30 \text{ mW} = V_{CE} \times I_C$

Using convenient V_{CE} values, the corresponding collector currents are calculated for the maximum power dissipation. For example, for $V_{CE} = 10$V,

$$I_C\,(max) = \frac{P_{D\,(max)}}{V_{CE}} = \frac{30 \text{ mW}}{10 \text{ V}} = 3\text{mA}$$

This locates the point *A* (10V, 3 mA) on the output characteristics. Similarly, many points such as *B, C, D etc.* can be located on the output characteristics. Now draw a curve through the above points to obtain the maximum power dissipation curve as shown in Fig. 8.60.

In order that transistor may not be destroyed, the transistor voltage and current (*i.e.* V_{CE} and I_C) conditions must at all times be maintained in the portion of the characteristics below the maximum power dissipation curve.

---

* The base-emitter junction conducts about the same current as the collector-base junction (*i.e.* $I_E \simeq I_C$). However, V_{BE} is very small (0.3 V for *Ge* transistor and 0.7 V for *Si* transistor). For this reason, power dissipated at the base-emitter junction is negligible.

** A transistor that is suitable for large power amplification is called a *power transistor.* It differs from other transistors mostly in size ; it is considerably larger to provide for handling the great amount of power.

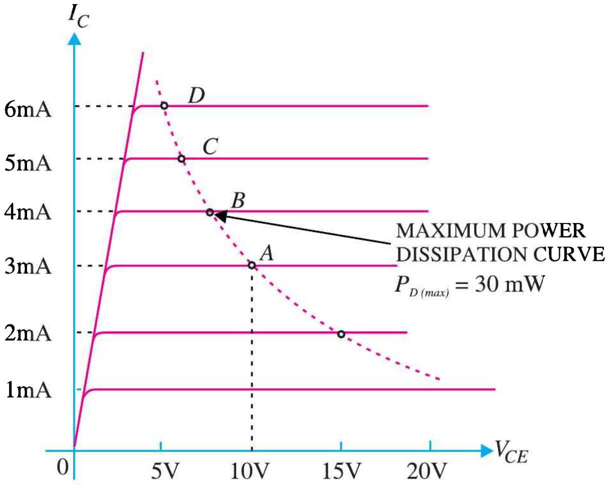


Fig. 8.60

Example 8.38. *The maximum power dissipation of a transistor is 100mW. If V_{CE} = 20V, what is the maximum collector current that can be allowed without destruction of the transistor?*

Solution. $P_{D\,(max)} = V_{CE} \times I_{C\,(max)}$

or $100 \text{ mW} = 20 \text{ V} \times I_{C\,(max)}$

$\therefore$ $I_{C\,(max)} = \dfrac{100 \text{ mW}}{20 \text{ V}} = \mathbf{5\ mA}$

Thus for V_{CE} = 20V, the maximum collector current allowed is 5 mA. If collector current exceeds this value, the transistor may be burnt due to excessive heat.

Note. Suppose the collector current becomes 7mA. The power produced will be 20 V × 7 mA = 140 mW. The transistor can only dissipate 100 mW. The remaining 40 mW will raise the temperature of the transistor and eventually it will be burnt due to excessive heat.

Example 8.39. *For the circuit shown in Fig. 8.61, find the transistor power dissipation. Assume that $\beta = 200$.*

Solution.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{(5 - 0.7)\,V}{1\,k\Omega} = 4.3 \text{ mA}$$

$\therefore$ $I_C = \beta I_B = 200 \times 4.3 = 860 \text{ mA}$

Now $V_{CE} = V_{CC} - I_C R_C = 5 - I_C \times 0 = 5\text{V}$

$\therefore$ Power dissipation, $P_D = V_{CE} \times I_C$

$= 5\text{V} \times 860 \text{ mA} = 4300 \text{ mW} = \mathbf{4.3W}$

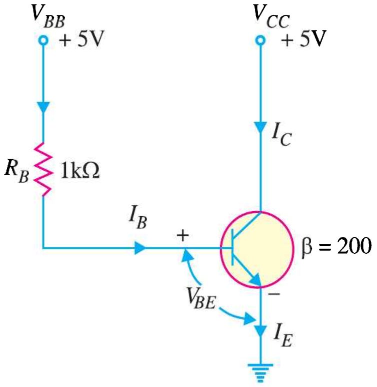


Fig. 8.61

Example 8.40. *For the circuit shown in Fig. 8.62, find the power dissipated in the transistor. Assume $\beta = 100$.*

Solution. The transistor is usually used with a resistor R_C connected between the collector and its power supply V_{CC} as shown is Fig. 8.62. The collector resistor R_C serves two purposes. Firstly, it allows us to control the voltage V_C at the collector. Secondly, it protects the transistor from excessive collector current I_C and, therefore, from excessive power dissipation.

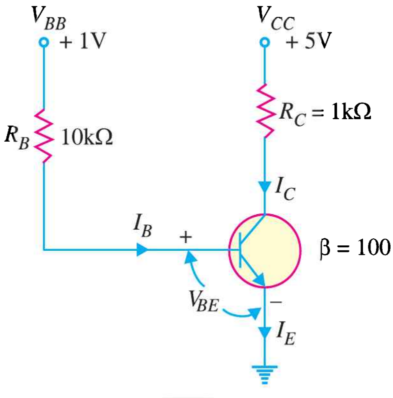


Fig. 8.62

Referring to Fig. 8.62 and applying Kirchhoff's voltage law to the base side, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{1V - 0.7V}{10\,k\Omega} = \frac{0.3V}{10\,k\Omega} = 0.03 \text{ mA}$$

Now $I_C = \beta I_B = 100 \times 0.03 = 3$ mA

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C = 5V - 3 \text{ mA} \times 1 \text{ k}\Omega = 5V - 3V = 2V$$

∴ Power dissipated in the transistor is

$$P_D = V_{CE} \times I_C = 2V \times 3 \text{ mA} = \mathbf{6\ mW}$$

Example 8.41. *The transistor in Fig. 8.63 has the following maximum ratings :*

$$P_{D\,(max)} = 800 \text{ mW} ;\ V_{CE\,(max)} = 15V ;\ I_{C\,(max)} = 100 \text{ mA}$$

Determine the maximum value to which V_{CC} can be adjusted without exceeding any rating. Which rating would be exceeded first ?

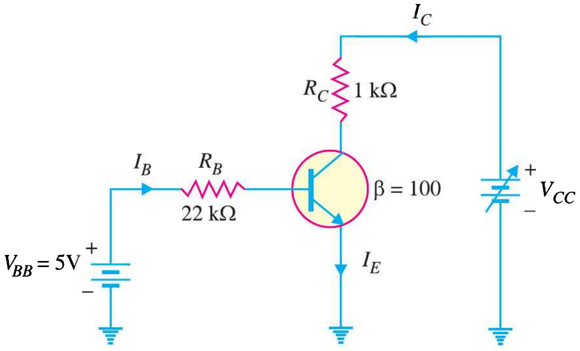


Fig. 8.63

Solution.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{22\,k\Omega} = \frac{4.3V}{22\,k\Omega} = 195\ \mu\text{A}$$

$$\therefore \quad I_C = \beta I_B = 100 \times 195\ \mu\text{A} = 19.5 \text{ mA}$$

Note that I_C is much less than $I_{C(max)}$ and will not change with V_{CC}. It is determined only by I_B and β. Therefore, **current rating is not exceeded.**

Now $V_{CC} = V_{CE} + I_C R_C$

We can find the value of V_{CC} when $V_{CE\,(max)} = 15V$.

$$\therefore \quad V_{CC\,(max)} = V_{CE\,(max)} + I_C R_C$$

$$= 15V + 19.5 \text{ mA} \times 1 \text{ k}\Omega = 15V + 19.5 \text{ V} = 34.5V$$

Therefore, we can increase V_{CC} to **34.5V** before $V_{CE\,(max)}$ is reached.

$$P_D = V_{CE\,(max)} I_C = (15V)\,(19.5 \text{ mA}) = 293 \text{ mW}$$

Since $P_{D\,(max)} = 800$ mW, **it is not exceeded** when $V_{CC} = 34.5V$.

If base current is removed causing the transistor to turn off, $V_{CE\,(max)}$ **will be exceeded** because the entire supply voltage V_{CC} will be dropped across the transistor.

8.24. Determination of Transistor Configuration

In practical circuits, you must be able to tell whether a given transistor is connected as a common emitter, common base or common collector. There is an easy way to ascertain it. Just locate the terminals where the input a.c. singal is applied to the transistor and where the a.c output is taken from the transistor. The remaining third terminal is the common terminal. For instance, if the a.c input is applied to the base and the a.c output is taken from the collector, then common terminal is the emitter. Hence the transistor is connected in **common emitter configuration.** If the a.c. input is applied to the base and a.c output is taken from the emitter, then common terminal is the collector. Therefore, the transistor is connected in **common collector configuration.**

8.25 Semiconductor Devices Numbering System

From the time semiconductor engineering came to existence, several numbering systems were adopted by different countries. However, the accepted numbering system is that announced by Proelectron Standardisation Authority in Belgium. According to this system of numbering semiconductor devices :

(*i*) Every semiconductor device is numbered by five alpha-numeric symbols, comprising either two letters and three numbers (*e.g.* BF194) or three letters and two numbers (*e.g.* BFX63). When two numbers are included in the symbol (*e.g.* BFX63), the device is intended for industrial and professional equipment. When the symbol contains three numbers (*e.g.* BF194) , the device is intended for entertainment or consumer equipment.

(*ii*) The first letter indicates the nature of semiconductor material. For example :

A = germanium, B = silicon, C = gallium arsenide, R = compound material (e.g. cadmium sulphide)

Thus AC125 is a germanium transistor whereas BC149 is a silicon transistor.

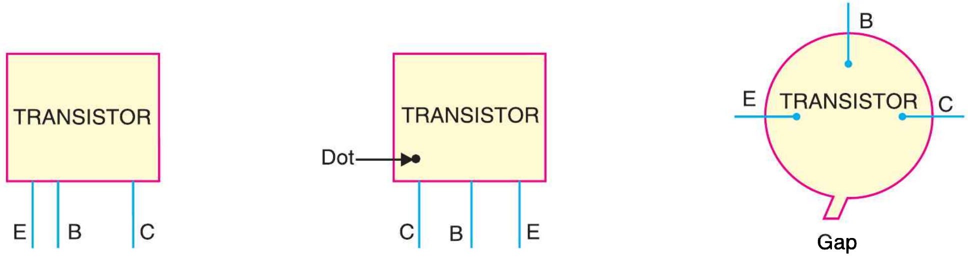
(*iii*) The second letter indicates the device and circuit function.

A = diode
B = Variable capacitance diode
C = A.F. low powered transistor
D = A.F. power transistor
E = Tunnel diode
F = H.F. low power transistor
G = Multiple device
H = Magnetic sensitive diode
K = Hall-effect device
L = H.F. power transistor
M = Hall-effect modulator
P = Radiation sensitive diode
Q = Radiation generating diode
R = Thyristor (SCR or triac)
S = Low power switching transistor
T = Thyristor (power)
U = Power switching transistor
X = diode, multiplier
Y = Power device
Z = Zener diode

8.26 Transistor Lead Identification

There are three leads in a transistor *viz.* collector, emitter and base. When a transistor is to be connected in a circuit, it is necessary to know which terminal is which. The identification of the leads of transistor varies with manufacturer. However, there are three systems in general use as shown in Fig. 8.64.

(*i*) When the leads of a transistor are in the same plane and unevenly spaced [See Fig. 8.64 (*i*)], they are identified by the positions and spacings of leads. The central lead is the base lead. The collector lead is identified by the larger spacing existing between it and the base lead. The remaining lead is the emitter.



(*i*) (*ii*) (*iii*)

Fig. 8.64

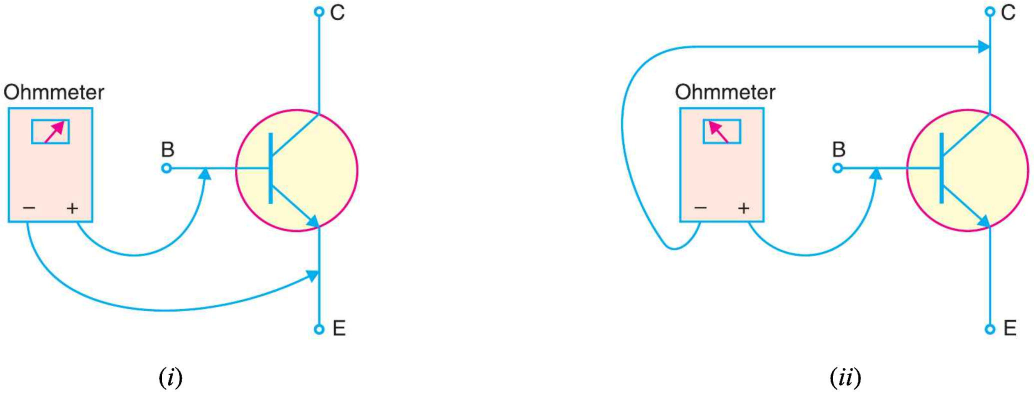
(*ii*) When the leads of a transistor are in the same plane but evenly spaced [See Fig. 8.64 (*ii*)], the central lead is the base, the lead identified by dot is the collector and the remaining lead is the emitter.

(*iii*) When the leads of a transistor are spaced around the circumference of a circle [See Fig. 8.64 (*iii*)], the three leads are generally in E-B-C order clockwise from a gap.

8.27 Transistor Testing

An ohmmeter can be used to check the state of a transistor *i.e.*, whether the transistor is good or not. We know that base-emitter junction of a transistor is forward biased while collector-base junction is reverse biased. Therefore, forward biased base-emitter junction should have low resistance and reverse biased collector-base junction should register a much higher resistance. Fig. 8.65 shows the process of testing an ***npn*** transistor with an ohmmeter.

(*i*) The forward biased base-emitter junction (biased by internal supply) should read a low resistance, typically 100 Ω to 1 kΩ as shown in Fig. 8.65 (*i*). If that is so, the transistor is good. However, if it fails this check, the transistor is faulty and it must be replaced.



(*i*) (*ii*)

Fig. 8.65

(*ii*) The reverse biased collector-base junction (again reverse biased by internal supply) should be checked as shown in Fig. 8.65 (*ii*). If the reading of the ohmmeter is 100 kΩ or higher, the transistor is good. If the ohmmeter registers a small resistance, the transistor is faulty and requires replacement.

Note. When testing a *pnp* transistor, the ohmmeter leads must be reversed. The results of the tests, however, will be the same.

8.28 Applications of Common Base Amplifiers

Common base amplifiers are not used as frequently as the *CE* amplifiers. The two important applications of *CB* amplifiers are : (*i*) to provide voltage gain without current gain and (*ii*) for impedance matching in high frequency applications. Out of the two, the high frequency applications are far more common.

(*i*) To provide voltage gain without current gain. We know that a *CB* amplifier has a high voltage gain while the current gain is nearly 1 (*i.e.* $A_i \simeq 1$). Therefore, this circuit can be used to provide high voltage gain without increasing the value of circuit current. For instance, consider the case where the output current from an amplifier has sufficient value for the required application but the voltage gain needs to be increased. In that case, *CB* amplifier will serve the purpose because it would increase the voltage without increasing the current. This is illustrated in Fig. 8.66. The *CB* amplifier will provide voltage gain without any current gain.

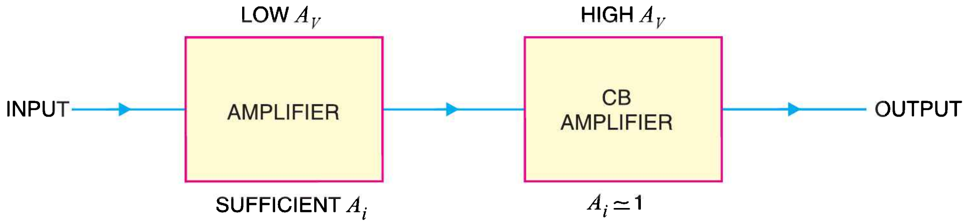

LOW A_V
HIGH A_V
INPUT
AMPLIFIER
CB AMPLIFIER
OUTPUT
SUFFICIENT A_i
$A_i \simeq 1$

Fig. 8.66

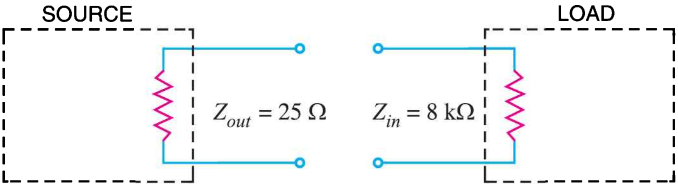

SOURCE
LOAD
$Z_{out} = 25\ \Omega$
$Z_{in} = 8\ k\Omega$

Fig. 8.67

(*ii*) **For impedance matching in high frequency applications.** Most high-frequency voltage sources have a very *low output impedance*. When such a low-impedance source is to be connected to a high-impedance load, you need a circuit to match the source impedance to the load impedance. Since a common-base amplifier has *low input impedance* and *high output impedance*, the common-base circuit will serve well in this situation. Let us illustrate this point with a numerical example. Suppose a high-frequency source with internal resistance 25 Ω is to be connected to a load of 8 kΩ as shown in Fig. 8.67. If the source is directly connected to the load, small source power will be transferred to the load due to mismatching. However, it is possible to design a *CB* amplifier that has an input impedance of nearly 25 Ω and output impedance of nearly 8 kΩ. If such a *CB* circuit is placed between the source and the load, the source will be matched to the load as shown in Fig. 8.68.

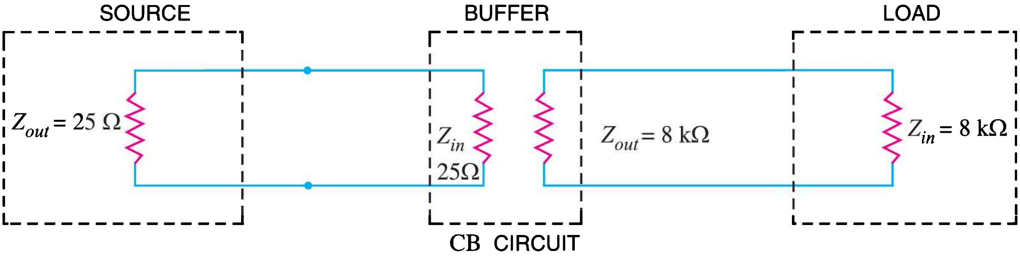

SOURCE
BUFFER
LOAD
$Z_{out} = 25\ \Omega$
Z_{in} 25Ω
$Z_{out} = 8\ k\Omega$
$Z_{in} = 8\ k\Omega$
CB CIRCUIT

Fig. 8.68

Note that source impedance very closely matches the input impedance of *CB* amplifier. Therefore, there is a maximum power transfer from the source to input of *CB* amplifier. The high output impedance of the amplifier very nearly matches the load resistance. As a result, there is a maximum power transfer from the amplifier to the load. The net result is that maximum power has been transferred from the original source to the original load. A common-base amplifier that is used for this purpose is called a *buffer amplifier*.

8.29 Transistors Versus Vacuum Tubes

Advantages of transistors

A transistor is a solid-state device that performs the same functions as the grid-controlled vacuum tube. However, due to the following advantages, the transistors have upstaged the vacuum tubes in most areas of electronics :

(*i*) **High voltage gain.** We can get much more voltage gain with a transistor than with a vacuum tube. Triode amplifiers normally have voltage gain of less than 75. On the other hand, transistor amplifiers can provide a voltage gain of 300 or more. This is a distinct advantage of transistors over the tubes.

(*ii*) **Lower supply voltage.** Vacuum tubes require much higher d.c. voltages than transistors. Vacuum tubes generally run at d.c. voltages ranging from 200V to 400V whereas transistors require much smaller d.c. voltages for their operation. The low voltage requirement permits us to build portable, light-weight transistor equipment instead of heavier vacuum-tube equipment.

(*iii*) **No heating.** A transistor does not require a heater whereas the vacuum tube can only operate with a heater. The heater requirement in vacuum tubes poses many problems. First, it makes the power supply bulky. Secondly, there is a problem of getting rid of heat. The heater limits the tube's useful life to a few thousand hours. Transistors, on the other hand, last for many years. This is the reason that transistors are permanently soldered into a circuit whereas tubes are plugged into sockets.

(*iv*) **Miscellaneous.** Apart from the above salient advantages, the transistors have superior edge over the tubes in the following respects :

(*a*) transistors are much smaller than vacuum tubes. This means that transistor circuits can be more compact and light-weight.

(*b*) transistors are mechanically strong due to solid-state.

(*c*) transistors can be integrated along with resistors and diodes to produce *IC*s which are extremely small in size.

Disadvantages of transistors

Although transistors are constantly maintaining superiority over the vacuum tubes, yet they suffer from the following drawbacks :

(*i*) **Lower power dissipation.** Most power transistors have power dissipation below 300W while vacuum tubes can easily have power dissipation in kW. For this reason, transistors cannot be used in high power applications e.g. transmitters, industrial control systems, microwave systems etc. In such areas, vacuum tubes find wide applications.

(*ii*) **Lower input impedance.** A transistors has low input impedance. A vacuum tube, on the other hand, has very high input impedance (of the order of MΩ) because the control grid draws negligible current. There are many electronic applications where we required high input impedance *e.g.* electronic voltmeter, oscilloscope etc. Such areas of application need vacuum tubes. It may be noted here that field-effect transistor (*FET*) has a very high input impedance and can replace a vacuum tube in almost all applications.

(*iii*) **Temperature dependence.** Solid-state devices are very much temperature dependent. A slight change in temperature can cause a significant change in the characteristics of such devices. On the other hand, small variations in temperature hardly affect the performance of tubes. It is a distinct disadvantage of transistors.

(*iv*) **Inherent variation of parameters.** The manufacture of solid-state devices is indeed a very difficult process. Inspite of best efforts, the parameters of transistors (*e.g.* β, V_{BE} *etc.*) are not the same even for the transistors of the same batch. For example, β for *BC* 148 transistors may vary between 100 and 600.

MULTIPLE-CHOICE QUESTIONS

1. A transistor has ....
(*i*) one *pn* junction
(*ii*) two *pn* junctions
(*iii*) three *pn* junctions
(*iv*) four *pn* junctions

2. The number of depletion layers in a transistor is ....
(*i*) four (*ii*) three
(*iii*) one (*iv*) two

3. The base of a transistor is .... doped.
(*i*) heavily (*ii*) moderately
(*iii*) lightly (*iv*) none of the above

4. The element that has the biggest size in a transistor is ....
(*i*) collector (*ii*) base
(*iii*) emitter
(*iv*) collector-base junction

5. In a *pnp* transistor, the current carriers are ....
(*i*) acceptor ions (*ii*) donor ions
(*iii*) free electrons (*iv*) holes

6. The collector of a transistor is .... doped.
(*i*) heavily (*ii*) moderately
(*iii*) lightly (*iv*) none of the above

7. A transistor is a .... operated device.
(*i*) current (*ii*) voltage
(*iii*) both voltage and current
(*iv*) none of the above

8. In an *npn* transistor, ... are the minority carriers.
(*i*) free electrons (*ii*) holes
(*iii*) donor ions (*iv*) acceptor ions

9. The emitter of a transistor is .... doped.
(*i*) lightly (*ii*) heavily
(*iii*) moderately (*iv*) none of the above

10. In a transistor, the base current is about .... of emitter current.
(*i*) 25% (*ii*) 20%
(*iii*) 35% (*iv*) 5%

11. At the base-emitter junction of a transistor, one finds ....
(*i*) reverse bias
(*ii*) a wide depletion layer
(*iii*) low resistance
(*iv*) none of the above

12. The input impedance of a transistor is ......
(*i*) high (*ii*) low
(*iii*) very high (*iv*) almost zero

13. Most of the majority carriers from the emitter ....
(*i*) recombine in the base
(*ii*) recombine in the emitter
(*iii*) pass through the base region to the collector
(*iv*) none of the above

14. The current I_B is ....
(*i*) electron current
(*ii*) hole current
(*iii*) donor ion current
(*iv*) acceptor ion current

15. In a transistor, ...
(*i*) $I_C = I_E + I_B$ (*ii*) $I_B = I_C + I_E$
(*iii*) $I_E = I_C - I_B$ (*iv*) $I_E = I_C + I_B$

16. The value of α of a transistor is ....
(*i*) more than 1 (*ii*) less than 1
(*iii*) 1 (*iv*) none of the above

17. $I_C = \alpha I_E +$ ....
(*i*) I_B (*ii*) I_{CEO}
(*iii*) I_{CBO} (*iv*) βI_B

18. The output impedance of a transistor is ....
(*i*) high (*ii*) zero
(*iii*) low (*iv*) very low

19. In a transistor, I_C = 100 mA and I_E = 100.5 mA. The value of β is ....
(*i*) 100 (*ii*) 50
(*iii*) about 1 (*iv*) 200

20. In a transistor if β = 100 and collector current is 10 mA, then I_E is ....
(*i*) 100 mA (*ii*) 100.1 mA
(*iii*) 110 mA (*iv*) none of the above

21. The relation between β and α is ....
(*i*) $\beta = \dfrac{1}{1-\alpha}$ (*ii*) $\beta = \dfrac{1-\alpha}{\alpha}$
(*iii*) $\beta = \dfrac{\alpha}{1-\alpha}$ (*iv*) $\beta = \dfrac{\alpha}{1+\alpha}$

22. The value of β for a transistor is generally ....

(*i*) 1 (*ii*) less than 1
(*iii*) between 20 and 500
(*iv*) above 500

23. The most commonly used transistor arrangement is .... arrangement.

(*i*) common emitter
(*ii*) common base
(*iii*) common collector
(*iv*) none of the above

24. The input impedance of a transistor connected in .... arrangement is the highest.

(*i*) common emitter
(*ii*) common collector
(*iii*) common base
(*iv*) none of the above

25. The output impedance of a transistor connected in .... arrangement is the highest.

(*i*) common emitter
(*ii*) common collector
(*iii*) common base
(*iv*) none of the above

26. The phase difference between the input and output voltages in a common base arrangement is ....

(*i*) 180° (*ii*) 90°
(*iii*) 270° (*iv*) 0°

27. The power gain of a transistor connected in .... arrangement is the highest.

(*i*) common emitter
(*ii*) common base
(*iii*) common collector
(*iv*) none of the above

28. The phase difference between the input and output voltages of a transistor connected in common emitter arrangement is ....

(*i*) 0° (*ii*) 180°
(*iii*) 90° (*iv*) 270°

29. The voltage gain of a transistor connected in .... arrangement is the highest.

(*i*) common base (*ii*) common collector
(*iii*) common emitter
(*iv*) none of the above

30. As the temperature of a transistor goes up, the base-emitter resistance ....

(*i*) decreases (*ii*) increases
(*iii*) remains the same
(*iv*) none of the above

31. The voltage gain of a transistor connected in common collector arrangement is ....

(*i*) equal to 1 (*ii*) more than 10
(*iii*) more than 100 (*iv*) less than 1

32. The phase difference between the input and output voltages of a transistor connected in common collector arrangement is ....

(*i*) 180° (*ii*) 0°
(*iii*) 90° (*iv*) 270°

33. $I_C = \beta I_B +$ ....

(*i*) I_{CBO} (*ii*) I_C
(*iii*) I_{CEO} (*iv*) αI_E

34. $I_C = \frac{\alpha}{1-\alpha} I_B +$ ....

(*i*) I_{CEO} (*ii*) I_{CBO}
(*iii*) I_C (*iv*) $(1-\alpha) I_B$

35. $I_C = \frac{\alpha}{1-\alpha} I_B + \frac{\text{.......}}{1-\alpha}$

(*i*) I_{CBO} (*ii*) I_{CEO}
(*iii*) I_C (*iv*) I_E

36. BC 147 transistor indicates that it is made of ....

(*i*) germanium (*ii*) silicon
(*iii*) carbon (*iv*) none of the above

37. $I_{CEO} =$ (........) I_{CBO}

(*i*) β (*ii*) $1 + \alpha$
(*iii*) $1 + \beta$ (*iv*) none of the above

38. A transistor is connected in *CB* mode. If it is now connected in *CE* mode with same bias voltages, the values of I_E, I_B and I_C will ....

(*i*) remain the same
(*ii*) increase
(*iii*) decrease (*iv*) none of the above

39. If the value of α is 0.9, then value of β is ....

(*i*) 9 (*ii*) 0.9
(*iii*) 900 (*iv*) 90

40. In a transistor, signal is transferred from a .... circuit.

(*i*) high resistance to low resistance
(*ii*) low resistance to high resistance
(*iii*) high resistance to high resistance
(*iv*) low resistance to low resistance

41. The arrow in the symbol of a transistor indicates the direction of ....

(*i*) electron current in the emitter
(*ii*) electron current in the collector
(*iii*) hole current in the emitter
(*iv*) donor ion current

42. The leakage current in *CE* arrangement is

.... that in *CB* arrangement.
(*i*) more than (*ii*) less than
(*iii*) the same as (*iv*) none of the above

43. A heat sink is generally used with a transistor to ....
(*i*) increase the forward current
(*ii*) decrease the forward current
(*iii*) compensate for excessive doping
(*iv*) prevent excessive temperature rise

44. The most commonly used semiconductor in the manufacture of a transistor is ....
(*i*) germanium (*ii*) silicon
(*iii*) carbon (*iv*) none of the above

45. The collector-base junction in a transistor has ....
(*i*) forward bias at all times
(*ii*) reverse bias at all times
(*iii*) low resistance
(*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iv*)	**3.** (*iii*)	**4.** (*i*)	**5.** (*iv*)
6. (*ii*)	**7.** (*i*)	**8.** (*ii*)	**9.** (*ii*)	**10.** (*iv*)
11. (*iii*)	**12.** (*ii*)	**13.** (*iii*)	**14.** (*i*)	**15.** (*iv*)
16. (*ii*)	**17.** (*iii*)	**18.** (*i*)	**19.** (*iv*)	**20.** (*ii*)
21. (*iii*)	**22.** (*iii*)	**23.** (*i*)	**24.** (*ii*)	**25.** (*iii*)
26. (*iv*)	**27.** (*i*)	**28.** (*ii*)	**29.** (*iii*)	**30.** (*i*)
31. (*iv*)	**32.** (*ii*)	**33.** (*iii*)	**34.** (*i*)	**35.** (*i*)
36. (*ii*)	**37.** (*iii*)	**38.** (*i*)	**39.** (*iv*)	**40.** (*ii*)
41. (*iii*)	**42.** (*i*)	**43.** (*iv*)	**44.** (*ii*)	**45.** (*ii*)

Chapter Review Topics

1. What is a transistor ? Why is it so called ?
2. Draw the symbol of ***npn*** and ***pnp*** transistor and specify the leads.
3. Show by means of a diagram how you normally connect external batteries in (*i*) ***pnp*** transistor (*ii*) ***npn*** transistor.
4. Describe the transistor action in detail.
5. Explain the operation of transistor as an amplifier.
6. Name the three possible transistor connections.
7. Define α. Show that it is always less than unity.
8. Draw the input and output characteristics of *CB* connection. What do you infer from these characteristics ?
9. Define β. Show that : $\beta = \frac{\alpha}{1-\alpha}$.
10. How will you determine the input and output characteristics of *CE* connection experimentally ?
11. Establish the following relations :

(*i*) $I_C = \alpha I_E + I_{CBO}$

(*ii*) $I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

(*iii*) $I_C = \beta I_B + I_{CEO}$

(*iv*) $\gamma = \frac{1}{1-\alpha}$

(*v*) $I_E = (\beta + 1) I_B + (\beta + 1) I_{CBO}$

12. How will you draw d.c. load line on the output characteristics of a transistor ? What is its importance?
13. Explain the following terms : (*i*) voltage gain (*ii*) power gain (*iii*) effective collector load.
14. Write short notes on the following : (*i*) advantages of transistors (*ii*) operating point (*iii*) d.c. load line.

Problems

1. In a transistor if I_C = 4.9mA and I_E = 5mA, what is the value of α ? **[0.98]**
2. In a transistor circuit, I_E = 1mA and I_C = 0.9mA. What is the value of I_B ? **[0.1 mA]**
3. Find the value of β if α = 0.99. **[100]**
4. In a transistor, β = 45, the voltage across 5kΩ resistance which is connected in the collector circuit is 5 volts. Find the base current. **[0.022 mA]**
5. In a transistor, I_B = 68 μA, I_E = 30 mA and β = 440. Find the value of α. Hence determine the value of I_C. **[0.99 ; 29.92 mA]**
6. The maximum collector current that a transistor can carry is 500 mA. If β = 300, what is the maximum allowable base current for the device ? **[1.67 mA]**
7. For the circuit shown in Fig. 8.69, draw the d.c. load line.

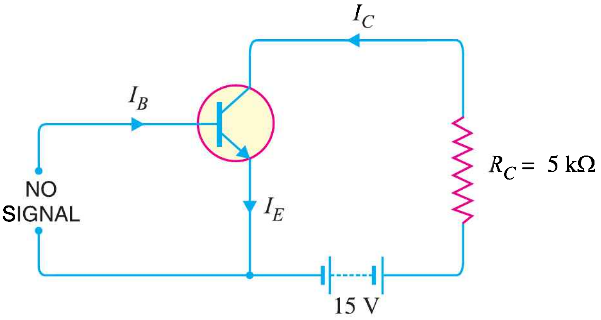


Fig. 8.69

8. Draw the d.c. load line for Fig. 8.70.

[The end points of load line are **6.06 mA** and **20 V]**

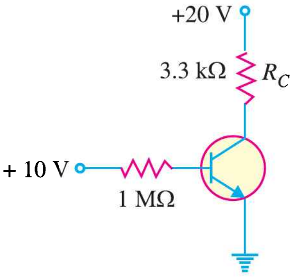


Fig. 8.70

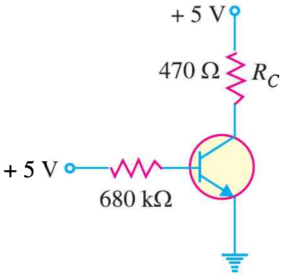


Fig. 8.71

9. If the collector resistance R_C in Fig. 8.70 is reduced to 1 kΩ, what happens to the d.c. load line ?

[The end points of d.c. load line are now **20 mA** and **20 V]**

10. Draw the d.c. load line for Fig. 8.71.

[The end points of d.c. load line are **10.6 mA** and **5V]**

11. If the collector resistance R_C in Fig. 8.71 is increased to 1 kΩ, what happens to the d.c. load line ?

[The end points of d.c. load line are now **5 mA** and **5 V]**

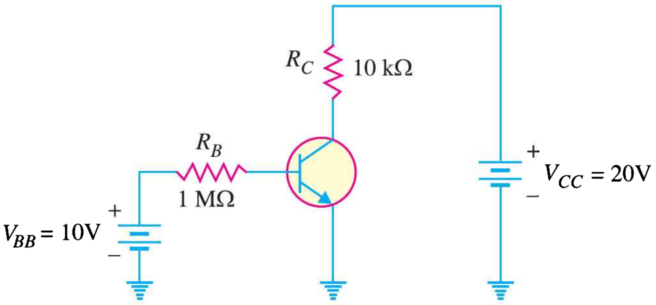

R_C
10 kΩ
R_B
1 MΩ
V_{BB} = 10V
+
–
+
V_{CC} = 20V
–

Fig. 8.72

12. Determine the intercept points of the d.c. load line on the vertical and horizontal axes of the collector curves in Fig. 8.72. **[2 mA ; 20 V]**

13. For the circuit shown in Fig. 8.73, find (*i*) the state of the transistor and (*ii*) transistor power. **[(*i*) active (*ii*) 4.52 mW]**

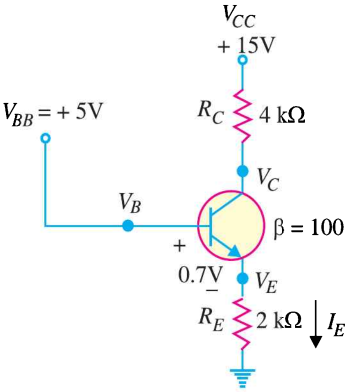

V_{CC}
+ 15V
V_{BB} = + 5V
R_C
4 kΩ
V_C
V_B
β = 100
+
0.7V
–
V_E
R_E
2 kΩ
I_E

Fig. 8.73

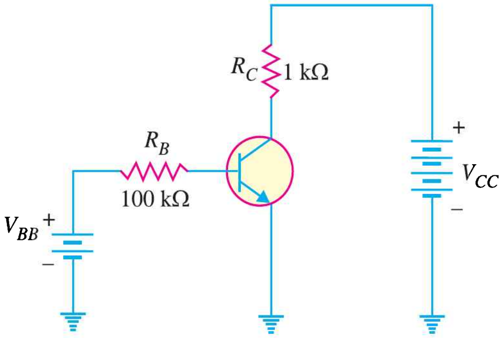

R_C
1 kΩ
R_B
100 kΩ
V_{BB}
+
–
+
V_{CC}
–

Fig. 8.74

14. A base current of 50 μA is applied to the transistor in Fig. 8.74 and a voltage of 5V is dropped across R_C. Calculate α for the transistor. **[0.99]**

15. A certain transistor is to be operated at a collector current of 50 mA. How high can V_{CE} go without exceeding $P_{D\,(max)}$ of 1.2 W ? **[24 V]**

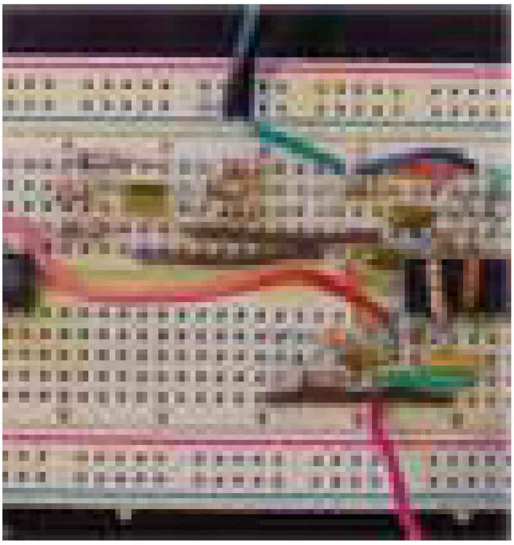
Discussion Questions

1. Why is a transistor low powered device ?
2. What is the significance of arrow in the transistor symbol ?
3. Why is collector wider than emitter and base ?
4. Why is collector current slightly less than emitter current ?
5. Why is base made thin ?

9

Transistor Biasing

9.1 Faithful Amplification
9.2 Transistor Biasing
9.3 Inherent Variations of Transistor Parameters
9.4 Stabilisation
9.5 Essentials of a Transistor Biasing Circuit
9.6 Stability Factor
9.7 Methods of Transistor Biasing
9.8 Base Resistor Method
9.9 Emitter Bias Circuit
9.10 Circuit Analysis of Emitter Bias
9.11 Biasing with Collector Feedback Resistor
9.12 Voltage Divider Bias Method
9.13 Stability Factor for Potential Divider Bias
9.14 Design of Transistor Biasing Circuits
9.15 Mid-Point Biasing
9.16 Which Value of β to be used?
9.17 Miscellaneous Bias Circuits
9.18 Silicon Versus Germanium
9.19 Instantaneous Current and Voltage Waveforms
9.20 Summary of Transistor Bias Circuits



INTRODUCTION

The basic function of transistor is to do amplification. The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. This increase in magnitude of the signal without any change in shape is known as *faithful amplification*. In order to achieve this, means are provided to ensure that input circuit (*i.e.* base-emitter junction) of the transistor remains forward biased and output circuit (*i.e.* collector-base junction) always remains reverse biased during all parts of the signal. This is known as transistor biasing. In this chapter, we shall discuss how transistor biasing helps in achieving faithful amplification.

9.1 Faithful Amplification

The process of raising the strength of a weak signal without any change in its general shape is known as **faithful amplification.**

The theory of transistor reveals that it will function properly if its input circuit (*i.e.* base-emitter junction) remains forward biased and output circuit (*i.e.* collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied :

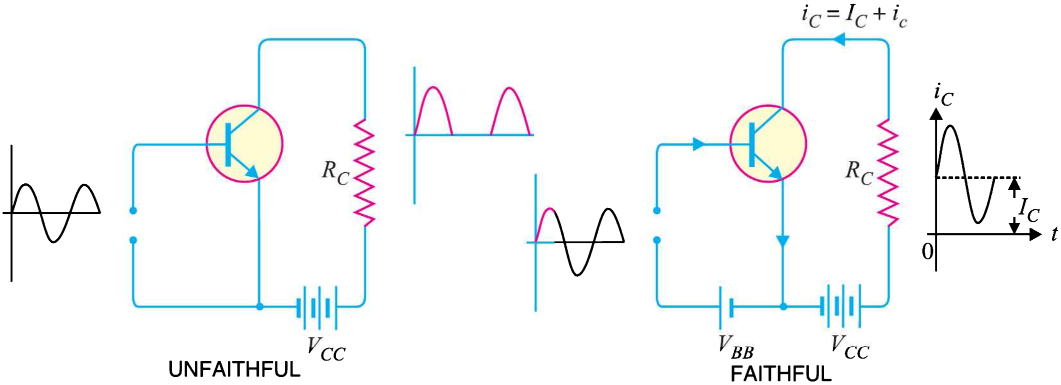
(*i*) Proper zero signal collector current

(*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant

(*iii*) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (*i*) and (*ii*) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (*iii*) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics *i.e.* between saturation to cut off.

(*i*) Proper zero signal collector current. Consider an *npn* transistor circuit shown in Fig. 9.1 (*i*). During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base-emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half-cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.



UNFAITHFUL AMPLIFICATION

(*i*)

FAITHFUL AMPLIFICATION

(*ii*)

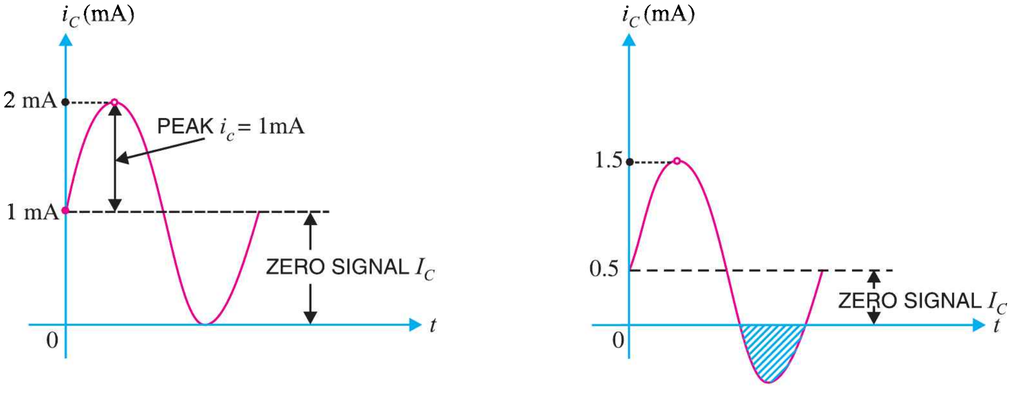
Fig. 9.1

Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. 9.1 (*ii*). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as *zero signal collector current* I_C. During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. *The value of zero signal collector current should be atleast equal to the maximum collector current due to signal alone i.e.*

Zero signal collector current ≥ Max. collector current due to signal alone

Illustration. Suppose a signal applied to the base of a transistor gives a peak collector current of 1mA. Then zero signal collector current must be atleast equal to 1mA so that even during the peak of negative half-cycle of the signal, there is no cut off as shown in Fig. 9.2 (*i*).

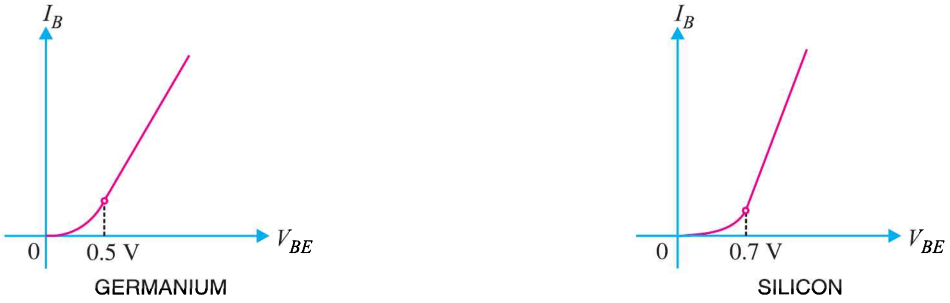
If zero signal collector current is less, say 0.5 mA as shown in Fig. 9.2 (*ii*), then some part (shaded portion) of the negative half-cycle of signal will be cut off in the output.



(*i*) (*ii*)

Fig. 9.2

(*ii*) **Proper minimum base-emitter voltage.** In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for *Si* transistors at any instant.



(*i*) (*ii*)

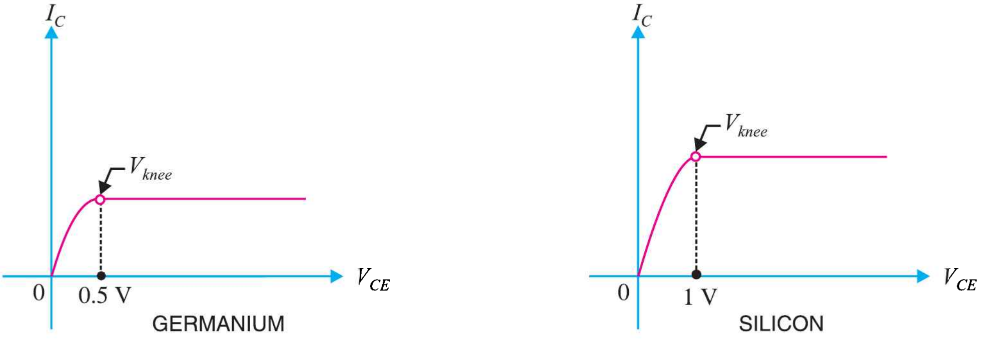
Fig. 9.3

The base current is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for *Si* transistors as shown in Fig. 9.3. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current. This will result in unfaithful amplification.

(*iii*) **Proper minimum V_{CE} at any instant.** For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called *knee voltage* (See Fig. 9.4).

---

* In practice, a.c. signals have small voltage level (< 0.1V) and if applied directly will not give any collector current.



(*i*) (*ii*)

Fig. 9.4

When V_{CE} is too low (less than 0.5V for *Ge* transistors and 1V for *Si* transistors), the collector-base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if V_{CE} is allowed to fall below V_{knee} during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when V_{CE} is greater than V_{knee}, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

9.2 Transistor Biasing

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely : (*i*) proper zero signal collector current, (*ii*) proper base-emitter voltage at any instant and (*iii*) proper collector-emitter voltage at any instant. It is the fulfilment of these conditions which is known as transistor biasing.

The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as **transistor biasing.**

The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as *biasing circuit*. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

Example 9.1. *An npn silicon transistor has V_{CC} = 6 V and the collector load R_C = 2.5 kΩ. Find :*

(i) The maximum collector current that can be allowed during the application of signal for faithful amplification.

(ii) The minimum zero signal collector current required.

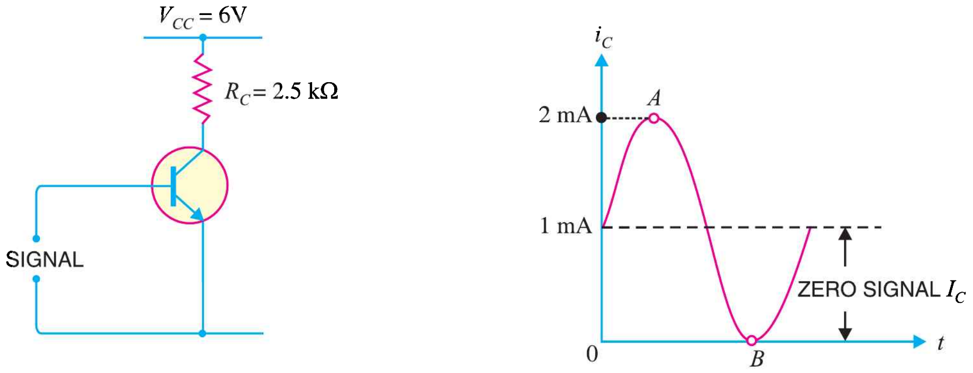
Solution. Collector supply voltage, V_{CC} = 6 V

Collector load, R_C = 2.5 kΩ

(***i***) We know that for faithful amplification, V_{CE} should not be less than 1V for silicon transistor.

∴ Max. voltage allowed across R_C = 6 − 1 = 5 V

∴ Max. allowed collector current = 5 V/R_C = 5 V/2.5 kΩ = **2 mA**



(*i*) (*ii*)

Fig. 9.5

Thus, the maximum collector current allowed during any part of the signal is 2 mA. If the collector current is allowed to rise above this value, V_{CE} will fall below 1 V. Consequently, value of β will fall, resulting in unfaithful amplification.

(***ii***) During the negative peak of the signal, collector current can at the most be allowed to become zero. As the negative and positive half cycles of the signal are equal, therefore, the change in collector current due to these will also be equal but in opposite direction.

∴ Minimum zero signal collector current required = 2 mA/2 = **1 mA**

During the positive peak of the signal [point *A* in Fig. 9.5 (*ii*)], $i_C = 1 + 1 = 2$mA and during the negative peak (point *B*),

$$i_C = 1 - 1 = 0 \text{ mA}$$

Example 9.2. *A transistor employs a 4 kΩ load and V_{CC} = 13V. What is the maximum input signal if β = 100 ? Given V_{knee} = 1V and a change of 1V in V_{BE} causes a change of 5mA in collector current.*

Solution.

Collector supply voltage, V_{CC} = 13 V

Knee voltage, V_{knee} = 1 V

Collector load, R_C = 4 kΩ

∴ Max. allowed voltage across R_C = 13 − 1 = 12 V

∴ Max. allowed collector current, $i_C = \dfrac{12 \text{ V}}{R_C} = \dfrac{12 \text{ V}}{4 \text{ k}\Omega} = 3 \text{ mA}$

Maximum base current, $i_B = \dfrac{i_C}{\beta} = \dfrac{3 \text{ mA}}{100} = 30\ \mu\text{A}$

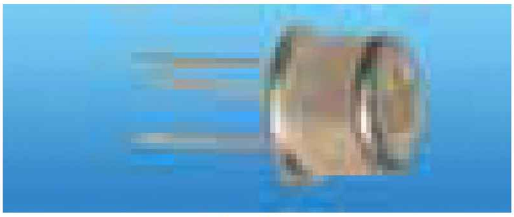
Now $\dfrac{\text{Collector current}}{\text{Base voltage (signal voltage)}} = 5 \text{ mA/V}$

∴ Base voltage (signal voltage) $= \dfrac{\text{Collector current}}{5 \text{ mA/V}} = \dfrac{3 \text{ mA}}{5 \text{ mA/V}} = \mathbf{600\ mV}$

9.3 Inherent Variations of Transistor Parameters

In practice, the transistor parameters such as β, V_{BE} are not the same for every transistor even of the same type. To give an example, BC147 is a silicon *npn* transistor with β varying from 100 to 600 *i.e.* β for one transistor may be 100 and for the other it may be 600, although both of them are *BC*147.

This large variation in parameters is a characteristic of transistors. The major reason for these variations is that transistor is a new device and manufacturing techniques have not too much advanced. For instance, it has not been possible to control the base width and it may vary, although slightly, from one transistor to the other even of the same type. Such small variations result in large change in transistor parameters such as β, V_{BE} etc.



Transistor

The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification. It is, therefore, very important that biasing network be so designed that it should be able to work with all transistors of one type whatever may be the spread in β or V_{BE}. In other words, the operating point should be independent of transistor parameters variations.

9.4 Stabilisation

The collector current in a transistor changes rapidly when

(*i*) the temperature changes,

(*ii*) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (*i.e.* zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates to make the operating point independent of these variations. This is known as stabilisation.

The process of making operating point independent of temperature changes or variations in transistor parameters is known as **stabilisation.**

Once stabilisation is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor *i.e.* the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation. Stabilisation of the operating point is necessary due to the following reasons :

(*i*) Temperature dependence of I_C

(*ii*) Individual variations

(*iii*) Thermal runaway

(*i*) **Temperature dependence of I_C.** The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point *i.e.* to hold I_C constant inspite of temperature variations.

(*ii*) **Individual variations.** The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilise the operating point *i.e.* to hold I_C constant irrespective of individual variations in transistor parameters.

(*iii*) **Thermal runaway.** The collector current for a *CE* configuration is given by :

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \quad ...(i)$$

The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CBO} also increases. It is clear from exp. (*i*) that if I_{CBO} increases, the collector current I_C increases by $(\beta + 1)\, I_{CBO}$. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out.

The self-destruction of an unstabilised transistor is known as **thermal runaway.**

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised *i.e.* I_C is kept constant. In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in βI_B will compensate for the increase in $(\beta + 1)\, I_{CBO}$, keeping I_C nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

9.5 Essentials of a Transistor Biasing Circuit

It has already been discussed that transistor biasing is required for faithful amplification.

The biasing network associated with the transistor should meet the following requirements :

(*i*) It should ensure proper zero signal collector current.

(*ii*) It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silicon transistors at any instant.

(*iii*) It should ensure the stabilisation of operating point.

9.6 Stability Factor

It is desirable and necessary to keep I_C constant in the face of variations of I_{CBO} (sometimes represented as I_{CO}). The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor S. It is defined as under :

*The rate of change of collector current I_C w.r.t. the collector leakage current *I_{CO} at constant β and I_B is called* **stability factor** *i.e.*

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}. Thus a stability factor 50 of a circuit means that I_C changes 50 times as much as any change in I_{CO}. In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible. The ideal value of S is 1 but it is never possible to achieve it in practice. Experience shows that values of S exceeding 25 result in unsatisfactory performance.

The general expression of stability factor for a C.E. configuration can be obtained as under:

$$I_C = \beta I_B + (\beta + 1)\, I_{CO}$$

** Differentiating above expression *w.r.t.* I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

or
$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad \left[\because \frac{dI_{CO}}{dI_C} = \frac{1}{S}\right]$$

or
$$S = \frac{\beta + 1}{1 - \beta\left(\dfrac{dI_B}{dI_C}\right)}$$

---

* $I_{CBO} = I_{CO}$ = collector leakage current in *CB* arrangement

** Assuming β to be independent of I_C

9.7 Methods of Transistor Biasing

In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery V_{BB} which was separate from the battery V_{CC} used in the output circuit. However, in the interest of simplicity and economy, it is desirable that transistor circuit should have a single source of supply—the one in the output circuit (*i.e.* V_{CC}). The following are the most commonly used methods of obtaining transistor biasing from one source of supply (*i.e.* V_{CC}) :

(*i*) Base resistor method

(*ii*) Emitter bias method

(*iii*) Biasing with collector-feedback resistor

(*iv*) Voltage-divider bias

In all these methods, the same basic principle is employed *i.e.* required value of base current (and hence I_C) is obtained from V_{CC} in the zero signal conditions. The value of collector load R_C is selected keeping in view that V_{CE} should not fall below 0.5 V for germanium transistors and 1 V for silicon transistors.

For example, if $\beta = 100$ and the zero signal collector current I_C is to be set at 1mA, then I_B is made equal to $I_C/\beta = 1/100 = 10\ \mu A$. Thus, the biasing network should be so designed that a base current of 10 μA flows in the zero signal conditions.

9.8 Base Resistor Method

In this method, a high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply for *npn* transistor (See Fig. 9.6) and between base and negative end of supply for *pnp* transistor. Here, the required zero signal base current is provided by V_{CC} and it flows through R_B. It is because now base is positive *w.r.t.* emitter *i.e.* base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.

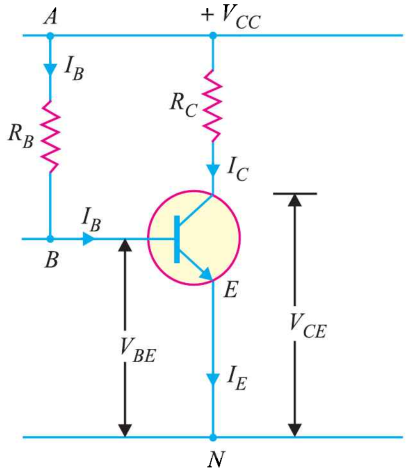


Fig. 9.6

Circuit analysis. It is required to find the value of R_B so that required collector current flows in the zero signal conditions. Let I_C be the required zero signal collector current.

$$\therefore \quad I_B = \frac{I_C}{\beta}$$

Considering the closed circuit *ABENA* and applying Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\text{or} \quad I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad \text{... } (i)$$

As V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual, therefore, value of R_B can be readily found from exp. (*i*).

Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. It then follows from exp. (*i*) that :

$$R_B = \frac{V_{CC}}{I_B}$$

It may be noted that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. Hence, R_B can always be found directly, and for this reason, this method is sometimes called *fixed-bias method.*

Stability factor. As shown in Art. 9.6,

$$\text{Stability factor,} \quad S = \frac{\beta + 1}{1 - \beta\left(\dfrac{dI_B}{dI_C}\right)}$$

In fixed-bias method of biasing, I_B is independent of I_C so that $dI_B/dI_C = 0$. Putting the value of $dI_B / dI_C = 0$ in the above expression, we have,

$$\text{Stability factor,} \quad S = \beta + 1$$

Thus the stability factor in a fixed bias is $(\beta + 1)$. This means that I_C changes $(\beta + 1)$ times as much as any change in I_{CO}. For instance, if $\beta = 100$, then $S = 101$ which means that I_C increases 101 times faster than I_{CO}. Due to the large value of S in a fixed bias, it has poor thermal stability.

Advantages :

(*i*) This biasing circuit is very simple as only one resistance R_B is required.

(*ii*) Biasing conditions can easily be set and the calculations are simple.

(*iii*) There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages :

(*i*) This method provides poor stabilisation. It is because there is no means to stop a self-increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.

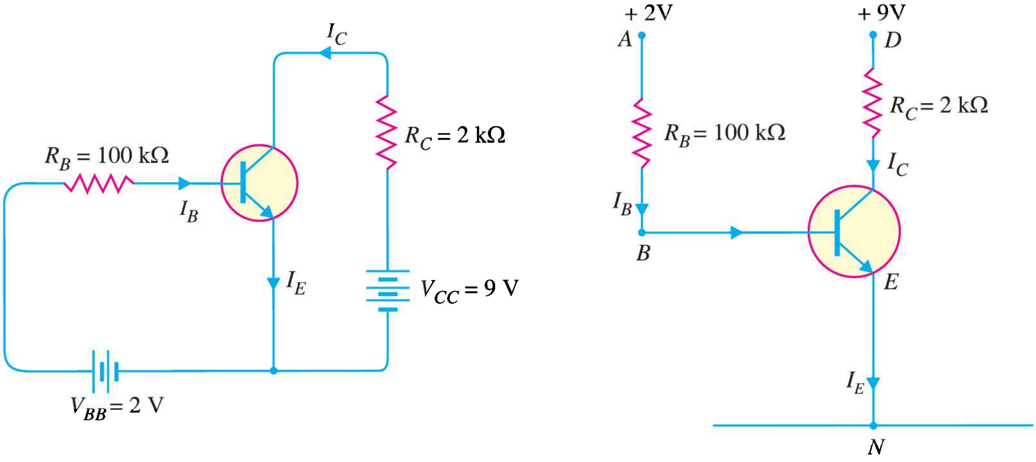
(*ii*) The stability factor is very high. Therefore, there are strong chances of thermal runaway.

Due to these disadvantages, this method of biasing is rarely employed.

Example 9.3. *Fig. 9.7 (i) shows biasing with base resistor method. (i) Determine the collector current I_C and collector-emitter voltage V_{CE}. Neglect small base-emitter voltage. Given that $\beta = 50$.*

(ii) If R_B in this circuit is changed to 50 kΩ, find the new operating point.

Solution.



(*i*) (*ii*)

Fig. 9.7

In the circuit shown in Fig. 9.7 (*i*), biasing is provided by a battery V_{BB} (= 2V) in the base circuit which is separate from the battery V_{CC} (= 9V) used in the output circuit. The same circuit is shown in a simplified way in Fig. 9.7 (*ii*). Here, we need show only the supply voltages, + 2V and + 9V. It may be noted that negative terminals of the power supplies are grounded to get a complete path of current.

(*i*) Referring to Fig.9.7 (*ii*) and applying Kirchhoff 's voltage law to the circuit *ABEN*, we get,

$$I_B R_B + V_{BE} = 2\text{ V}$$

As V_{BE} is negligible,

$$\therefore \quad I_B = \frac{2\text{V}}{R_B} = \frac{2\text{V}}{100\text{ k}\Omega} = 20\ \mu\text{A}$$

$$\text{Collector current, } I_C = \beta I_B = 50 \times 20\ \mu\text{A} = 1000\ \mu\text{A} = \mathbf{1\ mA}$$

Applying Kirchhoff's voltage law to the circuit *DEN*, we get,

$$I_C R_C + V_{CE} = 9$$

or $$1\text{ mA} \times 2\text{ k}\Omega + V_{CE} = 9$$

or $$V_{CE} = 9 - 2 = \mathbf{7\ V}$$

(*ii*) When R_B is made equal to 50 kΩ, then it is easy to see that base current is doubled *i.e.* $I_B = 40\ \mu$A.

$$\therefore \quad \text{Collector current, } I_C = \beta I_B = 50 \times 40 = 2000\ \mu\text{A} = 2\text{ mA}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C R_C = 9 - 2\text{ mA} \times 2\text{ k}\Omega = 5\text{ V}$$

∴ New operating point is **5 V, 2 mA.**

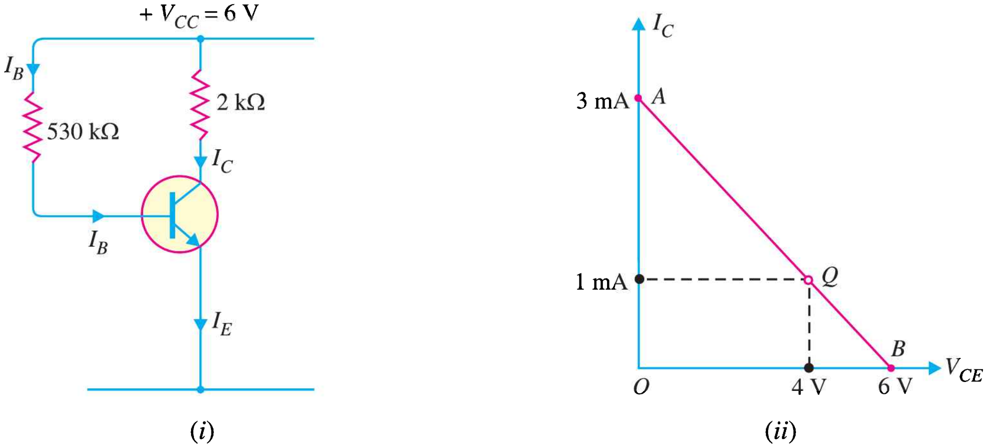
Example 9.4. *Fig. 9.8 (i) shows that a silicon transistor with* β = *100 is biased by base resistor method. Draw the d.c. load line and determine the operating point. What is the stability factor* ?

Solution. $V_{CC} = 6$ V, $R_B = 530$ kΩ, $R_C = 2$ kΩ

D.C. load line. Referring to Fig. 9.8 (*i*), $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} = 6$ V. This locates the first point *B* (*OB* = 6V) of the load line on collector-emitter voltage axis as shown in Fig. 9.8 (*ii*).

When $V_{CE} = 0$, $I_C = V_{CC}/R_C$ = 6V/2 kΩ = 3 mA. This locates the second point *A* (*OA* = 3mA) of the load line on the collector current axis. By joining points *A* and *B*, d.c. load line *AB* is constructed [See Fig. 9.8 (*ii*)].



(*i*) (*ii*)

Fig. 9.8

Operating point Q. As it is a silicon transistor, therefore, $V_{BE} = 0.7\text{V}$. Referring to Fig. 9.8 (*i*), it is clear that :

$$I_B R_B + V_{BE} = V_{CC}$$

or
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{(6 - 0.7)\text{ V}}{530\text{ k}\Omega} = 10\ \mu\text{A}$$

$\therefore$ Collector current, $I_C = \beta I_B = 100 \times 10 = 1000\ \mu\text{A} = 1\text{ mA}$

Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 6 - 1\text{ mA} \times 2\text{ k}\Omega = 6 - 2 = 4\text{ V}$

$\therefore$ Operating point is **4 V, 1 mA.**

Fig. 9.8 (*ii*) shows the operating point Q on the d.c. load line. Its co-ordinates are $I_C = 1\text{mA}$ and $V_{CE} = 4\text{V}$.

$$\text{Stability factor} = \beta + 1 = 100 + 1 = \mathbf{101}$$

Example 9.5. *(i) A germanium transistor is to be operated at zero signal $I_C = 1\text{mA}$. If the collector supply $V_{CC} = 12\text{V}$, what is the value of R_B in the base resistor method ? Take $\beta = 100$.*

(ii) If another transistor of the same batch with $\beta = 50$ is used, what will be the new value of zero signal I_C for the same R_B ?

Solution. $V_{CC} = 12\text{ V}, \quad \beta = 100$

As it is a *Ge* transistor, therefore,

$$V_{BE} = 0.3\text{ V}$$

(*i*) Zero signal $I_C = 1\text{ mA}$

$\therefore$ Zero signal $I_B = I_C/\beta = 1\text{ mA}/100 = 0.01\text{ mA}$

Using the relation, $V_{CC} = I_B R_B + V_{BE}$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.3}{0.01\text{ mA}}$$

$$= 11.7\text{ V}/0.01\text{ mA} = \mathbf{1170\ k\Omega}$$

(*ii*) Now $\beta = 50$

Again using the relation, $V_{CC} = I_B R_B + V_{BE}$

$$\therefore \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.3}{1170\text{ k}\Omega}$$

$$= 11.7\text{ V}/1170\text{ k}\Omega = 0.01\text{ mA}$$

$\therefore$ Zero signal $I_C = \beta I_B = 50 \times 0.01 = \mathbf{0.5\ mA}$

Comments. It is clear from the above example that with the change in transistor parameter β, the zero signal collector current has changed from 1mA to 0.5mA. Therefore, base resistor method cannot provide stabilisation.

Example 9.6. *Calculate the values of three currents in the circuit shown in Fig. 9.9.*

Solution. Applying Kirchhoff's voltage law to the base side and taking resistances in kΩ and currents in mA, we have,

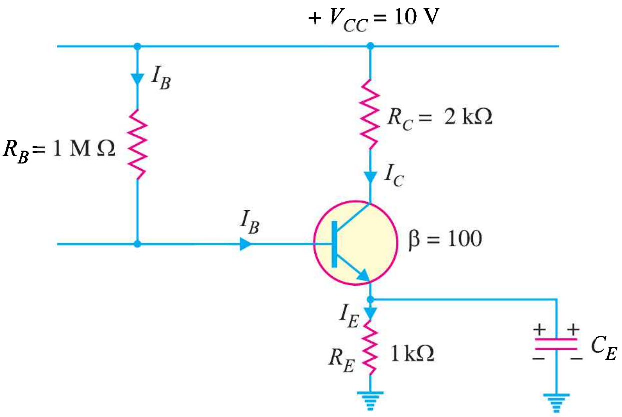


Fig. 9.9

$$
\begin{aligned}
V_{CC} &= I_B R_B + V_{BE} + I_E \times 1 \\
\textit{or} \quad 10 &= 1000\, I_B + {}^{*}0 + (I_C + I_B) \\
\textit{or} \quad 10 &= 1000\, I_B + (\beta\, I_B + I_B) \\
\textit{or} \quad 10 &= 1000\, I_B + (100\, I_B + I_B) \\
\textit{or} \quad 10 &= 1101\, I_B \\
\therefore \quad I_B &= 10/1101 = \mathbf{0.0091\ mA} \\
I_C &= \beta\, I_B = 100 \times 0.0091 = \mathbf{0.91\ mA} \\
I_E &= I_C + I_B = 0.91 + 0.0091 = \mathbf{0.919\ mA}
\end{aligned}
$$

Example 9.7. *Design base resistor bias circuit for a CE amplifier such that operating point is $V_{CE} = 8V$ and $I_C = 2$ mA. You are supplied with a fixed 15V d.c. supply and a silicon transistor with β = 100. Take base-emitter voltage $V_{BE} = 0.6V$. Calculate also the value of load resistance that would be employed.*

Solution. Fig. 9.10 shows *CE* amplifier using base resistor method of biasing.

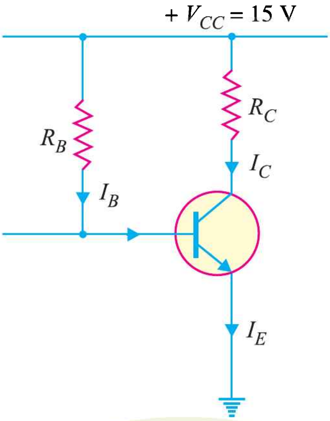


Fig. 9.10

$$
\begin{aligned}
V_{CC} &= 15\text{ V} ;\ \beta = 100 ;\ V_{BE} = 0.6\text{V} \\
V_{CE} &= 8\text{ V} ;\ I_C = 2\text{ mA};\ R_C = ?\ ;\ R_B = ? \\
V_{CC} &= V_{CE} + I_C R_C \\
\text{or} \quad 15\text{ V} &= 8\text{ V} + 2\text{ mA} \times R_C \\
\therefore \quad R_C &= \frac{(15-8)\text{ V}}{2\text{mA}} = \mathbf{3.5\ k\Omega} \\
I_B &= I_C/\beta = 2/100 = 0.02\text{ mA} \\
V_{CC} &= I_B R_B + V_{BE}
\end{aligned}
$$

---

* Neglecting V_{BE} as it is generally very small.

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{(15 - 0.6)\text{ V}}{0.02\text{ mA}} = \mathbf{720\ k\Omega}$$

Example 9.8. *A *base bias circuit in Fig. 9.11 is subjected to an increase in temperature from 25°C to 75°C. If $\beta = 100$ at 25°C and 150 at 75°C, determine the percentage change in Q-point values (V_{CE} and I_C) over this temperature range. Neglect any change in V_{BE} and the effects of any leakage current.*

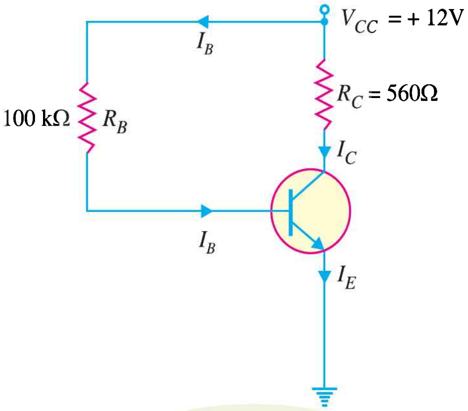


Fig. 9.11

Solution.

At 25°C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{12\ V - 0.7\ V}{100\ k\Omega} = 0.113\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 100 \times 0.113\text{ mA} = 11.3\text{ mA}$$

and $$V_{CE} = V_{CC} - I_C R_C = 12\text{V} - (11.3\text{ mA})(560\Omega) = 5.67\text{V}$$

At 75 °C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega} = 0.113\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 150 \times 0.113\text{ mA} = 17\text{ mA}$$

and $$V_{CE} = V_{CC} - I_C R_C = 12\text{V} - (17\text{ mA})(560\ \Omega) = 2.48\text{V}$$

$$\text{\%age change in } I_C = \frac{I_{C\,(75°C)} - I_{C\,(25°C)}}{I_{C\,(25°C)}} \times 100$$

$$= \frac{17\text{ mA} - 11.3\text{ mA}}{11.3\text{ mA}} \times 100 = \mathbf{50\%}\ (\textit{increase})$$

Note that I_C changes by the same percentage as β.

$$\text{\%age change in } V_{CE} = \frac{V_{CE\,(75°C)} - V_{CE\,(25°C)}}{V_{CE\,(25°C)}} \times 100$$

$$= \frac{2.48\text{V} - 5.67\text{V}}{5.67\text{V}} \times 100 = \mathbf{-56.3\%}\ (\textit{decrease})$$

Comments. It is clear from the above example that Q-point is extremely dependent on β in a base bias circuit. Therefore, base bias circuit is very unstable. Consequently, this method is normally not used if linear operation is required. However, it can be used for switching operation.

Example 9.9. *In base bias method, how Q-point is affected by changes in V_{BE} and I_{CBO}.*

Solution. In addition to being affected by change in β, the Q-point is also affected by changes in V_{BE} and I_{CBO} in the base bias method.

(*i*) Effect of V_{BE}. The base-emitter-voltage V_{BE} decreases with the increase in temperature (and vice-versa). The expression for I_B in base bias method is given by ;

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

---

* Note that base resistor method is also called *base bias method.*

It is clear that decrease in V_{BE} increases I_B. This will shift the Q-point ($I_C = \beta I_B$ and $V_{CE} = V_{CC} - I_C R_C$). The effect of change in V_{BE} is negligible if $V_{CC} >> V_{BE}$ (V_{CC} atleast 10 times greater than V_{BE}).

(*ii*) **Effect of I_{CBO}.** The reverse leakage current I_{CBO} has the effect of decreasing the net base current and thus increasing the base voltage. It is because the flow of I_{CBO} creates a voltage drop across R_B that adds to the base voltage as shown in Fig. 9.12. Therefore, change in I_{CBO} shifts the Q-point of the base bias circuit. However, in modern transistors, I_{CBO} is usually less than 100 nA and its effect on the bias is negligible if $V_{BB} >> I_{CBO} R_B$.

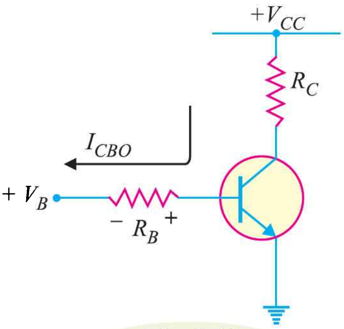
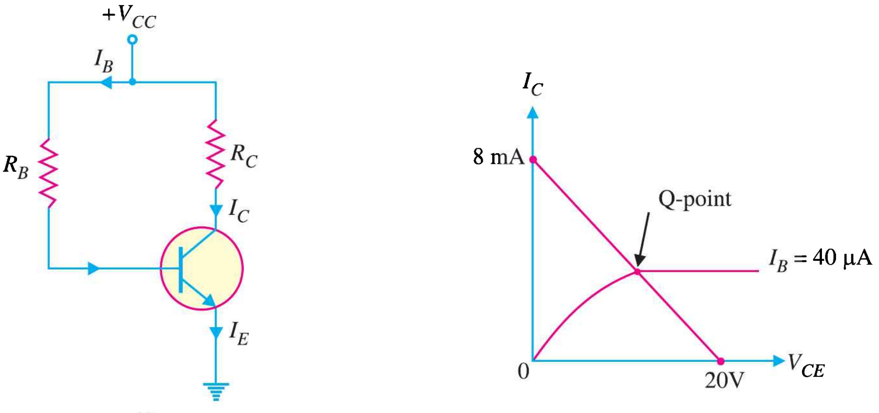


Fig. 9.12

Example 9.10. *Fig. 9.13 (i) shows the base resistor transistor circuit. The device (i.e. transistor) has the characteristics shown in Fig. 9.13 (ii). Determine* V_{CC}, R_C *and* R_B.



(*i*) (*ii*)

Fig. 9.13

Solution. From the d.c load line, V_{CC} = **20V.**

$$\text{Max. } I_C = \frac{V_{CC}}{R_C} \text{ (when } V_{CE} = 0\text{V)}$$

$$\therefore \quad R_C = \frac{V_{CC}}{\text{Max. } I_C} = \frac{20\text{V}}{8\text{mA}} = \mathbf{2.5\ k\Omega}$$

Now
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

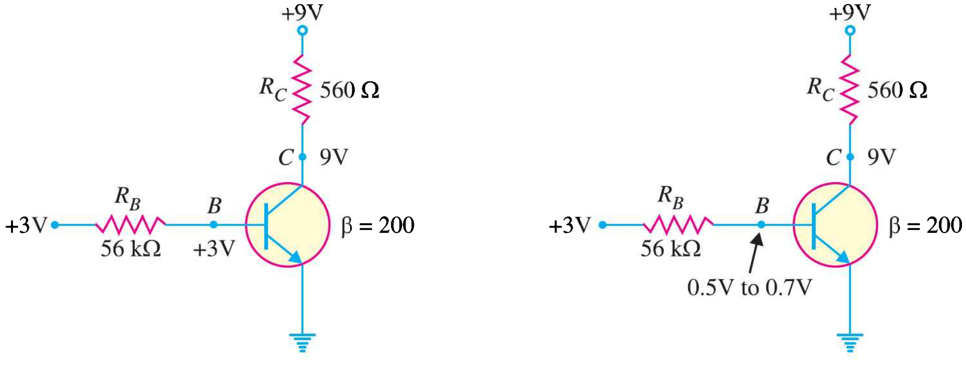
$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{V} - 0.7\text{V}}{40\ \mu\text{A}} = \frac{19.3\text{V}}{40\ \mu\text{A}} = \mathbf{482.5\ k\Omega}$$

Example 9.11. *What fault is indicated in (i) Fig. 9.14 (i) and (ii) Fig. 9.14 (ii) ?*

Solution.

(*i*) The obvious fault in Fig. 9.14 (*i*) is that the **base is internally open.** It is because 3V at the base and 9V at the collector mean that transistor is in cut-off state.

(*ii*) The obvious fault in Fig. 9.14 (*ii*) is that **collector is internally open.** The voltage at the base is correct. The voltage of 9V appears at the collector because the 'open' prevents collector current.



(*i*) (*ii*)

Fig. 9.14

9.9 Emitter Bias Circuit

Fig. 9.15 shows the emitter bias circuit. This circuit differs from base-bias circuit in two important respects. First, it uses two separate d.c. voltage sources ; one positive (+ V_{CC}) and the other negative (– V_{EE}). Normally, the two supply voltages will be equal. For example, if V_{CC} = + 20V (d.c.), then V_{EE} = – 20V (d.c.). Secondly, there is a resistor R_E in the emitter circuit.

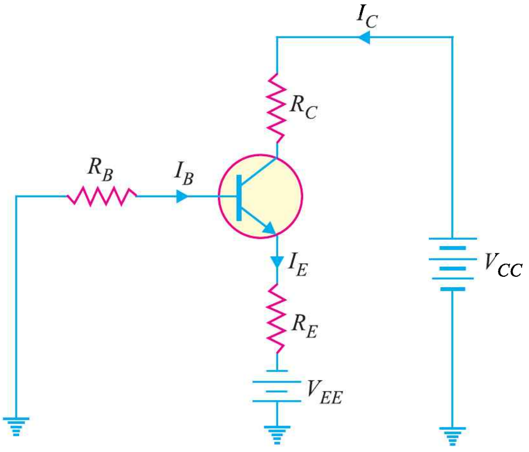


Fig. 9.15

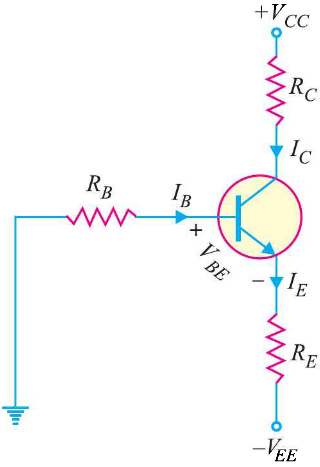


Fig. 9.16

We shall first redraw the circuit in Fig. 9.15 as it usually appears on schematic diagrams. This means deleting the battery symbols as shown in Fig. 9.16. All the information is still (See Fig. 9.16) on the diagram except that it is in condensed form. That is a negative supply voltage – V_{EE} is applied to the bottom of R_E and a positive voltage of + V_{CC} to the top of R_C.

9.10 Circuit Analysis of Emitter Bias

Fig. 9.16 shows the emitter bias circuit. We shall find the Q-point values (*i.e.* d.c. I_C and d.c. V_{CE}) for this circuit.

(*i*) **Collector current (I_C).** Applying Kirchhoff's voltage law to the base-emitter circuit in Fig. 9.16, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\therefore \quad V_{EE} = I_B R_B + V_{BE} + I_E R_E$$

Now $I_C \simeq I_E$ and $I_C = \beta I_B \quad \therefore \; I_B \simeq \dfrac{I_E}{\beta}$

Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $$V_{EE} - V_{BE} = I_E\,(R_B/\beta + R_E)$$

$$\therefore \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, we have,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

(*ii*) Collector-emitter voltage (V_{CE}). Fig. 9.17 shows the various voltages of the emitter bias circuit w.r.t. ground.

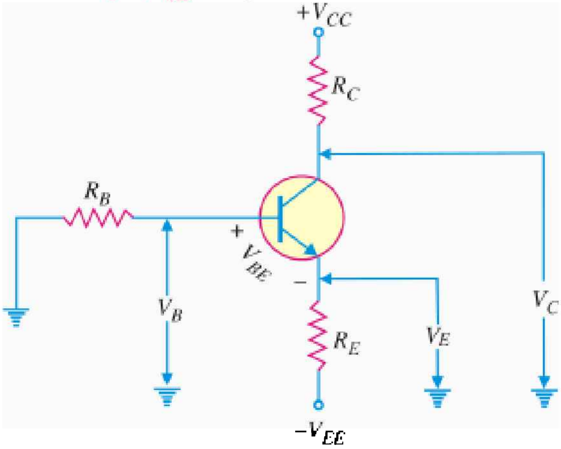


Fig. 9.17

Emitter voltage w.r.t. ground is

$$V_E = -V_{EE} + I_E R_E$$

Base voltage w.r.t. ground is

$$V_B = V_E + V_{BE}$$

Collector voltage w.r.t. ground is

$$V_C = V_{CC} - I_C R_C$$

Subtracting V_E from V_C and using the approximation $I_C \simeq I_E$, we have,

$$V_C - V_E = (V_{CC} - I_C R_C) - (-V_{EE} + I_C R_E) \qquad (\because I_E \simeq I_C)$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C\,(R_C + R_E)$$

Alternatively. Applying Kirchhoff's voltage law to the collector side of the emitter bias circuit in Fig. 9.16 (Refer back), we have,

$$V_{CC} - I_C R_C - V_{CE} - I_C{}^{*} R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C\,(R_C + R_E)$$

Stability of Emitter bias. The expression for collector current I_C for the emitter bias circuit is given by ;

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

---

* $I_C \simeq I_E$

It is clear that I_C is dependent on V_{BE} and β, both of which change with temperature.

If $R_E >> R_B/\beta$, then expression for I_C becomes :

$$I_C = \frac{V_{EE} - V_{BE}}{R_E}$$

This condition makes I_C ($\simeq I_E$) independent of β.

If $V_{EE} >> V_{BE}$, then I_C becomes :

$$I_C (\simeq I_E) = \frac{V_{EE}}{R_E}$$

This condition makes I_C ($\simeq I_E$) independent of V_{BE}.

If I_C ($\simeq I_E$) is independent of β and V_{BE}, the Q-point is not affected appreciably by the variations in these parameters. Thus emitter bias can provide stable Q-point if properly designed.

Example 9.12. *For the emitter bias circuit shown in Fig. 9.18, find I_E, I_C, V_C and V_{CE} for $\beta = 85$ and $V_{BE} = 0.7V$.*

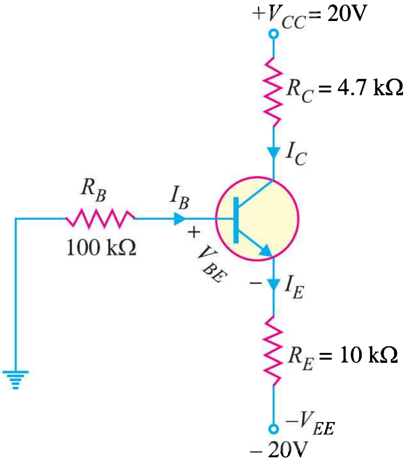


Fig. 9.18

Solution.

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.7V}{10\ k\Omega + 100\ k\Omega/85} = \mathbf{1.73\ mA}$$

$$V_C = V_{CC} - I_C R_C = 20V - (1.73\ mA)\ (4.7\ k\Omega) = \mathbf{11.9V}$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.73\ mA)\ (10\ k\Omega) = -2.7V$$

$$\therefore \quad V_{CE} = V_C - V_E = 11.9 - (-2.7V) = \mathbf{14.6V}$$

Note that operating point (or Q – point) of the circuit is 14.6V, 1.73 mA.

Example 9.13. *Determine how much the Q-point in Fig. 9.18 (above) will change over a temperature range where β increases from 85 to 100 and V_{BE} decreases from 0.7V to 0.6V.*

Solution.

For $\beta = 85$ and $V_{BE} = 0.7V$

As calculated in the above example, $I_C = 1.73$ mA and $V_{CE} = 14.6V$.

For $\beta = 100$ and $V_{BE} = 0.6V$

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.6V}{10\ k\Omega + 100\ k\Omega/100} = \frac{19.4V}{11\ k\Omega} = 1.76\ mA$$

$$V_C = V_{CC} - I_C R_C = 20V - (1.76\ mA)\ (4.7\ k\Omega) = 11.7V$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.76\ mA)\ (10\ k\Omega) = -2.4V$$

$$\therefore \quad V_{CE} = V_C - V_E = 11.7 - (-2.4) = 14.1\text{V}$$

$$\%\text{ age change in } I_C = \frac{1.76\text{ mA} - 1.73\text{ mA}}{1.73\text{ mA}} \times 100 = \mathbf{1.7\%}\ (\textit{increase})$$

$$\%\text{ age change in } V_{CE} = \frac{14.1\text{V} - 14.6\text{V}}{14.1\text{V}} \times 100 = \mathbf{-3.5\%}\ (\textit{decrease})$$

9.11 Biasing with Collector Feedback Resistor

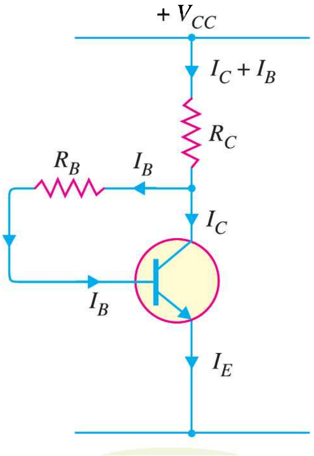


Fig. 9.19

In this method, one end of R_B is connected to the base and the other end to the collector as shown in Fig. 9.19. Here, the required zero signal base current is determined *not* by V_{CC} but by the collector-base voltage V_{CB}. It is clear that V_{CB} forward biases the base-emitter junction and hence base current I_B flows through R_B. This causes the zero signal collector current to flow in the circuit.

Circuit analysis. The required value of R_B needed to give the zero signal current I_C can be determined as follows. Referring to Fig. 9.19,

$$V_{CC} = {}^*I_C R_C + I_B R_B + V_{BE}$$

$$\text{or} \quad R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

$$= \frac{V_{CC} - V_{BE} - \beta\, I_B R_C}{I_B} \qquad (\because I_C = \beta\, I_B)$$

$$\text{Alternatively, } V_{CE} = V_{BE} + V_{CB}$$

$$\text{or} \quad V_{CB} = V_{CE} - V_{BE}$$

$$\therefore \quad R_B = \frac{V_{CB}}{I_B} = \frac{V_{CE} - V_{BE}}{I_B}\,; \quad \text{where} \quad I_B = \frac{I_C}{\beta}$$

It can be shown mathematically that stability factor S for this method of biasing is less than $(\beta + 1)$ *i.e.*

Stability factor, $S < (\beta + 1)$

Therefore, this method provides better thermal stability than the fixed bias.

Note. It can be easily proved (See **example 9.17) that Q-point values (I_C and V_{CE}) for the circuit shown in Fig. 9.19 are given by ;

$$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C}$$

$$\text{and} \quad V_{CE} = V_{CC} - I_C R_C$$

Advantages

(*i*) It is a simple method as it requires only one resistance R_B.

(*ii*) This circuit provides some stabilisation of the operating point as discussed below :

$$V_{CE} = V_{BE} + V_{CB}$$

---

* Actually voltage drop across $R_C = (I_B + I_C)\, R_C$.
However, $I_B << I_C$. Therefore, as a reasonable approximation, we can say that drop across $R_C = I_C R_C$.

** Put $R_E = 0$ for the expression of I_C in exmaple 9.17. It is because in the present circuit (Fig. 9.19), there is no R_E.

Suppose the temperature increases. This will increase collector leakage current and hence the total collector current. But as soon as collector current increases, V_{CE} decreases due to greater drop across R_C. The result is that V_{CB} decreases *i.e.* lesser voltage is available across R_B. Hence the base current I_B decreases. The smaller I_B tends to decrease the collector current to original value.

Disadvantages

(*i*) The circuit does not provide good stabilisation because stability factor is fairly high, though it is lesser than that of fixed bias. Therefore, the operating point does change, although to lesser extent, due to temperature variations and other effects.

(*ii*) This circuit provides a negative feedback which reduces the gain of the amplifier as explained hereafter. During the positive half-cycle of the signal, the collector current increases. The increased collector current would result in greater voltage drop across R_C. This will reduce the base current and hence collector current.

Example 9.14. *Fig. 9.20 shows a silicon transistor biased by collector feedback resistor method. Determine the operating point. Given that* $\beta = 100$.

Solution. $V_{CC} = 20\text{V}, R_B = 100\text{ k}\Omega, R_C = 1\text{k}\Omega$

Since it is a silicon transistor, $V_{BE} = 0.7\text{ V}$.

Assuming I_B to be in mA and using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - \beta\, I_B R_C}{I_B}$$

or $$100 \times I_B = 20 - 0.7 - 100 \times I_B \times 1$$

or $$200\, I_B = 19.3$$

or $$I_B = \frac{19.3}{200} = 0.096\text{ mA}$$

∴ Collector current, $I_C = \beta\, I_B = 100 \times 0.096 = 9.6\text{ mA}$

Collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 20 - 9.6\text{ mA} \times 1\text{ k}\Omega = 10.4\text{ V}$$

∴ Operating point is **10.4 V, 9.6 mA.**

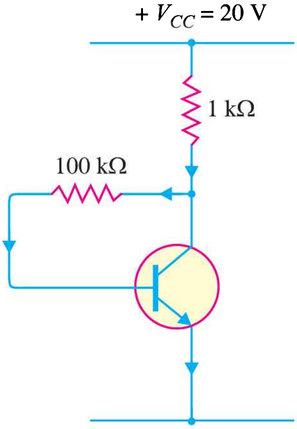


Fig. 9.20

Alternatively

$$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{20\text{V} - 0.7\text{V}}{100\text{ k}\Omega/100 + 1\text{ k}\Omega} = \frac{19.3\text{V}}{2\text{ k}\Omega} = \mathbf{9.65\text{ mA}}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{V} - 9.65\text{ mA} \times 1\text{ k}\Omega = \mathbf{10.35V}$$

A very slight difference in the values is due to manipulation of calculations.

Example 9.15. *(i) It is required to set the operating point by biasing with collector feedback resistor at* $I_C = 1\text{mA}$, $V_{CE} = 8\text{V}$. *If* $\beta = 100$, $V_{CC} = 12\text{V}$, $V_{BE} = 0.3\text{V}$, *how will you do it ?*

(*ii*) *What will be the new operating point if* $\beta = 50$, *all other circuit values remaining the same ?*

Solution. $V_{CC} = 12\text{V}, V_{CE} = 8\text{V}, I_C = 1\text{mA}$

$\beta = 100, V_{BE} = 0.3\text{V}$

(*i*) To obtain the required operating point, we should find the value of R_B.

Now, collector load is

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{(12 - 8)\text{ V}}{1\text{ mA}} = 4\text{ k}\Omega$$

Also $$I_B = \frac{I_C}{\beta} = \frac{1\text{ mA}}{100} = 0.01\text{ mA}$$

Using the relation, $$R_B = \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B}$$

$$= \frac{12 - 0.3 - 100 \times 0.01 \times 4}{0.01} = \mathbf{770\text{ k}\Omega}$$

(*ii*) Now $\beta = 50$, and other circuit values remain the same.

∴ $$V_{CC} = V_{BE} + I_B R_B + \beta I_B R_C$$

or $$12 = 0.3 + I_B (R_B + \beta R_C)$$

or $$11.7 = I_B (770 + 50 \times 4)$$

or $$I_B = \frac{11.7\text{ V}}{970\text{ k}\Omega} = 0.012\text{ mA}$$

∴ Collector current, $I_C = \beta I_B = 50 \times 0.012 = 0.6\text{ mA}$

∴ Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 12 - 0.6\text{ mA} \times 4\text{ k}\Omega = 9.6\text{ V}$

∴ New operating point is **9.6 V, 0.6 mA.**

Comments. It may be seen that operating point is changed when a new transistor with lesser β is used. Therefore, biasing with collector feedback resistor does not provide very good stabilisation. It may be noted, however, that change in operating point is less than that of base resistor method.

Example 9.16. *It is desired to set the operating point at 2V, 1mA by biasing a silicon transistor with collector feedback resistor R_B. If $\beta = 100$, find the value of R_B.*

Solution.

For a silicon transistor,

$$V_{BE} = 0.7\text{ V}$$

$$I_B = \frac{I_C}{\beta} = 1/100 = 0.01\text{ mA}$$

Now $$V_{CE} = V_{BE} + V_{CB}$$

or $$2 = 0.7 + V_{CB}$$

∴ $$V_{CB} = 2 - 0.7 = 1.3\text{ V}$$

∴ $$R_B = \frac{V_{CB}}{I_B} = \frac{1.3\text{V}}{0.01\text{ mA}} = \mathbf{130\text{ k}\Omega}$$

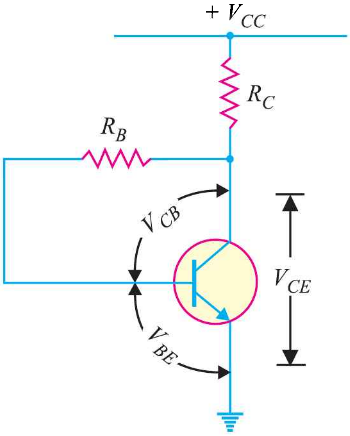


Fig. 9.21

Example 9.17. *Find the Q-point values (I_C and V_{CE}) for the collector feedback bias circuit shown in Fig. 9.22.*

Solution. Fig. 9.22 shows the currents in the three resistors (R_C, R_B and R_E) in the circuit. By following the path through V_{CC}, R_C, R_B, V_{BE} and R_E and applying Kirchhoff's voltage law, we have,

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

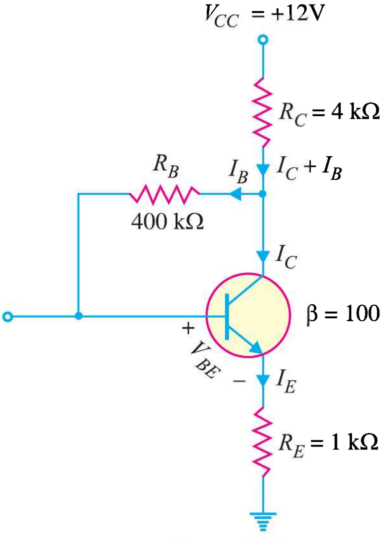


Fig. 9.22

Now $I_B + I_C \simeq I_C$; $I_E \simeq I_C$ and $I_B = \dfrac{I_C}{\beta}$

$$\therefore \quad V_{CC} - I_C R_C - \frac{I_C}{\beta} R_B - V_{BE} - I_C R_E = 0$$

$$\text{or} \quad I_C \left(R_E + \frac{R_B}{\beta} + R_C\right) = V_{CC} - V_{BE}$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$$

Putting the given circuit values, we have,

$$I_C = \frac{12\text{V} - 0.7\text{V}}{1\text{ k}\Omega + 400\text{ k}\Omega/100 + 4\text{ k}\Omega}$$

$$= \frac{11.3\text{V}}{9\text{ k}\Omega} = 1.26\text{ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 12\text{V} - 1.26\text{ mA } (4\text{k}\Omega + 1\text{ k}\Omega)$$

$$= 12\text{V} - 6.3\text{V} = 5.7\text{V}$$

∴ The operating point is **5.7V, 1.26 mA.**

Example 9.18. *Find the d.c. bias values for the collector-feedback biasing circuit shown in Fig. 9.23. How does the circuit maintain a stable Q point against temperature variations ?*

Solution. The collector current is

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$$

$$= \frac{10\text{V} - 0.7\text{V}}{0 + 100\text{ k}\Omega/100 + 10\text{ k}\Omega}$$

$$= \frac{9.3\text{V}}{11\text{ k}\Omega} = 0.845\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 10\text{V} - 0.845\text{ mA} \times 10\text{ k}\Omega$$

$$= 10\text{V} - 8.45\text{ V} = 1.55\text{V}$$

∴ Operating point is **1.55V, 0.845 mA.**

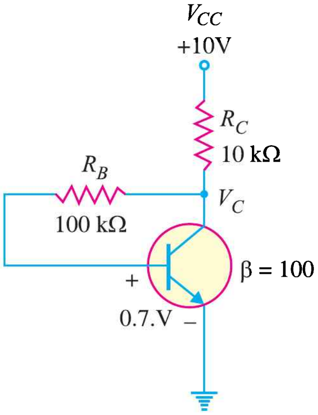


Fig. 9.23

Stability of Q-point. We know that β varies directly with temperature and V_{BE} varies inversely with temperature. As the temperature goes up, β goes up and V_{BE} goes down. The increase in β increases I_C (= βI_B). The decrease in V_{BE} increases I_B which in turn increases I_C. As I_C tries to increase, the voltage drop across R_C (= $I_C R_C$) also tries to increases. This tends to reduce collector voltage V_C (See Fig. 9.23) and, therefore, the voltage across R_B. The reduced voltage across R_B reduces I_B and offsets the attempted increase in I_C and attempted decrease in V_C. The result is that the collector-feedback circuit maintains a stable Q-point. The reverse action occurs when the temperature decreases.

9.12 Voltage Divider Bias Method

This is the most widely used method of providing biasing and stabilisation to a transistor. In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC} (See Fig. 9.24) and provide biasing. The emitter resistance R_E provides stabilisation. The name "voltage divider" comes from the voltage divider formed by R_1 and R_2. The voltage drop across R_2 forward biases the base-emitter junction. This causes the base current and hence collector current flow in the zero signal conditions.

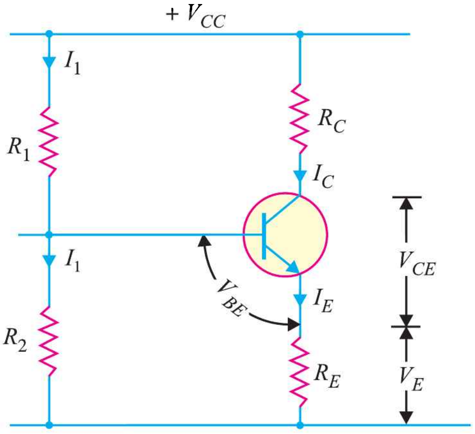


Fig. 9.24

Circuit analysis. Suppose that the current flowing through resistance R_1 is I_1. As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1.

(*i*) **Collector current $\mathbf{I_C}$:**

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

∴ Voltage across resistance R_2 is

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Applying Kirchhoff's voltage law to the base circuit of Fig. 9.24,

$$V_2 = V_{BE} + V_E$$

or $$V_2 = V_{BE} + I_E R_E$$

or $$I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \simeq I_C$

∴ $$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \text{...}(i)$$

It is clear from exp. (*i*) above that I_C does not at all depend upon β. Though I_C depends upon V_{BE} but in practice $V_2 >> V_{BE}$ so that I_C is practically independent of V_{BE}. Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilisation is ensured. It is due to this reason that potential divider bias has become universal method for providing transistor biasing.

(*ii*) **Collector-emitter voltage $\mathbf{V_{CE}}$.** Applying Kirchhoff's voltage law to the collector side,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + I_C R_E \qquad (\because I_E \simeq I_C)$$

$$= I_C (R_C + R_E) + V_{CE}$$

$$\therefore \quad V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Stabilisation. In this circuit, excellent stabilisation is provided by R_E. Consideration of eq. (*i*) reveals this fact.

$$V_2 = V_{BE} + I_C R_E$$

Suppose the collector current I_C increases due to rise in temperature. This will cause the voltage drop across emitter resistance R_E to increase. As voltage drop across R_2 (*i.e.* V_2) is *independent of I_C, therefore, V_{BE} decreases. This in turn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Stability factor. It can be shown mathematically (See Art. 9.13) that stability factor of the circuit is given by :

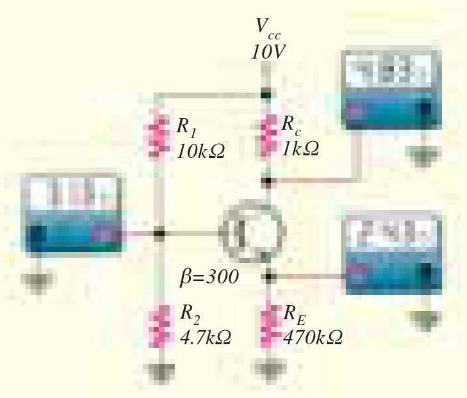
$$\text{Stability factor, } S = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E}$$

$$= (\beta + 1) \times \frac{1 + \frac{R_0}{R_E}}{\beta + 1 + \frac{R_0}{R_E}}$$

$$\text{where } R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

If the ratio R_0/R_E is very small, then R_0/R_E can be neglected as compared to 1 and the stability factor becomes :

$$\text{Stability factor} = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$



A voltage divider biased transistor with correct voltages

This is the smallest possible value of S and leads to the maximum possible thermal stability. Due to design **considerations, R_0 / R_E has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

Example 9.19. *Fig. 9.25 (i) shows the voltage divider bias method. Draw the d.c. load line and determine the operating point. Assume the transistor to be of silicon.*

Solution.

d.c. load line. The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

When $I_C = 0$, $V_{CE} = V_{CC} = 15\text{V}$. This locates the first point *B* (*OB* = 15V) of the load line on the collector-emitter voltage axis.

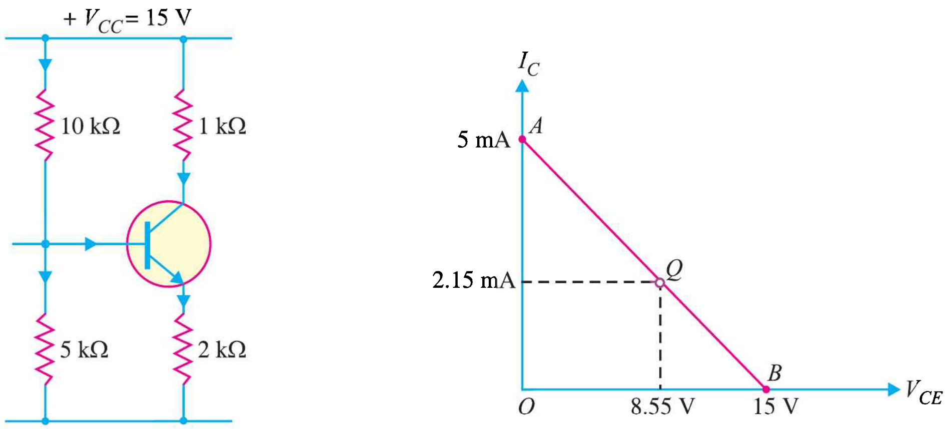
$$\text{When } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15 \text{ V}}{(1 + 2) \text{ k}\Omega} = 5 \text{ mA}$$

This locates the second point *A* (*OA* = 5 mA) of the load line on the collector current axis. By joining points *A* and *B*, the d.c. load line *AB* is constructed as shown in Fig. 9.25 (*ii*).

---

* Voltage drop across $R_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$

** Low value of R_0 can be obtained by making R_2 very small. But with low value of R_2, current drawn from V_{CC} will be large. This puts restrictions on the choice of R_0. Increasing the value of R_E requires greater V_{CC} in order to maintain the same value of zero signal collector current. Therefore, the ratio R_0/R_E cannot be made very small from design point of view.



(*i*) (*ii*)

Fig. 9.25

Operating point. For silicon transistor,

$$V_{BE} = 0.7 \text{ V}$$

Voltage across 5 kΩ is

$$V_2 = \frac{V_{CC}}{10+5} \times 5 = \frac{15 \times 5}{10+5} = 5 \text{ V}$$

$$\therefore \quad \text{Emitter current, } I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{5 - 0.7}{2 \text{ k}\Omega} = \frac{4.3 \text{ V}}{2 \text{ k}\Omega} = 2.15 \text{ mA}$$

∴ Collector current is

$$I_C \simeq I_E = 2.15 \text{ mA}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 15 - 2.15 \text{ mA} \times 3 \text{ k}\Omega = 15 - 6.45 = 8.55 \text{ V}$$

∴ Operating point is **8.55 V, 2.15 mA.**

Fig.9.25 (*ii*) shows the operating point *Q* on the load line. Its co-ordinates are I_C = 2.15 mA, V_{CE} = 8.55 V.

Example 9.20. *Determine the operating point of the circuit shown in the previous problem by using Thevenin's theorem.*

Solution. The circuit is redrawn and shown in Fig. 9.26 (*i*) for facility of reference. The d.c. circuit to the left of base terminal *B* can be replaced by Thevenin's equivalent circuit shown in Fig. 9.26 (*ii*). Looking to the left from the base terminal *B* [See Fig. 9.26 (*i*)], Thevenin's equivalent voltage E_0 is given by :

$$E_0 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \left(\frac{15}{10+5}\right) \times 5 = 5 \text{ V}$$

Again looking to the left from the base terminal *B* [See Fig. 9.26 (*i*)], Thevenin's equivalent resistance R_0 is given by :

$$R_0 = \frac{R_1 \, R_2}{R_1 + R_2}$$

Fig. 9.26 (*ii*) shows the replacement of bias portion of the circuit of Fig. 9.26 (*i*) by its Thevenin's equivalent.

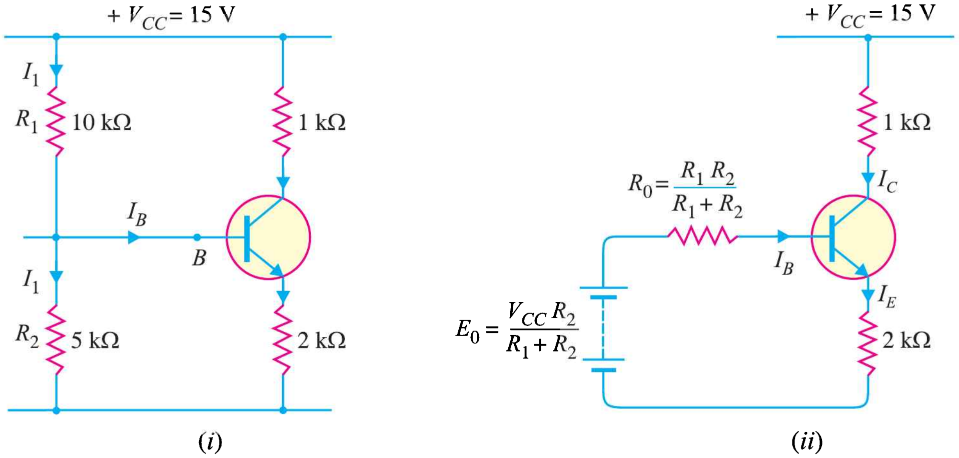


Fig. 9.26

Referring to Fig. 9.26 (*ii*), we have,

$$E_0 = I_B R_0 + V_{BE} + I_E R_E = I_B R_0 + V_{BE} + I_C R_E \qquad (\because I_E \simeq I_C)$$

$$= I_B R_0 + V_{BE} + \beta I_B R_E = I_B (R_0 + \beta R_E) + V_{BE}$$

or
$$I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E}$$

∴ Collector current,
$$I_C = \beta I_B = \frac{\beta(E_0 - V_{BE})}{R_0 + \beta R_E}$$

Dividing the numerator and denominator of R.H.S. by β, we get,

$$I_C = \frac{E_0 - V_{BE}}{\frac{R_0}{\beta} + R_E}$$

As *$R_0/\beta << R_E$, therefore, R_0/β may be neglected as compared to R_E.

∴
$$I_C = \frac{E_0 - V_{BE}}{R_E} = \frac{5 - 0.7}{2\text{ k}\Omega} = 2.15\text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 15 - 2.15\text{ mA} \times 3\text{ k}\Omega$$

$$= 15 - 6.45 = 8.55\text{ V}$$

∴ Operating point is **8.55 V, 2.15 mA.**

Example 9.21. *A transistor uses potential divider method of biasing. R_1 = 50 kΩ, R_2 = 10 kΩ and R_E = 1kΩ. If V_{CC} = 12 V, find :*

(i) the value of I_C ; given V_{BE} = 0.1V

(ii) the value of I_C ; given V_{BE} = 0.3V. Comment on the result.

Solution. R_1 = 50 kΩ, R_2 = 10 kΩ, R_E = 1 kΩ , V_{CC} = 12 V

(*i*) When V_{BE} = 0.1 V,

Voltage across R_2,
$$V_2 = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10}{50 + 10} \times 12 = 2\text{ V}$$

∴ Collector current,
$$I_C = \frac{V_2 - V_{BE}}{R_E} = \frac{2 - 0.1}{1\text{ k}\Omega} = \mathbf{1.9\text{ mA}}$$

---

* In fact, this condition means that I_B is very small as compared to I_1, the current flowing through R_1 and R_2.

(*ii*) When $V_{BE} = 0.3$ V,

$$\text{Collector current, } I_C = \frac{V_2 - V_{BE}}{R_E} = \frac{2 - 0.3}{1\text{ k}\Omega} = \mathbf{1.7\ mA}$$

Comments. From the above example, it is clear that although V_{BE} varies by 300%, the value of I_C changes only by nearly 10%. This explains that in this method, I_C is almost independent of transistor parameter variations.

Example 9.22. *Calculate the emitter current in the voltage divider circuit shown in Fig. 9.27. Also find the value of* V_{CE} *and collector potential* V_C.

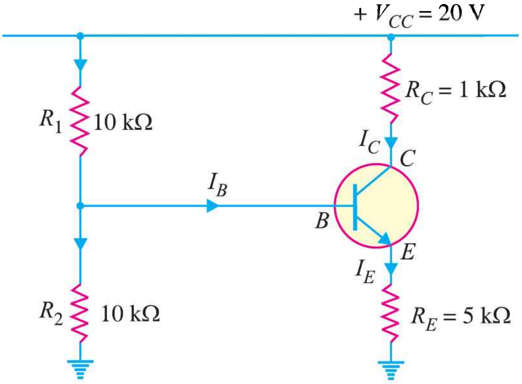


Fig. 9.27

Solution.

$$\text{Voltage across } R_2, V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \left(\frac{20}{10 + 10}\right) 10 = 10\text{ V}$$

Now $\quad V_2 = V_{BE} + I_E R_E$

As V_{BE} is generally small, therefore, it can be neglected.

$$\therefore \quad I_E = \frac{V_2}{R_E} = \frac{10\text{ V}}{5\text{ k}\Omega} = \mathbf{2\ mA}$$

Now $\quad I_C \simeq I_E = 2$ mA

$$\therefore \quad V_{CE} = V_{CC} - I_C (R_C + R_E) = 20 - 2\text{ mA } (6\text{ k}\Omega)$$

$$= 20 - 12 = \mathbf{8\ V}$$

$$\text{Collector potential, } V_C = V_{CC} - I_C R_C = 20 - 2\text{ mA} \times 1\text{ k}\Omega$$

$$= 20 - 2 = \mathbf{18\ V}$$

9.13 Stability Factor For Potential Divider Bias

We have already seen (See example 9.20) how to replace the potential divider circuit of potential divider bias by Thevenin's equivalent circuit. The resulting potential divider bias circuit is redrawn in Fig. 9.28 in order to find the stability factor *S* for this biasing circuit. Referring to Fig. 9.28 and applying Kirchhoff's voltage law to the base circuit, we have,

$$E_0 - I_B R_0 - V_{BE} - I_E R_E = 0$$

or $\quad E_0 = I_B R_0 + V_{BE} + (I_B + I_C) R_E$

Considering V_{BE} to be constant and differentiating the above equation w.r.t. I_C, we have,

$$0 = R_0 \frac{dI_B}{dI_C} + 0 + R_E \frac{dI_B}{dI_C} + R_E$$

or $$0 = \frac{dI_B}{dI_C}(R_0 + R_E) + R_E$$

$$\therefore \quad \frac{dI_B}{dI_C} = \frac{-R_E}{R_0 + R_E} \qquad \text{...}(i)$$

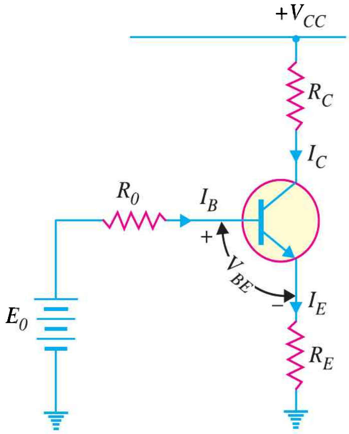


Fig. 9.28

The general expression for stability factor is

$$\text{Stability factor, } S = \frac{\beta + 1}{1 - \beta \dfrac{dI_B}{dI_C}}$$

Putting the value of dI_B/dI_C from eq. (*i*) into the expression for S, we have,

$$S = \frac{\beta + 1}{1 - \beta \dfrac{-R_E}{R_0 + R_E}} = \frac{\beta + 1}{1 + \left(\dfrac{\beta R_E}{R_0 + R_E}\right)}$$

$$= \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E} = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E(\beta + 1)}$$

$$\therefore \quad S = (\beta + 1) \times \frac{R_0 + R_E}{R_E(\beta + 1) + R_0}$$

Dividing the numerator and denominator of R.H.S. of the above equation by R_E, we have,

$$S = (\beta + 1) \times \frac{1 + R_0 / R_E}{\beta + 1 + R_0 / R_E} \qquad \text{...}(ii)$$

Eq. (*ii*) gives the formula for the stability factor S for the potential divider bias circuit. The following points may be noted carefully :

(*i*) For greater thermal stability, the value of S should be small. This can be achieved by making R_0/R_E small. If R_0/R_E is made very small, then it can be neglected as compared to 1.

$$\therefore \quad S = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$

This is the ideal value of S and leads to the maximum thermal stability.

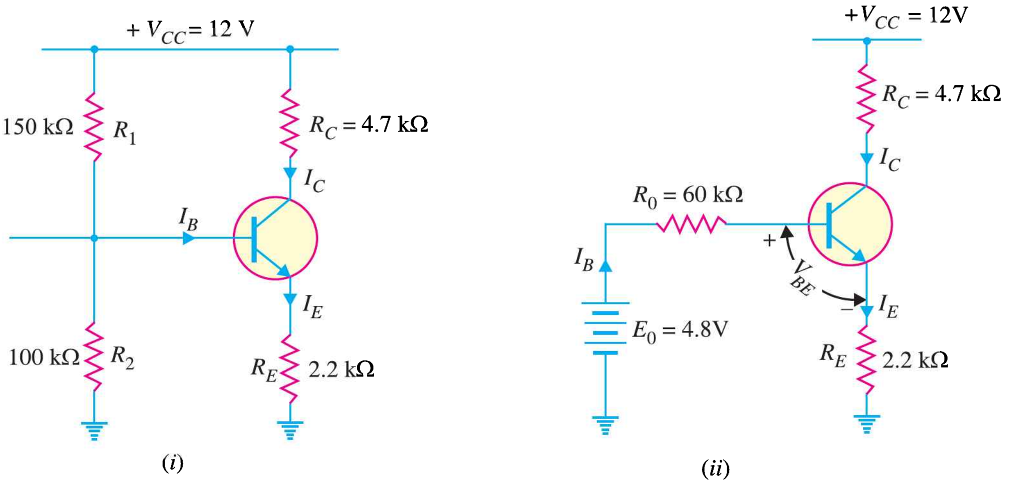
(*ii*) The ratio *R_0/R_E can be made very small by decreasing R_0 and increasing R_E. Low value of

---

* Remember, R_0 = Thevenin's equivalent resistance = $\dfrac{R_1 R_2}{R_1 + R_2}$

R_0 can be obtained by making R_2 very small. But with low value of R_2, current drawn from V_{CC} will be large. This puts restriction on the choice of R_0. Increasing the value of R_E requires greater V_{CC} in order to maintain the same zero signal collector current. Due to these limitations, a compromise is made in the selection of the values of R_0 and R_E. Generally, these values are so selected that $S \simeq 10$.

Example 9.23. *For the circuit shown in Fig. 9.29 (i), find the operating point. What is the stability factor of the circuit ? Given that* $\beta = 50$ *and* $V_{BE} = 0.7V$.



(*i*) (*ii*)

Fig. 9.29

Solution. Fig. 9.29 (*i*) shows the circuit of potential divider bias whereas Fig. 9.29 (*ii*) shows it with potential divider circuit replaced by Thevenin's equivalent circuit.

$$E_0 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{12\text{V}}{150\text{ k}\Omega + 100\text{ k}\Omega} \times 100\text{ k}\Omega = 4.8\text{V}$$

$$R_0 = \frac{R_1 R_2}{R_1 + R_2} = \frac{150\text{ k}\Omega \times 100\text{ k}\Omega}{150\text{ k}\Omega + 100\text{ k}\Omega} = 60\text{ k}\Omega$$

$$\therefore \quad I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E} \qquad \text{...... (See Ex. 9.20)}$$

$$= \frac{4.8\text{V} - 0.7\text{V}}{60\text{ k}\Omega + 50 \times 2.2\text{ k}\Omega} = \frac{4.1\text{V}}{170\text{ k}\Omega} = 0.024\text{ mA}$$

Now $\quad I_C = \beta I_B = 50 \times 0.024 = 1.2\text{ mA}$

$$\therefore \quad V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 12\text{V} - 1.2\text{mA}\,(4.7\text{ k}\Omega + 2.2\text{ k}\Omega) = 3.72\text{V}$$

$\therefore$ Operating point is **3.72V, 1.2 mA.**

$$\text{Now} \quad \frac{R_0}{R_E} = \frac{60\text{ k}\Omega}{2.2\text{ k}\Omega} = 27.3$$

$$\therefore \quad \text{Stability factor, } S = (\beta + 1) \times \frac{1 + R_0/R_E}{\beta + 1 + R_0/R_E}$$

$$= (50 + 1) \times \frac{1 + 27.3}{50 + 1 + 27.3} = \mathbf{18.4}$$

Note. We can also find the value of I_C and V_{CE} (See Art. 9.12) as under :

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \text{where } V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

and $$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

However, by replacing the potential divider circuit by Thevenin's equivalent circuit, the expression for I_C can be found more accurately. If not mentioned in the problem, any one of the two methods can be used to obtain the solution.

Example 9.24. *The circuit shown in Fig. 9.30 (i) uses silicon transistor having $\beta = 100$. Find the operating point and stability factor.*

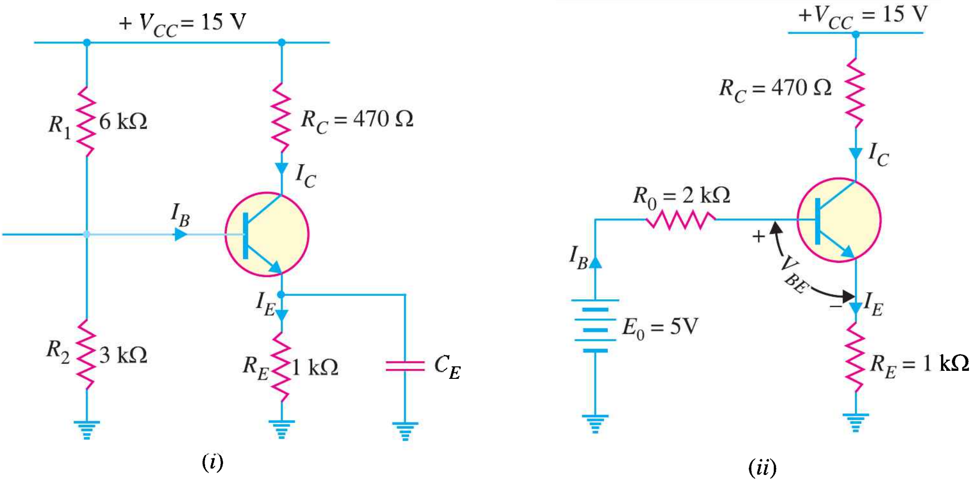


Fig 9.30

Solution. Fig. 9.30 (*i*) shows the circuit of potential divider bias whereas Fig. 9.30 (*ii*) shows it with potential divider circuit replaced by Thevenin's equivalent circuit.

$$E_0 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{15\text{V}}{6\text{ k}\Omega + 3\text{ k}\Omega} \times 3\text{ k}\Omega = \frac{15\text{V}}{9\text{ k}\Omega} \times 3\text{ k}\Omega = 5\text{V}$$

$$R_0 = \frac{R_1 R_2}{R_1 + R_2} = \frac{6\text{ k}\Omega \times 3\text{ k}\Omega}{6\text{ k}\Omega + 3\text{ k}\Omega} = 2\text{ k}\Omega$$

Now $$I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E}$$

$$= \frac{5\text{V} - 0.7\text{V}}{2\text{ k}\Omega + 100 \times 1\text{k}\Omega} = \frac{4.3\text{V}}{102\text{ k}\Omega} = 0.042\text{mA}$$

∴ $$I_C = \beta I_B = 100 \times 0.042 = 4.2\text{ mA}$$

and $$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 15\text{V} - 4.2\text{mA}\ (470\Omega + 1\text{ k}\Omega) = 8.83\text{V}$$

∴ Operating point is **8.83V ; 4.2 mA.**

Now $$R_0 / R_E = 2\text{ k}\Omega / 1\text{ k}\Omega = 2$$

∴ Stability factor, $$S = (\beta + 1) \times \frac{1 + R_0 / R_E}{\beta + 1 + R_0 / R_E}$$

$$= (100 + 1) \times \frac{1 + 2}{100 + 1 + 2} = \mathbf{2.94}$$

9.14 Design of Transistor Biasing Circuits

(For low powered transistors)

In practice, the following steps are taken to design transistor biasing and stabilisation circuits :

Step 1. It is a common practice to take $R_E = 500 - 1000\Omega$. Greater the value of R_E, better is the stabilisation. However, if R_E is very large, higher voltage drop across it leaves reduced voltage drop across the collector load. Consequently, the output is decreased. Therefore, a compromise has to be made in the selection of the value of R_E.

Step 2. The zero signal current I_C is chosen according to the signal swing. However, in the initial stages of most transistor amplifiers, zero signal I_C = 1mA is sufficient. The major advantages of selecting this value are :

(*i*) The output impedance of a transistor is very high at 1mA. This increases the voltage gain.

(*ii*) There is little danger of overheating as 1mA is quite a small collector current.

It may be noted here that working the transistor below zero signal I_C = 1mA is not advisable because of strongly non-linear transistor characteristics.

Step 3. The values of resistances R_1 and R_2 are so selected that current I_1 flowing through R_1 and R_2 is atleast 10 times I_B *i.e.* $I_1 \geq 10\, I_B$. When this condition is satisfied, good stabilisation is achieved.

Step 4. The zero signal I_C should be a little more (say 20%) than the maximum collector current swing due to signal. For example, if collector current change is expected to be 3mA due to signal, then select zero signal $I_C \simeq 3.5$ mA. It is important to note this point. Selecting zero signal I_C below this value may cut off a part of negative half-cycle of a signal. On the other hand, selecting a value much above this value (say 15mA) may unnecessarily overheat the transistor, resulting in wastage of battery power. Moreover, a higher zero signal I_C will reduce the value of R_C (for same V_{CC}), resulting in reduced voltage gain.

Example 9.25. *In the circuit shown in Fig. 9.31, the operating point is chosen such that* I_C = *2mA,* $V_{CE} = 3V$*. If* $R_C = 2.2\ k\Omega$, $V_{CC} = 9V$ *and* $\beta = 50$*, determine the values of* R_1, R_2 *and* R_E*. Take* $V_{BE} = 0.3V$ *and* $I_1 = 10 I_B$.

Solution. $R_C = 2.2\text{ k}\Omega$, $V_{CC} = 9\text{V}$, $\beta = 50$

$V_{BE} = 0.3$ V, $I_1 = 10\, I_B$

As I_B is very small as compared to I_1, therefore, we can assume with reasonable accuracy that I_1 flowing through R_1 also flows through R_2.

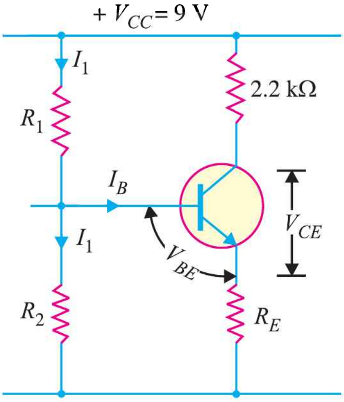


Fig. 9.31

$$\text{Base current, } I_B = \frac{I_C}{\beta} = \frac{2\ mA}{50} = 0.04\text{ mA}$$

Current through R_1 & R_2 is

$$I_1 = 10\, I_B = 10 \times 0.04 = 0.4\text{ mA}$$

Now
$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$\therefore \quad R_1 + R_2 = \frac{V_{CC}}{I_1} = \frac{9\text{ V}}{0.4\text{ mA}} = 22.5\text{ k}\Omega$$

Applying Kirchhoff's voltage law to the collector side of the circuit, we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

or $$V_{CC} = I_C R_C + V_{CE} + I_C R_E \qquad (\because I_C \simeq I_E)$$

or $$9 = 2 \text{ mA} \times 2.2 \text{ k}\Omega + 3 + 2 \text{ mA} \times R_E$$

$$\therefore \quad R_E = \frac{9 - 4.4 - 3}{2} = 0.8 \text{ k}\Omega = \mathbf{800\ \Omega}$$

Voltage across R_2, $V_2 = V_{BE} + V_E = 0.3 + 2 \text{ mA} \times 0.8 \text{ k}\Omega$

$$= 0.3 + 1.6 = 1.9 \text{ V}$$

$$\therefore \quad \text{Resistance } R_2 = V_2/I_1 = 1.9 \text{ V}/0.4 \text{ mA} = \mathbf{4.75\ k\Omega}$$

and $$R_1 = 22.5 - 4.75 = \mathbf{17.75\ k\Omega}$$

Example 9.26. *An npn transistor circuit (See Fig. 9.32) has* $\alpha = 0.985$ *and* $V_{BE} = 0.3V$. *If* $V_{CC} = 16V$, *calculate* R_1 *and* R_C *to place Q point at* $I_C = 2mA$, $V_{CE} = 6$ *volts.*

Solution. $\alpha = 0.985, \quad V_{BE} = 0.3 \text{ V}, \quad V_{CC} = 16 \text{ V}$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1 - 0.985} = 66$$

$$\text{Base current, } I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{66} = 0.03 \text{ mA}$$

Voltage across R_2, $V_2 = V_{BE} + V_E = 0.3 + 2 \text{ mA} \times 2 \text{ k}\Omega$

$$= 4.3 \text{ V}$$

$\therefore$ Voltage across $R_1 = V_{CC} - V_2 = 16 - 4.3 = 11.7 \text{ V}$

$\therefore$ Current through R_1 & R_2 is

$$I_1 = \frac{V_2}{R_2} = \frac{4.3 \text{ V}}{20 \text{ k}\Omega} = 0.215 \text{ mA}$$

$$\therefore \quad \text{Resistance } R_1 = \frac{\text{Voltage across } R_1}{I_1} = \frac{11.7 \text{ V}}{0.215 \text{ mA}}$$

$$= \mathbf{54.4\ k\Omega}$$

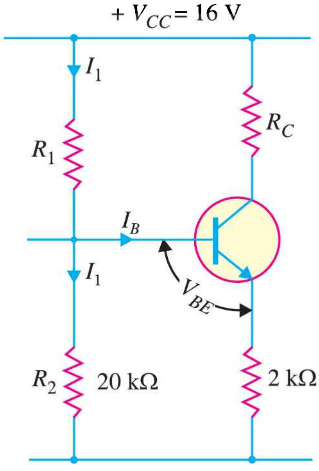


Fig. 9.32

Voltage across $R_C = V_{CC} - V_{CE} - V_E$

$$= 16 - 6 - 2 \times 2 = 6 \text{ V}$$

$$\therefore \quad \text{Collector resistance, } R_C = \frac{\text{Voltage across } R_C}{I_C} = \frac{6 \text{ V}}{2 \text{ mA}} = \mathbf{3\ k\Omega}$$

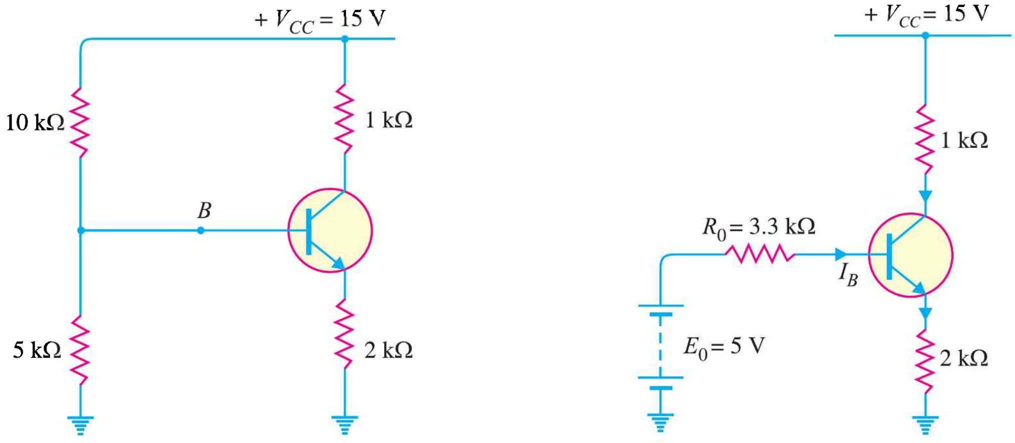
Example 9.27. *Calculate the exact value of emitter current in the circuit shown in Fig. 9.33 (i). Assume the transistor to be of silicon and* $\beta = 100$.

Solution. In order to obtain accurate value of emitter current I_E, we shall replace the bias portion of the circuit shown in Fig. 9.33 (*i*) by its Thevenin's equivalent. Fig. 9.33 (*ii*) shows the desired circuit.

Looking from the base terminal B to the left, Thevenin's voltage E_0 is given by :

$$E_0 = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5}{10 + 5} \times 15 = 5 \text{ V}$$

Again looking from the base terminal B to the left, Thevenin's resistance R_0 is given by;



(*i*) (*ii*)

Fig. 9.33

$$R_0 = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 5}{10 + 5} = \frac{50}{15} = 3.3\ \text{k}\Omega$$

Applying Kirchhoff's voltage law to the base-emitter loop [See Fig. 9.33 (*ii*)],

$$E_0 = I_B R_0 + V_{BE} + I_E R_E$$

Since $I_E \simeq I_C$, therefore, $I_B = I_E/\beta$.

$$\therefore \quad E_0 = \frac{I_E}{\beta} R_0 + V_{BE} + I_E R_E$$

$$= I_E \left(\frac{R_0}{\beta} + R_E \right) + V_{BE}$$

$$\therefore \quad I_E = \frac{E_0 - V_{BE}}{\frac{R_0}{\beta} + R_E} = \frac{5 - 0.7}{\frac{3.3}{100} + 2} \qquad \text{(For } Si \text{ transistor, } V_{BE} = 0.7\text{V)}$$

$$= \frac{4.3\ \text{V}}{2.033\ \text{k}\Omega} = \mathbf{2.11\ mA}$$

Example 9.28. *The potential divider circuit shown in Fig. 9.34 has the values as follows: $I_E = 2mA$, $I_B = 50\mu A$, $V_{BE} = 0.2V$, $R_E = 1k\Omega$, $R_2 = 10\ k\Omega$ and $V_{CC} = 10V$. Find the value of R_1.*

Solution. In this problem, we shall consider that currents through R_1 and R_2 are different, although in practice this difference is very small.

$$\text{Voltage across } R_2,\ V_2 = V_{BE} + I_E R_E = 0.2 + 2\ \text{mA} \times 1\ \text{k}\Omega$$

$$= 0.2 + 2 = 2.2\ \text{V}$$

$$\text{Current through } R_2,\ I_2 = \frac{V_2}{R_2} = \frac{2.2\ \text{V}}{10\ \text{k}\Omega} = 0.22\ \text{mA}$$

$$\text{Current through } R_1,\ I_1 = I_2 + I_B = 0.22 + 0.05 = 0.27\ \text{mA}$$

$$\text{Voltage across } R_1,\ V_1 = V_{CC} - V_2 = 10 - 2.2 = 7.8\ \text{V}$$

$$\therefore \quad R_1 = \frac{V_1}{I_1} = \frac{7.8\ \text{V}}{0.27\ \text{mA}} = \mathbf{28.89\ k\Omega}$$

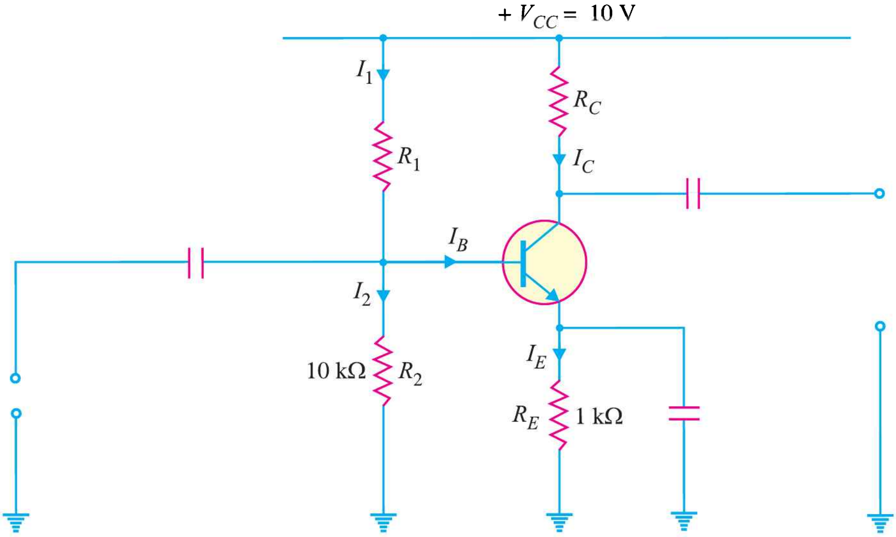


Fig. 9.34

Example 9.29. *Fig. 9.35 shows the potential divider method of biasing. What will happen if*

(*i*) *resistance R_2 is shorted* (*ii*) *resistance R_2 is open-circuited*

(*iii*) *resistance R_1 is shorted* (*iv*) *resistance R_1 is open ?*

Solution. (*i*) If resistance R_2 is shorted, the base will be grounded. It will be left without forward bias and the transistor will be cut off *i.e.*, output will be zero.

(*ii*) If resistance R_2 is open, the forward bias will be very high. The collector current will be very high while collector-emitter voltage will be very low.

(*iii*) If resistance R_1 is shorted, the transistor will be in saturation due to excessive forward bias. The base will be at V_{CC} and emitter will be only slightly below V_{CC}.

(*iv*) If R_1 is open, the transistor will be without forward bias. Hence the transistor will be cut off *i.e.* output will be zero.

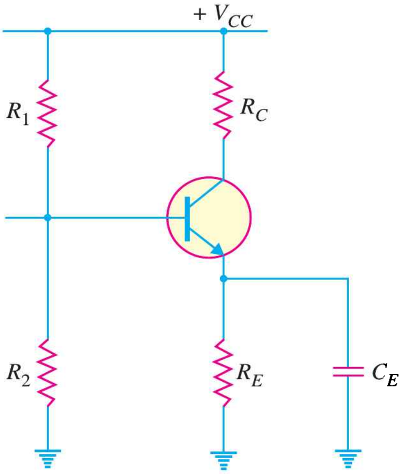


Fig. 9.35

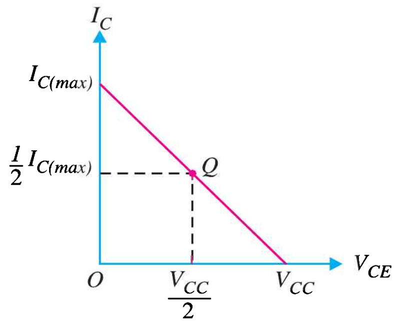


Fig. 9.36

9.15 Mid-Point Biasing

Mid-point biasing

When an amplifier circuit is so designed that operating point Q lies at the centre of d.c. load line, the amplifier is said to be *midpoint biased*. When the amplifier is mid-point biased, the Q-point provides values of I_C and V_{CE} that are one-half of their maximum possible values. This is illustrated in Fig. 9.36. Since the Q-point is centred on the load line;

$$I_C = \frac{1}{2} I_{C\,(max)} \;;\quad V_{CE} = \frac{V_{CC}}{2}$$

When a transistor is used as an amplifier, it is always designed for mid point bias. The reason is that midpoint biasing allows optimum operation of the amplifier. In other words, midpoint biasing provides the largest possible output. This point is illustrated in Fig. 9.37 where Q-point is centred on the load line.

When an ac signal is applied to the base of the transistor, collector current and collector- emitter voltage will both vary around their Q-point values. Since Q-point is centred, I_C and V_{CE} can both make the maximum possible transitions above and below their initial dc values. If Q-point is located above centre on the load line, the input may cause the transistor to saturate. As a result, a part of the output wave will be clipped off. Similarly, if Q-point is below midpoint on the load line, the input may cause the transistor to go into cut off. This can also cause a portion of the output to be clipped. It follows, therefore, that midpoint biased amplifier circuit allows the best possible ac operation of the circuit.

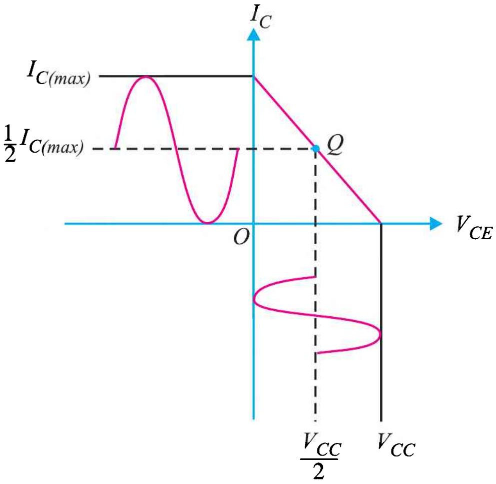


Fig. 9.37

Example 9.30. *Determine whether or not the circuit shown in Fig. 9.38 (i) is midpoint biased.*

Solution. Let us first construct the dc load line.

$$I_{C\,(max)} = \frac{V_{CC}}{R_C} = \frac{8\text{ V}}{2\text{ k}\Omega} = 4\text{ mA}$$

This locates the point A (OA = 4 mA) of the dc load line.

$$V_{CE(max)} = V_{CC} = 8\text{ V}$$

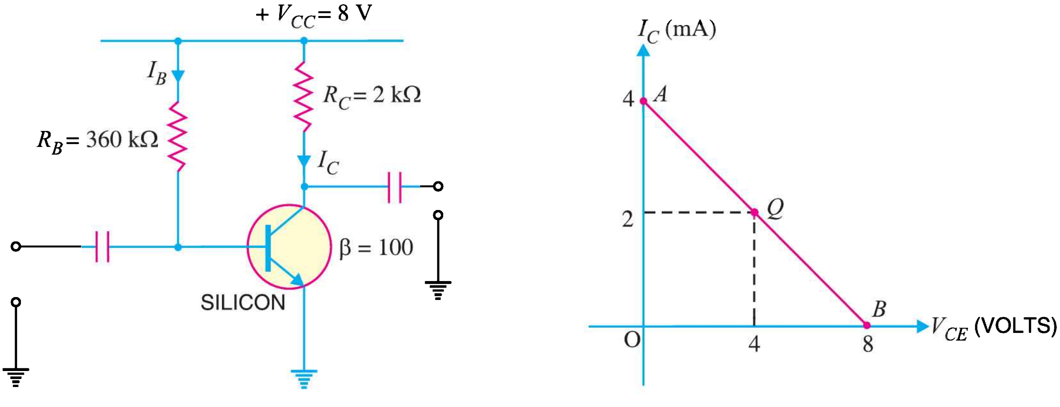
This locates the point B (OB = 8V) of the dc load line. By joining these two points, dc load line AB is constructed [See Fig. 9.38 (*ii*)].

Operating point. Referring to Fig. 9.38 (*i*), we have,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{8\text{ V} - 0.7\text{ V}}{360\text{ k}\Omega} = 20.28\ \mu\text{A}$$

$$\therefore \quad I_C = \beta I_B = 100\ (20.28\ \mu\text{A}) = 2.028\text{ mA}$$

$$\text{Also} \quad V_{CE} = V_{CC} - I_C R_C = 8\text{ V} - (2.028\text{ mA})\ (2\text{ k}\Omega) = 3.94\text{ V}$$



(*i*) (*ii*)

Fig. 9.38

Since V_{CE} is nearly one-half of V_{CC}, *the amplifier circuit is midpoint biased.*

Note. We can determine whether or not the circuit is midpoint biased without drawing the dc load line. By definition, a circuit is midpoint biased when the Q-point value of V_{CE} is one-half of V_{CC}. Therefore, all that you have to do is to find the operating point Q of the circuit. If the Q-point value of V_{CE} is one-half of V_{CC}, the circuit is midpoint biased.

Example 9.31. *Determine whether or not the circuit shown in Fig. 9.39 is midpoint biased.*

Solution. In order to determine whether the circuit is midpoint biased or not, we shall first find the operating point of the circuit.

Voltage across R_2 is

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

$$= \frac{10}{12 + 2.7} \times 2.7 = 1.84 \text{ V}$$

∴ Emitter current is

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$= \frac{1.84 - 0.7}{180} = 6.33 \text{ mA}$$

∴ Collector current is

$$I_C \simeq I_E = \mathbf{6.33\ mA}$$

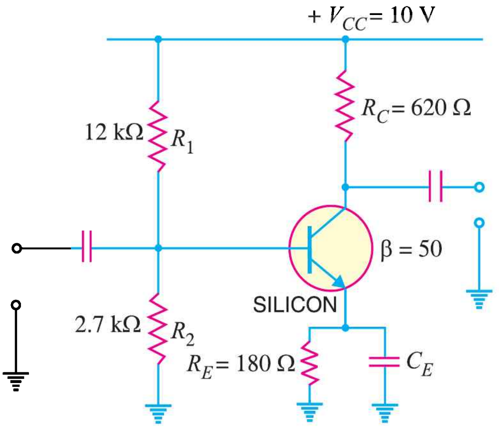


Fig. 9.39

Collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 10 - 6.33 (0.62 + 0.18) = \mathbf{4.94\ V}$$

Since Q-point value of V_{CE} is approximately one-half of V_{CC} (= 10 V), *the circuit is midpoint biased.* Note that answer has been obtained without the use of a dc load line.

9.16 Which Value of β to be used ?

While analysing a biasing circuit, we have to refer to the specification sheet for the transistor to obtain the value of β. Normally, the transistor specification sheet lists a minimum value (β_{min}) and maximum value (β_{max}) of β. In that case, the *geometric average of the two values* should be used.

$$\beta_{av} = \sqrt{\beta_{min} \times \beta_{max}}$$

Note. If only one value of β is listed on the specification sheet, we should then use that value.

Example 9.32. *Find the value of I_B for the circuit shown in Fig. 9.40. Given that β has a range of 100 to 400 when $I_C = 10$ mA.*

Solution. Voltage across R_2 is

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{10}{1.5 + 0.68} \times 0.68 = 3.12 \text{ V}$$

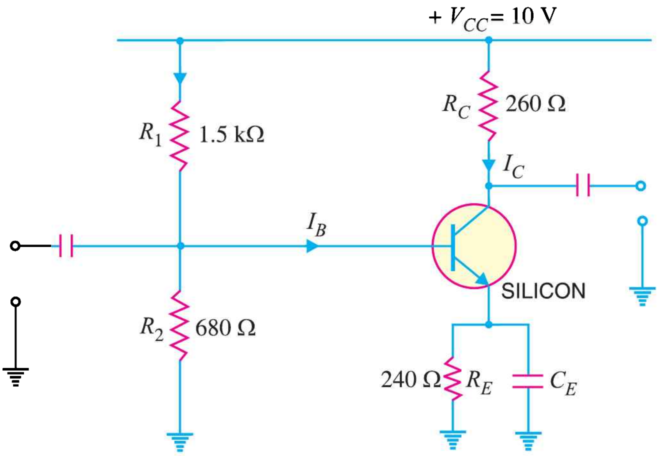


Fig. 9.40

$$\therefore \quad \text{Emitter current, } I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{3.12 - 0.7}{0.24} = 10 \text{ mA}$$

$$\therefore \quad \text{Collector current, } I_C \simeq I_E = 10 \text{ mA}$$

It is given that β has a range of 100 to 400 when Q-point value of I_C is 10mA.

$$\therefore \quad \beta_{av} = \sqrt{\beta_{min} \times \beta_{max}} = \sqrt{100 \times 400} = 200$$

$$\therefore \quad \text{Base current, } I_B = \frac{I_E}{\beta_{av} + 1} = \frac{10 \text{ mA}}{200 + 1} = \mathbf{49.75\ \mu A}$$

9.17 Miscellaneous Bias Circuits

In practice, one may find that bias circuits which do not always confirm to the basic forms considered in this chapter. There may be slight circuit modifications. However, such bias circuits should not pose any problem if the basic approach to transistor biasing is understood. We shall solve a few examples to show how the basic concepts of biasing can be applied to any biasing circuit.

Example 9.33. *Calculate the operating point of the circuit shown in Fig. 9.41. Given β = 60 and $V_{BE} = 0.7$V.*

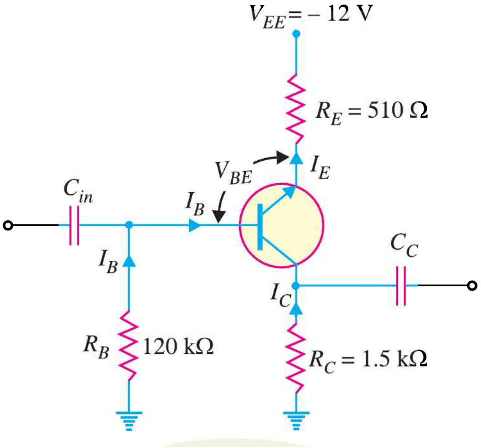

$V_{EE} = -12$ V
$R_E = 510\ \Omega$
V_{BE}
I_E
C_{in}
I_B
I_B
C_C
I_C
R_B 120 kΩ
$R_C = 1.5$ kΩ

Fig. 9.41

Solution. Such a problem should not pose any difficulty. We are to simply find the d.c. values. Note that capacitors behave as open to d.c. Applying Kirchhoff's voltage law to the path passing through R_B, V_{BE}, R_E and V_{EE}, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

or $$V_{EE} = I_B R_B + V_{BE} + I_C R_E \qquad (\because I_E \simeq I_C)$$

or $$V_{EE} - V_{BE} = I_B R_B + \beta I_B R_E \qquad (\because I_C = \beta I_B)$$

$$\therefore \qquad I_B = \frac{V_{EE} - V_{BE}}{R_B + \beta R_E}$$

$$= \frac{12\text{V} - 0.7\text{V}}{120\ \text{k}\Omega + 60 \times 0.510\ \text{k}\Omega} = \frac{11.3\text{V}}{150.6\ \text{k}\Omega} = 0.075\ \text{mA}$$

Now $$I_C = \beta I_B = 60 \times 0.075\ \text{mA} = 4.5\ \text{mA}$$

and $$V_{CE} = V_{EE} - I_C (R_C + R_E)$$

$$= 12\text{V} - 4.5\ \text{mA}\ (1.5\ \text{k}\Omega + 0.510\ \text{k}\Omega) = 2.96\text{V}$$

$\therefore$ Operating point is **2.96V, 4.5 mA.**

Example 9.34. *Find the operating point for the circuit shown in Fig. 9.42. Assume $\beta = 45$ and $V_{BE} = 0.7V$.*

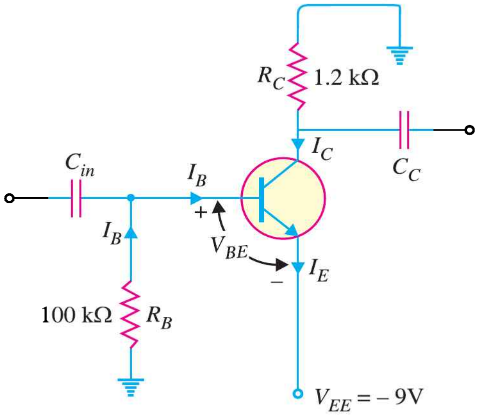

R_C 1.2 kΩ
I_C
C_C
C_{in}
I_B
+
V_{BE}
–
I_B
I_E
100 kΩ R_B
$V_{EE} = -9$V

Fig. 9.42

Solution.

$$V_{EE} = I_B R_B + V_{BE}$$

or $$I_B = \frac{V_{EE} - V_{BE}}{R_B} = \frac{(9 - 0.7)\text{ V}}{100\text{ k}\Omega} = 0.083\text{ mA}$$

∴ $$I_C = \beta I_B = 45 \times 0.083\text{ mA} = 3.73\text{ mA}$$

Also $$V_{EE} = I_C R_C + V_{CE}$$

∴ $$V_{CE} = V_{EE} - I_C R_C = 9\text{V} - (3.73\text{ mA})\,(1.2\text{ k}\Omega) = 4.52\text{V}$$

∴ Operating point is **4.52V, 3.73 mA.**

Example 9.35. *It is desired to design the biasing circuit of an amplifier in Fig. 9.43 in such a way to have an operating point of 6V, 1 mA. If transistor has $\beta = 150$, find R_E, R_C, R_1 and R_2. Assume $V_{BE} = 0.7V$.*

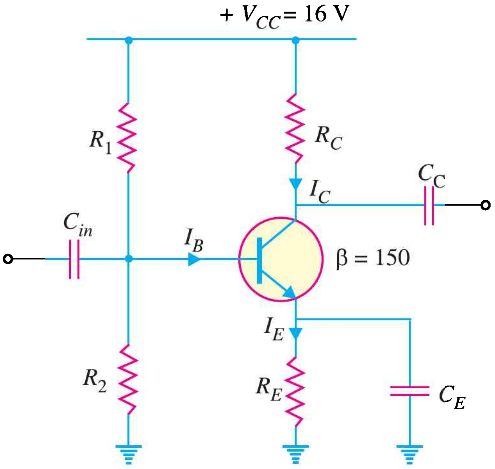


Fig. 9.43

Solution. We are given V_{CC}, β and the operating point. It is desired to find the component values. For good design, voltage across R_E (*i.e.*, V_E) should be one-tenth of V_{CC} *i.e.*

$$V_E = \frac{V_{CC}}{10} = \frac{16\text{V}}{10} = 1.6\text{V}$$

∴ $$R_E = \frac{V_E}{I_E} = \frac{V_E}{I_C} = \frac{1.6\text{V}}{1\text{ mA}} = \mathbf{1.6\text{ k}\Omega}$$

Now $$V_{CC} = I_C R_C + V_{CE} + V_E$$

∴ $$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{16 - 6\text{V} - 1.6\text{V}}{1\text{ mA}} = \mathbf{8.4\text{ k}\Omega}$$

$$V_2 = V_E + V_{BE} = 1.6 + 0.7 = 2.3\text{V}$$

Now $$R_2 = \frac{1}{10}\,{}^{*}(\beta R_E) = \frac{1}{10}\,(150 \times 1.6\text{ k}\Omega) = \mathbf{24\text{ k}\Omega}$$

Also $$V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

or $$2.3\text{V} = \frac{16\text{V}}{\text{R}_1 + 24\text{ k}\Omega} \times 24\text{ k}\Omega \qquad \therefore R_1 = \mathbf{143\text{ k}\Omega}$$

---

* This relation stems from $I_1 = 10\,I_B$.

9.18 Silicon Versus Germanium

Although both silicon and germanium are used in semiconductor devices, the present day trend is to use silicon. The main reasons for this are :

(*i*) *Smaller I_{CBO}.* At room temperature, a silicon crystal has fewer free electrons than a germanium crystal. This implies that silicon will have much smaller collector cut off current (I_{CBO}) than that of germanium. In general, with germanium, I_{CBO} is 10 to 100 times greater than with silicon. The typical values of I_{CBO} at 25°C (the figures most often used for normal temperature) for small signal transistors are:

Silicon : 0.01 μA to 1μA

Germanium : 2 to 15 μA

(*ii*) *Smaller variation of I_{CBO} with temperature.* The variation of I_{CBO} with temperature is less in silicon as compared to germanium. A rough rule of thumb for germanium is that I_{CBO} approximately doubles with each 8 to 10°C rise while in case of silicon, it approximately doubles with each 12°C rise.

(*iii*) *Greater working temperature.* The structure of germanium will be destroyed at a temperature of approximately 100°C. The maximum normal working temperature of germanium is 70°C but silicon can be operated upto 150°C. Therefore, silicon devices are not easily damaged by excess heat.

(*iv*) *Higher PIV rating.* The *PIV* ratings of silicon diodes are greater than those of germanium diodes. For example, the *PIV* ratings of silicon diodes are in the neighbourhood of 1000V whereas the *PIV* ratings of germanium diodes are close to 400V.

The disadvantage of silicon as compared to germanium is that potential barrier of silicon diode (0.7V) is more than that of germanium diode (0.5V). This means that higher bias voltage is required to cause current flow in a silicon diode circuit. This drawback of silicon goes to the background in view of the other advantages of silicon mentioned above. Consequently, the modern trend is to use silicon in semiconductor devices.

Example 9.36. *A small signal germanium transistor operating at 25°C has $I_{CBO} = 5\ \mu A$, $\beta = 40$ and zero signal collector current = 2mA.*

(i) Find the collector cut- off current i.e. I_{CEO}.

(ii) Find the percentage change in zero signal collector current if the temperature rises to 55°C. Assume I_{CBO} doubles with every 10°C rise.

(iii) What will be the percentage change in silicon transistor under the same conditions? Given that I_{CBO} for silicon is 0.1μA at 25°C and I_{CBO} doubles for every 10°C rise.

Solution.

(*i*) $$I_{CEO} = (\beta + 1)\, I_{CBO} = (40 + 1)\,(5\ \mu A) = 205\ \mu A = \mathbf{0.205\ mA}$$

(*ii*) Rise in temperature = 55 − 25 = 30°C

Since I_{CBO} doubles for every 10°C rise, the new I_{CBO} in Ge transistor at 55°C will be 8 times that at 25°C *i.e.*

Now $$I_{CBO} = 8 \times 5 = 40\ \mu A$$

$$\therefore \quad I_{CEO} = (\beta + 1)\, I_{CBO} = (40 + 1)\,(40\ \mu A) = 1640\ \mu A = 1.64\ mA$$

∴ Zero signal collector current at 55°C

$$= 2 + 1.64 = 3.64\ mA$$

Percentage change in zero signal collector current

$$= \frac{3.64 - 2}{2} \times 100 = \mathbf{82\ \%}$$

i.e., zero signal collector current rises 82% above its original value due to 30°C rise in temperature.

(*iii*) With silicon transistor,

$$I_{CBO} = 0.1\ \mu A \text{ at } 25°C \text{ and } \beta = 40$$

$$\therefore \quad I_{CEO} = (\beta + 1)\, I_{CBO} = (40 + 1)\,(0.1\ \mu A)$$

$$= 4.1\ \mu\text{A} = 0.0041\ \text{mA}$$

A 30°C rise in temperature would cause I_{CEO} in silicon to increase 8 times.

$$\text{Now } I_{CEO} = 8 \times 0.0041 = 0.0328\ \text{mA}$$

∴ Zero signal collector current at 55°C

$$= 2 + 0.0328 = 2.0328\ \text{mA}$$

Percentage change in zero signal collector current

$$= \frac{2.0328 - 2}{2} \times 100 = \mathbf{1.6\ \%}$$

i.e., increase in zero signal collector current is 1.6%.

Comments. The above example shows that change in zero signal collector current with rise in temperature is very small in silicon as compared to germanium. In other words, temperature effects very slightly change the operating point of silicon transistors while they may cause a drastic change in germanium transistors. This is one of the reasons that silicon has become the main semiconductor material in use today.

Example 9.37. *A silicon transistor has $I_{CBO} = 0.02 \mu A$ at 27°C. The leakage current doubles for every 6°C rise in temperature. Calculate the base current at 57°C when the emitter current is 1mA. Given that $\alpha = 0.99$.*

Solution. A 30°C (57 – 27 = 30) rise in temperature would cause I_{CBO} to increase 32 times.

$$\therefore \quad \text{At } 57°\text{C}, \ I_{CBO} = 32 \times 0.02 = 0.64\ \mu\text{A} = 0.00064\ \text{mA}$$

$$\text{Now } I_C = \alpha I_E + I_{CBO}$$

$$= 0.99 \times 1 + 0.00064 = 0.9906\ \text{mA} = 0.000\ 64\ \text{mA}$$

$$\therefore \quad I_B = I_E - I_C = 1 - 0.9906 = 0.0094\ \text{mA} = \mathbf{9.4\ \mu A}$$

9.19 Instantaneous Current and Voltage Waveforms

It is worthwhile to show instantaneous current and voltage waveforms in an amplifier. Consider a *CE* amplifier biased by base resistor method as shown in Fig. 9.44. Typical circuit values have been assumed to make the treatment more illustrative. Neglecting V_{BE}, it is clear that zero signal base current $I_B = V_{CC}/R_B = 20\ \text{V}/1\text{M}\Omega = 20\ \mu\text{A}$. The zero signal collector current $I_C = \beta I_B = 100 \times 20\ \mu\text{A} = 2\text{mA}$. When signal of peak current 10 μA is applied, alternating current is superimposed on the d.c. base current. The collector current and collector-emitter voltage also vary as the signal changes. The instantaneous waveforms of currents and voltages are shown in Fig. 9.45. Note that base current, collector current and collector-emitter voltage waveforms are composed of (*i*) the d.c. component and (*ii*) the a.c. wave riding on the d.c.

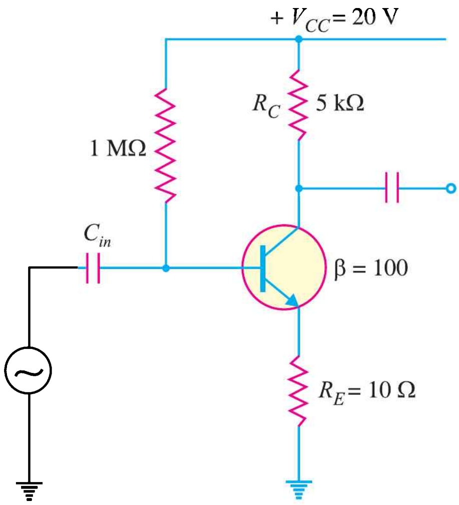


Fig. 9.44

(*i*) At π/2 radians, the base current is composed of 20 μA d.c. component plus 10 μA peak a.c. component, adding to 30 μA *i.e* $i_B = 20 + 10 = 30\ \mu\text{A}$. The corresponding collector current $i_C = 100 \times 30\ \mu\text{A} = 3$ mA. The corresponding collector-emitter voltage is

$$v_{CE} = V_{CC} - i_C R_C = 20\ \text{V} - 3\ \text{mA} \times 5\ \text{k}\Omega$$

$$= 20\ \text{V} - 15\ \text{V} = 5\ \text{V}$$

Note that as the input signal goes positive, the collector current increases and collector-emitter voltage decreases. Moreover, during the positive half cycle of the signal (*i.e.* from 0 to π rad.), the operating point moves from 20 μA to 20 + 10 = 30 μA and then back again *i.e.* operating point follows the path *Q* to *C* and back to *Q* on the load line.

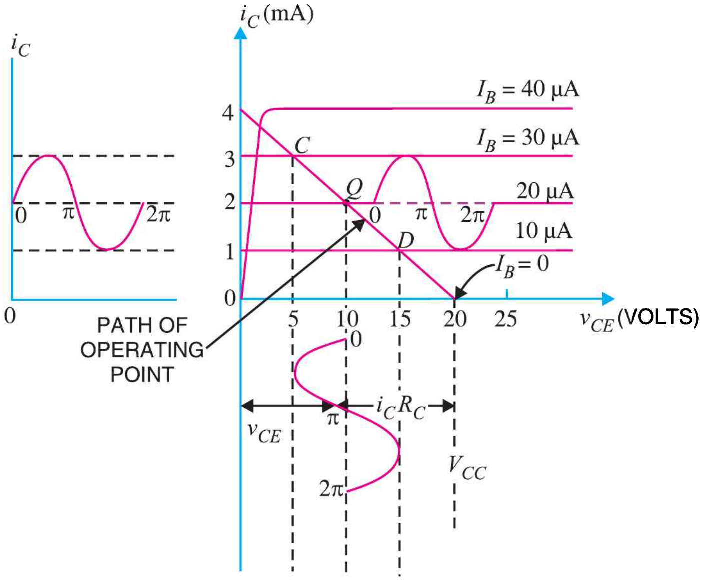


Fig. 9.45

(*ii*) During the negative half-cycle of the signal (from π to 2π rad.), the operating point goes from 20 μA to 20 – 10 = 10 μA and then back again *i.e.* the operating point follows the path *Q* to *D* and back to *Q* on the load line.

(*iii*) As the operating point moves along the path *CD* or *DC* due to the signal, the base current varies continuously. These variations in the base current cause both collector current and collector-emitter voltage to vary.

(*iv*) Note that when the input signal is maximum positive, the collector-emitter voltage is maximum negative. In other words, input signal voltage and output voltage have a phase difference of 180°. This is an important characteristic of *CE* arrangement.

Example 9.38. *What fault is indicated in Fig. 9.46 ? Explain your answer with reasons.*

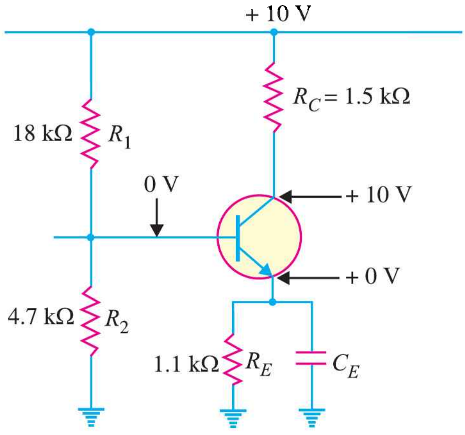


Fig. 9.46

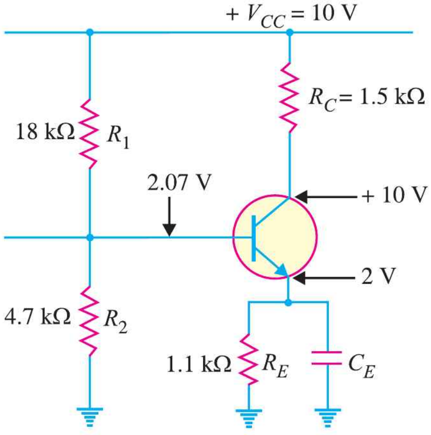


Fig. 9.47

Solution. Since V_B (*i.e.*, base voltage *w.r.t.* ground) is zero, it means that there is no path for current in the base circuit. The transistor will be biased off *i.e.*, $I_C = 0$ and $I_E = 0$. Therefore, $V_C = 10$ V ($\because I_C R_C = 0$) and $V_E = 0$. The obvious fault is that R_1 is open.

Example 9.39. *What fault is indicated in Fig. 9.47? Explain your answer with reasons.*

Solution. Based on the values of R_1, R_2 and V_{CC}, the voltage V_B at the base seems appropriate. In fact it is so as shown below :

$$\text{Voltage at base, } V_B = \text{Voltage across } R_2$$

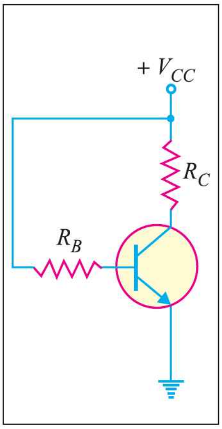
$$= \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{10}{18 + 4.7} \times 4.7 = 2.07 \text{ V}$$

The fact that $V_C = +10$ V and $V_E \simeq V_B$ reveals that $I_C = 0$ and $I_E = 0$. As a result, I_B drops to zero. The obvious fault is that R_E is open.

9.20 Summary Of Transistor Bias Circuits

In figures below, *npn* transistors are shown. Supply voltage polarities are reversed for *pnp* transistors.

BASE BIAS

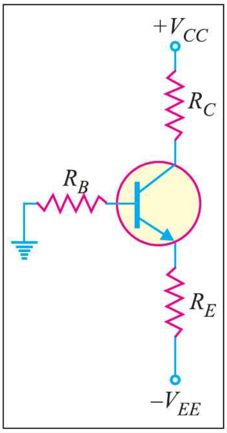


- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

- Collector-to-emitter voltage:
- $V_{CE} = V_{CC} - I_C R_C$

EMITTER BIAS

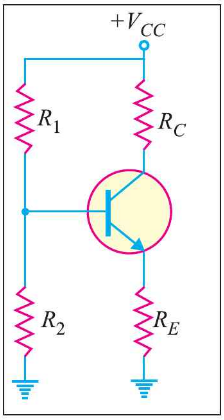


- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C \simeq \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

- Collector-to-emitter voltage:
- $V_{CE} \simeq V_{CC} + V_{EE} - I_C(R_C + R_E)$

VOLTAGE-DIVIDER BIAS

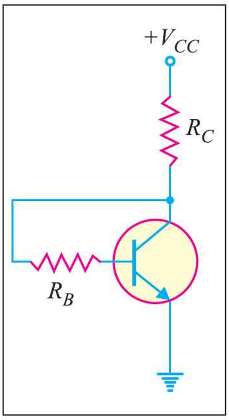


- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C \simeq \frac{\left(\frac{R_2}{R_1 + R_2}\right)V_{CC} - V_{BE}}{R_E}$$

- Collector-to-emitter voltage:
- $V_{CE} \simeq V_{CC} - I_C(R_C + R_E)$

COLLECTOR-FEEDBACK BIAS



- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C \simeq \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta}$$

- Collector-to-emitter voltage:
- $V_{CE} = V_{CC} - I_C R_C$

MULTIPLE-CHOICE QUESTIONS

1. Transistor biasing represents .... conditions.
(*i*) a.c.
(*ii*) d.c.
(*iii*) both a.c. and d.c.
(*iv*) none of the above

2. Transistor biasing is done to keep .... in the circuit.
(*i*) proper direct current
(*ii*) proper alternating current
(*iii*) the base current small
(*iv*) collector current small

3. Operating point represents ....
(*i*) values of I_C and V_{CE} when signal is applied
(*ii*) the magnitude of signal
(*iii*) zero signal values of I_C and V_{CE}
(*iv*) none of the above

4. If biasing is not done in an amplifier circuit, it results in ....
(*i*) decrease in base current
(*ii*) unfaithful amplification
(*iii*) excessive collector bias
(*iv*) none of the above

5. Transistor biasing is generally provided by a ....
(*i*) biasing circuit (*ii*) bias battery
(*iii*) diode (*iv*) none of the above

6. For faithful amplification by a transistor circuit, the value of V_{BE} should .... for a silicon transistor.
(*i*) be zero
(*ii*) be 0.01 V
(*iii*) not fall below 0.7 V
(*iv*) be between 0 V and 0.1 V

7. For proper operation of the transistor, its collector should have ....
(*i*) proper forward bias
(*ii*) proper reverse bias
(*iii*) very small size
(*iv*) none of the above

8. For faithful amplification by a transistor circuit, the value of V_{CE} should .... for silicon transistor.
(*i*) not fall below 1 V
(*ii*) be zero
(*iii*) be 0.2 V
(*iv*) none of the above

9. The circuit that provides the best stabilisation of operating point is ....
(*i*) base resistor bias
(*ii*) collector feedback bias
(*iii*) potential divider bias
(*iv*) none of the above

10. The point of intersection of d.c. and a.c. load lines represents ....
(*i*) operating point (*ii*) current gain
(*iii*) voltage gain (*iv*) none of the above

11. An ideal value of stability factor is ....
(*i*) 100 (*ii*) 200
(*iii*) more than 200 (*iv*) 1

12. The zero signal I_C is generally ...... mA in the initial stages of a transistor amplifier.
(*i*) 4 (*ii*) 1
(*iii*) 3 (*iv*) more than 10

13. If the maximum collector current due to signal alone is 3 mA, then zero signal collector current should be atleast equal to ....
(*i*) 6 mA (*ii*) 1.5 mA
(*iii*) 3 mA (*iv*) 1 mA

14. The disadvantage of base resistor method of transistor biasing is that it ....
(*i*) is complicated
(*ii*) is sensitive to changes in β
(*iii*) provides high stability
(*iv*) none of the above

15. The biasing circuit has a stability factor of 50. If due to temperature change, I_{CBO} changes by 1 μA, then I_C will change by ....
(*i*) 100 μA (*ii*) 25 μA
(*iii*) 20 μA (*iv*) 50 μA

16. For good stabilisation in voltage divider bias, the current I_1 flowing through R_1 and R_2 should be equal to or greater than ....

(*i*) 10 I_B (*ii*) 3 I_B

(*iii*) 2 I_B (*iv*) 4 I_B

17. The leakage current in a silicon transistor is about .... the leakage current in a germanium transistor.

(*i*) one hundredth (*ii*) one tenth

(*iii*) one thousandth (*iv*) one millionth

18. The operating point is also called the ....

(*i*) cut off point

(*ii*) quiescent point

(*iii*) saturation point

(*iv*) none of the above

19. For proper amplification by a transistor circuit, the operating point should be located at .... of the d.c. load line.

(*i*) the end point

(*ii*) middle

(*iii*) the maximum current point

(*iv*) none of the above

20. The operating point .... on the a.c. load line.

(*i*) also lies (*ii*) does not lie

(*iii*) may or may not lie

(*iv*) data insufficient

21. The disadvantage of voltage divider bias is that it has ....

(*i*) high stability factor

(*ii*) low base current

(*iii*) many resistors

(*iv*) none of the above

22. Thermal runaway occurs when ....

(*i*) collector is reverse biased

(*ii*) transistor is not biased

(*iii*) emitter is forward biased

(*iv*) junction capacitance is high

23. The purpose of resistance in the emitter circuit of a transistor amplifier is to ....

(*i*) limit the maximum emitter current

(*ii*) provide base-emitter bias

(*iii*) limit the change in emitter current

(*iv*) none of the above

24. In a transistor amplifier circuit, $V_{CE} = V_{CB} +$ ....

(*i*) V_{BE} (*ii*) 2 V_{BE}

(*iii*) 1.5 V_{BE} (*iv*) none of the above

25. The base resistor method is generally used in ....

(*i*) amplifier circuits

(*ii*) switching circuits

(*iii*) rectifier circuits

(*iv*) none of the above

26. For germanium transistor amplifier, V_{CE} should .... for faithful amplification.

(*i*) be zero

(*ii*) be 0.2 V

(*iii*) not fall below 0.7 V

(*iv*) none of the above

27. In a base resistor method, if the value of β changes by 50, then collector current will change by a factor of ....

(*i*) 25 (*ii*) 50

(*iii*) 100 (*iv*) 200

28. The stability factor of a collector feedback bias circuit is .... that of base resistor bias.

(*i*) the same as (*ii*) more than

(*iii*) less than (*iv*) none of the above

29. In the design of a biasing circuit, the value of collector load R_C is determined by ....

(*i*) V_{CE} consideration

(*ii*) V_{BE} consideration

(*iii*) I_B consideration

(*iv*) none of the above

30. If the value of collector current I_C increases, then value of V_{CE} ....

(*i*) remains the same

(*ii*) decreases

(*iii*) increases

(*iv*) none of the above

31. If the temperature increases, the value of V_{BE} ....

(*i*) remains the same

(*ii*) is increased

(*iii*) is decreased

(*iv*) none of the above

32. The stabilisation of operating point in potential divider method is provided by ....
(*i*) R_E consideration
(*ii*) R_C consideration
(*iii*) V_{CC} consideration
(*iv*) none of the above

33. The value of V_{BE} ....
(*i*) depends upon I_C to moderate extent
(*ii*) is almost independent of I_C
(*iii*) is strongly dependent on I_C
(*iv*) none of the above

34. When the temperature changes, the operating point is shifted due to ....
(*i*) change in I_{CBO}
(*ii*) change in V_{CC}
(*iii*) change in the values of circuit resistances
(*iv*) none of the above

35. The value of stability factor for a base-resistor bias is ....
(*i*) $R_B(\beta + 1)$ (*ii*) $(\beta + 1) R_C$
(*iii*) $(\beta + 1)$ (*iv*) $1 - \beta$

36. In a practical biasing circuit, the value of R_E is about ....
(*i*) 10 kΩ (*ii*) 1 MΩ
(*iii*) 100 kΩ (*iv*) 800 Ω

37. A silicon transistor is biased with base resistor method. If $\beta = 100$, $V_{BE} = 0.7$ V, zero signal collector current $I_C = 1$ mA and $V_{CC} = 6$ V, what is the value of base resistor R_B ?
(*i*) 105 kΩ (*ii*) 530 kΩ
(*iii*) 315 kΩ (*iv*) none of the above

38. In voltage divider bias, $V_{CC} = 25$ V ; $R_1 = 10$ kΩ; $R_2 = 2.2$ kΩ ; $R_C = 3.6$ kΩ and $R_E = 1$ kΩ. What is the emitter voltage ?
(*i*) 6.7 V (*ii*) 5.3 V
(*iii*) 4.9 V (*iv*) 3.8 V

39. In the above question, what is the collector voltage ?
(*i*) 12.3 V (*ii*) 14.8 V
(*iii*) 7.6 V (*iv*) 9.7 V

40. In voltage divider bias, operating point is 3 V, 2 mA. If $V_{CC} = 9$ V, $R_C = 2.2$ kΩ, what is the value of R_E ?
(*i*) 2000 Ω (*ii*) 1400 Ω
(*iii*) 800 Ω (*iv*) 1600 Ω

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*i*)	**3.** (*iii*)	**4.** (*ii*)	**5.** (*i*)
6. (*iii*)	**7.** (*ii*)	**8.** (*i*)	**9.** (*iii*)	**10.** (*i*)
11. (*iv*)	**12.** (*ii*)	**13.** (*iii*)	**14.** (*ii*)	**15.** (*iv*)
16. (*i*)	**17.** (*iii*)	**18.** (*ii*)	**19.** (*ii*)	**20.** (*i*)
21. (*iii*)	**22.** (*ii*)	**23.** (*iii*)	**24.** (*i*)	**25.** (*ii*)
26. (*iii*)	**27.** (*ii*)	**28.** (*iii*)	**29.** (*i*)	**30.** (*ii*)
31. (*iii*)	**32.** (*i*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*iii*)
36. (*iv*)	**37.** (*ii*)	**38.** (*iv*)	**39.** (*i*)	**40.** (*iii*)

Chapter Review Topics

1. What is faithful amplification ? Explain the conditions to be fulfilled to achieve faithful amplification in a transistor amplifier.
2. What do you understand by transistor biasing ? What is its need ?
3. What do you understand by stabilisation of operating point ?
4. Mention the essentials of a biasing circuit.
5. Describe the various methods used for transistor biasing. State their advantages and disadvantages.
6. Describe the potential divider method in detail. How stabilisation of operating point is achieved by this method ?

7. Mention the steps that are taken to design the transistor biasing and stabilisation circuits.

8. Write short notes on the following :

   (*i*) Operating point (*ii*) Stabilisation of operating point

Problems

1. An *npn* silicon transistor has V_{CC} = 5V and the collector load R_C = 2 kΩ. Find :

   (*i*) the maximum collector current that can be allowed during the application of signal for faithful amplification

   (*ii*) the minimum zero signal collector current required **[(*i*) 2mA (*ii*) 1mA]**

2. Fig. 9.48 shows biasing with base resistor method. Determine the operating point. Assume the transistor to be of silicon and take β = 100. **[I_C = 0.93 mA, V_{CE} = 17.3V]**

3. Fig. 9.49 shows biasing by base resistor method. If it is required to set the operating point at 1mA, 6 V, find the values of R_C and R_B. Given β =150, V_{BE} = 0.3 V. **[R_C = 3 kΩ, R_B = 0.3 MΩ]**

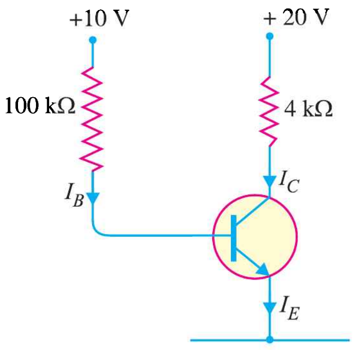


Fig. 9.48

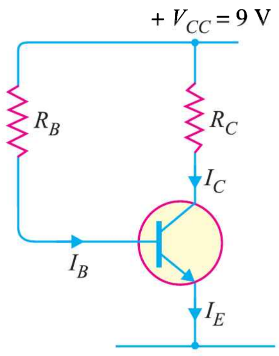


Fig. 9.49

4. A transistor amplifier is biased with feedback resistor R_B of 100 kΩ. If V_{CC} = 25 V, R_C = 1 kΩ and β = 200, find the values of zero signal I_C and V_{CE}. **[I_C = 16.2mA, V_{CE} = 8.8V]**

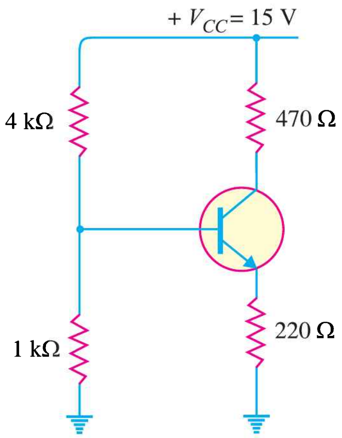


Fig. 9.50

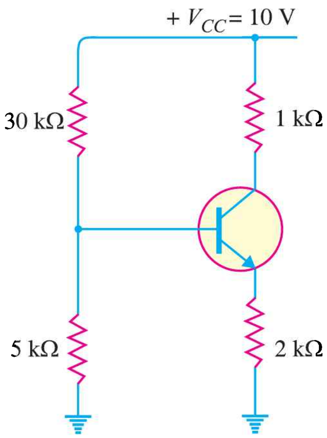


Fig. 9.51

5. Find the value of I_C for potential divider method if V_{CC} = 9V, R_E = 1kΩ, R_1 = 39 kΩ, R_2 = 10 kΩ, R_C = 2.7 kΩ, V_{BE} = 0.15 V and β = 90. **[1.5mA]**

6. In an *RC* coupled amplifier, the battery voltage is 16V and collector load R_C = 4 kΩ. It is required to set the operating point at I_C = 1mA, V_{CE} = 10V by potential divider method. If V_{BE} = 0.2 V and I_1 = 10 I_B, β = 100, find the various circuit values.

7. In the transistor circuit shown in Fig. 9.50, find the operating point. Assume the transistor to be of silicon. **[I_C = 10.5mA, V_{CE} = 7.75V]**

8. In a transistor circuit shown in Fig. 9.51, find the operating point. Assume silicon transistor is used. **[I_C = 0.365mA, V_{CE} = 8.9V]**

9. Determine whether or not the circuit shown in Fig. 9.52 is midpoint biased. **[Yes]**

10. What fault is indicated in Fig. 9.53 ? Give reasons for your answer. **[R_C is open]**

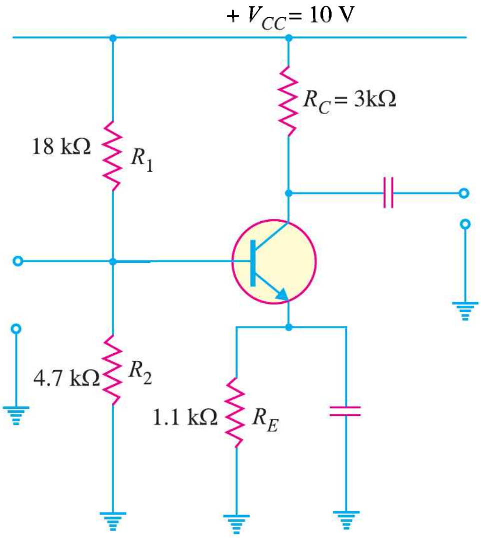


Fig. 9.52

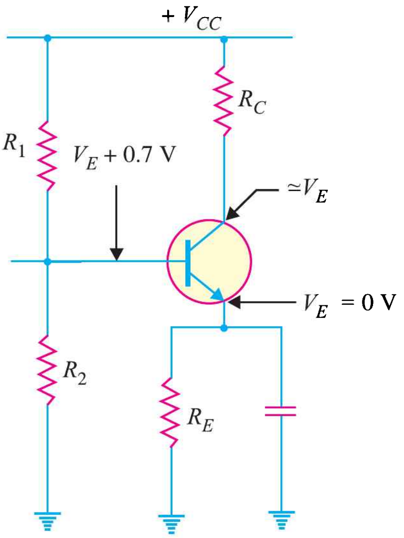
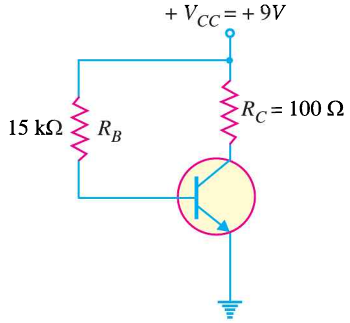


Fig. 9.53

11. Determine I_B, I_C and V_{CE} for a base-biased transistor circuit with the following values : β = 90 ; V_{CC} = 12V; R_B = 22 kΩ and R_C = 100Ω. **[I_B = 514 μA ; I_C = 46.3 mA ; V_{CE} = 7.37V]**

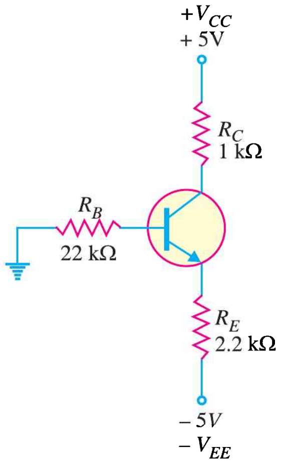
12. The base bias circuit in Fig. 9.54 is subjected to a temperature variation from 0°C to 70°C. The β decreases by 50% at 0°C and increases by 75% at 70°C from its normal value of 110 at 25°C. What are the changes in I_C and V_{CE} over the temperature range of 0°C to 70°C ?

[I_C = 59.6 mA ; V_{CE} = 5.96V]



+ V_{CC} = + 9V
15 kΩ
R_B
R_C = 100 Ω

Fig. 9.54



+V_{CC}
+ 5V
R_C
1 kΩ
R_B
22 kΩ
R_E
2.2 kΩ
– 5V
– V_{EE}

Fig. 9.55

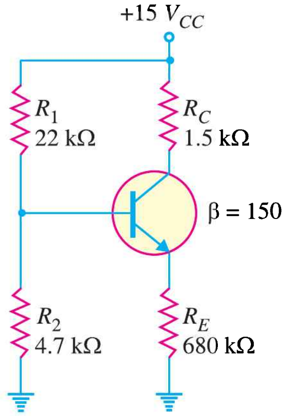
13. To what value can R_E in Fig. 9.55 be reduced without transistor going into saturation ? **[639Ω]**

14. When can the effect of β be neglected in the emitter bias circuit ? **[When $R_E >> R_B/\beta$]**

15. What is the minimum value of β in Fig. 9.56 that makes $R_{in\ (base)} \geq 10\ R_2$? **[69.1]**

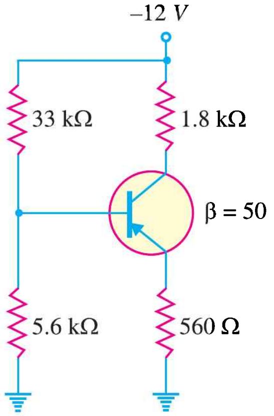
16. (*i*) Determine the base voltage V_B in Fig. 9.57.

    (*ii*) If R_E is doubled, what will be the value of V_B ? **[(*i*) 1.74V (*ii*) 1.74V]**



+15 V_{CC}
R_1
22 kΩ
R_C
1.5 kΩ
β = 150
R_2
4.7 kΩ
R_E
680 kΩ

Fig.9.56



–12 V
33 kΩ
1.8 kΩ
β = 50
5.6 kΩ
560 Ω

Fig. 9.57

17. (*i*) Find the Q-point values for Fig. 9.57.

    (*ii*) Find the minimum power rating of transistor in Fig. 9.57. **[(*i*) 1.41 mA ; – 8.67V (*ii*) 12.2 mW]**

18. A collector-feedback circuit uses an *npn* transistor with V_{CC} = 12V, R_C = 1.2 kΩ, R_B = 47 kΩ. Determine the collector voltage and the collector current if β = 200. **[7.87 mA ; 2.56V]**

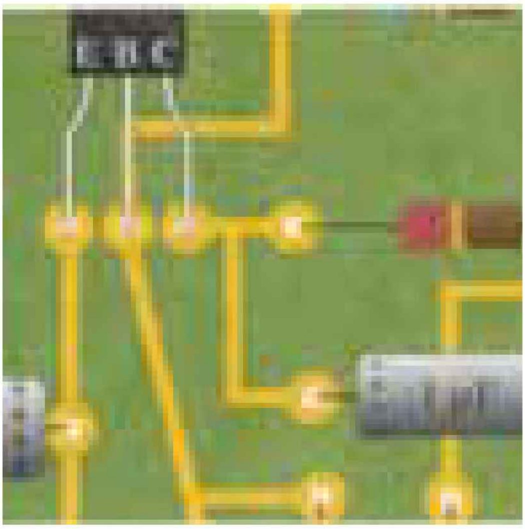
Discussion Questions

1. Why are transistor amplifiers always operated above knee voltage region ?
2. What is the utility of d.c. load line ?
3. Why have transistors inherent variations of parameters ?
4. Why is $\beta_{d.c.}$ different from $\beta_{a.c.}$?
5. Why has potential divider method of biasing become universal ?

10

Single Stage Transistor Amplifiers

10.1 Single Stage Transistor Amplifier
10.2 How Transistor Amplifies?
10.3 Graphical Demonstration of Transistor Amplifier
10.4 Practical Circuit of Transistor Amplifier
10.5 Phase Reversal
10.6 Input/Output Phase Relationships
10.7 D.C. and A.C. Equivalent Circuits
10.8 Load Line Analysis
10.9 Voltage Gain
10.10 A.C. Emitter Resistance
10.11 Formula for AC Emitter Resistance
10.12 Voltage Gain of CE Amplifier
10.13 Voltage Gain of Unloaded CE Amplifier
10.14 Voltage Gain of CE Amplifier without C_E
10.15 Input Impedance of CE Amplifier
10.16 Voltage Gain Stability
10.17 Swamped Amplifier
10.18 Classification of Amplifiers
10.19 Amplifier Equivalent Circuit
10.20 Equivalent Circuit with Signal Source
10.21 Gain and Transistor Configurations



INTRODUCTION

In the previous chapter, it was discussed that a properly biased transistor raises the strength of a weak signal and thus acts as an amplifier. Almost all electronic equipments must include means for amplifying electrical signals. For instance, radio receivers amplify very weak signals—sometimes a few millionth of a volt at antenna–until they are strong enough to fill a room with sound. The transducers used in the medical and scientific investigations generate signals in the microvolt (μV) and millivolt (mV) range. These signals must be amplified thousands and millions times before they will be strong enough to operate indicating instruments. Therefore, electronic amplifiers are a constant and important ingredient of electronic systems.

Our purpose here will be to discuss *single stage transistor amplifier*. By a *stage* we mean a single transistor with its bias and auxiliary equipment. It may be emphasised here that a practical amplifier is always a multistage amplifier *i.e.* it has a number of stages of amplification. However, it is profitable to consider the multistage amplifier in terms of single stages that are connected together. In this chapter, we shall confine our attention to single stage transistor amplifiers.

10.1 Single Stage Transistor Amplifier

When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as **single stage transistor amplifier.**

A single stage transistor amplifier has one transistor, bias circuit and other auxiliary components. Although a practical amplifier consists of a number of stages, yet such a complex circuit can be conveniently split up into separate single stages. By analysing carefully only a single stage and using this single stage analysis repeatedly, we can effectively analyse the complex circuit. It follows, therefore, that single stage amplifier analysis is of great value in understanding the practical amplifier circuits.

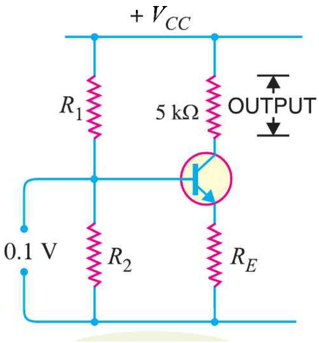


Fig. 10.1

10.2 How Transistor Amplifies ?

Fig. 10.1 shows a single stage transistor amplifier. When a weak a.c. signal is given to the base of transistor, a small base current (which is a.c.) starts flowing. Due to transistor action, a much larger (β times the base current) a.c. current flows through the collector load R_C. As the value of R_C is quite high (usually 4-10 kΩ), therefore, a large voltage appears across R_C. Thus, a weak signal applied in the base circuit appears in amplified form in the collector circuit. It is in this way that a transistor acts as an amplifier.

The action of transistor amplifier can be beautifully explained by referring to Fig. 10.1. Suppose a change of 0.1V in signal voltage produces a change of 2 mA in the collector current. Obviously, a signal of only 0.1V applied to the base will give an output voltage = 2 mA × 5 kΩ = 10V. Thus, the transistor has been able to raise the voltage level of the signal from 0.1V to 10V *i.e.* voltage amplification or stage gain is 100.

10.3 Graphical Demonstration of Transistor Amplifier

The function of transistor as an amplifier can also be explained graphically. Fig. 10.2 shows the output characteristics of a transistor in *CE* configuration. Suppose the zero signal base current is 10 μA *i.e.* this is the base current for which the transistor is biased by the biasing network. When an a.c. signal is applied to the base, it makes the base, say positive in the first half-cycle and negative in the second half-cycle. Therefore, the base and collector currents will increase in the first half-cycle when base-emitter junction is more forward-biased. However, they will decrease in the second half-cycle when the base-emitter junction is less forward biased.

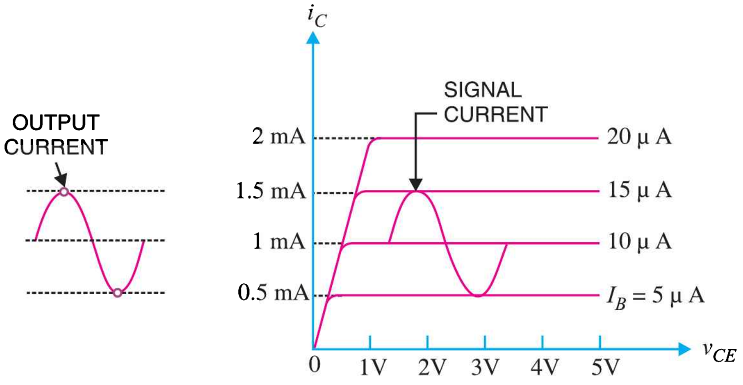


Fig. 10.2

For example, consider a sinusoidal signal which increases or decreases the base current by 5 μA in the two half-cycles of the signal. Referring to Fig. 10.2, it is clear that in the absence of signal, the base current is 10μA and the collector current is 1 mA. However, when the signal is applied in the base circuit, the base current and hence collector current change continuously. In the first half-cycle peak of the signal, the base current increases to 15 μA and the corresponding collector current is 1.5 mA. In the second half-cycle peak, the base current is reduced to 5 μA and the corresponding collector current is 0.5 mA. For other values of the signal, the collector current is inbetween these values *i.e.* 1.5 mA and 0.5 mA.

It is clear from Fig. 10.2 that 10 μA base current variation results in 1mA (1,000 μA) collector current variation *i.e.* by a factor of 100. This large change in collector current flows through collector resistance R_C. The result is that output signal is much larger than the input signal. Thus, the transistor has done amplification.

10.4 Practical Circuit of Transistor Amplifier

It is important to note that a transistor can accomplish faithful amplification only if proper associated circuitry is used with it. Fig. 10.3 shows a practical single stage transistor amplifier. The various circuit elements and their functions are described below :

(*i*) **Biasing circuit.** The resistances R_1, R_2 and R_E form the biasing and stabilisation circuit. The biasing circuit must establish a proper operating point otherwise a part of the negative half-cycle of the signal may be cut off in the output.

(*ii*) **Input capacitor C_{in}.** An electrolytic capacitor C_{in} ($\simeq$ 10 μF) is used to couple the signal to the base of the transistor. If it is not used, the signal source resistance will come across R_2 and thus change the bias. The capacitor C_{in} allows only a.c. signal to flow but isolates the signal source from R_2.*

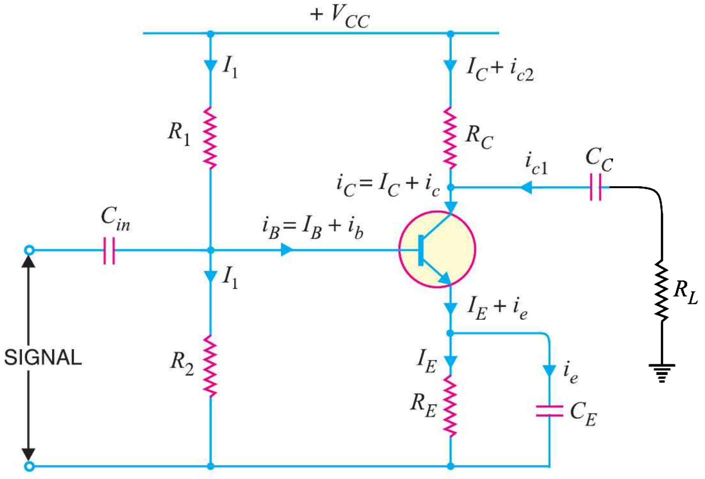


Fig. 10.3

(*iii*) **Emitter bypass capacitor C_E.** An emitter bypass capacitor C_E ($\simeq$ 100μ*F*) is used in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby reducing the output voltage.

(*iv*) **Coupling capacitor C_C.** The coupling capacitor C_C ($\simeq$ 10μ*F*) couples one stage of amplification to the next stage. If it is not used, the bias conditions of the next stage will be drastically changed due to the shunting effect of R_C. This is because R_C will come in parallel with the upper resistance R_1 of the biasing network of the next stage, thereby altering the biasing conditions of the latter. In short, the coupling capacitor C_C isolates the d.c. of one stage from the next stage, but allows the passage of a.c. signal.

---

* It may be noted that a capacitor offers infinite reactance to d.c. and blocks it completely whereas it allows a.c. to pass through it.

Various circuit currents. It is useful to mention the various currents in the complete amplifier circuit. These are shown in the circuit of Fig. 10.3.

(*i*) **Base current.** When no signal is applied in the base circuit, d.c. base current I_B flows due to biasing circuit. When a.c. signal is applied, a.c. base current i_b also flows. Therefore, with the application of signal, total base current i_B is given by:

$$i_B = I_B + i_b$$

(*ii*) **Collector current.** When no signal is applied, a d.c. collector current I_C flows due to biasing circuit. When a.c. signal is applied, a.c. collector current i_c also flows. Therefore, the total collector current i_C is given by:

$$i_C = I_C + i_c$$

where $I_C = \beta I_B$ = zero signal collector current

$i_c = \beta i_b$ = collector current due to signal.

(*iii*) **Emitter current.** When no signal is applied, a d.c. emitter current I_E flows. With the application of signal, total emitter current i_E is given by :

$$i_E = I_E + i_e$$

It is useful to keep in mind that :

$$I_E = I_B + I_C$$

$$i_e = i_b + i_c$$

Now base current is usually very small, therefore, as a reasonable approximation,

$$I_E \simeq I_C \quad \text{and} \quad i_e \simeq i_c$$

Example 10.1. *What is the role of emitter bypass capacitor C_E in CE amplifier circuit shown in Fig. 10.3 ? Illustrate with a numerical example.*

Solution. The emitter bypass capacitor C_E (See Fig. 10.3) connected in parallel with R_E plays an important role in the circuit. If it is not used, the amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby reducing the a.c. output voltage and hence the voltage gain of the amplifier.

Let us illustrate the effect of C_E with a numerical example. Suppose R_E = 1000Ω and capacitive reactance of C_E at the signal frequency is 100Ω (*i.e.* X_{C_E} = 100Ω). Then 10/11 of a.c emitter current will flow through C_E and only 1/11 through R_E. The signal voltage developed across R_E is, therefore, only 1/11 of the voltage which would have been developed if C_E were not present. In practical circuits, the value of C_E is so selected that it almost entirely bypasses the a.c. signal (the name for C_E is obvious). *For all practical purposes, we consider C_E to be a short for a.c. signals.*

Example 10.2. *Select a suitable value for the emitter bypass capacitor in Fig. 10.4 if the amplifier is to operate over a frequency range from 2 kHz to 10 kHz.*

Solution. An amplifier usually handles more than one frequency. Therefore, the value of C_E is so selected that it provides adequate bypassing for the *lowest* of all the frequencies. Then it will also be a good bypass ($X_C \propto 1/f$) for all the higher frequencies. Suppose the minimum frequency to be handled by C_E is f_{min}. Then C_E is considered a good bypass if at f_{min},

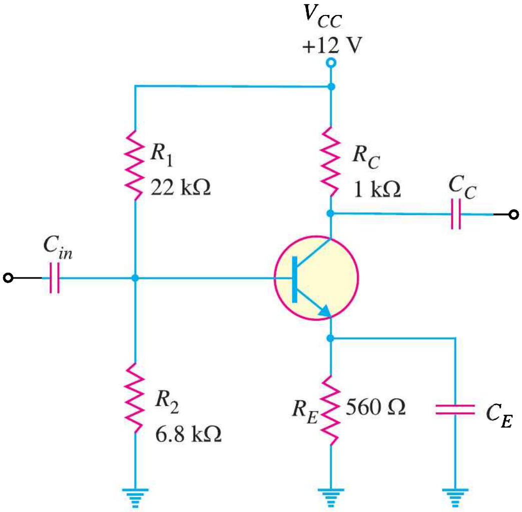


Fig. 10.4

$$X_{C_E} = \frac{R_E}{10}$$

In the given problem, $f_{min} = 2\text{kHz}$; $R_E = 560\Omega$.

$$\therefore \quad 10\, X_{C_E} = 560$$

$$\text{or} \quad X_{C_E} = 560/10 = 56\Omega$$

$$\text{or} \quad \frac{1}{2\pi\, f_{min}\, C_E} = 56$$

$$\therefore \quad C_E = \frac{1}{2\pi\, f_{min}\, 56} = \frac{1}{2\pi \times (2 \times 10^3) \times 56} = 1.42 \times 10^{-6}\, F = \mathbf{1.42\ \mu F}$$

Note. While discussing *CE* amplifier, the reader should be very particular about the role of C_E.

10.5 Phase Reversal

In common emitter connection, when the input signal voltage increases in the positive sense, the output voltage increases in the negative direction and *vice-versa*. In other words, there is a phase difference of 180° between the input and output voltage in *CE* connection. This is called phase reversal.*

The phase difference of 180° between the signal voltage and output voltage in a common emitter amplifier is known as **phase reversal.**

Consider a common emitter amplifier circuit shown in Fig. 10.5. The signal is fed at the input terminals (*i.e.* between base and emitter) and output is taken from collector and emitter end of supply. The total instantaneous output voltage v_{CE} is given by :

$$^{**}v_{CE} = V_{CC} - i_C R_C \quad \ldots(i)$$

---

* This is so if output is taken from collector and emitter end of supply as is always done. However, if the output is taken across R_C, it will be in phase with the input.

** Reactance of C_C (= 10μF) is negligible at ordinary signal frequencies. Therefore, it can be considered a short for the signal.

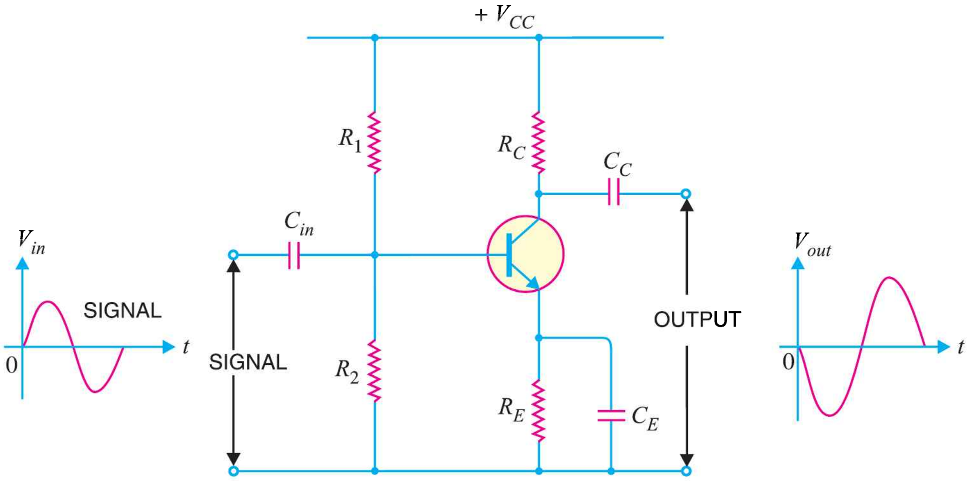


Fig. 10.5

When the signal voltage increases in the positive half-cycle, the base current also increases. The result is that collector current and hence voltage drop $i_C R_C$ increases. As V_{CC} is constant, therefore, output voltage v_{CE} decreases. In other words, as the signal voltage is increasing in the positive half-cycle, the output voltage is increasing in the negative sense *i.e.* output is 180° out of phase with the input. It follows, therefore, that in a common emitter amplifier, the positive half-cycle of the signal appears as amplified negative half-cycle in the output and *vice-versa*. It may be noted that amplification is not affected by this phase reversal.

The fact of phase reversal can be readily proved mathematically. Thus differentiating exp. (*i*), we get,

$$dv_{CE} = 0 - di_c R_C$$

or

$$dv_{CE} = - di_c R_C$$

The negative sign shows that output voltage is 180° out of phase with the input signal voltage.

Graphical demonstration. The fact of phase reversal in *CE* connection can be shown graphically with the help of output characteristics and load line (See Fig. 10.6).

In Fig. 10.6, *AB* is the load line. The base current fluctuates between, say ± 5 μA with 10μA as the zero signal base current. From the figure, it is clear that when the base current is maximum in the positive direction, v_{CE} becomes maximum in the negative direction (*point G* in Fig. 10.6). On the other hand, when the base current is maximum in the negative direction, v_{CE} is maximum in the positive sense (*point H* in Fig. 10.6). Thus, the in-

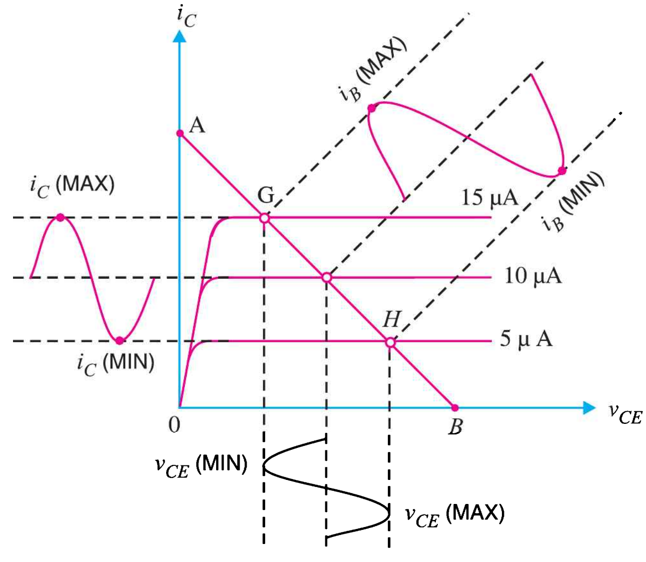


Fig. 10.6

put and output voltages are in *phase opposition* or equivalently, the transistor is said to produce a 180° phase reversal of output voltage *w.r.t.* signal voltage.

Note. No phase reversal of voltage occurs in common base and common collector amplifier. The a.c. output voltage is in phase with the a.c. input signal. For all three amplifier configurations; input and output currents are in phase.

Example 10.3. *Illustrate the phenomenon of phase reversal in CE amplifier assuming typical circuit values.*

Solution. In every type of amplifier, the input and output currents are in phase. However, common emitter amplifier has the unique property that input and output voltages are 180° out of phase, even though the input and output currents are in phase. This point is illustrated in Fig. 10.7. Here it is assumed that Q-point value of I_B = 10 μA, ac signal peak value is 5 μA and $\beta = 100$. This means that input current varies by 5 μA both above and below a 10 μA dc level. At any instant, the output current will be 100 times the input current at that instant. Thus when the input current is 10 μA, output current is $i_C = 100 \times 10$ μA = 1 mA. However, when the input current is 15 μA, then output current is $i_C = 100 \times 15$ μA = 1.5 mA and so on. Note that input and output currents are in phase.

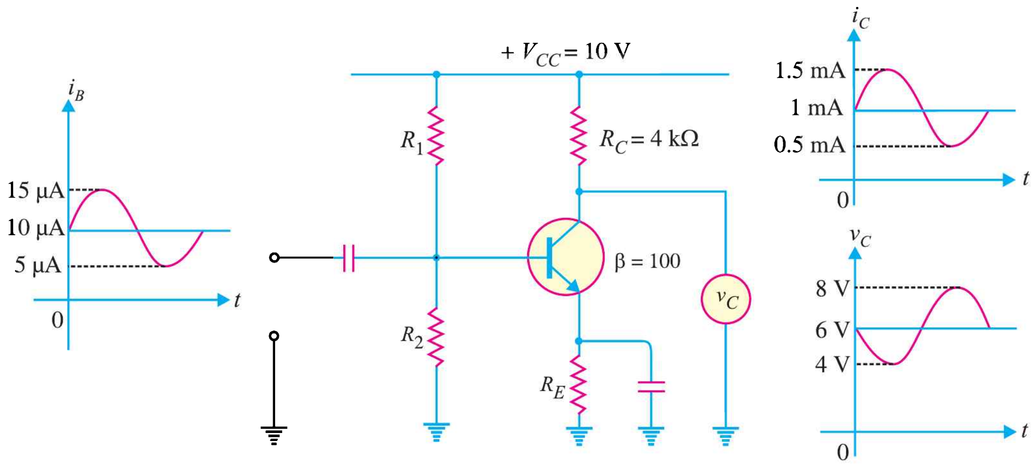


Fig. 10.7

The output voltage, $v_C = V_{CC} - i_C R_C$

(*i*) When signal current is zero (*i.e.*, in the absence of signal), i_C = 1 mA.

$$\therefore \quad v_C = V_{CC} - i_C R_C = 10\text{ V} - 1\text{ mA} \times 4\text{ k}\Omega = 6\text{V}$$

(*ii*) When signal reaches positive peak value, i_C = 1.5 mA.

$$\therefore \quad v_C = V_{CC} - i_C R_C = 10\text{ V} - 1.5\text{ mA} \times 4\text{ k}\Omega = 4\text{ V}$$

Note that as i_C increases from 1mA to 1.5 mA, v_C decreases from 6V to 4V. Clearly, output voltage is 180° out of phase from the input voltage as shown in Fig. 10.7.

(*iii*) When signal reaches negative peak, i_C = 0.5 mA.

$$\therefore \quad v_C = V_{CC} - i_C R_C = 10\text{ V} - 0.5\text{ mA} \times 4\text{ k}\Omega = 8\text{ V}$$

Note that as i_C decreases from 1.5 mA to 0.5 mA, v_C increases from 4 V to 8 V. Clearly, output voltage is 180° out of phase from the input voltage. The following points may be noted carefully about *CE* amplifier :

(*a*) The input voltage and input current are in phase.

(*b*) Since the input current and output current are in phase, input voltage and output current are in phase.

(c) Output current is 180° out of phase with the output voltage (v_C). *Therefore, input voltage and output voltage are 180° out of phase.*

10.6 Input/Output Phase Relationships

The following points regarding the input / output phase relationships between currents and voltages for the various transistor configurations may be noted :

(i) *For every amplifier type (CE, CB and CC), the input and output currents are in phase.* When the input current decreases, the output current also decreases and vice-versa.

(ii) *Remember that common emitter (CE) circuit is the* ***only configuration*** *that has input and output voltages 180° out of phase.*

(iii) For both common base (*CB*) and common collector (*CC*) circuits, the input and output voltages are in phase. If the input voltage decreases, the output voltage also decreases and vice-versa.

10.7 D.C. And A.C. Equivalent Circuits

In a transistor amplifier, both d.c. and a.c. conditions prevail. The d.c. sources set up d.c. currents and voltages whereas the a.c. source (*i.e.* signal) produces fluctuations in the transistor currents and voltages. Therefore, a simple way to analyse the action of a transistor is to split the analysis into two parts *viz.* a d.c. analysis and an a.c. analysis. In the d.c. analysis, we consider all the d.c. sources at the same time and work out the d.c. currents and voltages in the circuit. On the other hand, for a.c. analysis, we consider all the a.c. sources at the same time and work out the a.c. currents and voltages. By adding the d.c. and a.c. currents and voltages, we get the total currents and voltages in the circuit. For example, consider the amplifier circuit shown in Fig. 10.8. This circuit can be easily analysed by splitting it into *d.c. equivalent circuit* and *a.c equivalent circuit.*

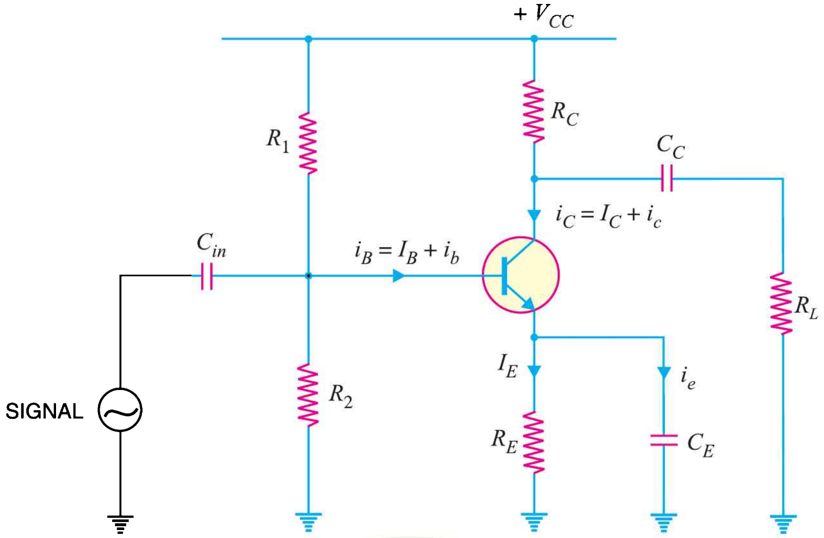


Fig. 10.8

(i) D. C. equivalent circuit. In the d.c. equivalent circuit of a transistor amplifier, only d.c. conditions are to be considered *i.e.* it is presumed that no signal is applied. As direct current cannot flow through a capacitor, therefore, *all the capacitors look like open circuits in the d.c. equivalent circuit.* It follows, therefore, that in order to draw the equivalent d.c. circuit, the following two steps are applied to the transistor circuit :

(a) Reduce all a.c. sources to zero.

(b) Open all the capacitors.

Applying these two steps to the circuit shown in Fig. 10.8, we get the d.c. equivalent circuit shown in Fig. 10.9. We can easily calculate the d.c. currents and voltages from this circuit.

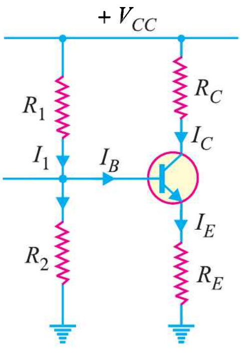


Fig. 10.9

(*ii*) A.C. equivalent circuit. In the a.c. equivalent circuit of a transistor amplifier, only a.c. conditions are to be considered. Obviously, the d.c. voltage is not important for such a circuit and may be considered zero. The capacitors are generally used to couple or bypass the a.c. signal. The designer intentionally selects capacitors that are large enough to appear as *short* circuits to the a.c. signal. It follows, therefore, that in order to draw the a.c. equivalent circuit, the following two steps are applied to the transistor circuit :

(***a***) Reduce all d.c. sources to zero (*i.e.* $V_{CC} = 0$).

(***b***) Short all the capacitors.

Applying these two steps to the circuit shown in Fig. 10.8, we get the a.c. *equivalent circuit shown in Fig. 10.10. We can easily calculate the a.c. currents and voltages from this circuit.

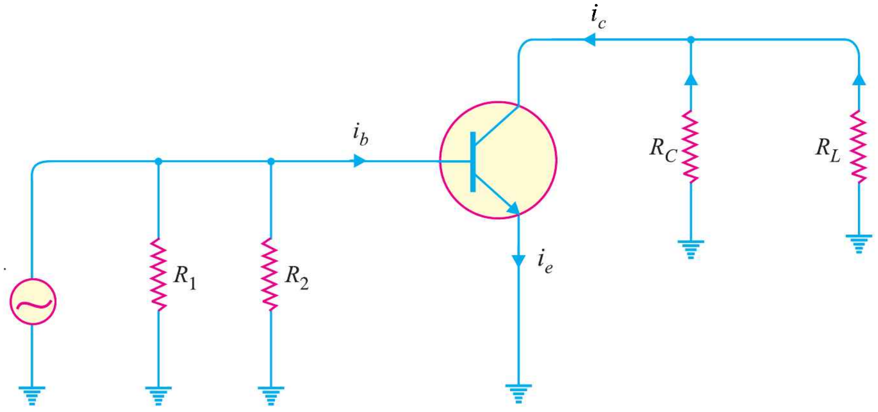


Fig. 10.10

It may be seen that total current in any branch is the sum of d.c. and a.c. currents through that branch. Similarly, the total voltage across any branch is the sum of d.c. and a.c. voltages across that branch.

Example 10.4. *For the transistor amplifier circuit shown in Fig. 10.8, determine :*

(i) d.c. load and a.c. load

(ii) maximum collector-emitter voltage and collector current under d.c. conditions

(iii) maximum collector-emitter voltage and collector current when a.c. signal is applied

Solution. Refer back to the transistor amplifier circuit shown in Fig. 10.8.

(***i***) The d.c. load for the transistor is Thevenin's equivalent resistance as seen by the collector and emitter terminals. Thus referring to the d.c. equivalent circuit shown in Fig. 10.9, Thevenin's equivalent resistance can be found by shorting the voltage source (*i.e.* V_{CC}) as shown in Fig. 10.11. Because a voltage source looks like a short, it will bypass all other resistances except R_C and R_E which will appear in series. Consequently, transistor amplifier will see a d.c. load of $R_C + R_E$ *i.e* d.c. load = $\mathbf{R_C + R_E}$

---

* Note that R_1 is also in parallel with transistor input so far as signal is concerned. Since R_1 is connected from the base lead to V_{CC} and V_{CC} is at "ac ground", R_1 is effectively connected from the base lead to ground as far as signal is concerned.

Referring to the a.c. equivalent circuit shown in Fig. 10.10, it is clear that as far as a.c. signal is concerned, resistance R_C appears in parallel with R_L. In other words, transistor amplifier sees an a.c. load equal to $R_C \parallel R_L$ *i.e.*

a.c. load, $R_{AC} = R_C \parallel R_L$

$$= \frac{\boldsymbol{R_C\, R_L}}{\boldsymbol{R_C + R_L}}$$

(ii) Referring to d.c. equivalent circuit of Fig. 10.9,

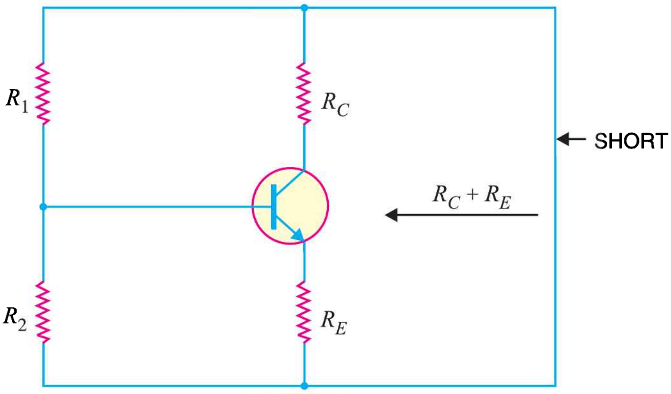


Fig. 10.11

$$V_{CC} = V_{CE} + I_C\,(R_C + R_E)$$

The maximum value of V_{CE} will occur when there is no collector current *i.e.* $I_C = 0$.

∴ Maximum $V_{CE} = \mathbf{V_{CC}}$

The maximum collector current will flow when $V_{CE} = 0$.

$$\therefore \quad \text{Maximum } I_C = \frac{\boldsymbol{V_{CC}}}{\boldsymbol{R_C + R_E}}$$

(iii) When no signal is applied, V_{CE} and I_C are the collector-emitter voltage and collector current respectively. When a.c. signal is applied, it causes changes to take place above and below the operating point Q (*i.e.* V_{CE} and I_C).

Maximum collector current due to a.c. signal = *I_C

∴ Maximum positive swing of a.c. collector-emitter voltage

$$= I_C \times R_{AC}$$

Total maximum collector-emitter voltage

$$= V_{CE} + I_C R_{AC}$$

Maximum positive swing of a.c. collector current

$$= V_{CE}/R_{AC}$$

∴ Total maximum collector current

$$= I_C + V_{CE}/R_{AC}$$

10.8 Load Line Analysis

The output characteristics are determined experimentally and indicate the relation between V_{CE} and I_C. However, the same information can be obtained in a much simpler way by representing the mathematical relation between I_C and V_{CE} graphically. As discussed before, the relationship between V_{CE} and I_C is linear so that it can be represented by a straight line on the output characteristics. This is known as a *load line*. The points lying on the load line give the possible values of V_{CE} and I_C in the output circuit. As in a transistor circuit both d.c. and a.c. conditions exist, therefore, there are two types of load lines, namely ; d.c. load line and a.c. load line. The former determines the locus of I_C and V_{CE} in the zero signal conditions and the latter shows these values when the signal is applied.

(i) **d.c. load line.** *It is the line on the output characteristics of a transistor circuit which gives the values of I_C and V_{CE} corresponding to zero signal or d.c. conditions.*

---

* For faithful amplification.

Consider the transistor amplifier shown in Fig. 10.12. In the absence of signal, d.c. conditions prevail in the circuit as shown in Fig. 10.13 (*i*). Referring to this circuit and applying Kirchhoff's voltage law,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

or

$$V_{CE} = V_{CC} - I_C\ (R_C + R_E) \qquad \ldots(i)$$

$$(\because\ I_E \simeq I_C)$$

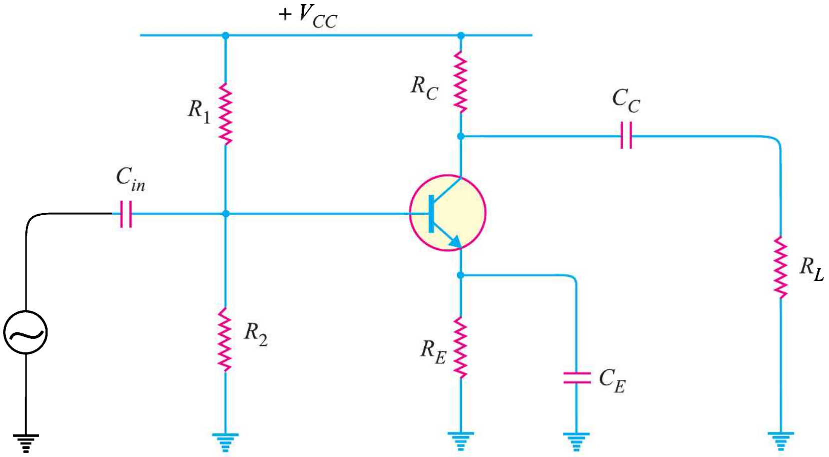


Fig. 10.12

As for a given circuit, V_{CC} and $(R_C + R_E)$ are constant, therefore, it is a first degree *equation and can be represented by a straight line on the output characteristics. This is known as *d.c. load line* and determines the loci of V_{CE} and I_C points in the zero signal conditions. The d.c. load line can be readily plotted by locating two *end points* of the straight line.

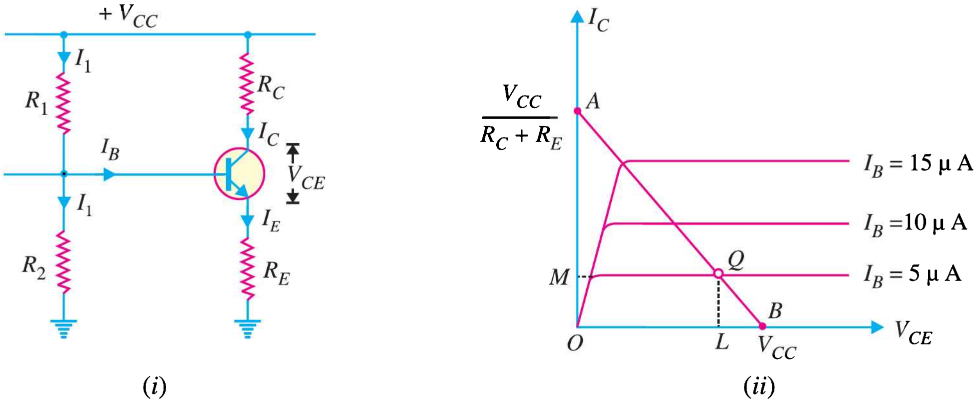


Fig. 10.13

The value of V_{CE} will be maximum when $I_C = 0$. Therefore, by putting $I_C = 0$ in exp. (*i*), we get,

$$\text{Max. } V_{CE} = V_{CC}$$

This locates the first point B ($OB = V_{CC}$) of the d.c. load line.

---

* This equation is known as **load line equation** since it relates the collector-emitter voltage (V_{CE}) to the collector current (I_C) flowing through the load.

The value of I_C will be maximum when $V_{CE} = 0$.

$$\therefore \qquad \text{Max. } I_C = \frac{V_{CC}}{R_C + R_E}$$

This locates the second point A ($OA = V_{CC}/R_C + R_E$) of the d.c. load line. By joining points A and B, d.c. load line AB is constructed [See Fig. 10.13 (*ii*)].

Alternatively. The two end points of the d.c. load line can also be determined in another way.

$$V_{CE} + I_C\,(R_C + R_E) = V_{CC}$$

Dividing throughout by V_{CC}, we have,

$$\frac{V_{CE}}{V_{CC}} + \frac{I_C}{(V_{CC}/R_C + R_E)} = 1 \qquad \text{...(}i\text{)}$$

The equation of a line having intercepts a and b on x-axis and y-axis respectively is given by ;

$$\frac{x}{a} + \frac{y}{b} = 1 \qquad \text{...(}ii\text{)}$$

Comparing eqs. (*i*) and (*ii*), we have,

$$\text{Intercept on } x\text{-axis} = V_{CC}$$

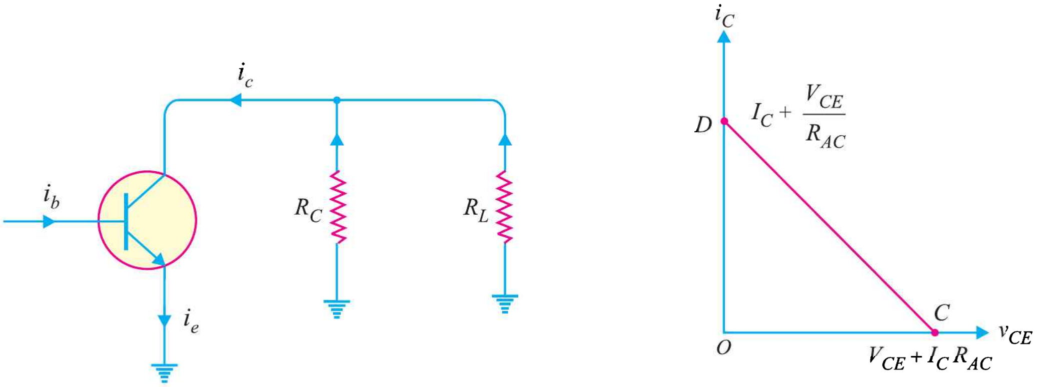
$$\text{Intercept on } y\text{-axis} = \frac{V_{CC}}{R_C + R_E}$$

With the construction of d.c. load line on the output characteristics, we get the complete information about the output circuit of transistor amplifier in the zero signal conditions. All the points showing zero signal I_C and V_{CE} will obviously lie on the d.c. load line. At the same time I_C and V_{CE} conditions in the circuit are also represented by the output characteristics. Therefore, actual operating conditions in the circuit will be represented by the point where d.c. load line intersects the base current curve under study. Thus, referring to Fig. 10.13 (*ii*), if $I_B = 5$ μA is set by the biasing circuit, then Q (*i.e.* intersection of 5 μA curve and load line) is the operating point.

(*ii*) a.c. load line. *This is the line on the output characteristics of a transistor circuit which gives the values of i_C and v_{CE} when signal is applied.*

Referring back to the transistor amplifier shown in Fig. 10.12, its a.c. equivalent circuit as far as output circuit is concerned is as shown in Fig. 10.14 (*i*). To add a.c. load line to the output characteristics, we again require two end points–one maximum collector-emitter voltage point and the other maximum collector current point. Under the application of a.c. signal, these values are (refer to example 10.4) :

Max. collector-emitter voltage $= V_{CE} + I_C R_{AC}$. This locates the point C of the a.c. load line on the collector-emitter voltage axis.



(*i*) (*ii*)

Fig. 10.14

$$\text{Maximum collector current} = I_C + \frac{V_{CE}}{R_{AC}}$$

where
$$R_{AC} = R_C \| R_L = \frac{R_C\, R_L}{R_C + R_L}$$

This locates the point *D* of a.c. load line on the collector-current axis. By joining points *C* and *D*, the a.c.load line *CD* is constructed [See Fig. 10.14 (*ii*)].

Example 10.5. *For the transistor amplifier shown in Fig. 10.15,* $R_1 = 10\ \text{k}\Omega$, $R_2 = 5\ \text{k}\Omega$, $R_C = 1\ \text{k}\Omega$, $R_E = 2\ \text{k}\Omega$ *and* $R_L = 1\ \text{k}\Omega$.

(i) Draw d.c. load line (ii) Determine the operating point (iii) Draw a.c. load line. Assume $V_{BE} = 0.7$ *V.*

Solution. (*i*) d.c. load line :

To draw d.c. load line, we require two end points *viz* maximum V_{CE} point and maximum I_C point.

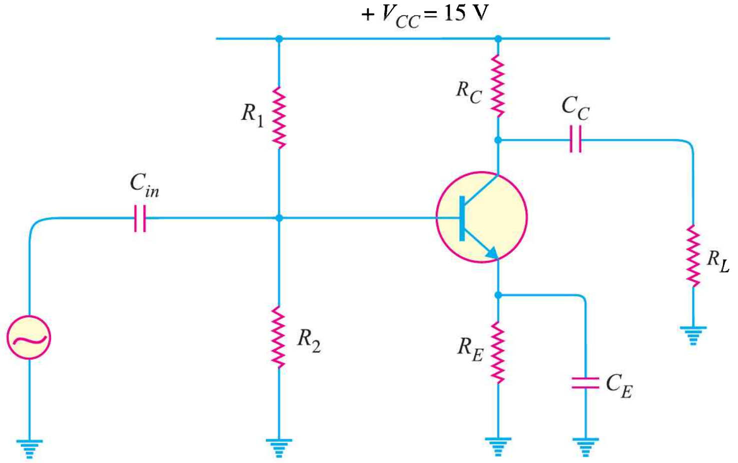


Fig. 10.15

$$\text{Maximum } V_{CE} = V_{CC} = 15 \text{ V [See Art. 10.8]}$$

This locates the point *B* (*OB*=15 V) of the d.c. load line.

$$\text{Maximum } I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15\ V}{(1+2)\ \text{k}\Omega} = 5 \text{ mA} \qquad \text{[See Art. 10.8]}$$

This locates the point *A* (*OA* = 5 mA) of the d.c. load line. Fig. 10.16 (*i*) shows the d.c. load line *AB*.

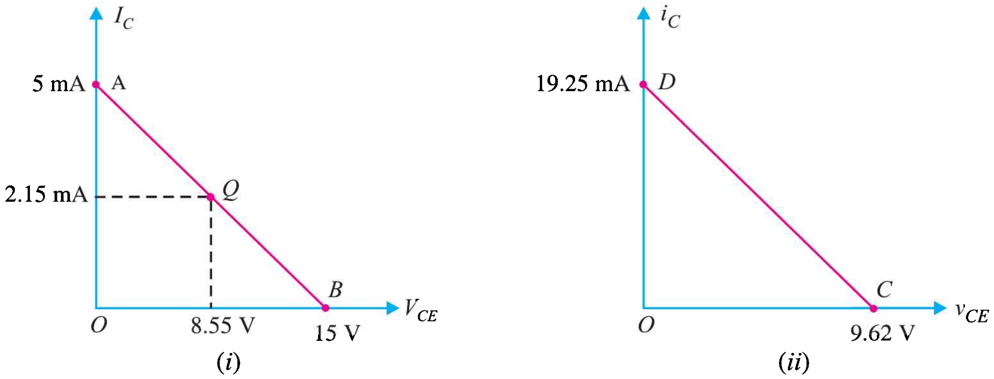


Fig. 10.16

(*ii*) **Operating point Q.** The voltage across R_2 (= 5 kΩ) is *5 V *i.e.* V_2 = 5 V.

$$\text{Now} \quad V_2 = V_{BE} + I_E R_E$$

$$\therefore \quad I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{(5-0.7)\,V}{2\text{ k}\Omega} = 2.15\text{ mA}$$

$$\therefore \quad I_C = I_E = 2.15\text{ mA}$$

$$\text{Now} \quad V_{CE} = V_{CC} - I_C(R_C + R_E) = 15 - 2.15\text{ mA} \times 3\text{ k}\Omega$$

$$= 8.55\text{ V}$$

∴ Operating point *Q* is **8.55 V, 2.15 mA.** This is shown on the d.c. load line.

(*iii*) **a.c. load line.** To draw a.c. load line, we require two end points *viz.* maximum collector-emitter voltage point and maximum collector current point when signal is applied.

$$\text{a.c. load, } R_{AC} = R_C \,||\, R_L = \frac{1\times 1}{1+1} = 0.5\text{ k}\Omega$$

∴ Maximum collector-emitter voltage

$$= V_{CE} + I_C R_{AC} \qquad \text{[See example 10.4]}$$

$$= 8.55 + 2.15\text{ mA} \times 0.5\text{ k}\Omega = 9.62\text{ volts}$$

This locates the point *C* (*OC* = 9.62 V) on the v_{CE} axis.

$$\text{Maximum collector current} = I_C + V_{CE}/R_{AC}$$

$$= 2.15 + (8.55\text{ V}/0.5\text{ k}\Omega) = 19.25\text{ mA}$$

This locates the point *D* (*OD* = 19.25mA) on the i_C axis. By joining points *C* and *D*, a.c. load line *CD* is constructed [See Fig. 10.16 (*ii*)].

Example 10.6. *In the transistor amplifier shown in Fig. 10.15,* R_C *= 10 kΩ,* R_L *= 30 kΩ and* V_{CC} *= 20V. The values* R_1 *and* R_2 *are such so as to fix the operating point at 10V, 1mA. Draw the d.c. and a.c. load lines. Assume* R_E *is negligible.*

Solution. d.c. load line. For drawing d.c. load line, two end points *viz.* maximum V_{CE} point and maximum I_C point are needed. Maximum V_{CE} = 20 V. This locates the point *B* (*OB* = 20V) of the d.c. load line on the V_{CE} axis.

$$\text{Maximum } I_C = \frac{V_{CC}}{R_C + R_E} = \frac{20\,V}{10\text{ k}\Omega} = 2\text{ mA}$$

This locates the point *A* (*OA* = 2 mA) on the I_C axis. By joining points *A* and *B*, the d.c. load line *AB* is constructed (See Fig. 10.17).

a.c. load line. To draw a.c. load line, we require two end points *viz* maximum collector-emitter voltage point and maximum collector current point when signal is applied.

$$\text{a.c. load, } R_{AC} = R_C \,||\, R_L = \frac{10\times 30}{10+30} = 7.5\text{ k}\Omega$$

Maximum collector-emitter voltage

$$= V_{CE} + I_C R_{AC}$$

$$= 10 + 1\text{ mA} \times 7.5\text{ k}\Omega = 10 + 7.5 = 17.5\text{ V}$$

This locates the point *D* (*OD* = 17.5 V) on the v_{CE} axis.

$$\text{Maximum collector current} = I_C + V_{CE}/R_{AC}$$

$$= 1\text{ mA} + 10\text{ V}/7.5\text{ k}\Omega = 1\text{ mA} + 1.33\text{ mA} = 2.33\text{ mA}$$

---

* Voltage across series combination of R_1 and R_2 is 15 V. Applying voltage divider theorem, voltage across R_2 = 5 V.

This locates the point C ($OC = 2.33$ mA) on the i_C axis. By joining points C and D, a.c. load line CD is constructed (See Fig. 10.17).

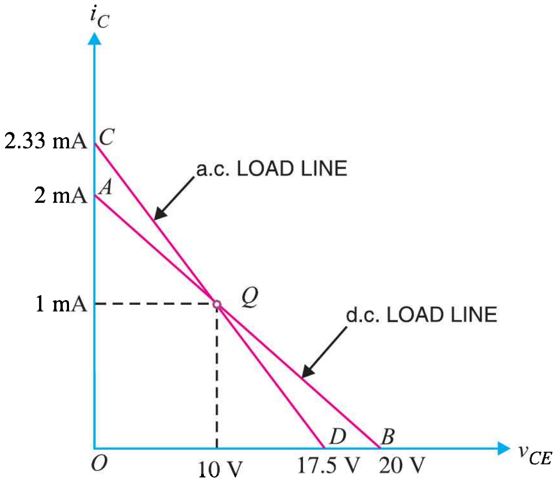

i_C
2.33 mA
C
2 mA
A
a.c. LOAD LINE
1 mA
Q
d.c. LOAD LINE
D
B
O
10 V
17.5 V
20 V
v_{CE}

Fig. 10.17

Comments. The reader may see that the operating point lies on both a.c. and d.c. load lines. It is not surprising because signal is a.c. and it becomes zero after every half-cycle. When the signal is zero, we have the exact d.c. conditions. Therefore, key point to keep in mind is that the point of intersection of d.c. and a.c. load lines is the operating point Q.

Example 10.7. *In a transistor amplifier, the operating point Q is fixed at 8V, 1mA. When a.c. signal is applied, the collector current and collector-emitter voltage change about this point. During the positive peak of signal,* $i_C = 1.5$ *mA and* $v_{CE} = 7$ *V and during negative peak,* $i_C = 0.5$*mA and* $v_{CE} = 9$*V. Show this phenomenon with the help of a.c. load line.*

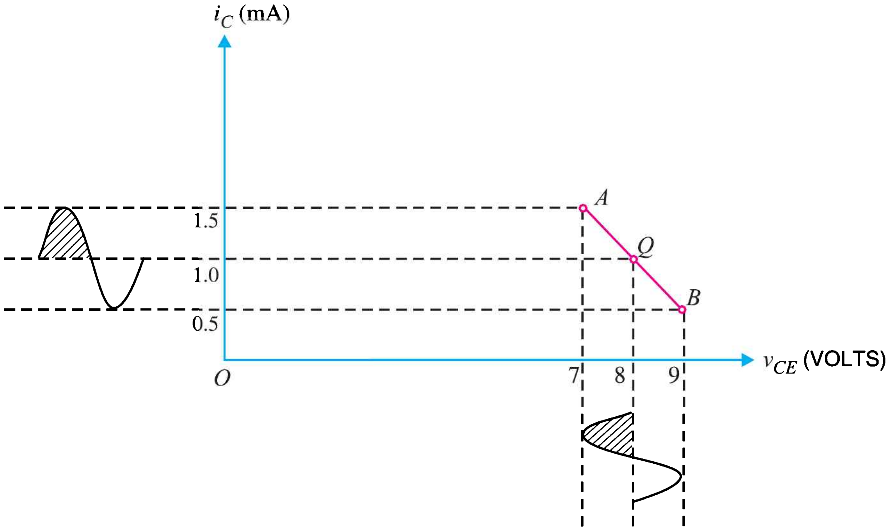

i_C (mA)
1.5
1.0
0.5
O
A
Q
B
7
8
9
v_{CE} (VOLTS)

Fig. 10.18

Solution. Fig. 10.18 shows the whole process. When no signal is applied, $v_{CE} = 8$ V and $i_C = 1$mA. This is represented by the operating point Q on the a.c. load line. During the positive half-cycle of a.c. signal, i_C swings from 1 mA to 1.5 mA and v_{CE} swings from 8 V to 7 V. This is represented by point A on the a.c. load line. During the negative half-cycle of the signal, i_C swings from 1 mA to 0.5 mA and v_{CE} swings from 8 V to 9 V. This is represented by the point B on the a.c. load line.

The following points may be noted :

(*i*) When a.c. signal is applied, the collector current and collector-emitter voltage variations take place about the operating point Q.

(*ii*) When a.c. signal is applied, operating point moves along the a.c. load line. In other words, at any instant of a.c. signal, the co-ordinates of collector current and collector-emitter voltage are on the a.c. load line.

10.9 Voltage Gain

The basic function of an amplifier is to raise the strength of an a.c. input signal. The voltage gain of the amplifier is the ratio of a.c. output voltage to the a.c. input signal voltage. Therefore, in order to find the voltage gain, we should consider only the a.c. currents and voltages in the circuit. For this purpose, we should look at the a.c. equivalent circuit of transistor amplifier. For facility of reference,the a.c. equivalent circuit of transistor amplifier is redrawn in Fig. 10.19.

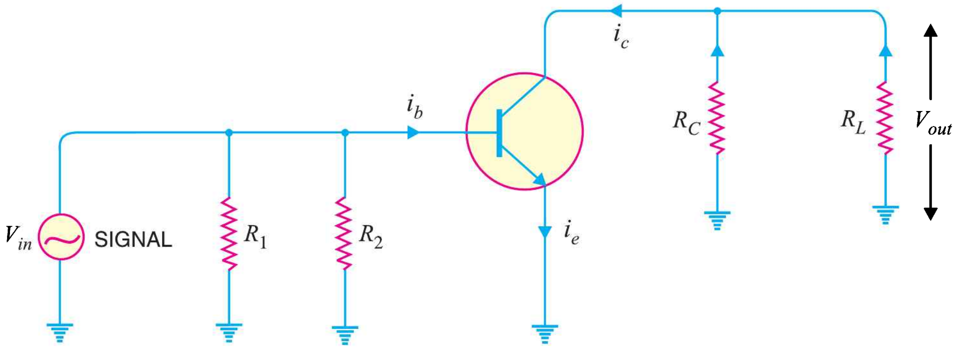


Fig. 10.19

It is clear that as far as a.c. signal is concerned, load R_C appears in parallel with R_L. Therefore, effective load for a.c. is given by :

$$\text{a.c. load, } R_{AC} = R_C \,||\, R_L = \frac{R_C \times R_L}{R_C + R_L}$$

$$\text{Output voltage, } V_{out} = i_c R_{AC}$$

$$\text{Input voltage, } V_{in} = i_b R_{in}$$

$$\therefore \quad \text{Voltage gain, } A_v = V_{out}/V_{in}$$

$$= \frac{i_c R_{AC}}{i_b R_{in}} = \beta \times \frac{R_{AC}}{R_{in}} \qquad \left(\because \frac{i_c}{i_b} = \beta\right)$$

Incidentally, power gain is given by;

$$A_p = \frac{i_c^2 R_{AC}}{i_b^2 R_{in}} = \beta^2 \times \frac{R_{AC}}{R_{in}}$$

Example 10.8. *In the circuit shown in Fig. 10.20, find the voltage gain. Given that* $\beta = 60$ *and input resistance* $R_{in} = 1\ k\Omega$.

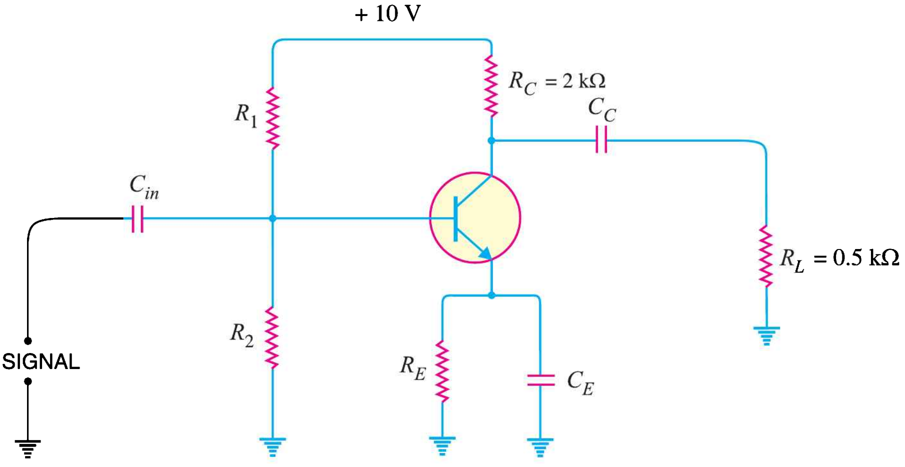


Fig. 10.20

Solution. So far as voltage gain of the circuit is concerned, we need only R_{AC}, β and R_{in}.

$$\text{Effective load, } R_{AC} = R_C \,||\, R_L$$

$$= \frac{R_C \times R_L}{R_C + R_L} = \frac{2 \times 0.5}{2 + 0.5} = 0.4\ \text{k}\Omega$$

$$\therefore \quad \text{Voltage gain} = \beta \times \frac{R_{AC}}{R_{in}} = \frac{60 \times 0.4\ \text{k}\Omega}{1\ \text{k}\Omega} = \mathbf{24}$$

Example 10.9. *In the circuit shown in Fig. 10.20, if* $R_C = 10\ k\Omega$, $R_L = 10\ k\Omega$, $R_{in} = 2.5\ k\Omega$, $\beta = 100$, *find the output voltage for an input voltage of 1mV r.m.s.*

Solution.

$$\text{Effective load, } R_{AC} = \frac{R_C \times R_L}{R_C + R_L} = \frac{10 \times 10}{10 + 10} = 5\ \text{k}\Omega$$

$$\text{Voltage gain} = \beta \times \frac{R_{AC}}{R_{in}} = 100 \times \frac{5\ \text{k}\Omega}{2.5\ \text{k}\Omega} = 200$$

or

$$\frac{V_{out}}{V_{in}} = 200$$

$$\therefore \quad V_{out} = 200 \times V_{in} = 200 \times 1\ \text{mV} = \mathbf{200\ mV}$$

Example 10.10. *In a transistor amplifier, when the signal changes by 0.02V, the base current changes by 10 μA and collector current by 1mA. If collector load* $R_C = 5\ k\Omega$ *and* $R_L = 10\ k\Omega$, *find: (i) current gain (ii) input impedance (iii) a.c. load (iv) voltage gain (v) power gain.*

Solution. $\Delta I_B = 10\ \mu\text{A}$, $\Delta I_C = 1\text{mA}$, $\Delta V_{BE} = 0.02\ \text{V}$, $R_C = 5\ \text{k}\Omega$, $R_L = 10\ \text{k}\Omega$

(*i*)

$$\text{Current gain, } \beta = \frac{\Delta I_C}{\Delta I_B} = \frac{1\,mA}{10\ \mu A} = \mathbf{100}$$

(*ii*) Input impedance, $R_{in} = \dfrac{\Delta V_{BE}}{\Delta I_B} = \dfrac{0.02\,V}{10\,\mu A} = \mathbf{2\ k\Omega}$

(*iii*) a.c. load, $R_{AC} = \dfrac{R_C \times R_L}{R_C + R_L} = \dfrac{5\times 10}{5+10} = \mathbf{3.3\ k\Omega}$

(*iv*) Voltage gain, $A_v = \beta \times \dfrac{R_{AC}}{R_{in}} = 100 \times \dfrac{3.3}{2} = \mathbf{165}$

(*v*) Power gain, A_p = current gain × voltage gain = 100 × 165 = **16500**

Example 10.11. *In Fig. 10.21, the transistor has* $\beta = 50$*. Find the output voltage if input resistance* $R_{in} = 0.5\ k\Omega$*.*

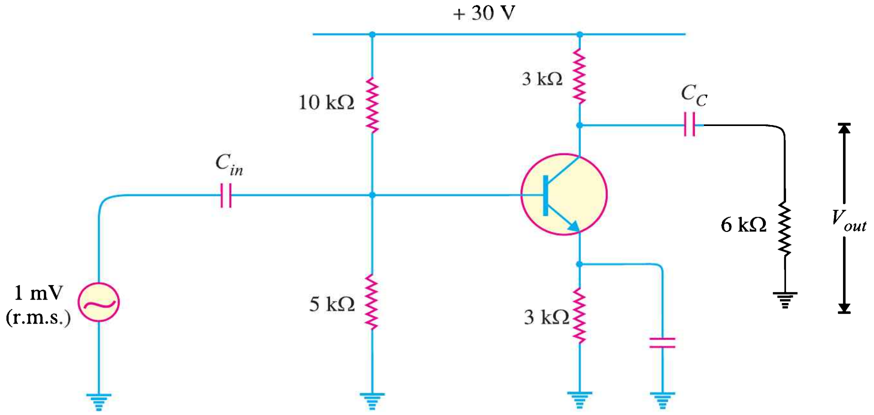


Fig. 10.21

Solution. $\beta = 50, \quad R_{in} = 0.5\ \text{k}\Omega$

a.c. load, $R_{AC} = R_C \,||\, R_L = \dfrac{R_C \times R_L}{R_C + R_L} = \dfrac{3\times 6}{3+6} = 2\ \text{k}\Omega$

∴ Voltage gain $= \beta \times R_{AC}/R_{in} = 50 \times 2/0.5 = 200$

or $\dfrac{V_{out}}{V_{in}} = 200$

∴ Output voltage, $V_{out} = 200 \times V_{in} = 200 \times (1\ \text{mV}) = \mathbf{200\ mV}$

Example 10.12. *Fig. 10.22 shows a transistor circuit. The manufacturer of the circuit shows that collector potential is to be + 6V. The voltage measured at point B by a technician is found to be + 4V. Is the circuit operating properly ?*

Solution. The voltage at point B is equal to the voltage across R_1. Now total voltage V_T across the series combination of R_1 and R_2 is 6 V. Therefore, using voltage divider method, we have,

$$V_B = \text{Voltage across } R_1$$

$$= \frac{R_1}{R_1 + R_2} \times V_T = \frac{1}{1+2} \times 6 = 2\ \text{V}$$

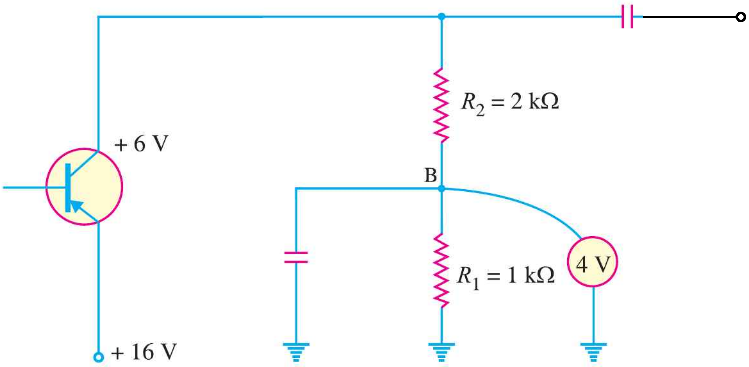


Fig. 10.22

The circuit is not operating properly. It is because the voltage at point B should be 2 V instead of 4 V.

10.10 A.C. Emitter Resistance

The ac or dynamic resistance of emitter-base junction diode of a transistor is called ac emitter resistance. It is defined as the change in base-emitter voltage divided by change in corresponding emitter current [See Fig. 10.23] *i.e.*

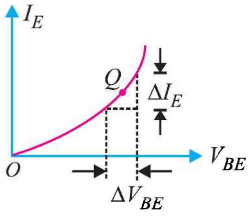


Fig. 10.23

$$R_{ac} = \frac{\Delta V_{BE}}{\Delta I_E}$$

For instance, suppose an ac base voltage change of 1 mV produces an ac emitter current change of 50 μA. Then emitter diode has an ac resistance of

$$R_{ac} = \frac{1\ \text{mV}}{50\ \mu A} = 20\ \Omega$$

10.11 Formula For AC Emitter Resistance

It can be shown mathematically that the ac resistance of emitter diode is given by ;

$$R_{ac} = \frac{25\ \text{mV}}{I_E}$$

where I_E = *dc* emitter current (= V_E/R_E) at Q point

Note the significance of this formula. It implies that ac emitter resistance can be found simply by substituting the quiescent value of emitter current into the equation. There is no need to have the characteristics available. It is important to keep in mind that this formula is accurate only for small signal operation. It is a usual practice to represent ac emitter resistance by r_e'.

$$\therefore \qquad r_e' = \frac{25\ \text{mV}}{I_E}$$

The subscript *e* indicates emitter. The lower case *r* is used to indicate an ac resistance. The prime shows that it is an internal resistance.

Example 10.13. *Determine the ac emitter resistance for the transistor circuit shown in Fig. 10.24.*

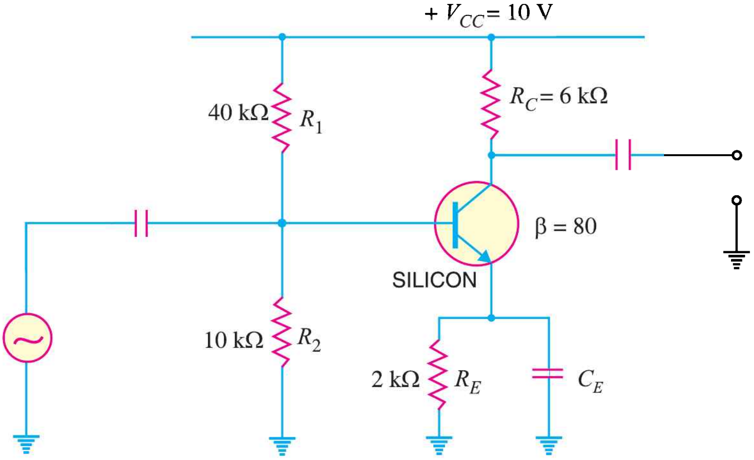


Fig. 10.24

Solution. Voltage across R_2, $V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{10}{40+10} \times 10 = 2\text{ V}$

Voltage across R_E, $V_E = V_2 - V_{BE} = 2 - 0.7 = 1.3\text{ V}$

Emitter current, $I_E = \frac{V_E}{R_E} = \frac{1.3\,V}{2\text{ k}\Omega} = 0.65\text{ mA}$

∴ *AC* emitter resistance, $r_e' = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{0.65\text{ mA}} = \mathbf{38.46\Omega}$

10.12 Voltage Gain of CE Amplifier

The voltage gain (A_v) of an amplifier is equal to a.c. output voltage (v_{out}) divided by a.c. input voltage (v_{in}) *i.e.* $A_v = v_{out}/v_{in}$. We have already seen that voltage gain of a *CE* amplifier is given by;

$$\text{Voltage gain, } A_v = \beta \times \frac{R_C}{R_{in}} \quad \text{... for unloaded amplifier}$$

$$= \beta \times \frac{R_{AC}}{R_{in}} \quad \text{... for loaded amplifier}$$

Remember that $R_{AC} = R_C \parallel R_L$

The above formula for A_v can be used if we know the values of R_C (or R_{AC}), β and R_{in}. Generally, all these values are not known. In that case, we can find the value of A_v in terms of *total a.c. collector resistance* and *total a.c. emitter resistance*. For the circuit shown in Fig. 10.25 (*with C_E connected across R_E*), it can be proved that the voltage gain is given by ;

$$\text{Voltage gain, } A_v = \frac{R_C}{r_e'} \quad \text{... for unloaded amplifier}$$

$$= \frac{R_{AC}}{r_e'} \quad \text{... for loaded amplifier}$$

10.13 Voltage Gain of Unloaded *CE* Amplifier

Fig. 10.25 shows the circuit of unloaded *CE* amplifier (*i.e.* no load R_L is connected to the circuit).

Note that emitter bypass capacitor C_E is connected in parallel with emitter resistance R_E. The capacitor C_E acts as a *short to the a.c. signal so that it bypasses the a.c. signal to the ground. Therefore, the emitter is effectively at a.c. ground. It is important to note that C_E plays an important role in determining the voltage gain (A_v) of the *CE* amplifier. If it is removed, the voltage gain of the amplifier is greatly reduced (soon you will see the reason for it).

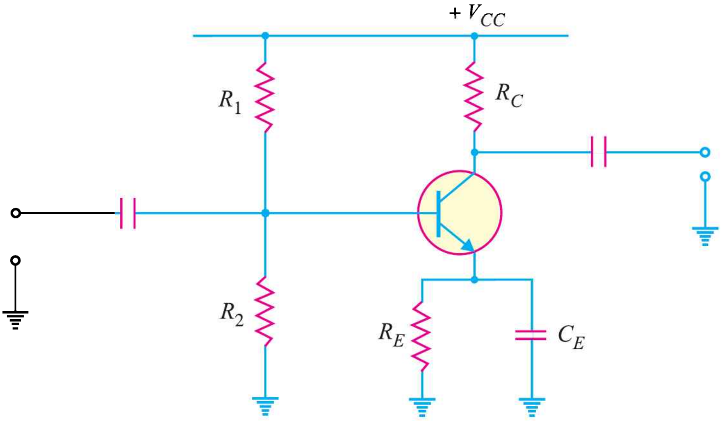
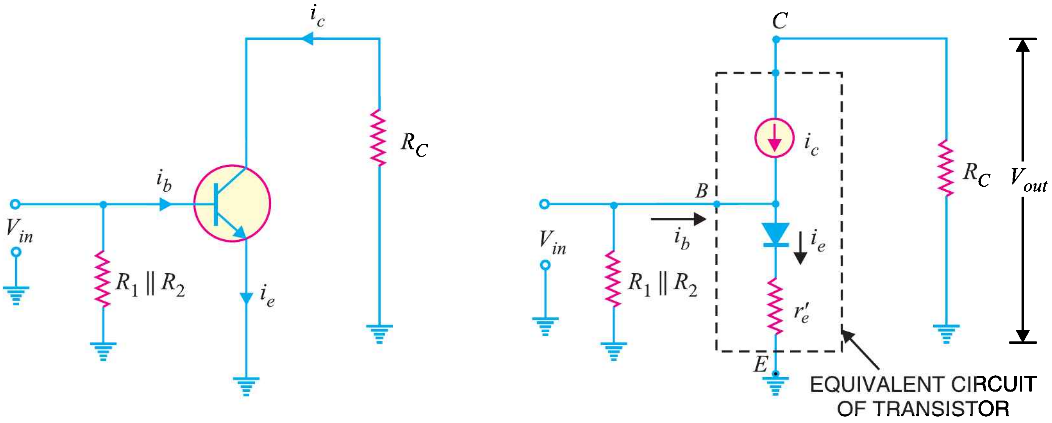

$+V_{CC}$
R_1
R_C
R_2
R_E
C_E

Fig. 10.25

$$\text{Voltage gain, } A_v = \frac{R_C}{r_e'}$$

where R_C = ac collector resistance

r_e' = ac emitter resistance = 25 mV/I_E


i_c
R_C
i_b
V_{in}
$R_1 \parallel R_2$
i_e
C
B
i_c
R_C
V_{out}
V_{in}
i_b
i_e
$R_1 \parallel R_2$
r_e'
E
EQUIVALENT CIRCUIT OF TRANSISTOR

(*i*) (*ii*)

Fig. 10.26

---

* The size of C_E is so selected that it offers negligible reactance to the frequencies handled by the amplifier (See Example 10.2).

Derivation. Fig. 10.25 shows the common emitter amplifier. The ac equivalent circuit of the amplifier is shown in Fig. 10.26. (*i*). Replacing the transistor by its *equivalent circuit, we get the circuit shown in Fig. 10.26 (*ii*). Note that current source is still connected between the collector and base terminals while the diode between the base and emitter terminals. Further, the input current is the base current (i_b) while the output current is still i_c.

Note that input voltage (V_{in}) is applied across the diode and r_e'. Assuming the diode to be ideal (so that it can be replaced by a wire), the *ac* emitter current is given by :

$$i_e = \frac{V_{in}}{r_e'}$$

or $$V_{in} = i_e r_e' \qquad \text{...}(i)$$

Assuming $i_c = i_e$, we have,

$$V_{out} = i_c R_C = i_e R_C$$

∴ Voltage gain, $$A_v = \frac{V_{out}}{V_{in}} = \frac{i_e R_C}{i_e r_e'} = \frac{R_C}{r_e'}$$

or $$A_v = \frac{R_C}{r_e'}$$

where R_C = total a.c. collector resistance

r_e' = total a.c. emitter resistance

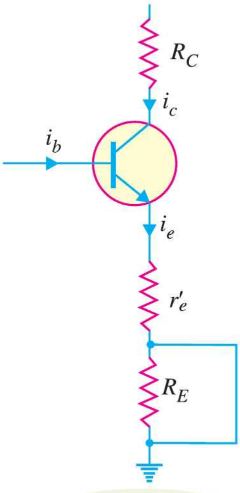
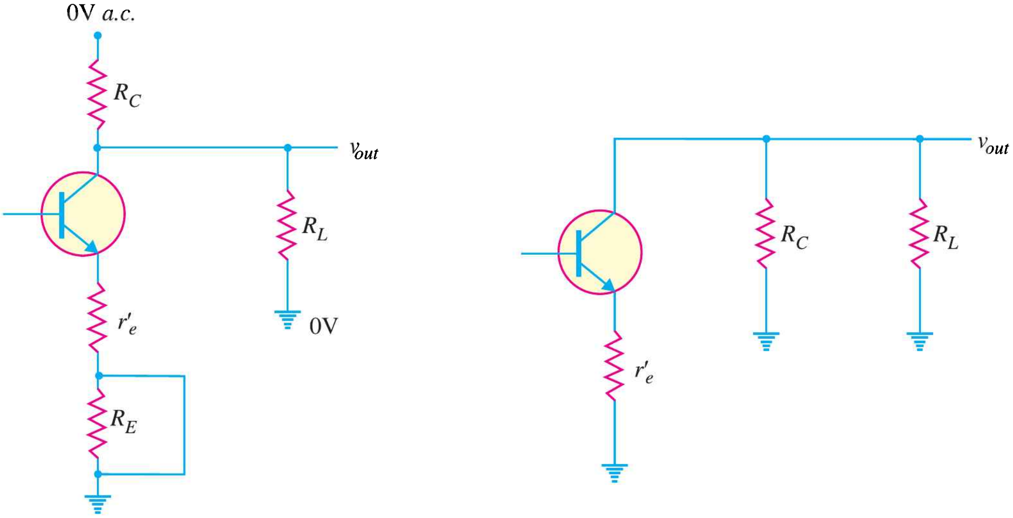


Fig. 10.27

Fig. 10.27 shows the simple a.c. model of *CE* amplifier with C_E connected across R_E. Note that C_E behaves as a short so that R_E is cut out from the emitter circuit for a.c. signal. Therefore, as for as a.c. signal is concerned, the total a.c. emitter resistance is r_e'.

Voltage gain for loaded amplifier. Fig. 10.28 (*i*) shows a part of a.c. equivalent circuit of the



(*i*) (*ii*)

Fig. 10.28

---

* The transistor equivalent circuit contains three components *viz.*,

(*i*) A resistor r_e' which represents ac emitter resistance.

(*ii*) A diode which represents the emitter-base junction of the transistor.

(*iii*) A current source which represents the current being supplied to R_C from the collector of the transistor.

CE amplifier. Note that load R_L is connected to the circuit. Remember that for a.c. analysis, V_{CC} = 0V *i.e.* at ground. Since both R_C and R_L are connected to the collector on one side and ground on the other, the two resistors are in *parallel as shown in Fig. 10.28 (*ii*).

$$\text{Total a.c. collector resistance, } R_{AC} = R_C \,||\, R_L = \frac{R_C R_L}{R_C + R_L}$$

$$\text{Total a.c. emitter resistance} = r'_e$$

$$\therefore \quad \text{Voltage gain, } A_v = \frac{R_{AC}}{r'_e}$$

10.14 Voltage Gain of *CE* Amplifier Without C_E

When we remove the emitter bypass capacitor from the *CE* amplifier shown in Fig. 10.25, the voltage gain of the circuit is greatly reduced. The reason is simple. Without the emitter bypass capacitor C_E, the emitter is no longer at the ac ground as shown in Fig. 10.29. Therefore, for the a.c. signal, both r'_e and R_E are in series. As a result, the voltage gain of the amplifier becomes :

$$\text{Voltage gain, } A_v = \frac{R_C}{r'_e + R_E} \quad \text{... for unloaded amplifier}$$

$$= \frac{R_{AC}}{r'_e + R_E} \quad \text{... for loaded amplifier}$$

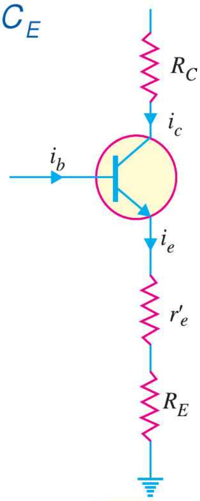


Fig. 10.29

Example 10.14. *For the amplifier circuit shown in Fig. 10.30, find the voltage gain of the amplifier with (i) C_E connected in the circuit (ii) C_E removed from the circuit.*

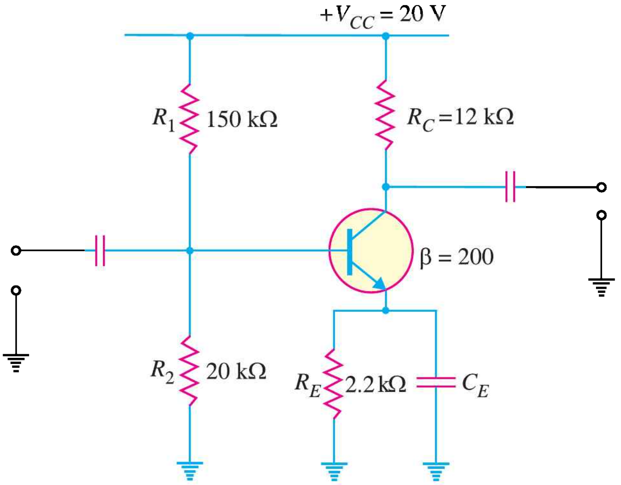


Fig. 10.30

Solution. We shall first find D.C. I_E and hence r'_e.

---

* Note that C_C behaves as a short for a.c. and is replaced by a wire in the two a.c. circuits.

In order to find D.C. I_E, we shall proceed as under :

$$\text{D.C. voltage across } R_2,\ V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{20}{150 + 20} \times 20 = 2.35\text{ V}$$

$$\text{D.C. voltage across } R_E,\ V_E = V_2 - V_{BE} = 2.35 - 0.7 = 1.65\text{ V}$$

$$\therefore \quad \text{D.C. emitter current, } I_E = \frac{V_E}{R_E} = \frac{1.65\,V}{2.2\text{ k}\Omega} = 0.75\text{ mA}$$

$$\therefore \quad \text{AC emitter resistance, } r_e' = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{0.75\text{ mA}} = 33.3\ \Omega$$

(*i*) **With C_E connected**

$$\text{Voltage gain, } A_v = \frac{R_C}{r_e'} = \frac{12\text{ k}\Omega}{33.3\ \Omega} = \mathbf{360}$$

(*ii*) **Without C_E**

$$\text{Voltage gain, } A_v = \frac{R_C}{r_e' + R_E} = \frac{12\text{ k}\Omega}{33.3\ \Omega + 2.2\text{ k}\Omega} = \mathbf{5.38}$$

What a difference the emitter bypass capacitor C_E makes ! With C_E connected, $A_v = 360$ and when C_E is removed, the voltage gain goes down to 5.38.

Example 10.15. *If in the above example, a load of 6 kΩ is connected (with C_E connected) to the collector terminal through a capacitor, what will be the voltage gain of the amplifier?*

Solution. Amplifiers are used to provide ac power to the load. When load R_L is connected to the collector terminal through a capacitor, the total ac resistance of collector changes to :

$$R_{AC} = R_C \,||\, R_L = 12\text{ k}\Omega \,||\, 6\text{ k}\Omega = \frac{12 \times 6}{12 + 6} = 4\text{ k}\Omega$$

The value of ac emitter resistance remains the same.

$$\therefore \quad \text{Voltage gain, } A_v = \frac{R_{AC}}{r_e'} = \frac{4\text{ k}\Omega}{33.3\ \Omega} = \mathbf{120}$$

Thus voltage gain of the amplifier is reduced from 360 to 120 when load is connected to the circuit.

Comments. This example shows the fact that voltage gain of the amplifier is *reduced* when load is connected to it. Conversely, if the load is removed from an amplifier, the voltage gain will *increase*. If a load goes open circuit, the effect will be the same as removing the load entirely. Thus the primary symptom of an open load in an amplifier is an *increase* in the voltage gain of the circuit.

Example 10.16. *For the circuit shown in Fig. 10.31, find (i) a.c. emitter resistance (ii) voltage gain (iii) d.c. voltage across both capacitors.*

Solution.

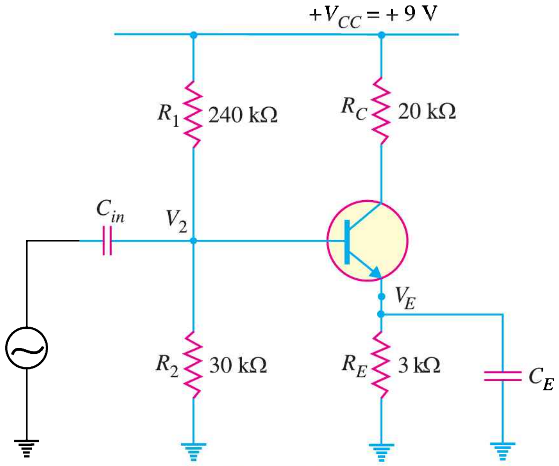
(*i*) In order to find a.c. emitter resistance r_e', we shall first find D.C. emitter current I_E. To find I_E, we proceed as under :

$$\text{D.C. voltage across } R_2,\ V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{9}{240 + 30} \times 30 = 1\text{V}$$

$$\text{D.C. voltage across } R_E,\ V_E = V_2 - V_{BE} = 1\text{V} - 0.7\text{V} = 0.3\text{V}$$

$$\therefore \quad \text{D.C. emitter current, } I_E = \frac{V_E}{R_E} = \frac{0.3\text{V}}{3\text{ k}\Omega} = 0.1\text{ mA}$$

$$\text{Now} \quad \text{A.C. emitter resistance, } r_e' = \frac{25\text{ mV}}{I_E} = \frac{25\text{mV}}{0.1\text{ mA}} = \mathbf{250\Omega}$$



$+V_{CC} = +9$ V
R_1
240 kΩ
R_C
20 kΩ
C_{in}
V_2
V_E
R_2
30 kΩ
R_E
3 kΩ
C_E

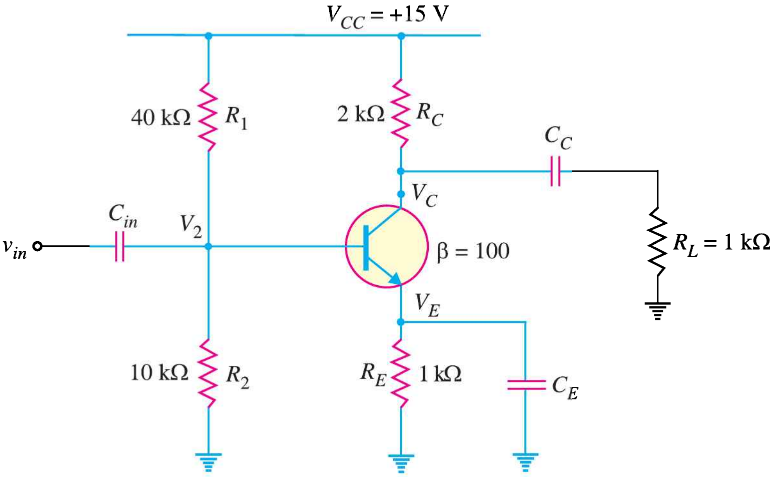
Fig. 10.31

(*ii*) Voltage gain, $A_v = \frac{R_C}{r'_e} = \frac{20\text{ k}\Omega}{250\ \Omega} = \mathbf{80}$

(*iii*) The d.c. voltage across input capacitor is equal to the d.c. voltage at the base of the transistor which is $V_2 = 1$V. Therefore, d.c. voltage across C_{in} is **1V.**

Similarly, d.c. voltage across C_E = d.c voltage at the emitter = V_E = **0.3V.**

Example 10.17. *For the circuit shown in Fig. 10.32, find (i) the d.c. bias levels (ii) d.c. voltages across the capacitors (iii) a.c. emitter resistance (iv) voltage gain and (v) state of the transistor.*



$V_{CC} = +15$ V
40 kΩ
R_1
2 kΩ
R_C
C_C
V_C
C_{in}
V_2
v_{in}
β = 100
$R_L = 1$ kΩ
V_E
10 kΩ
R_2
R_E
1 kΩ
C_E

Fig. 10.32

Solution.

(*i*) **D.C. bias levels.** The d.c. bias levels mean various d.c. currents and d.c. voltages.

$$\text{D.C. Voltage across } R_2, V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{15}{40+10}\ 10 = 3\text{V}$$

$$\therefore \quad \text{D.C. base voltage} = V_2 = \mathbf{3V}$$

$$\text{D.C. voltage across } R_E, V_E = V_2 - V_{BE} = 3\text{V} - 0.7\text{V} = \mathbf{2.3V}$$

$$\text{D.C. emitter current, } I_E = \frac{V_E}{R_E} = \frac{2.3\text{V}}{1\text{ k}\Omega} = \mathbf{2.3\ mA}$$

$$\begin{aligned}
\text{D.C. collector current, } I_C &= I_E = \mathbf{2.3\ mA}\\
\text{D.C. base current, } I_B &= I_C/\beta = 2.3\text{ mA}/100 = \mathbf{0.023\ mA}\\
\text{D.C. collector voltage, } V_C &= V_{CC} - I_C R_C\\
&= 15\text{V} - 2.3\text{ mA} \times 2\text{ k}\Omega = \mathbf{10.4V}
\end{aligned}$$

Therefore, all d.c. bias levels stand calculated.

(*ii*)
$$\begin{aligned}
\text{D.C. voltage across } C_{in} &= V_2 = \mathbf{3V}\\
\text{D.C. voltage across } C_E &= V_E = \mathbf{2.3V}\\
\text{D.C. voltage across } C_C &= V_C = \mathbf{10.4V}
\end{aligned}$$

(*iii*)
$$\text{a.c. emitter resistance, } r_e' = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{2.3\text{ mA}} = \mathbf{10.9\Omega}$$

(*iv*) Total a.c. collector resistance is given by ;

$$R_{AC} = R_C \| R_L = \frac{R_C R_L}{R_C + R_L} = \frac{2 \times 1}{2 + 1} = 0.667\text{ k}\Omega$$

$$\therefore \quad \text{Voltage gain, } A_v = \frac{R_{AC}}{r_e'} = \frac{0.667\text{ k}\Omega}{10.9\ \Omega} = \mathbf{61.2}$$

(*v*) As calculated above, $V_C = 10.4\text{V}$ and $V_E = 2.3\text{V}$. Since $V_C > V_E$, the transistor is in **active state.**

Example 10.18. *An amplifier has a voltage gain of 132 and* $\beta = 200$. *Determine the power gain and output power of the amplifier if the input power is 60 μW.*

Solution.

$$\begin{aligned}
\text{Power gain, } A_p &= \text{current gain} \times \text{voltage gain}\\
&= \beta \times A_v = 200 \times 132 = \mathbf{26400}\\
\text{Output power, } P_{out} &= A_p \times P_{in} = (26400)(60\ \mu\text{W}) = \mathbf{1.584\ W}
\end{aligned}$$

Example 10.19. *For the circuit shown in Fig. 10.33, determine (i) the current gain (ii) the voltage gain and (iii) the power gain. Neglect the a.c. emitter resistance for the transistor.*

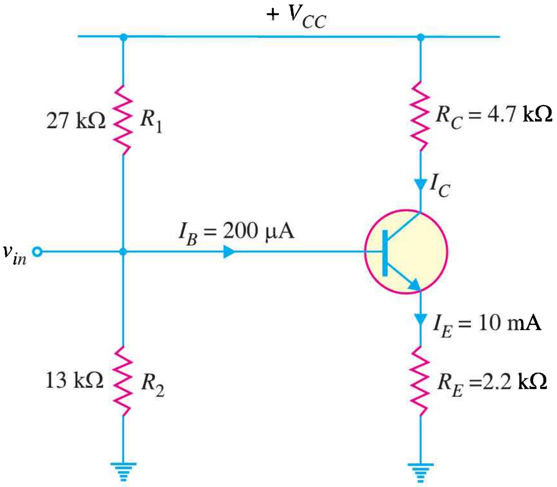


Fig. 10.33

Solution. In most practical circuits, the value of a.c. emitter resistance r_e' for the transistor is generally quite small as compared to R_E and can be neglected in circuit calculations with reasonable accuracy.

(*i*) $$I_C = I_E - I_B = 10\text{ mA} - 200\ \mu\text{A} = 9.8\text{ mA}$$

$$\text{Current gain, } A_i = \beta = \frac{I_{out}}{I_{in}} = \frac{I_C}{I_B} = \frac{9.8\text{ mA}}{200\ \mu\text{A}} = \mathbf{49}$$

(*ii*) $$\text{Voltage gain, } A_v = \frac{R_C}{R_E} = \frac{4.7\text{ k}\Omega}{2.2\text{ k}\Omega} = \mathbf{2.14}$$

(*iii*) $$\text{Power gain, } A_p = A_i \times A_v = 49 \times 2.14 = \mathbf{105}$$

10.15 Input Impedance of *CE* Amplifier

When one CE amplifier is being used to drive another, the input impedance of the second amplifier will serve as the load resistance of the first. Therefore, in order to calculate the voltage gain (A_v) of the first amplifier stage correctly, we must calculate the input impedance of the second stage.

The input impedance of an amplifier can be found by using the ac equivalent circuit of the amplifier as shown in Fig. 10.34.

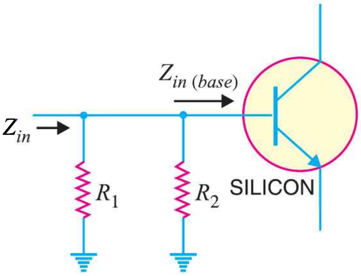


Fig. 10.34

$$Z_{in} = R_1 \,||\, R_2 \,||\, Z_{in\,(base)}$$

where Z_{in} = input impedance of the amplifier

$Z_{in\,(base)}$ = input impedance of transistor base

Now $Z_{in\,(base)} = {}^*\beta\, r_e'$

The input impedance [Z_{in}] is always less than the input impedance of the base [$Z_{in(base)}$].

Example 10.20. *Determine the input impedance of the amplifier circuit shown in Fig. 10.35.*

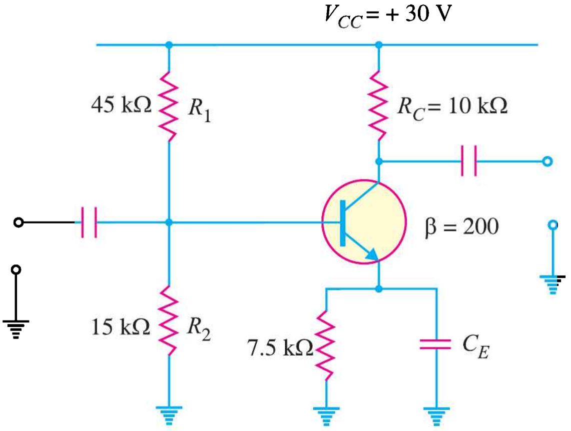


Fig. 10.35

Solution. Voltage across R_2, $V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{30}{45 + 15} \times 15 = 7.5\text{ V}$

---

* $Z_{in(base)} = \frac{V_{in}}{i_b} = \frac{i_e r_e'}{i_b}$. Since $\frac{i_e}{i_b}$ is approximately equal to β, $Z_{in\,(base)} = \beta\, r_e'$.

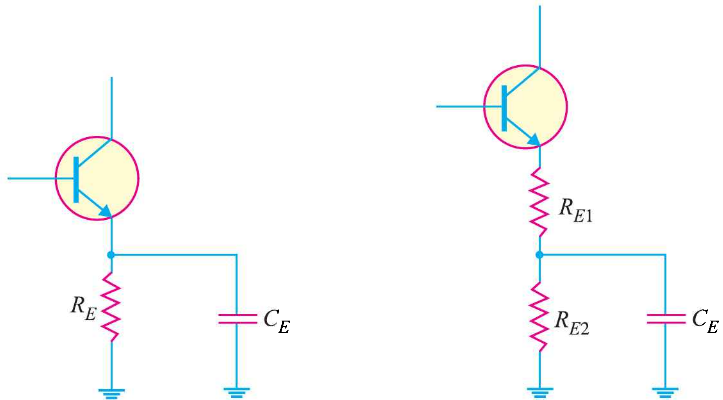
$$\begin{aligned}
\text{Voltage across } R_E, V_E &= V_2 - V_{BE} = 7.5 - 0.7 \simeq 7.5\text{ V}\\
\text{Emitter current, } I_E &= \frac{V_E}{R_E} = \frac{7.5\text{ V}}{7.5\text{ k}\Omega} = 1\text{ mA}\\
\text{AC emitter resistance, } r'_e &= 25\text{ mV}/I_E = 25\text{ mV}/1\text{ mA} = 25\ \Omega\\
Z_{in\,(base)} &= \beta\, r'_e = 200 \times 25 = 5 \times 10^3\ \Omega = 5\text{ k}\Omega\\
\therefore \qquad Z_{in} &= R_1 \,\|\, R_2 \,\|\, Z_{in\,(base)}\\
&= 45\text{ k}\Omega \,\|\, 15\text{ k}\Omega \,\|\, 5\text{ k}\Omega = \mathbf{3.45\ k\Omega}
\end{aligned}$$

10.16 Voltage Gain Stability

One important consideration for an amplifier is the stability of its voltage gain. An amplifier should have voltage gain values that are stable so that the output of the circuit is predictable under all normal conditions. In a standard *CE* amplifier, the entire d.c. emitter resistance R_E is bypassed by the bypass emitter capacitor C_E. Therefore, the total a.c. emitter resistance is r'_e. The voltage gain of such an amplifier at no-load is given by ;

$$\text{Voltage gain, } A_v = \frac{R_C}{r'_e} \quad \text{where } r'_e = \frac{25\text{ mV}}{I_E}$$

The voltage gain of a standard *CE* amplifier is quite large. However, the drawback of the circuit is that its voltage gain changes with emitter current I_E, temperature variations and transistor replacement. For example, if emitter current I_E increases, the a.c. emitter resistance r'_e decreases. This changes the voltage gain of the amplifier. Similarly, when the temperature varies or when a transistor is replaced, the a.c. current gain β changes. This will also result in the change in voltage gain. In order to stabilise the voltage gain, the emitter resistance R_E is partially bypassed by C_E. Such an amplifier is called a *swamped amplifier.*



Standard *CE* Amplifier
(*i*)

Swamped Amplifier
(*ii*)

Fig. 10.36

Fig. 10.36 (*i*) shows the emitter leg of a standard *CE* amplifier while Fig. 10.36 (*ii*) shows the emitter leg of swamped amplifier. In swamped amplifier, the resistance R_E is split into two parts *viz.* R_{E1} and R_{E2}. Only R_{E2} is bypassed by C_E while R_{E1} is not.

10.17 Swamped Amplifier

Fig. 10.37 shows the circuit of a swamped amplifier. Note that d.c. emitter resistance R_E is divided into two parts *viz.* R_{E1} and R_{E2}. Only resistance R_{E2} is bypassed by the capacitor C_E while resistance

R_{E1} is not. This method swamps or minimises the effect of r'_e on the voltage gain without reducing the voltage gain too much. Now the total a.c. emitter resistance is ($r'_e + R_{E1}$) instead of r'_e as in a standard *CE* amplifier. Therefore, the voltage gain of a swamped amplifier at no-load becomes :

$$\text{Voltage gain, } A_v = \frac{R_C}{r'_e + R_{E1}}$$

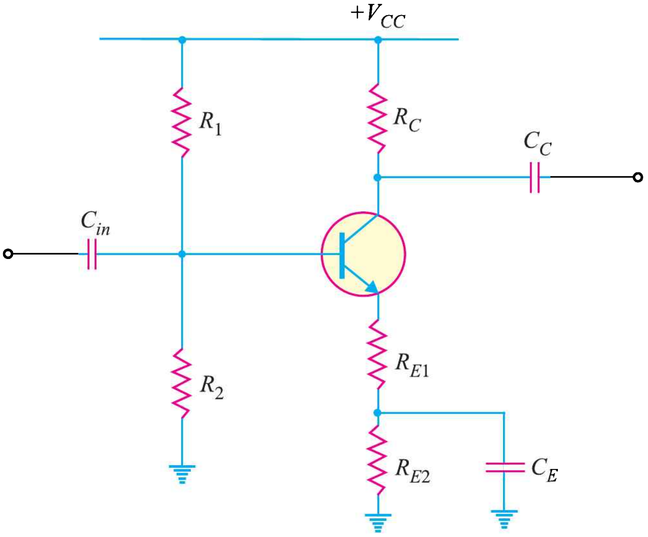


Fig. 10.37

If $R_{E1} \geq 10\ r'_e$, then the effect of r'_e is almost negligible and the voltage gain is given by ;

$$A_v \simeq \frac{R_C}{R_{E1}}$$

Therefore, the voltage gain is essentially independent of r'_e or it is reasonably stabilised.

Effect of swamping on $Z_{in\,(base)}$. The $Z_{in\,(base)}$ with R_E completely bypassed is $Z_{in\,(base)} = \beta\ r'_e$. When the emitter resistance is partially bypassed, the portion of the resistance that is unbypassed (*i.e.* R_{E1}) is seen by the a.c. signal and appears in series with r'_e. Therefore, for swamped amplifier,

$$Z_{in\,(base)} = \beta\,(r'_e + R_{E1})$$

Example 10.21. *Determine the value of voltage gain (A_v) for the swamped amplifier shown in Fig. 10.38. What will be $Z_{in\,(base)}$ for this circuit ?*

Solution. In order to find voltage gain (A_v), we first determine D.C. emitter current I_E and then a.c. emitter resistance r'_e. The value of I_E can be determined as under :

$$\text{D.C. voltage across } R_2,\ V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{10}{18 + 4.7} \times 4.7 = 2.1\text{V}$$

$$\text{D.C. voltage across } R_E,\ V_E = V_2 - V_{BE} = 2.1\text{V} - 0.7\text{V} = 1.4\text{V}$$

$$\text{D.C. emitter current, } I_E = \frac{V_E}{R_{E1} + R_{E2}} = \frac{1.4\text{V}}{300\ \Omega + 900\ \Omega} = 1.16\text{ mA}$$

$$\therefore \quad \text{a.c. emitter resistance, } r'_e = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{1.16\text{ mA}} = 21.5\Omega$$

$$\text{Voltage gain, } A_v = \frac{R_C}{r'_e + R_{E1}} = \frac{1.5\text{ k}\Omega}{21.5\Omega + 300\ \Omega} = \mathbf{4.66}$$

Input impedance of transistor base is given by ;

$$Z_{in\,(base)} = \beta\,(r_e' + R_{E1}) = 150\,(21.5\Omega + 300\Omega) = \mathbf{48.22\ k\Omega}$$

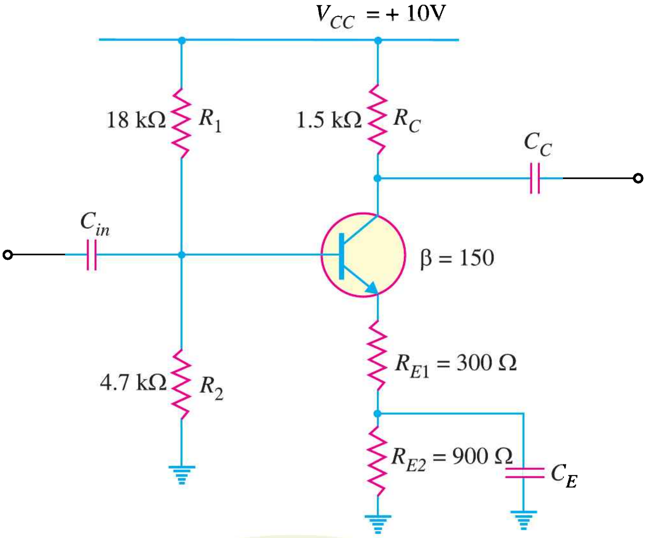


Fig. 10.38

Example 10.22. *Determine the change in voltage gain for the amplifier in example 10.21 when r_e' doubles in value.*

Solution.

$$\text{Voltage gain, } A_v = \frac{R_C}{r_e' + R_{E1}}$$

When r_e' doubles, the value of A_v becomes :

$$A_v = \frac{R_C}{2r_e' + R_{E1}} = \frac{1.5\ \text{k}\Omega}{2 \times 21.5\ \Omega + 300\ \Omega} = 4.37$$

$\therefore$ Change in gain = 4.66 – 4.37 = 0.29

Therefore, percentage change from the original value

$$= \frac{4.66 - 4.37}{4.66} \times 100 = \frac{0.29}{4.66} \times 100 = \mathbf{6.22\%}\ (\textit{decrease})$$

Consequently, the change in A_v is only 6.22% from the original value. In an amplifier that is not swamped, doubling the value of r_e' would cause the value of A_v to change (decrease) by *50%. Thus the voltage gain (A_v) of the amplifier becomes more stable by swamping the emitter circuit.

Example 10.23. *Fig. 10.39 shows the circuit of a **standard CE amplifier. The emitter circuit of this amplifier is swamped as shown in Fig. 10.40. Find :*

(i) *input impedance of transistor base [i.e. $Z_{in\,(base)}$] for each circuit.*

(ii) *input impedance (Z_{in}) for each circuit.*

---

* Original $A_v = \frac{R_C}{r_e'}$; Final $A_v = \frac{R_C}{2\,r_e'}$. Obviously, a change of 50% from the original value.

** Remember that in a standard *CE* amplifier, the emitter resistance R_E is completely bypassed by the capacitor C_E.

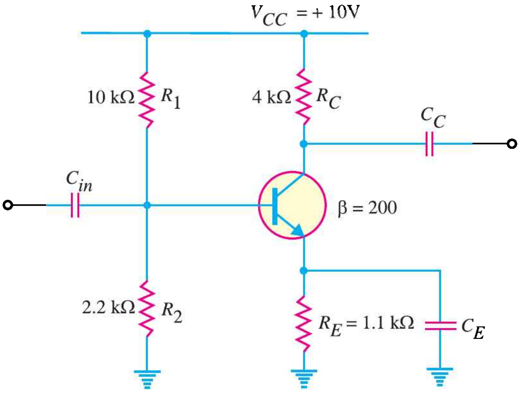


Fig. 10.39

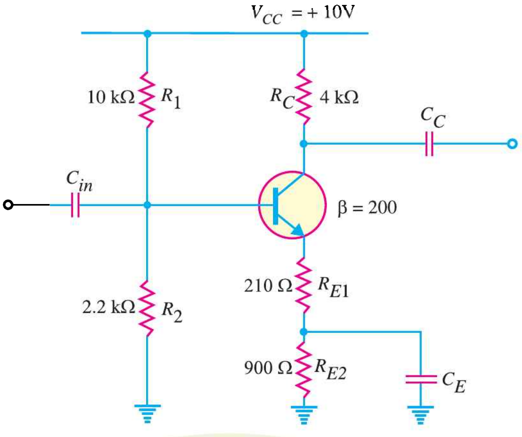


Fig. 10.40

Solution. Both the circuits have the same value of a.c. emitter resistance r'_e. Therefore, following the standard procedure for finding r'_e gives us a value of *25Ω for both circuits.

(*i*) $Z_{in\,(base)}$

For the standard *CE* amplifier shown in Fig. 10.39, we have,

$$Z_{in\,(base)} = \beta r'_e = 200 \times 25\Omega = \mathbf{5\ k\Omega}$$

For the swamped amplifier shown in Fig. 10.40, we have,

$$Z_{in\,(base)} = \beta\,(r'_e + R_{E1})$$

$$= 200\ (25\Omega + 210\ \Omega) = 47000\Omega = \mathbf{47\ k\Omega}$$

(*ii*) Z_{in}

For the standard *CE* amplifier shown in Fig. 10.39, we have,

$$Z_{in} = R_1 \parallel R_2 \parallel Z_{in\,(base)}$$

$$= 10\ \text{k}\Omega \parallel 2.2\ \text{k}\Omega \parallel 5\ \text{k}\Omega = \mathbf{1.33\ k\Omega}$$

For the swamped amplifier circuit shown in Fig. 10.40, we have,

$$Z_{in} = R_1 \parallel R_2 \parallel Z_{in\,(base)}$$

$$= 10\ \text{k}\Omega \parallel 2.2.\ \text{k}\Omega \parallel 47\ \text{k}\Omega = \mathbf{1.74\ k\Omega}$$

Note that swamping increases the input impedance (Z_{in}) of the amplifier. This reduces the amplifier's loading effects on a previous stage.

Example 10.24. *Find the voltage gain for both circuits of example 10.23.*

Solution.

For the standard *CE* amplifier shown in Fig. 10.39, the voltage gain (A_v) is given by ;

$$A_v = \frac{R_C}{r'_e} = \frac{4\ \text{k}\Omega}{25\ \Omega} = \mathbf{160}$$

For the swamped amplifier shown in Fig. 10.40, the voltage gain (A_v) is given by ;

---

* $V_2 = \dfrac{V_{CC}}{R_1 + R_2} \times R_2 = \dfrac{10}{10 + 2.2} \times 2.2 = 1.8\text{V}$; $V_E = V_2 - V_{BE} = 1.8\text{V} - 0.7\text{V} = 1.1\text{V}$

$I_E = \dfrac{V_E}{R_E} = \dfrac{1.1\text{V}}{1.1\ \text{k}\Omega} = 1\ \text{mA}$ $\quad\therefore\quad r'_e = \dfrac{25\ \text{mV}}{I_E} = \dfrac{25\ \text{mV}}{1\ \text{mA}} = 25\Omega$

$$A_v = \frac{R_C}{r'_e + R_{E1}} = \frac{4\text{ k}\Omega}{25\ \Omega + 210\ \Omega} = \frac{4\text{ k}\Omega}{235\ \Omega} = \mathbf{17}$$

The following points may be noted ;

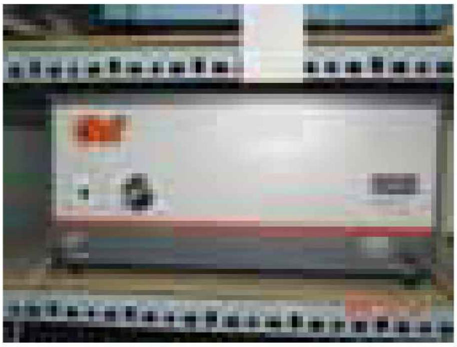
(*i*) The two circuits are identical for d.c. analysis purposes. Both have a total of 1.1. kΩ d.c. resistance in their emitter circuits.

(*ii*) For a standard *CE* amplifier, the total a.c. emitter resistance is r'_e. When this amplifier is swamped, the total a.c. emitter resistance is increased to ($r'_e + R_{E1}$).

(*iii*) Swamping reduces the voltage gain of the amplifier. However, the gain of a swamped amplifier is more stable than that of a comparable standard *CE* amplifier.

10.18 Classification Of Amplifiers

The transistor amplifiers may be classified as to their *usage, frequency capabilities, coupling methods* and *mode of operation.*



Radio amplifiers

(*i*) ***According to use.*** The classifications of amplifiers as to usage are basically *voltage amplifiers* and *power amplifiers*. The former primarily increases the voltage level of the signal whereas the latter mainly increases the power level of the signal.

(*ii*) ***According to frequency capabilities.*** According to frequency capabilities, amplifiers are classified as *audio amplifiers, radio frequency amplifiers* etc. The former are used to amplify the signals lying in the audio range *i.e.* 20 Hz to 20 kHz whereas the latter are used to amplify signals having very high frequency.

(*iii*) ***According to coupling methods.*** The output from a single stage amplifier is usually insufficient to meet the practical requirements. Additional amplification is often necessary. To do this, the output of one stage is coupled to the next stage. Depending upon the coupling device used, the amplifiers are classified as *R-C coupled amplifiers, transformer coupled amplifiers* etc.

(*iv*) ***According to mode of operation.*** The amplifiers are frequently classified according to their mode of operation as *class A, class B* and *class C* amplifiers. This classification depends on the portion of the input signal cycle during which collector current is expected to flow. Thus, class *A* amplifier is one in which collector current flows for the entire a.c. signal. Class *B* amplifier is one in which collector current flows for half-cycle of input a.c. signal. Finally, class *C* amplifier is one in which collector current flows for less than half-cycle of a.c. signal.

Example 10.25. *What do you understand by following amplifiers:*

(i) Class A voltage amplifier *(ii) Audio voltage amplifier*

(iii) Class B power amplifier *(iv) Class A transformer coupled power amplifier ?*

Solution. (*i*) Class *A* voltage amplifier means that it raises the voltage level of the signal and its mode of operation is such that collector current flows for the whole input signal.

(*ii*) Audio voltage amplifier means that it raises the voltage level of audio signal (*i.e.* one having frequency range 20 Hz to 20 kHz) and its mode of operation is class *A*.

(*iii*) It means that this amplifier raises the power level of the signal and its mode of operation is such that collector current flows for half-cycle of the signal only.

(*iv*) It means that power amplification is being done, coupling is by transformer and mode of operation is class A.

10.19 Amplifier Equivalent Circuit

An amplifier can be replaced by an equivalent circuit for the purpose of analysis. Fig. 10.41 (*i*) shows the amplifier circuit while Fig. 10.41 (*ii*) shows its equivalent circuit.

V_1 = input signal voltage to the amplifier

I_1 = input signal current

R_{in} = input resistance of the amplifier

A_0 = voltage gain of the amplifier when no load is connected

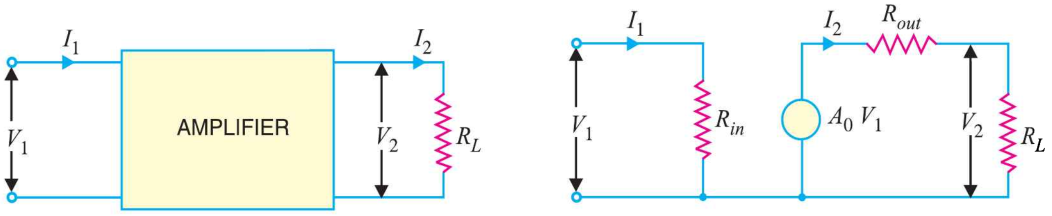
I_2 = output current

V_2 = output voltage across load R_L

R_{out} = output resistance of the amplifier

R_L = load resistance

A_v = voltage gain when load R_L is connected



(*i*) (*ii*)

Fig. 10.41

Note that capability of the amplifier to produce voltage gain is represented by the voltage generator A_0V_1. The voltage gain of the loaded amplifier is A_v. Clearly, A_v will be less than A_0 due to voltage drop in R_{out}.

10.20 Equivalent Circuit with Signal Source

If the signal source of voltage E_S and resistance R_S is considered, the amplifier equivalent circuit will be as shown in Fig. 10.42.

Referring to Fig. 10.42, we have,

$$I_1 = \frac{E_S}{R_S + R_{in}}$$

$$\therefore \quad V_1 = I_1 R_{in} = \frac{E_S R_{in}}{R_S + R_{in}}$$

$$I_2 = \frac{A_0 V_1}{R_{out} + R_L} \qquad \text{...}(i)$$

$$= \frac{A_0 I_1 R_{in}}{R_{out} + R_L} \qquad \text{...}(ii)$$

$$\therefore \quad V_2 = I_2 R_L = \frac{A_0 V_1 R_L}{R_{out} + R_L} \qquad \text{...}(iii)$$

$$\text{Voltage gain, } A_v = \frac{V_2}{V_1} = \frac{A_0 R_L}{R_{out} + R_L}$$

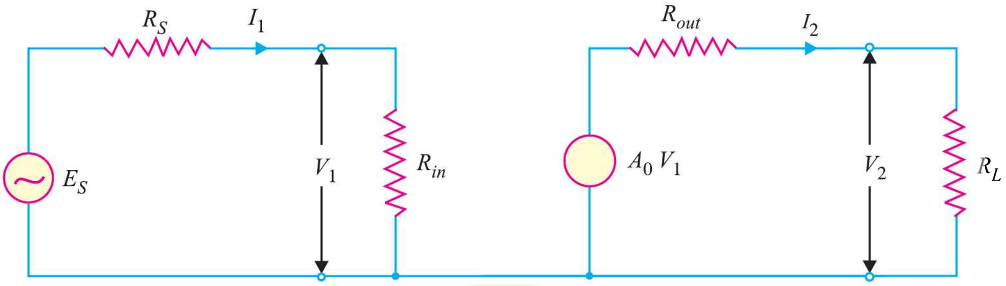


Fig. 10.42

$$\text{Current gain, } A_i = \frac{I_2}{I_1} = \frac{A_0 R_{in}}{R_{out} + R_L}$$

$$\text{Power gain, } A_p = \frac{I_2^2 R_L}{I_1^2 R_{in}} = \frac{(I_2 R_L) I_2}{(I_1 R_{in}) I_1}$$

$$= \frac{V_2 I_2}{V_1 I_1} = \left(\frac{V_2}{V_1}\right) \times \left(\frac{I_2}{I_1}\right)$$

$$= A_v \times A_i$$

Note. The use of such an equivalent circuit is restricted to the signal quantities only. Further, in drawing the equivalent circuit, it is assumed that exact linear relationship exists between input and output signals *i.e.* the amplifier produces no waveform distortion.

Example 10.26. *An amplifier has an open circuit voltage gain of 1000, an input resistance of 2 kΩ and an output resistance of 1Ω. Determine the input signal voltage required to produce an output signal current of 0.5A in 4Ω resistor connected across the output terminals.*

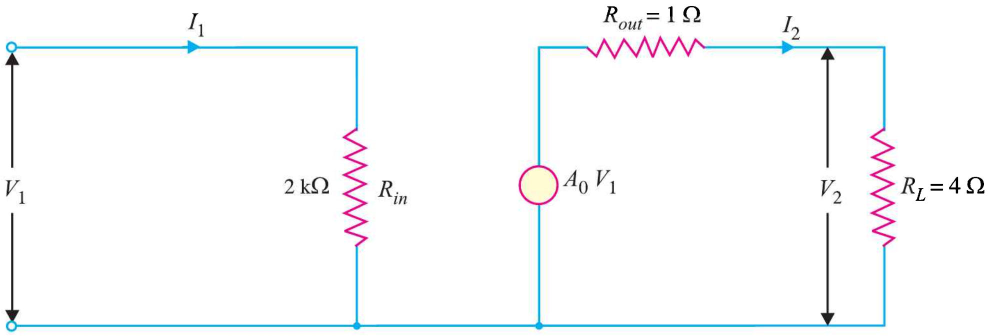


Fig. 10.43

Solution. Fig. 10.43 shows the equivalent circuit of the amplifier. Here $A_0 = 1000$.

$$\frac{I_2}{I_1} = \frac{A_0 R_{in}}{R_{out} + R_L} \qquad \text{[See Art. 10.20]}$$

$$= \frac{1000 \times 2000}{1 + 4} = 4 \times 10^5$$

$$\therefore \qquad I_1 = \frac{I_2}{4 \times 10^5} = \frac{0.5}{4 \times 10^5} = 1.25 \times 10^{-6}\ \text{A}$$

Now $$V_1 = I_1 R_{in} = (1.25 \times 10^{-6}) \times 2000 = 2.5 \times 10^{-3}\text{ V} = \mathbf{2.5\ mV}$$

Example 10.27. *An amplifier has an open circuit voltage gain of 1000, an output resistance of 15Ω and an input resistance of 7kΩ. It is supplied from a signal source of e.m.f. 10mV and internal resistance 3kΩ. The amplifier feeds a load of 35 Ω. Determine (i) the magnitude of output voltage and (ii) power gain.*

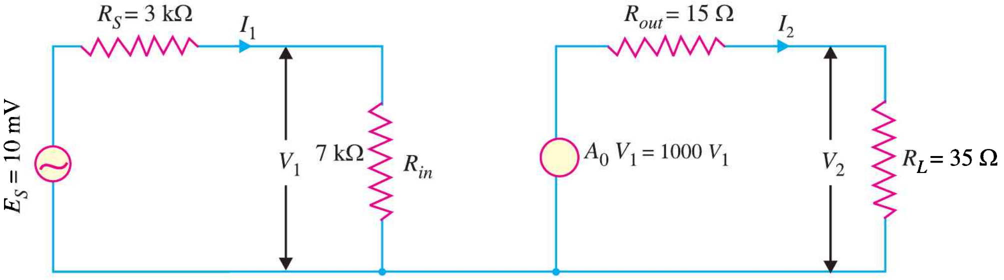


Fig. 10.44

Solution. (*i*)
$$I_1 = \frac{E_S}{R_S + R_{in}} = \frac{10 \times 10^{-3}}{3000 + 7000} = 10^{-6}\text{ A}$$
$$V_1 = I_1 R_{in} = 10^{-6} \times 7000 = 7 \times 10^{-3}\text{ V}$$
$$A_v = \frac{V_2}{V_1} = \frac{A_0 R_L}{R_{out} + R_L} = \frac{1000 \times 35}{15 + 35} = 700$$
$$\therefore \quad V_2 = 700\, V_1 = 700 \times 7 \times 10^{-3} = \mathbf{4.9\ V}$$

(*ii*) Output power,
$$P_2 = \frac{V_2^2}{R_L} = \frac{(4.9)^2}{35} = 0.686\text{ W}$$

Input power,
$$P_1 = \frac{V_1^2}{R_{in}} = \frac{(7 \times 10^{-3})^2}{7000} = 7 \times 10^{-9}\text{ W}$$

∴ Power gain,
$$A_p = \frac{P_2}{P_1} = \frac{0.686}{7 \times 10^{-9}} = \mathbf{98 \times 10^6}$$

Example 10.28. *An amplifier, when loaded by 2 kΩ resistor, has a voltage gain of 80 and a current gain of 120. Determine the necessary signal voltage and current to give an output voltage of 1V. What is the power gain of the amplifier ?*

Solution.
$$A_v = \frac{V_2}{V_1} = 80$$
$$\therefore \quad V_1 = V_2/80 = 1/80 = 0.0125\text{ V} = \mathbf{12.5\ mV}$$
$$A_v = \frac{A_0 R_L}{R_{out} + R_L} \qquad \text{...[See Art. 10.20]}$$
$$A_i = \frac{A_0 R_{in}}{R_{out} + R_L} \qquad \text{...[See Art. 10.20]}$$
$$\therefore \quad \frac{A_v}{A_i} = \frac{R_L}{R_{in}}$$
or
$$\frac{80}{120} = \frac{2}{R_{in}}$$
$$\therefore \quad R_{in} = 120 \times 2/80 = 3\text{ k}\Omega$$

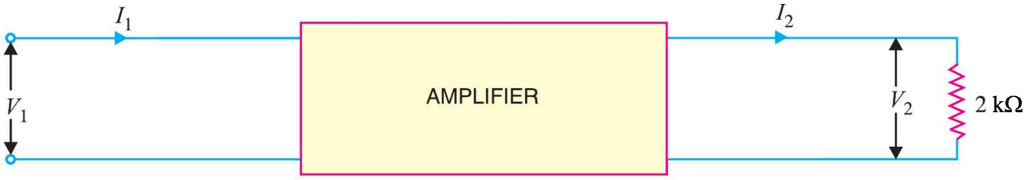


Fig. 10.45

$$I_1 = V_1/R_{in} = 12.5\text{ mV}/3\text{ k}\Omega = \mathbf{4.17\ \mu A}$$

$$\text{Power gain} = A_v \times A_i = 80 \times 120 = \mathbf{9600}$$

10.21 Gain and Transistor Configurations

We know that the process of raising the strength of an a.c. signal is called amplification and the circuit used to preform this function is called an amplifier. There are three types of gain : *current gain, voltage gain* and *power gain*.

(*i*) The *common emitter (CE) amplifier* exhibits all there types gain . From input to output, current will increase, voltage will increase and power will increase.

(*ii*) The *common base (CB) amplifier* has voltage gain and power gain but no current gain. Note that the current gain of a *CB* circuit is less than 1.

(*iii*) The *common collector (CC) amplifier* has current gain and power gain but no voltage gain.

It is important to note that the type of gain an amplifier has depends upon the transistor configuration. Consequently, the choice of an amplifier for a given application often depends on the type of gain that is desired. Since *CE* arrangement is widely used (in about 90% applications), we shall be mainly concentrating on this type of circuit.

MULTIPLE-CHOICE QUESTIONS

1. A single stage transistor amplifier contains .... and associated circuitry.
(*i*) two transistors (*ii*) one transistor
(*iii*) three transistors
(*iv*) none of the above

2. The phase difference between the output and input voltages of a *CE* amplifier is ....
(*i*) 180° (*ii*) 0°
(*iii*) 90° (*iv*) 270°

3. It is generally desired that a transistor should have .... input impedance.
(*i*) low (*ii*) very low
(*iii*) high (*iv*) very high

4. When an a.c. signal is applied to an amplifier, the operating point moves along ....
(*i*) d.c. load line (*ii*) a.c. load line
(*iii*) both d.c. and a.c. load lines
(*iv*) none of the above

5. If the collector supply is 10 V, then collector cut off voltage under d.c. conditions is ....
(*i*) 20 V (*ii*) 5 V
(*iii*) 2 V (*iv*) 10 V

6. In the zero signal conditions, a transistor sees .... load.
(*i*) d.c. (*ii*) a.c.
(*iii*) both d.c. and a.c
(*iv*) none of the above

7. The input capacitor in an amplifier is the .... capacitor.
(*i*) coupling (*ii*) bypass
(*iii*) leakage (*iv*) none of the above

8. The point of intersection of d.c. and a.c. load lines is called ....
(*i*) saturation point (*ii*) cut off point
(*iii*) operating point (*iv*) none of the above

9. The slope of a.c. load line is .... that of d.c. load line.
(*i*) the same as (*ii*) more than
(*iii*) less than (*iv*) none of the above

10. If a transistor amplifier draws 2 mA when input voltage is 10 V, then its input impedance is ....

(*i*) 20 kΩ (*ii*) 0.2 kΩ
(*iii*) 10 kΩ (*iv*) 5 kΩ

11. When a transistor amplifier is operating, the current in any branch is ....

(*i*) sum of a.c. and d.c.
(*ii*) a.c. only (*iii*) d.c. only
(*iv*) difference of a.c. and d.c.

12. The purpose of capacitors in a transistor amplifier is to ....

(*i*) protect the transistor
(*ii*) cool the transistor
(*iii*) couple or bypass a.c. component
(*iv*) provide biasing

13. In the d.c. equivalent circuit of a transistor amplifier, the capacitors are considered ....

(*i*) short (*ii*) open
(*iii*) partially short (*iv*) none of the above

14. In a *CE* amplifier, voltage gain = ... × $\frac{R_{AC}}{R_{in}}$

(*i*) α (*ii*) (1 + α)
(*iii*) (1 + β) (*iv*) β

15. In practice, the voltage gain of an amplifier is expressed ....

(*i*) as volts (*ii*) as a number
(*iii*) in *db* (*iv*) none of the above

16. If the power and current gains of a transistor amplifier are 16500 and 100 respectively, then voltage gain is ....

(*i*) 165 (*ii*) 165×10^4
(*iii*) 100 (*iv*) none of the above

17. If R_C and R_L represent the collector resistance and load resistance respectively in a single stage transistor amplifier, then a.c. load is ....

(*i*) $R_L + R_C$ (*ii*) $R_C \| R_L$
(*iii*) $R_L - R_C$ (*iv*) R_C

18. In a *CE* amplifier, the phase difference between voltage across collector load R_C and signal voltage is ....

(*i*) 180° (*ii*) 270°
(*iii*) 90° (*iv*) 0°

19. In the a.c. equivalent circuit of a transistor amplifier, the capacitors are considered ....

(*i*) short (*ii*) open
(*iii*) partially open (*iv*) none of the above

20. In a single stage transistor amplifier, R_C and R_L represent collector resistance and load resistance respectively. The transistor sees a d.c. load of ....

(*i*) $R_C + R_L$ (*ii*) $R_C \| R_L$
(*iii*) R_L (*iv*) R_C

21. The purpose of d.c. conditions in a transistor is to ....

(*i*) reverse bias the emitter
(*ii*) forward bias the collector
(*iii*) set up operating point
(*iv*) none of the above

22. An amplifier has a power gain of 100. Its *db* gain is........

(*i*) 10 *db* (*ii*) 20 *db*
(*iii*) 40 *db* (*iv*) none of the above

23. In order to get more voltage gain from a transistor amplifier, the transistor used should have ....

(*i*) thin base (*ii*) thin collector
(*iii*) wide emitter (*iv*) none of the above

24. The purpose of a coupling capacitor in a transistor amplifier is to ....

(*i*) increase the output impedance of transistor
(*ii*) protect the transistor
(*iii*) pass a.c. and block d.c.
(*iv*) provide biasing

25. The purpose of emitter capacitor (*i.e.* capacitor across R_E) is to ....

(*i*) avoid voltage gain drop
(*ii*) forward bias the emitter
(*iii*) reduce noise in the amplifier
(*iv*) none of the above

26. The ratio of output to input impedance of a *CE* amplifier is ....

(*i*) about 1 (*ii*) low
(*iii*) high (*iv*) moderate

27. If a transistor amplifier feeds a load of low resistance (*e.g.* speaker), then voltage gain will be ....

(*i*) high (*ii*) very high
(*iii*) moderate (*iv*) low

28. If the input capacitor of a transistor amplifier is short-circuited, then ....

(*i*) transistor will be destroyed
(*ii*) biasing conditions will change

(*iii*) signal will not reach the base
(*iv*) none of the above

29. The radio wave picked up by the receiving antenna is amplified about .... times to have reasonable sound output.
(*i*) 1000 (*ii*) a million
(*iii*) 100 (*iv*) 10000

30. A *CE* amplifier is also called .... circuit.
(*i*) grounded emitter
(*ii*) grounded base
(*iii*) grounded collector
(*iv*) none of the above

31. The d.c. load of a transistor amplifier is generally .... that of a.c. load.
(*i*) the same as (*ii*) less than
(*iii*) more than (*iv*) none of the above

32. The value of collector load R_C in a transistor amplifier is .... the output impedance of the transistor.
(*i*) the same as (*ii*) less than
(*iii*) more than (*iv*) none of the above

33. A single stage transistor amplifier with collector load R_C and emitter resistance R_E has a d.c. load of ....
(*i*) R_C (*ii*) $R_C \parallel R_E$
(*iii*) $R_C - R_E$ (*iv*) $R_C + R_E$

34. In transistor amplifiers, we generally use .... capacitors.
(*i*) electrolytic (*ii*) mica
(*iii*) paper (*iv*) air

35. A single stage transistor amplifier with no load sees an a.c. load of ....
(*i*) $R_C + R_E$ (*ii*) R_C
(*iii*) $R_C \parallel R_E$ (*iv*) R_C / R_E

36. The output power of a transistor amplifier is more than the input power because the additional power is supplied by ....
(*i*) transistor (*ii*) biasing circuit
(*iii*) collector supply V_{CC}
(*iv*) none of the above

37. A transistor converts ....
(*i*) d.c. power into a.c. power
(*ii*) a.c. power into d.c. power
(*iii*) high resistance into low resistance
(*iv*) none of the above

38. A transistor amplifier has high output impedance because ....
(*i*) emitter is heavily doped
(*ii*) collector has reverse bias
(*iii*) collector is wider than emitter or base
(*iv*) none of the above

39. For highest power gain, one would use .... configuration.
(*i*) *CC* (*ii*) *CB*
(*iii*) *CE* (*iv*) none of the above

40. *CC* configuration is used for impedance matching because its ....
(*i*) input impedance is very high
(*ii*) input impedance is low
(*iii*) output impedance is very low
(*iv*) none of the above

Answers to Multiple-Choice Questions

1.	(*ii*)	**2.**	(*i*)	**3.**	(*iii*)	**4.**	(*ii*)	**5.**	(*iv*)
6.	(*i*)	**7.**	(*i*)	**8.**	(*iii*)	**9.**	(*ii*)	**10.**	(*iv*)
11.	(*i*)	**12.**	(*iii*)	**13.**	(*ii*)	**14.**	(*iv*)	**15.**	(*iii*)
16.	(*i*)	**17.**	(*ii*)	**18.**	(*iv*)	**19.**	(*i*)	**20.**	(*iv*)
21.	(*iii*)	**22.**	(*ii*)	**23.**	(*i*)	**24.**	(*iii*)	**25.**	(*i*)
26.	(*iv*)	**27.**	(*iv*)	**28.**	(*ii*)	**29.**	(*ii*)	**30.**	(*i*)
31.	(*iii*)	**32.**	(*ii*)	**33.**	(*iv*)	**34.**	(*i*)	**35.**	(*ii*)
36.	(*iii*)	**37.**	(*i*)	**38.**	(*ii*)	**39.**	(*iii*)	**40.**	(*i*)

Chapter Review Topics

1. What do you understand by single stage transistor amplifiers ?
2. Explain with the help of output characteristics how the variations in base current affect collector current variations. Assume the base current varies sinusoidally.

3. Draw the circuit of a practical single stage transistor amplifier. Explain the function of each component.
4. Show the various currents and voltages in a single stage transistor amplifier.
5. Show that the output voltage of a single stage common emitter transistor amplifier is 180° out of phase with the input voltage.
6. What do you understand by d.c. and a.c. load lines ? How will you construct them on the output characteristics ?
7. Draw the d.c. and a.c. equivalent circuits of a transistor amplifier.
8. Derive an expression for the voltage gain of a transistor amplifier from its a.c. equivalent circuit.
9. Write short notes on the following :

   (*i*) phase reversal   (*ii*) d.c. and a.c. load lines

   (*iii*) operating point   (*iv*) classification of amplifiers.

Problems

1. In transistor amplifier, the collector current swings from 2 mA to 5 mA as the base current is changed from 5 μA to 15 μA. Find the current gain. **[300]**
2. A transistor amplifier employs a 4 kΩ as collector load. If the input resistance is 1 kΩ, determine the voltage gain. Given $\beta = 100$, g_m =10 mA/volt and signal voltage = 50 mV. **[1.04]**
3. Fig. 10.46 shows the transistor amplifier. If $R_C = 4$ kΩ, $R_E = 5$ kΩ and $V_{CC} = 30$ V, draw the d.c. load line.

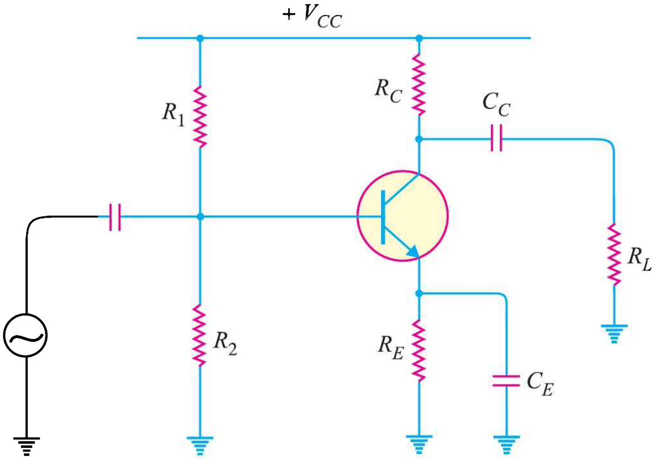
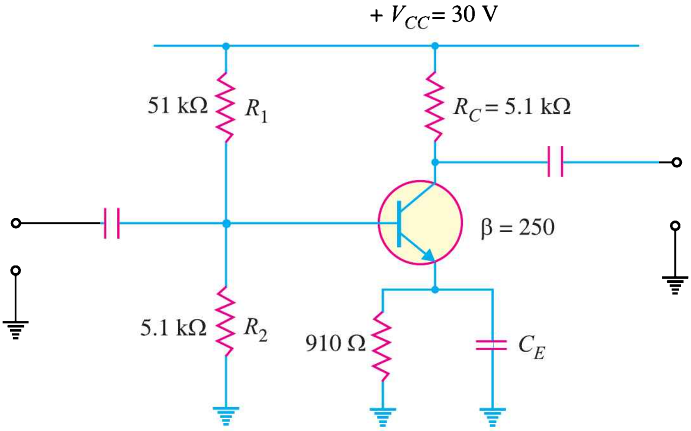


Fig. 10.46

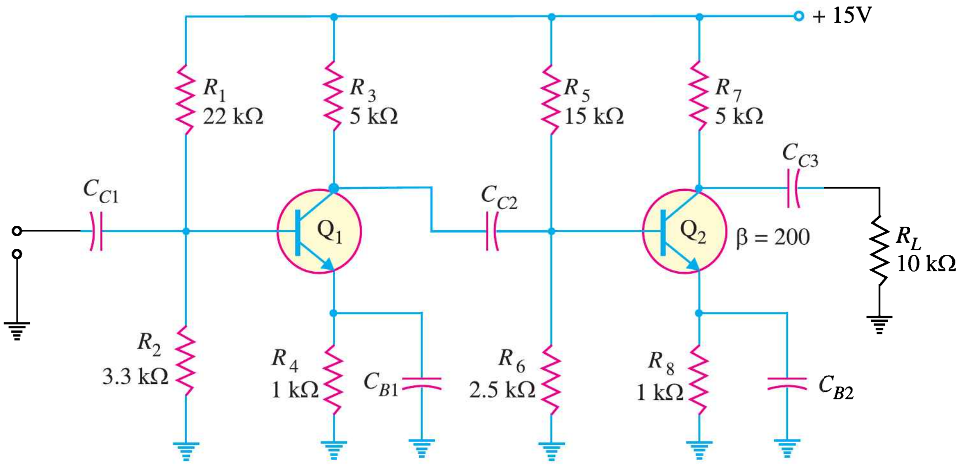
4. Find the operating point for Fig. 10.46, $V_{CC} = 30$ V, $R_1 = 20$ kΩ, $R_2 = 20$ kΩ, $R_C = 4$ kΩ, $R_E = 5$ kΩ. **[13.2V, 1.85mA]**
5. For the circuit shown in Fig. 10.46, find the voltage gain if $\beta = 100$, $R_C = 3$ kΩ, $R_L = 6$ kΩ and R_{in} = 2 kΩ. **[100]**
6. In the circuit shown in Fig. 10.46, $V_{CC} = 30$ V, $R_1 = 2$ kΩ, $R_2 = 1$ kΩ, $R_C = 2$ kΩ, $R_L = 2$ kΩ, $R_E = 1$ kΩ. Draw the d.c. and a.c. load lines.
7. A voltage-divider biased circuit has an emitter voltage of 2 V and an emitter resistor of 4.7 kΩ. What is the ac resistance of emitter diode ? **[58.7 Ω]**
8. A transistor amplifier has a dc collector current of 5 mA. What is the ac resistance of the base if β = 200 ? **[1000 Ω]**
9. Determine the voltage gain for the amplifier circuit shown in Fig. 10.47.



+ V_{CC} = 30 V
51 kΩ
R_1
R_C = 5.1 kΩ
β = 250
5.1 kΩ
R_2
910 Ω
C_E

Fig. 10.47

10. What is the input impedance of the amplifier circuit shown in Fig. 10.47 ? **[1.75 kΩ]**
11. A voltage-divider biased amplifier has the values of R_1 = 40 kΩ, R_2 = 10 kΩ, R_C = 6 kΩ ; R_E = 2 kΩ, V_{CC} = +10V and β = 80. Determine the a.c. emitter resistance of the transistor. **[38.46Ω]**
12. A standard *CE* amplifier has the following values : V_{CC} = 30V, R_1 = 51 kΩ, R_2 = 5.1 kΩ, R_C = 5.1 kΩ, R_E = 910Ω and β = 250. Determine the voltage gain of the amplifier. **[455.4]**
13. A *CE* amplifier has a voltage gain A_v = 59.1 and β = 200. Determine the power gain and output power of the amplifier when input power is 80 μW.. **[11820 ; 945.6 mW]**
14. Determine the voltage gain for the first stage in Fig. 10.48. **[53.03]**
15. If the value of β for the second stage in Fig. 10.48 is increased to 280, determine the voltage gain of the first amplifier stage. **[58.08]**



+ 15V
R_1
22 kΩ
R_3
5 kΩ
R_5
15 kΩ
R_7
5 kΩ
C_{C3}
C_{C1}
C_{C2}
Q_1
Q_2
β = 200
R_L
10 kΩ
R_2
3.3 kΩ
R_4
1 kΩ
C_{B1}
R_6
2.5 kΩ
R_8
1 kΩ
C_{B2}

Fig. 10.48

Discussion Questions

1. Does phase reversal affect amplification ?
2. Why does ac load differ from dc load ?
3. What is the importance of load line analysis ?
4. Why is ac load line steeper than dc load line?
5. What is the significance of operating point ?

11

Multistage Transistor Amplifiers

11.1 Multistage Transistor Amplifier
11.2 Role of Capacitors in Transistor Amplifiers
11.3 Important Terms
11.4 Properties of dB Gain
11.5 RC Coupled Transistor Amplifier
11.6 Transformer-Coupled Amplifier
11.7 Direct-Coupled Amplifier
11.8 Comparison of Different Types of Coupling
11.9 Difference Between Transistor And Tube Amplifiers

INTRODUCTION

The output from a single stage amplifier is usually insufficient to drive an output device. Inther words, the gain of a single amplifier is inadequate for practical purposes. Conse quently, additional amplification over two or three stages is necessary. To achieve this, the output of each amplifier stage is *coupled* in some way to the input of the next stage. The resulting system is referred to as multistage amplifier. It may be emphasised here that a practical amplifier is always a multistage amplifier. For example, in a transistor radio receiver, the number of amplification stages may be six or more. In this chapter, we shall focus our attention on the various multistage transistor amplifiers and their practical applications.

11.1 Multistage Transistor Amplifier

A transistor circuit containing more than one stage of amplification is known as **multistage transistor amplifier.**

In a multistage amplifier, a number of single amplifiers are connected in ***cascade arrangement* *i.e.* output of first stage is connected to the input of the second stage through a suitable *coupling device* and so on. The purpose of coupling device (*e.g.* a capacitor, transformer etc.) is (*i*) to transfer a.c. output of one stage to the input of the next stage and (*ii*) to isolate the d.c. conditions of one stage from the next stage. Fig. 11.1 shows the block diagram of a 3-stage amplifier. Each stage consists of one transistor and associated circuitry and is coupled to the next stage through a coupling device. The name of the amplifier is usually given after the type of coupling used. *e.g.*

Name of coupling	*Name of multistage amplifier*
RC coupling	R-C coupled amplifier
Transformer coupling	Transformer coupled amplifier
Direct coupling	Direct coupled amplifier

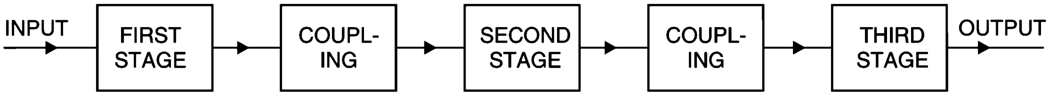


Fig. 11.1

(*i*) In *RC* coupling, a capacitor is used as the coupling device. The capacitor connects the output of one stage to the input of the next stage in order to pass the a.c. signal on while blocking the d.c. bias voltages.

(*ii*) In transformer coupling, transformer is used as the coupling device. The transformer coupling provides the same two functions (*viz.* to pass the signal on and blocking d.c.) but permits in addition impedance matching.

(*iii*) In direct coupling or d.c. coupling, the individual amplifier stage bias conditions are so designed that the two stages may be directly connected without the necessity for d.c. isolation.

11.2 Role of Capacitors in Transistor Amplifiers

Regardless of the manner in which a capacitor is connected in a transistor amplifier, its behaviour towards d.c. and a.c. is as follows. *A capacitor blocks d.c. i.e. a capacitor behaves as an "open**" to d.c.* Therefore, for d.c. analysis, we can remove the capacitors from the transistor amplifier circuit. A capacitor offers reactance (= $1/2\pi fC$) to a.c. depending upon the values of f and C. In practical transistor circuits, the size of capacitors is so selected that they offer negligible (ideally zero) reactance to the range of frequencies handled by the circuits. Therefore, *for a.c. analysis, we can replace the capacitors by a short i.e. by a wire.* The capacitors serve the following two roles in transistor amplifiers :

1. As coupling capacitors
2. As bypass capacitors

1. As coupling capacitors. In most applications, you will not see a single transistor amplifier. Rather we use a multistage amplifier *i.e.* a number of transistor amplifiers are connected in series or cascaded. The capacitors are commonly used to connect one amplifier stage to another. When a capacitor is used for this purpose, it is called a *coupling capacitor.* Fig. 11.2 shows the coupling capacitors (C_{C1}; C_{C2} ; C_{C3} and C_{C4}) in a multistage amplifier. A coupling capacitor performs the following two functions :

(*i*) It blocks d.c. *i.e.* it provides d.c. isolation between the two stages of a multistage amplifier.

---

* The term *cascaded* means *connected in series.*

** $X_C = \dfrac{1}{2\pi fC}$. For d.c., $f = 0$ so that $X_C \rightarrow \infty$. Therefore, a capacitor behaves as an open to d.c.

(*ii*) It passes the a.c. signal from one stage to the next with little or no distortion.

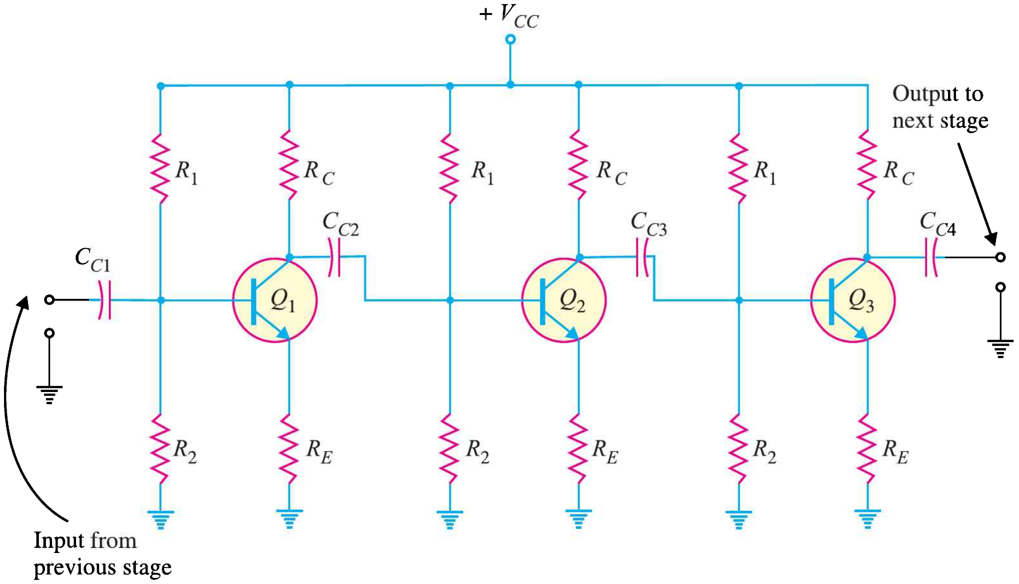


Fig. 11.2

2. As bypass capacitors. Like a coupling capacitor, a bypass capacitor also blocks d.c. and behaves as a short or wire (due to proper selection of capacitor size) to an a.c. signal. But it is used for a different purpose. A bypass capacitor is connected in parallel with a circuit component (*e.g.* resistor) to bypass the a.c. signal and hence the name. Fig. 11.3 shows a bypass capacitor C_E connected across the emitter resistance R_E. Since C_E behaves as a short to the a.c. signal, the whole of a.c. signal (i_e) passes through it. Note that C_E keeps the emitter at a.c. ground. Thus for a.c. purposes, R_E does not exist. We have already seen in the previous chapter that C_E plays an important role in determining the voltage gain of the amplifier circuit. If C_E is removed, the voltage gain of the amplifier is greatly reduced. Note that C_{in} is the coupling capacitor in this circuit.

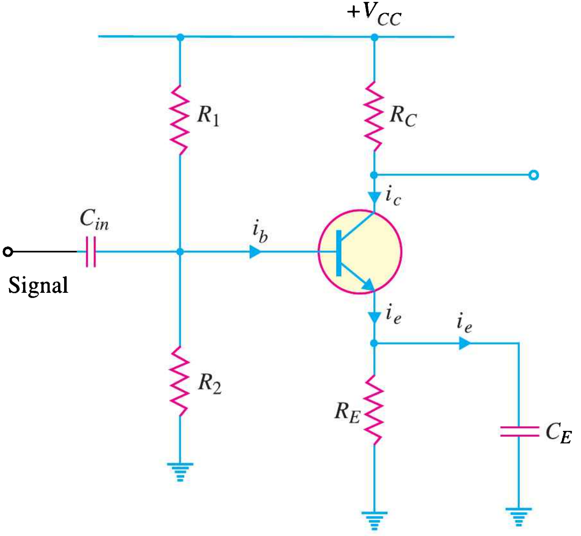


Fig. 11.3

11.3 Important Terms

In the study of multistage amplifiers, we shall frequently come across the terms *gain*, *frequency response*, *decibel gain* and *bandwidth*. These terms stand discussed below :

(*i*) **Gain.** *The ratio of the output *electrical quantity to the input one of the amplifier is called its* **gain.**

---

* Accordingly, it can be current gain or voltage gain or power gain.

The gain of a multistage amplifier is equal to the product of gains of individual stages. For instance, if G_1, G_2 and G_3 are the individual voltage gains of a three-stage amplifier, then total voltage gain G is given by :

$$*G = G_1 \times G_2 \times G_3$$

It is worthwhile to mention here that in practice, total gain G is less than $G_1 \times G_2 \times G_3$ due to the loading effect of next stages.

(*ii*) **Frequency response.** The voltage gain of an amplifier varies with signal frequency. It is because reactance of the capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve between voltage gain and signal frequency of an amplifier is known as *frequency response*. Fig. 11.4 shows the frequency response of a typical amplifier. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at f_r, called *resonant frequency*. If the frequency of signal increases beyond f_r, the gain decreases.

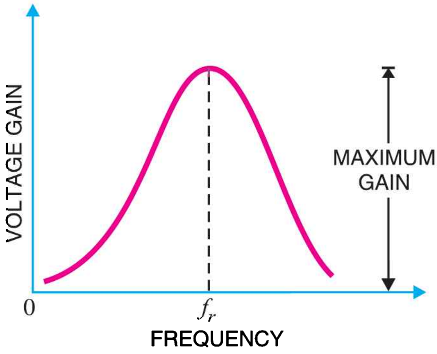


Fig. 11.4

The performance of an amplifier depends to a considerable extent upon its frequency response. While designing an amplifier, appropriate steps must be taken to ensure that gain is essentially uniform over some specified frequency range. For instance, in case of an audio amplifier, which is used to amplify speech or music, it is necessary that all the frequencies in the sound spectrum (*i.e.* 20 Hz to 20 kHz) should be uniformly amplified otherwise speaker will give a distorted sound output.

(*iii*) **Decibel gain.** Although the gain of an amplifier can be expressed as a number, yet it is of great practical importance to assign it a unit. The unit assigned is *bel or decibel* (*db*).

The common logarithm (*log to the base 10*) *of power gain is known as* **bel power gain** *i.e.*

$$\text{Power gain} = \log_{10} \frac{P_{out}}{P_{in}} \; bel$$

$$1 \text{ bel} = 10 \; db$$

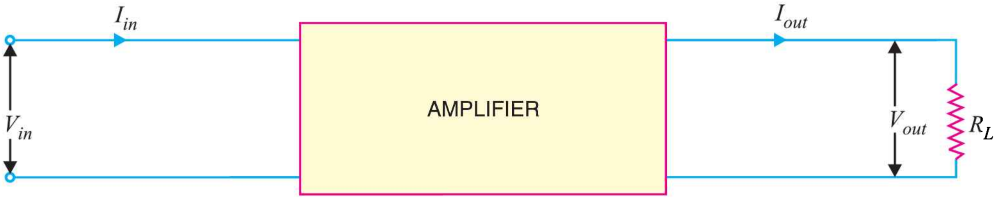


Fig. 11.5

---

* This can be easily proved. Supporse the input to first stage is V.

$$\text{Output of first stage} = G_1 V$$

$$\text{Output of second stage} = (G_1 V)\, G_2 = G_1 G_2 V$$

$$\text{Output of third stage} = (G_1 G_2 V) G_3 = G_1 G_2 G_3 V$$

$$\text{Total gain, } G = \frac{\text{Output of third stage}}{\text{V}}$$

or

$$G = \frac{G_1\, G_2\, G_3\, V}{V} = G_1 \times G_2 \times G_3$$

$$\therefore \quad \text{Power gain} = 10 \log_{10} \frac{P_{out}}{P_{in}} \, db$$

If the two powers are developed in the same resistance or equal resistances, then,

$$P_1 = \frac{V_{in}^2}{R} = I_{in}^2 R$$

$$P_2 = \frac{V_{out}^2}{R} = I_{out}^2 R$$

$$\therefore \quad \text{Voltage gain in } db = 10 \log_{10} \frac{V_{out}^2 / R}{V_{in}^2 / R} = 20 \log_{10} \frac{V_{out}}{V_{in}}$$

$$\text{Current gain in } db = 10 \log_{10} \frac{I_{out}^2 R}{I_{in}^2 R} = 20 \log_{10} \frac{I_{out}}{I_{in}}$$

Advantages. The following are the advantages of expressing the gain in *db* :

(*a*) The unit *db* is a logarithmic unit. Our ear response is also logarithmic *i.e.* loudness of sound heard by ear is not according to the intensity of sound but according to the log of intensity of sound. Thus if the intensity of sound given by speaker (*i.e.* power) is increased 100 times, our ears hear a doubling effect ($\log_{10} 100 = 2$) *i.e.* as if loudness were doubled instead of made 100 times. Hence, this unit tallies with the natural response of our ears.

(*b*) When the gains are expressed in *db*, the overall gain of a multistage amplifier is the sum of gains of individual stages in *db*. Thus referring to Fig. 11.6,

$$\text{Gain as number} = \frac{V_2}{V_1} \times \frac{V_3}{V_2}$$

$$\begin{aligned} \text{Gain in } db &= 20 \log_{10} \frac{V_2}{V_1} \times \frac{V_3}{V_2} \\ &= 20 \log_{10} \frac{V_2}{V_1} + 20 \log_{10} \frac{V_3}{V_2} \\ &= \text{1st stage gain in } db + \text{2nd stage gain in } db \end{aligned}$$

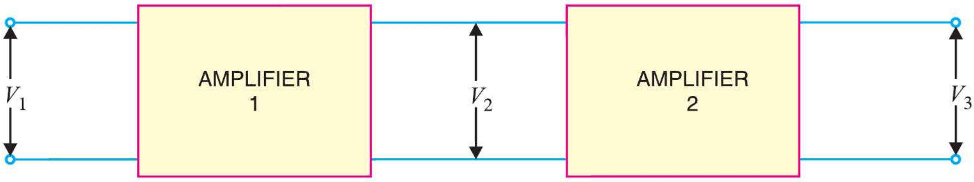


Fig. 11.6

However, absolute gain is obtained by multiplying the gains of individual stages. Obviously, it is easier to add than to multiply.

(*iv*) Bandwidth. *The range of frequency over which the voltage gain is equal to or greater than *70.7% of the maximum gain is known as* **bandwidth.**

---

* The human ear is not a very sensitive hearing device. It has been found that if the gain falls to 70.7% of maximum gain, the ear cannot detect the change. For instance, if the gain of an amplifier is 100, then even if the gain falls to 70.7, the ear cannot detect the change in intensity of sound and hence no distortion will be heard. However, if the gain falls below 70.7, the ear will hear clear distortion.

The voltage gain of an amplifier changes with frequency. Referring to the frequency response in Fig. 11.7, it is clear that for any frequency lying between f_1 and f_2, the gain is equal to or greater than 70.7% of the maximum gain. Therefore, $f_1 - f_2$ is the bandwidth. It may be seen that f_1 and f_2 are the limiting frequencies. The former (f_1) is called *lower cut-off frequency* and the latter (f_2) is known as *upper cut-off frequency*. For distortionless amplification, it is important that signal frequency range must be within the bandwidth of the amplifier.

40 decibels phone

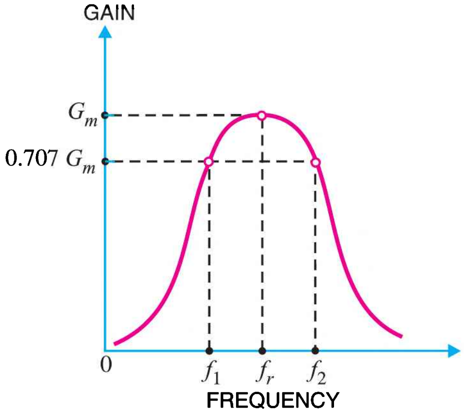


Fig. 11.7

The bandwidth of an amplifier can also be defined in terms of *db*. Suppose the maximum voltage gain of an amplifier is 100. Then 70.7% of it is 70.7.

∴ Fall in voltage gain from maximum gain

$$= 20 \log_{10} 100 - 20 \log_{10} 70.7$$

$$= 20 \log_{10} \frac{100}{70.7}\ db$$

$$= 20 \log_{10} 1.4142\ db = 3\ db$$

Hence **bandwidth** *of an amplifier is the range of frequency at the limits of which its voltage gain falls by 3 db from the maximum gain.*

The frequency f_1 or f_2 is also called *3-db frequency* or *half-power frequency*.

The 3-*db* designation comes from the fact that voltage gain at these frequencies is 3*db* below the maximum value. The term half-power is used because when voltage is down to 0.707 of its maximum value, the power (proportional to V^2) is down to $(0.707)^2$ or one-half of its maximum value.

Example 11.1. *Find the gain in db in the following cases :*

(i) Voltage gain of 30 *(ii) Power gain of 100*

Solution.

(*i*) Voltage gain $= 20 \log_{10} 30\ db$ = **29.54 db**

(*ii*) Power gain $= 10 \log_{10} 100\ db$ = **20 db**

Example 11.2. *Express the following gains as a number :*

(i) Power gain of 40 db *(ii) Power gain of 43 db*

Solution.

(*i*) Power gain = 40 *db* = 4 *bel*

If we want to find the gain as a number, we should work from logarithm back to the original number.

$\therefore$ Gain = Antilog 4 = 10^4 = **10,000**

(*ii*) Power gain = 43 *db* = 4.3 *bel*

$\therefore$ Power gain = Antilog 4.3 = 2×10^4 = **20,000**

Alternatively. $10 \log_{10} \frac{P_2}{P_1} = 43\ db$

or $\log_{10} \frac{P_2}{P_1} = 43/10 = 4.3$

$\therefore$ $\frac{P_2}{P_1} = (10)^{4.3} = \mathbf{20{,}000}$

In general, we have,

$$\frac{V_2}{V_1} = (10)^{gain\ in\ db/20}$$

$$\frac{P_2}{P_1} = (10)^{gain\ in\ db/10}$$

Example 11.3. *A three-stage amplifier has a first stage voltage gain of 100, second stage voltage gain of 200 and third stage voltage gain of 400. Find the total voltage gain in db .*

Solution.

First-stage voltage gain in *db* = $20 \log_{10} 100 = 20 \times 2 = 40$

Second-stage voltage gain in *db* = $20 \log_{10} 200 = 20 \times 2.3 = 46$

Third-stage voltage gain in *db* = $20 \log_{10} 400 = 20 \times 2.6 = 52$

$\therefore$ Total voltage gain = 40 + 46 + 52 = **138 db**

Example 11.4. (*i*) *A multistage amplifier employs five stages each of which has a power gain of 30. What is the total gain of the amplifier in db ?*

(*ii*) *If a negative feedback of 10 db is employed, find the resultant gain.*

Solution. Absolute gain of each stage = 30

No. of stages = 5

(*i*) Power gain of one stage in *db* = $10 \log_{10} 30 = 14.77$

$\therefore$ Total power gain = 5×14.77 = **73.85 db**

(*ii*) Resultant power gain with negative feedback

= 73.85 − 10 = **63.85 db**

It is clear from the above example that by expressing the gain in *db*, calculations have become very simple.

Example 11.5. *In an amplifier, the output power is 1.5 watts at 2 kHz and 0.3 watt at 20 Hz, while the input power is constant at 10 mW. Calculate by how many decibels gain at 20 Hz is below that at 2 kHz ?*

Solution.

db power gain at 2 kHz. At 2 kHz, the output power is 1.5 W and input power is 10 mW.

$\therefore$ Power gain in *db* = $10 \log_{10} \frac{1.5\text{ W}}{10\text{ mW}} = 21.76$

db power gain at 20 Hz. At 20Hz, the output power is 0.3 W and input power is 10 mW.

$\therefore$ Power gain in *db* = $10 \log_{10} \frac{0.3\text{ W}}{10\text{ mW}} = 14.77$

Fall in gain from 2 kHz to 20 Hz = 21.76 − 14.77 = **6.99 db**

Example 11.6. *A certain amplifier has voltage gain of 15 db. If the input signal voltage is 0.8V, what is the output voltage ?*

Solution.

$$
\begin{aligned}
& db \text{ voltage gain} &&= 20 \log_{10} V_2/V_1\\
\text{or} \quad & 15 &&= 20 \log_{10} V_2/V_1\\
\text{or} \quad & 15/20 &&= \log_{10} V_2/V_1\\
\text{or} \quad & 0.75 &&= \log_{10} V_2/0.8
\end{aligned}
$$

Taking antilogs, we get,

$$
\begin{aligned}
& \text{Antilog } 0.75 &&= \text{Antilog } (\log_{10} V_2/0.8)\\
\text{or} \quad & 10^{0.75} &&= V_2/0.8\\
\therefore \quad & V_2 &&= 10^{0.75} \times 0.8 = \mathbf{4.5\ V}
\end{aligned}
$$

Example 11.7. *An amplifier has an open-circuit voltage gain of 70 db and an output resistance of 1.5 kΩ. Determine the minimum value of load resistance so that voltage gain is not more than 67db.*

Solution.

$$
\begin{aligned}
& A_0 &&= 70\ db \quad ; \quad A_v = 67\ db\\
& A_0 \text{ in } db - A_v \text{ in } db &&= 70 - 67 = 3\ db\\
\text{or} \quad & 20 \log_{10} A_0 - 20 \log_{10} A_v &&= 3\\
\text{or} \quad & 20 \log_{10} \frac{A_0}{A_v} &&= 3\\
\text{or} \quad & \frac{A_0}{A_v} &&= (10)^{3/20} = 1.41\\
\text{But} \quad & \frac{A_v}{A_0} &&= \frac{R_L}{R_{out} + R_L} \qquad \text{[See Art. 10.20]}\\
\therefore \quad & \frac{1}{1.41} &&= \frac{R_L}{1.5 + R_L}\\
\text{or} \quad & R_L &&= \mathbf{3.65\ k\Omega}
\end{aligned}
$$

Example 11.8. *An amplifier feeding a resistive load of 1kΩ has a voltage gain of 40 db. If the input signal is 10 mV, find (i) output voltage (ii) load power.*

Solution.

$$
\begin{aligned}
(i) \quad & \frac{V_{out}}{V_{in}} &&= (10)^{db\ gain/20} = (10)^{40/20} = 100\\
\therefore \quad & V_{out} &&= 100 \times V_{in} = 100 \times 10 \text{ mV} = 1000 \text{ mV} = \mathbf{1\ V}\\
(ii) \quad & \text{Load power} &&= \frac{V_{out}^2}{R_L} = \frac{(1)^2}{1000} = 10^{-3} \text{ W} = \mathbf{1\ mW}
\end{aligned}
$$

Example 11.9. *An amplifier rated at 40W output is connected to a 10Ω speaker.*

(i) Calculate the input power required for full power output if the power gain is 25 db.

(ii) Calculate the input voltage for rated output if the amplifier voltage gain is 40 db.

Solution.

(*i*) Power gain in $db = 10 \log_{10} \frac{P_2}{P_1}$ or $25 = 10 \log_{10} \frac{40\text{W}}{P_1}$

$$\therefore \quad P_1 = \frac{40\text{W}}{\text{antilog } 2.5} = \frac{40\text{W}}{3.16 \times 10^2} = \frac{40\text{W}}{316} = \mathbf{126.5\ mW}$$

(*ii*) Voltage gain in *db* $= 20 \log_{10} \frac{V_2}{V_1}$ or $40 = 20 \log_{10} \frac{V_2}{V_1}$

$$\therefore \quad \frac{V_2}{V_1} = \text{antilog } 2 = 100$$

Now $V_2 = \sqrt{P_2 R} = \sqrt{40\text{W} \times 10\ \Omega} = 20\text{ V}$

$$\therefore \quad V_1 = \frac{V_2}{100} = \frac{20\text{V}}{100} = \mathbf{200\ mV}$$

Example 11.10. *In an amplifier, the maximum voltage gain is 2000 and occurs at 2 kHz. It falls to 1414 at 10 kHz and 50 Hz. Find :*

(i) Bandwidth (ii) Lower cut-off frequency (iii) Upper cut-off frequency.

Solution.

(*i*) Referring to the frequency response in Fig. 11.8, the maximum gain is 2000. Then 70.7% of this gain is 0.707 × 2000 = 1414. It is given that gain is 1414 at 50 Hz and 10 kHz. As bandwidth is the range of frequency over which gain is equal or greater than 70.7% of maximum gain,

∴ Bandwidth = **50 Hz to 10 kHz**

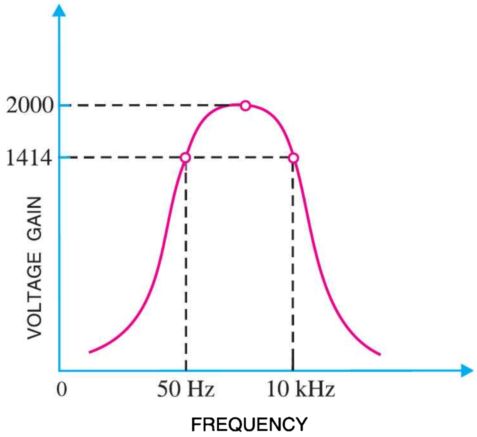


Fig. 11.8

(*ii*) The frequency (on lower side) at which the voltage gain of the amplifier is exactly 70.7% of the maximum gain is known as *lower cut-off frequency*. Referring to Fig. 11.8, it is clear that :

Lower cut-off frequency = **50 Hz**

(*iii*) The frequency (on the higher side) at which the voltage gain of the amplifier is exactly 70.7% of the maximum gain is known as *upper cut-off frequency*. Referring to Fig. 11.8, it is clear that:

Upper cut-off frequency = **10 kHz**

Comments. As bandwidth of the amplifier is 50 Hz to 10 kHz, therefore, it will amplify the signal frequencies lying in this range without any distortion. However, if the signal frequency is not in this range, then there will be distortion in the output.

Note. The *db* power rating of communication equipment is normally less than 50 *db*.

11.4 Properties of db Gain

The power gain expressed as a number is called ordinary power gain. Similarly, the voltage gain expressed as a number is called ordinary voltage gain.

1. Properties of *db* power gain. The following are the useful rules for *db* power gain :

(*i*) *Each time the ordinary power gain increases (decreases) by a factor of 10, the db power gain increases (decreases) by 10 db.*

For example, suppose the ordinary power gain increases from 100 to 1000 (*i.e.* by a factor of 10).

$$\therefore \quad \text{Increase in } db \text{ power gain} = 10\log_{10}1000 - 10\log_{10}100 = 30 - 20 = 10\ db$$

This property also applies for the decrease in power gain.

(*ii*) *Each time the ordinary power gain increases (decreases) by a factor of 2, the db power gain increases (decreases) by 3 db.*

For example, suppose the power gain increases from 100 to 200 (*i.e.* by a factor of 2).

$$\therefore \quad \text{Increase in } db \text{ power gain} = 10\log_{10}200 - 10\log_{10}100 = 23 - 20 = 3\ db$$

2. Properties of db voltage gain. The following are the useful rules for *db* voltage gain :

(*i*) *Each time the ordinary voltage gain increases (decreases) by a factor of 10, the db voltage gain increases (decreases) by 20 db.*

For example, suppose the voltage gain increases from 100 to 1000 (*i.e.* by a factor of 10).

$$\therefore \quad \text{Increase in } db \text{ voltage gain} = 20\log_{10}1000 - 20\log_{10}100 = 60 - 40 = 20\ db$$

(*ii*) *Each time the ordinary voltage gain increases (decreases) by a factor of 2, the db voltage gain increases (decreases) by 6 db.*

For example, suppose the voltage gain increases from 100 to 200 (*i.e.* by a factor of 2).

$$\therefore \quad \text{Increase in } db \text{ voltage gain} = 20\log_{10}200 - 20\log_{10}100 = 46 - 40 = 6\ db$$

11.5 RC Coupled Transistor Amplifier

This is the most popular type of coupling because it is cheap and provides excellent audio fidelity over a wide range of frequency. It is usually employed for voltage amplification. Fig. 11.9 shows two stages of an *RC* coupled amplifier. A coupling capacitor C_C is used to connect the output of first stage to the base (*i.e. input*) of the second stage and so on. As the coupling from one stage to next is achieved by a coupling capacitor followed by a connection to a shunt resistor, therefore, such amplifiers are called *resistance - capacitance coupled amplifiers.*

The resistances R_1, R_2 and R_E form the biasing and stabilisation network. The emitter bypass capacitor offers low reactance path to the signal. Without it, the voltage gain of each stage would be lost. The coupling capacitor C_C transmits a.c. signal but blocks d.c. This prevents d.c. interference between various stages and the shifting of operating point.

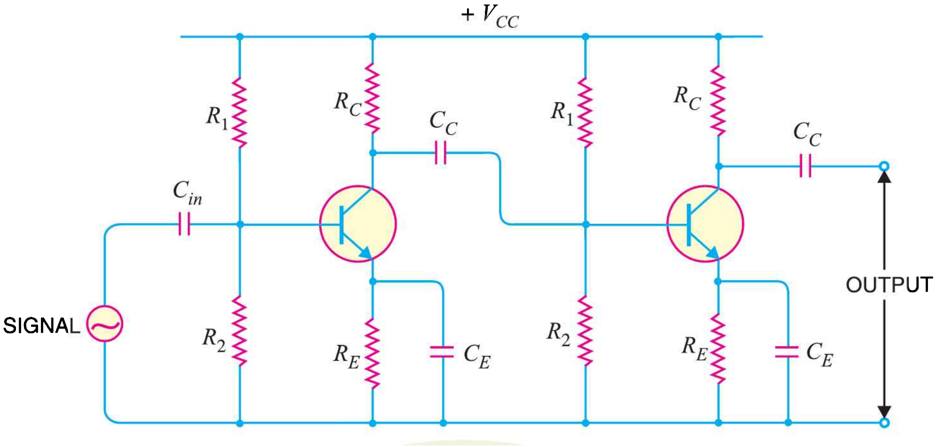


Fig. 11.9

Operation. When a.c. signal is applied to the base of the first transistor, it appears in the amplified form across its collector load R_C. The amplified signal developed across R_C is given to base of next stage through coupling capacitor C_C. The second stage does further amplification of the signal. In this way, the *cascaded* (one after another) stages amplify the signal and the overall gain is considerably increased.

It may be mentioned here that total gain is less than the product of the gains of individual stages. It is because when a second stage is made to follow the first stage, the *effective load resistance* of first stage is reduced due to the shunting effect of the input resistance of second stage. This reduces the gain of the stage which is loaded by the next stage. For instance, in a 3-stage amplifier, the gain of first and second stages will be reduced due to loading effect of next stage. However, the gain of the third stage which has no loading effect of subsequent stage, remains unchanged. The overall gain shall be equal to the product of the gains of three stages.

Frequency response. Fig.11.10 shows the frequency response of a typical *RC* coupled amplifier. It is clear that voltage gain drops off at low (< 50 Hz) and high (> 20 kHz) frequencies whereas it is uniform over ***mid-frequency*** range (50 Hz to 20 kHz). This behaviour of the amplifier is briefly explained below :

(*i*) *At low frequencies* (< 50 Hz), the reactance of coupling capacitor C_C is quite high and hence very small part of signal will pass from one stage to the next stage. Moreover, C_E cannot shunt the emitter resistance R_E effectively because of its large reactance at low frequencies. These two factors cause a falling of voltage gain at low frequencies.

(*ii*) *At high frequencies* (> 20 kHz), the reactance of C_C is very small and it behaves as a short circuit. This increases the loading effect of next stage and serves to reduce the voltage gain. Moreover, at high frequency, capacitive reactance of base-emitter junction is low which increases the base current. This reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency.

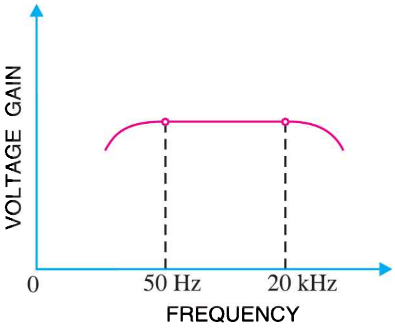


Fig. 11.10

(*iii*) *At mid-frequencies* (50 Hz to 20 kHz), the voltage gain of the amplifier is constant. The effect of coupling capacitor in this frequency range is such so as to maintain a uniform voltage gain. Thus, as the frequency increases in this range, reactance of C_C decreases which tends to increase the gain. However, at the same time, lower reactance means higher loading of first stage and hence lower gain. These two factors almost cancel each other, resulting in a uniform gain at mid-frequency.

Advantages

(*i*) It has excellent frequency response. The gain is constant over the audio frequency range which is the region of most importance for speech, music etc.

(*ii*) It has lower cost since it employs resistors and capacitors which are cheap.

(*iii*) The circuit is very compact as the modern resistors and capacitors are small and extremely light.

Disadvantages

(*i*) The *RC* coupled amplifiers have low voltage and power gain. It is because the low resistance presented by the input of each stage to the preceding stage decreases the effective load resistance (R_{AC}) and hence the gain.

(*ii*) They have the tendency to become noisy with age, particularly in moist climates.

(*iii*) Impedance matching is poor. It is because the output impedance of *RC* coupled amplifier is several hundred ohms whereas the input impedance of a speaker is only a few ohms. Hence, little power will be transferred to the speaker.

Applications.

The *RC* coupled amplifiers have excellent audio fidelity over a wide range of frequency. Therefore, they are widely used as voltage amplifiers *e.g.* in the initial stages of public address system. If other type of coupling (*e.g.* transformer coupling) is employed in the initial stages, this results in frequency distortion which may be amplified in next stages. However, because of poor impedance matching, *RC* coupling is rarely used in the final stages.

RC Coupled Amplifiers

Note. When there is an even number of cascaded stages (2, 4, 6 etc), the output signal is not inverted from the input. When the number of stages is odd (1, 3, 5 etc.), the output signal is inverted from the input.

Example 11.11 *A single stage amplifier has a voltage gain of 60. The collector load* $R_C = 500\ \Omega$ *and the input impedance is 1kΩ. Calculate the overall gain when two such stages are cascaded through R-C coupling. Comment on the result.*

Solution. The gain of second stage remains 60 because it has no loading effect of any stage. However, the gain of first stage is less than 60 due to the loading effect of the input impedance of second stage.

$$\therefore \quad \text{Gain of second stage} = 60$$

$$\text{Effective load of first stage} = R_C \parallel R_{in} = \frac{500 \times 1000}{500 + 1000} = 333\ \Omega$$

$$\text{Gain of first stage} = 60 \times 333/500 = 39.96$$

$$\text{Total gain} = 60 \times 39.96 = \mathbf{2397}$$

Comments. The gain of individual stage is 60. But when two stages are coupled, the gain is *not* 60 × 60 = 3600 as might be expected rather it is less and is equal to 2397 in this case. It is because the first stage has a loading effect of the input impedance of second stage and consequently its gain is reduced. However, the second stage has no loading effect of any subsequent stage. Hence, the gain of second stage remains 60.

Example 11.12. *Fig. 11.11 shows two-stage RC coupled amplifier. If the input resistance* R_{in} *of each stage is 1kΩ, find : (i) voltage gain of first stage (ii) voltage gain of second stage (iii) total voltage gain.*

Solution.

$$R_{in} = 1\ \text{k}\Omega\ ; \quad \beta = 100\ ; \quad R_C = 2\ \text{k}\Omega$$

(*i*) The first stage has a loading of input resistance of second stage.

$$\therefore \quad \text{Effective load of first stage, } R_{AC} = R_C \parallel R_{in} = \frac{2 \times 1}{2 + 1} = 0.66\ \text{k}\Omega$$

$$\therefore \quad \text{Voltage gain of first stage} = \beta \times R_{AC} / R_{in} = 100 \times 0.66/1 = \mathbf{66}$$

(*ii*) The collector of the second stage sees a load of only R_C (= 2 kΩ) as there is no loading effect of any subsequent stage.

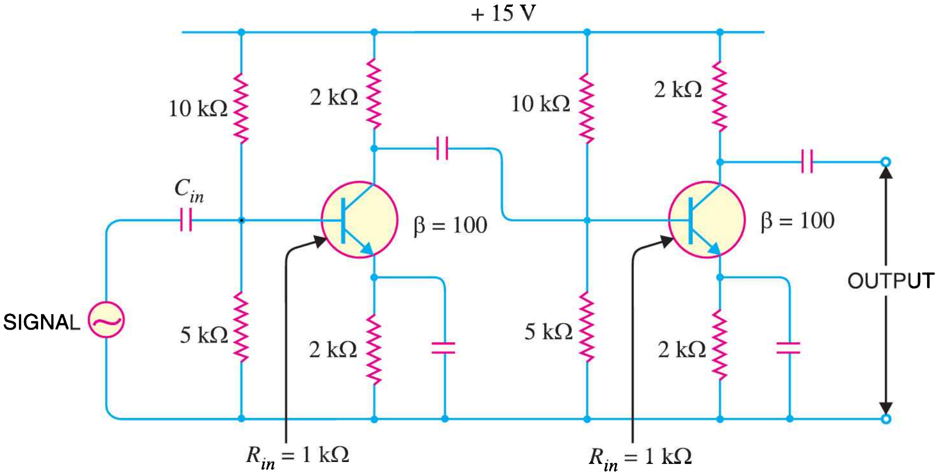


Fig. 11.11

∴ Voltage gain of second stage

$$= \beta \times R_C / R_{in} = 100 \times 2/1 = \mathbf{200}$$

(*iii*) Total voltage gain $= 66 \times 200 = \mathbf{13200}$

Example 11.13. *A single stage amplifier has collector load $R_C = 10\ k\Omega$; input resistance $R_{in} = 1 k\Omega$ and $\beta = 100$. If load $R_L = 100\Omega$, find the voltage gain. Comment on the result.*

Solution. Effective collector load, $R_{AC} = R_C \,||\, R_L = 10\ \text{k}\Omega \,||\, 100\ \Omega = {}^{*}100\ \Omega$

$$\therefore \quad \text{Voltage gain} = \beta \times \frac{R_{AC}}{R_{in}} = 100 \times \frac{100}{1000} = \mathbf{10}$$

Comments. As the load (*e.g.* speaker) is only of 100 ohms, therefore, effective load of the amplifier is too much reduced. Consequently, voltage gain is quite small. Under such situations, we can use a *transformer* to improve the voltage gain and signal handling capability. For example, if the output to 100 Ω load is delivered through a step-down transformer, the effective collector load and hence voltage gain can be increased.

Example 11.14. *Fig. 11.12 shows a 2-stage RC coupled amplifier. What is the biasing potential for the second stage ? If the coupling capacitor C_C is replaced by a wire, what would happen to the circuit ?*

Solution. Referring to Fig. 11.12, we have,

$$\text{Voltage across } R_4,\ V_B = \frac{V_{CC}}{R_3 + R_4} \times R_4 = \frac{20}{10 + 2.2} \times 2.2 = \mathbf{3.6\ V}$$

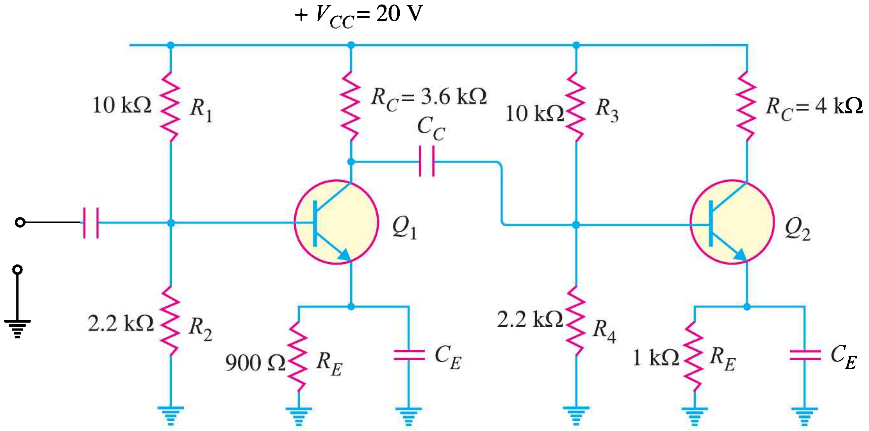
Thus biasing potential for the second stage is 3.6 V.

When the coupling capacitor C_C is replaced by a wire, this changes the entire picture. It is because now R_C of the first stage is in parallel with R_3 of the second stage as shown in Fig. 11.13(*i*). The total resistance of R_C (= 3.6 kΩ) and R_3 (= 10 kΩ) is given by:

---

[*] 10 kΩ || 100 Ω is essentially 100 Ω.

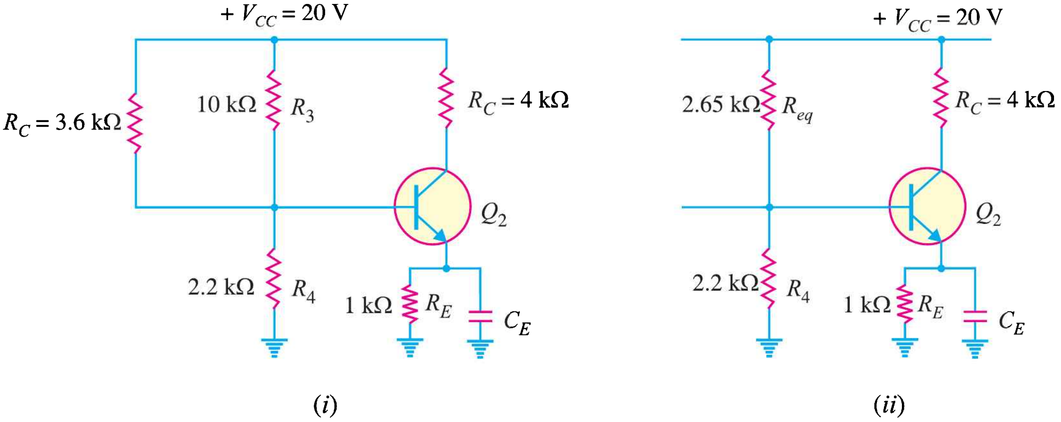
$$R_{eq} = \frac{R_3 \, R_C}{R_3 + R_C} = \frac{10 \times 3.6}{10 + 3.6} = 2.65 \text{ k}\Omega$$



+ V_{CC} = 20 V
10 kΩ
R_1
R_C = 3.6 kΩ
C_C
10 kΩ
R_3
R_C = 4 kΩ
Q_1
Q_2
2.2 kΩ
R_2
900 Ω
R_E
C_E
2.2 kΩ
R_4
1 kΩ
R_E
C_E

Fig. 11.12

The circuit shown in Fig. 11.13 (*i*) then reduces to the one shown in Fig. 11.13 (*ii*). Referring to Fig. 11.13 (*ii*), we have,



+ V_{CC} = 20 V
R_C = 3.6 kΩ
10 kΩ
R_3
R_C = 4 kΩ
Q_2
2.2 kΩ
R_4
1 kΩ
R_E
C_E
+ V_{CC} = 20 V
2.65 kΩ
R_{eq}
R_C = 4 kΩ
Q_2
2.2 kΩ
R_4
1 kΩ
R_E
C_E

(*i*) (*ii*)

Fig. 11.13

$$\text{Voltage across } R_4, \, V_B = \frac{V_{CC}}{R_{eq} + R_4} \times R_4 = \frac{20}{2.65 + 2.2} \times 2.2 = 9.07 \text{ V}$$

Thus the biasing potential of second stage is drastically changed. The 9.07 V at the base of Q_2 would undoubtedly cause the transistor to saturate and the device would be rendered useless as an amplifier. This example explains the importance of dc isolation in a multistage amplifier. The use of coupling capacitor allows each amplifier stage to maintain its independent biasing potential while allowing the ac output from one stage to pass on to the next stage.

Example 11.15. *Fig. 11.14 shows a 2-stage RC coupled amplifier. Find the voltage gain of (i) first stage (ii) second stage and (iii) overall voltage gain.*

Solution. (*i*) Voltage gain of First stage. The input impedance of the second stage is the load for the first stage. In order to find input impedance of second stage, we shall first find r'_e (*ac* emitter resistance) for the second stage.

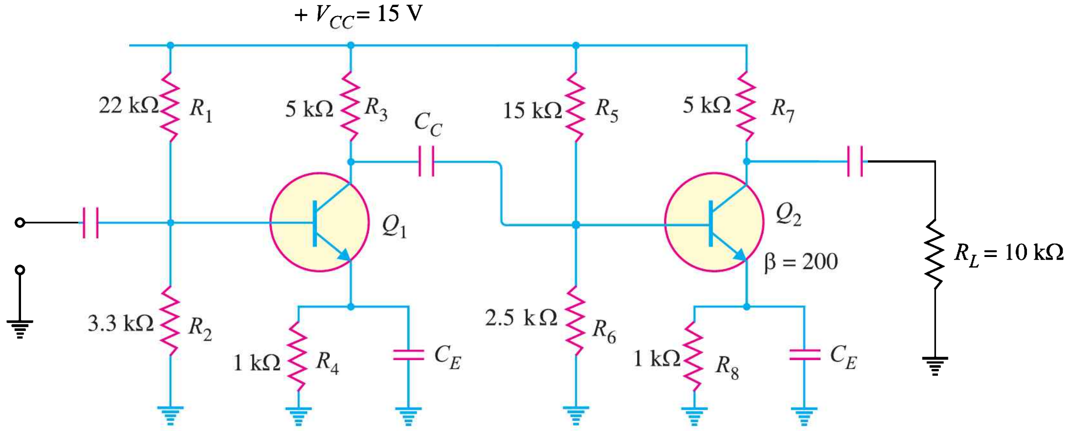


Fig. 11.14

$$\text{Voltage across } R_6 = \frac{V_{CC}}{R_5 + R_6} \times R_6 = \frac{15}{15 + 2.5} \times 2.5 = 2.14 \text{ V}$$

$$\text{Voltage across } R_8 = 2.14 - 0.7 = 1.44 \text{ V}$$

$$\text{Emitter current in } R_8, I_E = \frac{1.44 \text{ V}}{R_8} = \frac{1.44 \text{ V}}{1 \text{ k}\Omega} = 1.44 \text{ mA}$$

$$r'_e \text{ for second stage} = \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{1.44 \text{ mA}} = 17.4\ \Omega$$

Similarly, it can be shown that r'_e for the first stage is 19.8 Ω .

$$Z_{in(base)} \text{ for second stage} = \beta \times r'_e \text{ for second stage} = 200 \times (17.4\ \Omega) = 3.48 \text{ k}\Omega$$

$$\text{Input impedance of the second stage, } Z_{in} = R_5 \,||\, R_6 \,||\, Z_{in(base)}$$

$$= 15 \text{ k}\Omega \,||\, 2.5 \text{ k}\Omega \,||\, 3.48 \text{ k}\Omega = 1.33 \text{ k}\Omega$$

∴ Effective collector load for first stage is

$$R_{AC} = R_3 \,||\, Z_{in} = 5 \text{ k}\Omega \,||\, 1.33 \text{ k}\Omega = 1.05 \text{ k}\Omega$$

$$\text{Voltage gain of first stage} = \frac{R_{AC}}{r'_e \text{ for first stage}} = \frac{1.05 \text{ k}\Omega}{19.8\ \Omega} = \mathbf{53}$$

(*ii*) **Voltage gain of second stage.** The load R_L (= 10 kΩ) is the load for the second stage.

∴ Effective collector load for second stage is

$$R_{AC} = R_7 \,||\, R_L = 5 \text{ k}\Omega \,||\, 10 \text{ k}\Omega = 3.33 \text{ k}\Omega$$

$$\therefore \quad \text{Voltage gain of second stage} = \frac{R_{AC}}{r'_e \text{ for second stage}} = \frac{3.33 \text{ k}\Omega}{17.4\ \Omega} = \mathbf{191.4}$$

(*iii*) **Overall voltage gain.** Overall voltage gain = First stage gain × Second stage gain

$$= 53 \times 191.4 = \mathbf{10144}$$

11.6 Transformer-Coupled Amplifier

The main reason for low voltage and power gain of *RC* coupled amplifier is that the effective load (R_{AC}) of each stage is *decreased due to the low resistance presented by the input of each stage to the preceding stage. If the effective load resistance of each stage could be increased, the voltage and power gain could be increased. This can be achieved by transformer coupling. By the use of **impedance-changing properties of transformer, the low resistance of a stage (or load) can be reflected as a high load resistance to the previous stage.

---

* The input impedance of an amplifier is low while its output impedance is very high. When they are coupled to make a multistage amplifier, the high output impedance of one stage comes in parallel with the low input impedance of next state. Hence effective load (R_{AC}) is decreased.

** The resistance on the secondary side of a transformer reflected on the primary depends upon the turn ratio of the transformer.

Transformer coupling is generally employed when the load is small. It is mostly used for power amplification. Fig. 11.15 shows two stages of transformer coupled amplifier. A coupling transformer is used to feed the output of one stage to the input of the next stage. The primary *P* of this transformer is made the collector load and its secondary *S* gives input to the next stage.

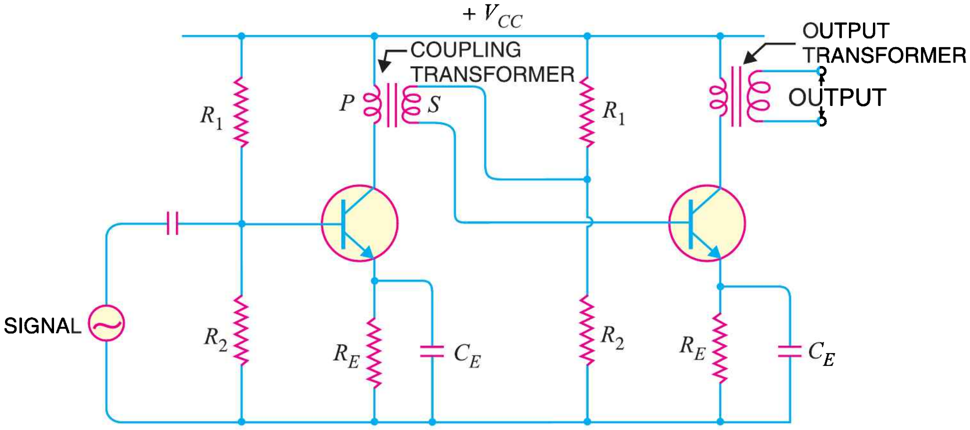


Fig. 11.15

Operation. When an a.c. signal is applied to the base of first transistor, it appears in the amplified form across primary *P* of the coupling transformer. The voltage developed across primary is transferred to the input of the next stage by the transformer secondary as shown in Fig.11.15. The second stage renders amplification in an exactly similar manner.

Frequency response. The frequency response of a transformer coupled amplifier is shown in Fig.11.16. It is clear that frequency response is rather poor *i.e.* gain is constant only over a small range of frequency. The output voltage is equal to the collector current multiplied by reactance of primary. At low frequencies, the reactance of primary begins to fall, resulting in decreased gain. At high frequencies, the capacitance between turns of windings acts as a bypass condenser to reduce the output voltage and hence gain. It follows, therefore, that there will be disproportionate amplification of frequencies in a complete signal such as music, speech etc. Hence, transformer-coupled amplifier introduces *frequency distortion*.

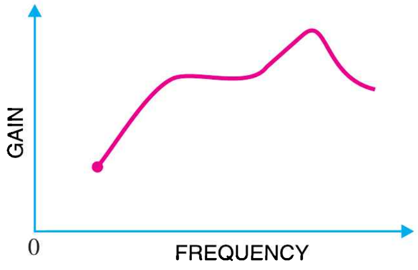


Fig. 11.16

It may be added here that in a properly designed transformer, it is possible to achieve a fairly constant gain over the audio frequency range. But a transformer that achieves a frequency response comparable to *RC* coupling may cost 10 to 20 times as much as the inexpensive *RC* coupled amplifier.

Advantages

(*i*) No signal power is lost in the collector or base resistors.

(*ii*) An excellent impedance matching can be achieved in a transformer coupled amplifier. It is easy to make the inductive reactance of primary equal to the output impedance of the transistor and inductive reactance of secondary equal to the input impedance of next stage.

(*iii*) Due to excellent impedance matching, transformer coupling provides higher gain. As a matter of fact, a single stage of properly designed transformer coupling can provide the gain of two stages of *RC* coupling.

Disadvantages

(*i*) It has a poor frequency response *i.e.*the gain varies considerably with frequency.

(*ii*) The coupling transformers are bulky and fairly expensive at audio frequencies.

(*iii*) Frequency distortion is higher *i.e.* low frequency signals are less amplified as compared to the high frequency signals.

(*iv*) Transformer coupling tends to introduce **hum* in the output.

Applications. Transformer coupling is mostly employed for *impedance matching*. In general, the last stage of a multistage amplifier is the *power stage*. Here, a concentrated effort is made to transfer maximum power to the output device *e.g.* a loudspeaker. For maximum power transfer, the impedance of power source should be equal to that of load. Usually, the impedance of an output device is a few ohms whereas the output impedance of transistor is several hundred times this value. In order to match the impedance, a step-down transformer of proper turn ratio is used. The impedance of secondary of the transformer is made equal to the load impedance and primary impedance equal to the output impedance of transistor. Fig. 11.17 illustrates the impedance matching by a step-down transformer. The output device (*e.g.* speaker) connected to the secondary has a small resistance R_L. The load R'_L appearing on the primary side will be:

$$^{**}R'_L = \left(\frac{N_P}{N_S}\right)^2 R_L$$

For instance, suppose the transformer has turn ratio $N_P : N_S :: 10 : 1$. If $R_L = 100\ \Omega$, then load appearing on the primary is :

$$R'_L = \left(\frac{10}{1}\right)^2 \times 100\ \Omega = 10\ \text{k}\Omega$$

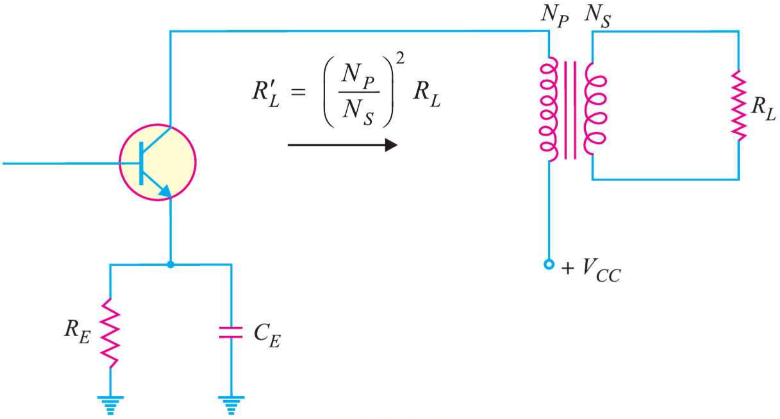


Fig. 11.17

---

* There are hundreds of turns of primary and secondary. These turns will multiply an induced e.m.f. from nearby power wiring. As the transformer is connected in the base circuit, therefore, the induced hum voltage will appear in amplified form in the output.

** Suppose primary and secondary of transformer carry currents I_P and I_S respectively. The secondary load R_L can be transferred to primary as R'_L provided the power loss remains the same *i.e.*,

$$I_P^2 R'_L = I_S^2 R_L$$

or $$R'_L = \left(\frac{I_S}{I_P}\right)^2 \times R_L = \left(\frac{N_P}{N_S}\right)^2 \times R_L \qquad \left(\because \frac{I_S}{I_P} = \frac{N_P}{N_S}\right)$$

Thus the load on the primary side is comparable to the output impedance of the transistor. This results in maximum power transfer from transistor to the primary of transformer. This shows that low value of load resistance (*e.g.* speaker) can be "stepped-up" to a more favourable value at the collector of transistor by using appropriate turn ratio.

Example 11.16. *A transformer coupling is used in the final stage of a multistage amplifier. If the output impedance of transistor is 1kΩ and the speaker has a resistance of 10Ω, find the turn ratio of the transformer so that maximum power is transferred to the load.*

Solution.

For maximum power transfer, the impedance of the primary should be equal to the output impedance of transistor and impedance of secondary should be equal to load impedance *i.e.*

$$\text{Primary impedance} = 1\text{ k}\Omega = 1000\ \Omega$$

Let the turn ratio of the transformer be $n\ (= N_P/N_S)$.

$$\text{Primary impedance} = \left(\frac{N_P}{N_S}\right)^2 \times \text{Load impedance}$$

$$\therefore \quad \left(\frac{N_P}{N_S}\right)^2 = \frac{\text{Primary impedance}}{\text{Load impedance}}$$

$$\text{or} \quad n^2 = 1000/10 = 100$$

$$\therefore \quad n = \sqrt{100} = \mathbf{10}$$

A step-down transformer with turn ratio 10 : 1 is required.

Example 11.17. *Determine the necessary transformer turn ratio for transferring maximum power to a 16Ω load from a source that has an output impedance of 10 kΩ. Also calculate the voltage across the external load if the terminal voltage of the source is 10V r.m.s.*

Solution.

For maximum power transfer, the impedance of the primary should be equal to the output impedance of the source.

$$\text{Primary impedance, } R'_L = 10\text{ k}\Omega = 10{,}000\ \Omega$$

$$\text{Load impedance, } R_L = 16\ \Omega$$

Let the turn ratio of the transformer be $n\ (= N_P/N_S)$.

$$\therefore \quad R'_L = \left(\frac{N_P}{N_S}\right)^2 R_L$$

$$\text{or} \quad \left(\frac{N_P}{N_S}\right)^2 = \frac{R'_L}{R_L} = \frac{10{,}000}{16} = 625$$

$$\text{or} \quad n^2 = 625$$

$$\text{or} \quad n = \sqrt{625} = \mathbf{25}$$

$$\text{Now} \quad \frac{V_S}{V_P} = \frac{N_S}{N_P}$$

$$\therefore \quad V_S = \left(\frac{N_S}{N_P}\right) \times V_P = \frac{1}{25} \times 10 = \mathbf{0.4\ V}$$

Example 11.18. *The output resistance of the transistor shown in Fig. 11.18 is 3kΩ. The primary of the transformer has a d.c. resistance of 300 Ω and the load connected across secondary is 3Ω. Calculate the turn ratio of the transformer for transferring maximum power to the load.*

Solution.

$$\text{D.C. resistance of primary, } R_P = 300\ \Omega$$

$$\text{Load resistance, } R_L = 3\ \Omega$$

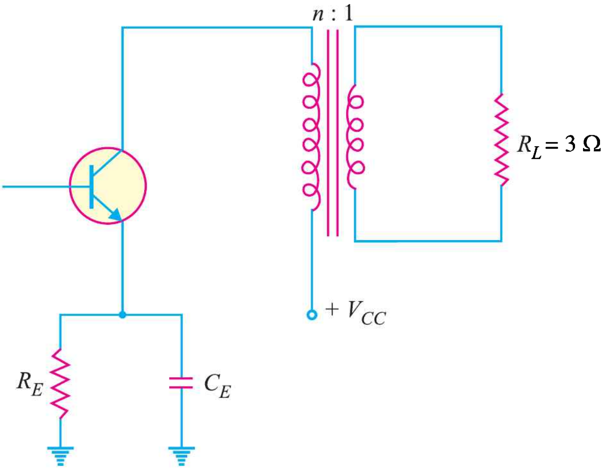


Fig. 11.18

Let n ($= N_P/N_S$) be the required turn ratio. When no signal is applied, the transistor 'sees' a load of R_P (= 300 Ω) only. However, when a.c. signal is applied, the load R_L in the secondary is reflected in the primary as n^2R_L. Consequently, the transistor now 'sees' a load of R_P in series with n^2R_L.

For transference of maximum power,

$$\text{Output resistance of transistor} = R_P + n^2R_L$$

or $$3000 = 300 + n^2 \times 3$$

or $$n^2 = \frac{3000 - 300}{3} = 900$$

∴ $$n = \sqrt{900} = \mathbf{30}$$

Example 11.19. *A transistor uses transformer coupling for amplification. The output impedance of transistor is 10 kΩ while the input impedance of next stage is 2.5 kΩ. Determine the inductance of primary and secondary of the transformer for perfect impedance matching at a frequency of 200 Hz.*

Solution. $$\text{Frequency}, f = 200\text{Hz}$$

$$\text{Output impedance of transistor} = 10\ \text{k}\Omega = 10^4\ \Omega$$

$$\text{Input impedance of next stage} = 2.5\ \text{k}\Omega = 2.5 \times 10^3\ \Omega$$

Primary inductance. Consider the primary side of the transformer. For perfect impedance matching,

$$\text{Output impedance of transistor} = \text{Primary impedance}$$

or $$10^4 = 2\,\pi f L_P$$

∴ $$\text{Primary inductance}, L_P = \frac{10^4}{2\pi \times 200} = \mathbf{8\ H}$$

Secondary inductance. Consider the secondary side of transformer. For impedance matching,

$$\text{Input impedance of next stage} = \text{Impedance of secondary}$$

or $$2.5 \times 10^3 = 2\,\pi f L_S$$

∴ $$\text{Secondary inductance}, L_S = \frac{2.5 \times 10^3}{2\pi \times 200} = \mathbf{2\ H}$$

Example 11.20. *In the above example, find the number of primary and secondary turns. Given that core section of the transformer is such that 1 turn gives an inductance of 10μH.*

Solution.

We know that inductance of a coil is directly proportional to the square of number of turns of the coil *i.e.*

$$L \propto N^2$$

or $$L = KN^2$$

Now $$L = 10\,\mu H = 10^{-5}\text{ H}, \quad N = 1 \text{ turn}$$

$$\therefore \quad 10^{-5} = K(1)^2$$

or $$K = 10^{-5}$$

$$\text{Primary inductance} = K\,N_P^2$$

or $$8 = 10^{-5}\,N_P^2$$

$$\therefore \quad \text{Primary turns, } N_P = \sqrt{8 \times 10^5} = \mathbf{894}$$

Similarly, $$\text{Secondary turns, } N_S = \sqrt{2 \times 10^5} = \mathbf{447}$$

11.7 Direct-Coupled Amplifier

There are many applications in which extremely low frequency (< 10 Hz) signals are to be amplified *e.g.* amplifying photo-electric current, thermo-couple current etc. The coupling devices such as capacitors and transformers cannot be used because the electrical sizes of these components become very large at extremely low frequencies. Under such situations, one stage is *directly* connected to the next stage without any intervening coupling device. This type of coupling is known as *direct coupling*.

Circuit details. Fig. 11.19 shows the circuit of a three-stage direct-coupled amplifier. It uses *complementary transistors. Thus, the first stage uses *npn* transistor, the second stage uses *pnp* transistor and so on. This arrangement makes the design very simple. The output from the collector of first transistor T_1 is fed to the input of the second transistor T_2 and so on.

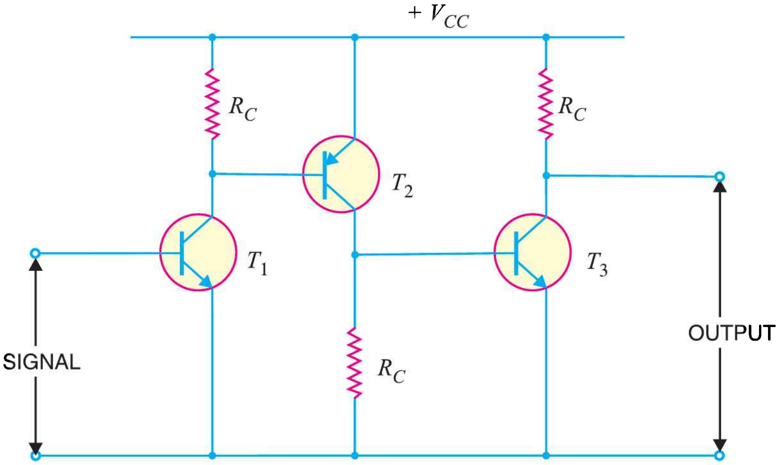


Fig. 11.19

---

[*] This makes the circuit stable w.r.t. temperature changes. In this connection (*i.e., npn* followed by *pnp*), the direction of collector current increase β, when the temperature rises, is opposite for the two transistors. Thus the variation in one transistor tends to cancel that in the other.

The weak signal is applied to the input of first transistor T_1. Due to transistor action, an amplified output is obtained across the collector load R_C of transistor T_1. This voltage drives the base of the second transistor and amplified output is obtained across its collector load. In this way, direct coupled amplifier raises the strength of weak signal.

Advantages

(*i*) The circuit arrangement is simple because of minimum use of resistors.

(*ii*) The circuit has low cost because of the absence of expensive coupling devices.

Disadvantages

(*i*) It cannot be used for amplifying high frequencies.

(*ii*) The operating point is shifted due to temperature variations.

Example 11.21. *Fig. 11.20 shows a direct coupled two-stage amplifier. Determine (i) d.c. voltages for both stages (ii) voltage gain of each stage and overall voltage gain.*

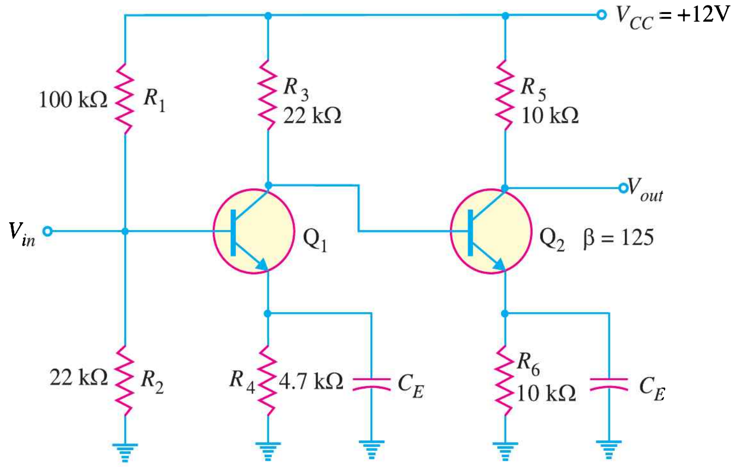


Fig. 11.20

Solution. Note that direct-coupled amplifier has no coupling capacitors between the stages.

(*i*) **D.C. voltages.** We shall now determine the d.c. voltages for both the stages following the established procedure.

First stage

$$\text{D.C. current thro' } R_1 \text{ and } R_2 = \frac{V_{CC}}{R_1 + R_2} = \frac{12\text{V}}{100\text{ k}\Omega + 22\text{ k}\Omega} = 0.098\text{ mA}$$

$$\text{D.C. voltage across } R_2 = 0.098\text{ mA} \times R_2 = 0.098\text{ mA} \times 22\text{ k}\Omega = \mathbf{2.16V}$$

This is the d.c. voltage at the base of transistor Q_1.

$$\text{D.C. voltage at the emitter, } V_{E1} = 2.16 - V_{BE} = 2.16\text{V} - 0.7\text{V} = \mathbf{1.46V}$$

$$\text{D.C. emitter current, } I_{E1} = \frac{V_{E1}}{R_4} = \frac{1.46\text{V}}{4.7\text{ k}\Omega} = 0.31\text{ mA}$$

$$\text{D.C. collector current, } I_{C1} = 0.31\text{ mA} \quad (\because I_{C1} \simeq I_{E1})$$

$$\text{D.C. voltage at collector, } V_{C1} = V_{CC} - I_{C1}\,R_3$$

$$= 12\text{V} - 0.31\text{ mA} \times 22\text{ k}\Omega = \mathbf{5.18V}$$

Second stage

$$\text{D.C. base voltage} = V_{C1} = \mathbf{5.18V}$$

$$\text{D.C. emitter voltage, } V_{E2} = V_{C1} - V_{BE} = 5.18\text{V} - 0.7\text{V} = \mathbf{4.48V}$$

$$\text{D.C. emitter current, } I_{E2} = \frac{V_{E2}}{R_6} = \frac{4.48\text{V}}{10\text{ k}\Omega} = 0.448\text{ mA}$$

$$\text{D.C. voltage at collector, } V_{C2} = V_{CC} - I_{C2}R_5 \quad (\because I_{E2} \simeq I_{C2})$$

$$= 12\text{V} - 0.448\text{ mA} \times 10\text{ k}\Omega = \mathbf{7.52V}$$

(*ii*) Voltage gain To find voltage gain, we shall use the standard formula : total a.c. collector load divided by total a.c. emitter resistance.

First stage

$$r'_{e1} = \frac{25\text{ mV}}{I_{E1}} = \frac{25\text{ mV}}{0.31\text{ mA}} = 80.6\Omega$$

Input impedance Z_{in} of the second stage is given by ;

$$Z_{in} = \beta r'_{e2}$$

$$\text{Here } r'_{e2} = \frac{25\text{ mV}}{I_{E2}} = \frac{25\text{ mV}}{0.448\text{ mA}} = 55.8\Omega$$

$$\therefore \quad Z_{in} = \beta r'_{e2} = 125 \times (55.8\Omega) \simeq 7000\Omega = 7\text{ k}\Omega$$

$$\text{Total a.c. collector load, } R_{AC} = R_3 \,||\, Z_{in} = 22\text{ k}\Omega \,||\, 7\text{ k}\Omega = 5.31\text{ k}\Omega$$

$$\therefore \quad \text{Voltage gain, } A_{v1} = \frac{R_{AC}}{r'_{e1}} = \frac{5.31\text{ k}\Omega}{80.6\,\Omega} = \mathbf{66}$$

Second stage. There is no loading effect of any subsequent stage. Therefore, total a.c. collector load, $R_{AC} = R_5 = 10\text{ k}\Omega$.

$$\text{Voltage gain, } A_{v2} = \frac{R_5}{r'_{e2}} = \frac{10\text{ k}\Omega}{55.8\,\Omega} = \mathbf{179}$$

$$\text{Overall voltage gain} = A_{v1} \times A_{v2} = 66 \times 179 = \mathbf{11{,}814}$$

11.8 Comparison of Different Types of Coupling

S. No	Particular	*RC* coupling	Transformer coupling	Direct coupling
1.	*Frequency response*	Excellent in the audio frequency range	Poor	Best
2.	*Cost*	Less	More	Least
3.	*Space and weight*	Less	More	Least
4.	*Impedance matching*	Not good	Excellent	Good
5.	*Use*	For voltage amplification	For power amplification	For amplifiying extremely low frequencies

11.9 Difference Between Transistor and Tube Amplifiers

Although both transistors and grid-controlled tubes (*e.g.* triode, tetrode and pentode) can render the job of amplification, they differ in the following respects :

(*i*) The electron tube is a voltage driven device while transistor is a current operated device.

(*ii*) The input and output impedances of the electron tubes are generally quite large. On the other hand, input and output impedances of transistors are relatively small.

(*iii*) Voltages for transistor amplifiers are much smaller than those of tube amplifiers.

(*iv*) Resistances of the components of a transistor amplifier are generally smaller than the resistances of the corresponding components of the tube amplifier.

(*v*) The capacitances of the components of a transistor amplifier are usually larger than the corresponding components of the tube amplifier.

MULTIPLE-CHOICE QUESTIONS

1. A radio receiver has .... of amplification.
(*i*) one stage (*ii*) two stages
(*iii*) three stages
(*iv*) more than three stages

2. *RC* coupling is used for .... amplification.
(*i*) voltage (*ii*) current
(*iii*) power (*iv*) none of the above

3. In an *RC* coupled amplifier, the voltage gain over mid-frequency range ....
(*i*) changes abruptly with frequency
(*ii*) is constant
(*iii*) changes uniformly with frequency
(*iv*) none of the above

4. In obtaining the frequency response curve of an amplifier, the ....
(*i*) amplifier level output is kept constant
(*ii*) amplifier frequency is held constant
(*iii*) generator frequency is held constant
(*iv*) generator output level is held constant

5. An advantage of *RC* coupling scheme is the ....
(*i*) good impedance matching
(*ii*) economy
(*iii*) high efficiency (*iv*)none of the above

6. The best frequency response is of .... coupling.
(*i*) *RC* (*ii*) transformer
(*iii*) direct (*iv*) none of the above

7. Transformer coupling is used for .... amplification.
(*i*) power (*ii*) voltage
(*iii*) current (*iv*) none of the above

8. In an *RC* coupling scheme, the coupling capacitor C_C must be large enough ....
(*i*) to pass d.c. between the stages
(*ii*) not to attenuate the low frequencies
(*iii*) to dissipate high power
(*iv*) none of the above

9. In *RC* coupling, the value of coupling capacitor is about ....
(*i*) 100 pF (*ii*) 0.1 μF
(*iii*) 0.01 μF (*iv*) 10 μF

10. The noise factor of an ideal amplifier expressed in *db* is ....
(*i*) 0 (*ii*) 1
(*iii*) 0.1 (*iv*) 10

11. When a multistage amplifier is to amplify d.c. signal, then one must use .... coupling.
(*i*) *RC* (*ii*) transformer
(*iii*) direct (*iv*) none of the above

12. .... coupling provides the maximum voltage gain.
(*i*) *RC* (*ii*) transformer
(*iii*) direct (*iv*) impedance

13. In practice, voltage gain is expressed ....
(*i*) in *db* (*ii*) in volts
(*iii*) as a number (*iv*) none of the above

14. Transformer coupling provides high efficiency because ....
(*i*) collector voltage is stepped up
(*ii*) d.c. resistance is low
(*iii*) collector voltage is stepped down
(*iv*) none of the above

15. Transformer coupling is generally employed when load resistance is ....
(*i*) large (*ii*) very large
(*iii*) small (*iv*) none of the above

16. If a three-stage amplifier has individual stage gains of 10 *db*, 5 *db* and 12 *db*, then total gain in *db* is ....
(*i*) 600 *db* (*ii*) 24 *db*
(*iii*) 14 *db* (*iv*) 27 *db*

17. The final stage of a multistage amplifier uses ....
(*i*) *RC* coupling
(*ii*) transformer coupling
(*iii*) direct coupling
(*iv*) impedance coupling

18. The ear is not sensitive to........
- (*i*) frequency distortion
- (*ii*) amplitude distortion
- (*iii*) frequency as well as amplitude distortion
- (*iv*) none of the above

19. *RC* coupling is not used to amplify extremely low frequencies because ....
- (*i*) there is considerable power loss
- (*ii*) there is hum in the output
- (*iii*) electrical size of coupling capacitor becomes very large
- (*iv*) none of the above

20. In transistor amplifiers, we use .... transformer for impedance matching.
- (*i*) step up (*ii*) step down
- (*iii*) same turn ratio (*iv*) none of the above

21. The lower and upper cut off frequencies are also called .... frequencies.
- (*i*) sideband (*ii*) resonant
- (*iii*) half-resonant
- (*iv*) half-power

22. A gain of 1,000,000 times in power is expressed by ....
- (*i*) 30 *db* (*ii*) 60 *db*
- (*iii*) 120 *db* (*iv*) 600 *db*

23. A gain of 1000 times in voltage is expressed by ....
- (*i*) 60 *db* (*ii*) 30 *db*
- (*iii*) 120 *db* (*iv*) 600 *db*

24. 1 *db* corresponds to .... change in power level.
- (*i*) 50% (*ii*) 35%
- (*iii*) 26% (*iv*) 22%

25. 1 *db* corresponds to .... change in voltage or current level.
- (*i*) 40% (*ii*) 80%
- (*iii*) 20% (*iv*) 25%

26. The frequency response of transformer coupling is ....
- (*i*) good (*ii*) very good
- (*iii*) excellent (*iv*) poor

27. In the initial stages of a multistage amplifier, we use ....
- (*i*) *RC* coupling
- (*ii*) transformer coupling
- (*iii*) direct coupling
- (*iv*) none of the above

28. The total gain of a multistage amplifier is less than the product of the gains of individual stages due to ....
- (*i*) power loss in the coupling device
- (*ii*) loading effect of next stage
- (*iii*) the use of many transistors
- (*iv*) the use of many capacitors

29. The gain of an amplifier is expressed in *db* because ....
- (*i*) it is a simple unit
- (*ii*) calculations become easy
- (*iii*) human ear response is logarithmic
- (*iv*) none of the above

30. If the power level of an amplifier reduces to half, the *db* gain will fall by ....
- (*i*) 0.5 *db* (*ii*) 2 *db*
- (*iii*) 10 *db* (*iv*) 3 *db*

31. A current amplification of 2000 is a gain of ....
- (*i*) 3 *db* (*ii*) 66 *db*
- (*iii*) 20 *db* (*iv*) 200 *db*

32. An amplifier receives 0.1 W of input signal and delivers 15 W of signal power. What is the power gain in *db* ?
- (*i*) 21.8 *db* (*ii*) 14.6 *db*
- (*iii*) 9.5 *db* (*iv*) 17.4 *db*

33. The power output of an audio system is 18 W. For a person to notice an increase in the output (loudness or sound intensity) of the system, what must the output power be increased to ?
- (*i*) 14.2 W (*ii*) 11.6 W
- (*iii*) 22.68 W (*iv*) none of the above

34. The output of a microphone is rated at – 52 *db*. The reference level is 1 V under specified sound conditions. What is the output voltage of this microphone under the same sound conditions ?
- (*i*) 1.5 mV (*ii*) 6.2 mV
- (*iii*) 3.8 mV (*iv*) 2.5 mV

35. *RC* coupling is generally confined to low power applications because of ....

(*i*) large value of coupling capacitor
(*ii*) low efficiency
(*iii*) large number of components
(*iv*) none of the above

36. The number of stages that can be directly coupled is limited because ....

(*i*) changes in temperature cause thermal instability
(*ii*) circuit becomes heavy and costly
(*iii*) it becomes difficult to bias the circuit
(*iv*) none of the above

37. The purpose of RC or transformer coupling is to ....

(*i*) block a.c.
(*ii*) separate bias of one stage from another
(*iii*) increase thermal stability
(*iv*) none of the above

38. The upper or lower cut off frequency is also called .... frequency.

(*i*) resonant (*ii*) sideband
(*iii*) 3 *db* (*iv*) none of the above

39. The bandwidth of a single stage amplifier is .... that of a multistage amplifier.

(*i*) more than (*ii*) the same as
(*iii*) less than (*iv*) data insufficient

40. The value of emitter capacitor C_E in a multi-stage amplifier is about ....

(*i*) 0.1 μF (*ii*) 100 pF
(*iii*) 0.01 μF (*iv*) 50 μF

Answers to Multiple-Choice Questions

1.	(*iv*)	**2.**	(*i*)	**3.**	(*ii*)	**4.**	(*iv*)	**5.**	(*ii*)
6.	(*iii*)	**7.**	(*i*)	**8.**	(*ii*)	**9.**	(*iv*)	**10.**	(*i*)
11.	(*iii*)	**12.**	(*ii*)	**13.**	(*i*)	**14.**	(*ii*)	**15.**	(*iii*)
16.	(*iv*)	**17.**	(*ii*)	**18.**	(*i*)	**19.**	(*iii*)	**20.**	(*ii*)
21.	(*iv*)	**22.**	(*ii*)	**23.**	(*i*)	**24.**	(*iii*)	**25.**	(*i*)
26.	(*iv*)	**27.**	(*i*)	**28.**	(*ii*)	**29.**	(*iii*)	**30.**	(*iv*)
31.	(*ii*)	**32.**	(*i*)	**33.**	(*iii*)	**34.**	(*iv*)	**35.**	(*ii*)
36.	(*i*)	**37.**	(*ii*)	**38.**	(*iii*)	**39.**	(*i*)	**40.**	(*iv*)

Chapter Review Topics

1. What do you understand by multistage transistor amplifier ? Mention its need.
2. Explain the following terms : (*i*) Frequency response (*ii*) Decibel gain (*iii*) Bandwidth.
3. Explain transistor *RC* coupled amplifier with special reference to frequency response, advantages, disadvantages and applications.
4. With a neat circuit diagram, explain the working of transformer-coupled transistor amplifier.
5. How will you achieve impedance matching with transformer coupling ?
6. Explain direct coupled transistor amplifier.

Problems

1. The absolute voltage gain of an amplifier is 73. Find its decibel gain. **[37db]**
2. The input power to an amplifier is 15mW while output power is 2W. Find the decibel gain of the amplifier. **[21.25db]**
3. What is the *db* gain for an increase of power level from 12W to 24W ? **[3 db]**
4. What is the *db* gain for an increase of voltage from 4mV to 8mV ? **[6 db]**
5. A two-stage amplifier has first-stage voltage gain of 20 and second stage voltage gain of 400. Find the total decibel gain. **[78 db]**

6. A multistage amplifier consists of three stages ; the voltage gain of stages are 60, 100 and 160. Calculate the overall gain in *db*. **[119.64db]**

7. A multistage amplifier consists of three stages ; the voltage gains of the stages are 30, 50 and 60. Calculate the overall gain in *db*. **[99.1db]**

8. In an *RC* coupled amplifier, the mid-frequency gain is 2000. What will be its value at upper and lower cut-off frequencies? **[1414]**

9. A three-stage amplifier employs *RC* coupling. The voltage gain of each stage is 50 and $R_C = 5\ \text{k}\Omega$ for each stage. If input impedance of each stage is 2 kΩ, find the overall decibel voltage gain. **[80 db]**

10. We are to match a 16Ω speaker load to an amplifier so that the effective load resistance is 10 kΩ. What should be the transformer turn ratio ? **[25]**

11. Determine the necessary transformer turn ratio for transferring maximum power to a 50 ohm load from a source that has an output impedance of 5 kΩ. Also find the voltage across the external load if the terminal voltage of the source is 10V r.m.s. **[10, 1V]**

12. We are to match an 8Ω speaker load to an amplifier so that the effective load resistance is 8 kΩ. What should be the transformer turn ratio ? **[10]**

Discussion Questions

1. Why does *RC* coupling give constant gain over mid-frequency range ?
2. Why does transformer coupling give poor frequency response ?
3. How will you get frequency response comparable to *RC* coupling in a transformer coupling ?
4. Why is transformer coupling used in the final stage of a multistage amplifier ?
5. Why do you avoid *RC* or transformer coupling for amplifying extremely low frequency signals ?
6. Why do you prefer to express the gain in *db* ?

12

Transistor Audio Power Amplifiers

12.1 Transistor Audio Power Amplifier
12.2 Small-Signal and Large-Signal Amplifiers
12.3 Output Power of Amplifier
12.4 Difference Between Voltage and Power Amplifiers
12.5 Performance Quantities of Power Amplifiers
12.6 Classification of Power Amplifiers
12.7 Expression for Collector Efficiency
12.8 Maximum Collector Efficiency of Series – Fed Class A Amplifier
12.9 Maximum Collector Efficiency of Transformer Coupled Class A Power Amplifier
12.10 Important Points About Class A Power Amplifier
12.11 Thermal Runaway
12.12 Heat Sink
12.13 Mathematical Analysis
12.14 Stages Of A Practical Power Amplifier
12.15 Driver Stage
12.16 Output Stage
12.17 Push-Pull Amplifier
12.18 Maximum Efficiency for Class B Power Amplifier
12.19 Complementary-Symmetry Amplifier

INTRODUCTION

A practical amplifier always consists of a number of stages that amplify a weak signal until sufficient power is available to operate a loudspeaker or other output device. The first few stages in this multistage amplifier have the function of only voltage amplification. However, the last stage is designed to provide maximum power. This final stage is known as *power stage*.

The term audio means the range of frequencies which our ears can hear. The range of human hearing extends from 20 Hz to 20 kHz. Therefore, audio amplifiers amplify electrical signals that have a frequency range corresponding to the range of human hearing *i.e.* 20 Hz to 20 kHz. Fig. 12.1 shows the block diagram of an audio amplifier. The early stages build up the voltage level of the signal while the last stage builds up power to a level sufficient to operate the loudspeaker. In this chapter, we shall talk about the final stage in a multistage amplifier—the power amplifier.

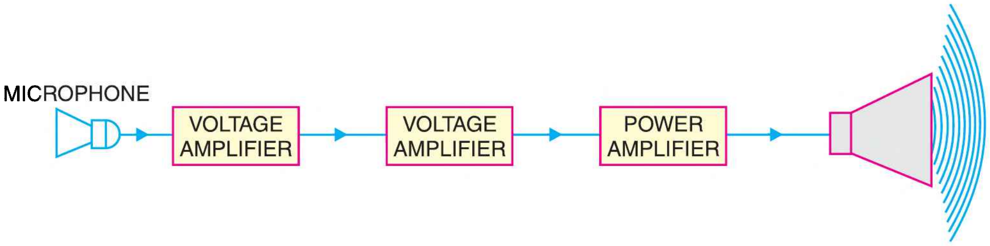


Fig. 12.1

12.1 Transistor Audio Power Amplifier

A transistor amplifier which raises the power level of the signals that have audio frequency range is known as **transistor audio power amplifier.**

In general, the last stage of a multistage amplifier is the *power stage.* The power amplifier differs from all the previous stages in that here a concentrated effort is made to obtain maximum output power. A transistor that is suitable for power amplification is generally called a *power transistor.* It differs from other transistors mostly in size ; it is considerably larger to provide for handling the great amount of power. Audio power amplifiers are used to deliver a large amount of power to a low resistance load. Typical load values range from 300Ω (for transmission antennas) to 8Ω (for loudspeakers). Although these load values do not cover every possibility, they do illustrate the fact that audio power amplifiers usually drive low-resistance loads. The typical power output rating of a power amplifier is 1W or more.

Transistor Audio Power Amplifiers

12.2 Small-Signal and Large-Signal Amplifiers

The input signal to a multistage amplifier is generally small (a few mV from a cassette or CD or a few μV from an antenna). Therefore, the first few stages of a multistage amplifier handle small signals and have the function of only voltage amplification. However, the last stage handles a large signal and its job is to produce a large amount of power in order to operate the output device (*e.g.* speaker).

(*i*) **Small-signal amplifiers.** Those amplifiers which handle small input a.c. signals (a few μV or a few mV) are called *small-signal amplifiers.* Voltage amplifiers generally fall in this class. The small-signal amplifiers are designed to operate over the linear portion of the output characteristics. Therefore, the transistor parameters such as current gain, input impedance, output impedance etc. do not change as the amplitude of the signal changes. Such amplifiers amplify the signal with little or no distortion.

(*ii*) **Large-signal amplifiers.** Those amplifiers which handle large input a.c. signals (a few volts) are called *large-signal amplifiers.* Power amplifiers fall in this class. The large-signal amplifiers are designed to provide a large amount of a.c. power output so that they can operate the output device *e.g.* a speaker. The main features of a large-signal amplifier or power amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling and the impedance matching to the output device. It may be noted that all large-signal amplifiers are not necessarily power amplifiers but it is safe to say that most are. In general, where amount of power involved is 1W or more, the amplifier is termed as *power amplifier.*

12.3 Output Power of Amplifier

An amplifier converts d.c. power drawn from d.c. supply V_{CC} into a.c. output power. The output power is always less than the input power because losses occur in the various resistors present in the circuit. For example, consider the R-C coupled amplifier circuit shown in Fig. 12.2. The currents are flowing through various resistors causing I^2R loss. Thus power loss in R_1 is $I_1^2 R_1$, power loss in R_C is $I_C^2 R_C$, power loss in R_E is $I_E^2 R_E$ and so on. All these losses appear as heat. Therefore, losses occuring in an amplifier not only decrease the efficiency but they also increase the temperature of the circuit.

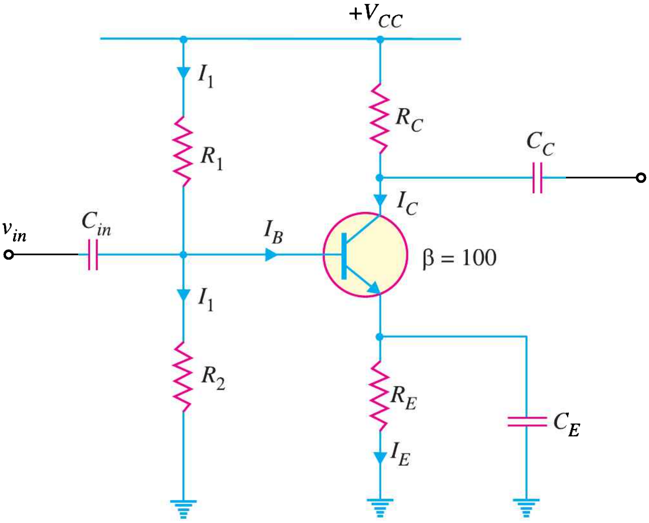


Fig. 12.2

When load R_L is connected to the amplifier, A.C. output power, $P_O = \dfrac{V_L^2}{R_L}$

where V_L = r.m.s. value of load voltage

Example 12.1. *If in Fig. 12.2; R_1 = 10 kΩ ; R_2 = 2.2 kΩ ; R_C = 3.6 kΩ ; R_E = 1.1. kΩ and V_{CC} = + 10 V, find the d.c. power drawn from the supply by the amplifier.*

Solution. The current I_1 flowing through R_1 also flows through R_2 (a reasonable assumption because I_B is small).

$$I_1 = \frac{V_{CC}}{R_1 + R_2} = \frac{10\text{V}}{10\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{10\text{V}}{12.2\text{ k}\Omega} = 0.82\text{ mA}$$

D.C. voltage across R_2, $V_2 = I_1 R_2 = 0.82\text{ mA} \times 2.2\text{ k}\Omega = 1.8\text{V}$

D.C. voltage across R_E, $V_E = V_2 - V_{BE} = 1.8\text{V} - 0.7\text{V} = 1.1\text{V}$

D.C. emitter current, $I_E = V_E/R_E = 1.1\text{V}/1.1\text{ k}\Omega = 1\text{ mA}$

$\therefore \quad I_C \simeq I_E = 1\text{ mA}$

Total d.c current I_T drawn from the supply is

$$I_T = I_C + I_1 = 1\text{ mA} + 0.82\text{ mA} = 1.82\text{ mA}$$

∴ D.C. power drawn from the supply is

$$P_{dc} = V_{CC} I_T = 10\text{V} \times 1.82\text{ mA} = \mathbf{18.2\text{ mW}}$$

Example 12.2. *Determine the a.c. load power for the circuit shown in Fig. 12.3.*

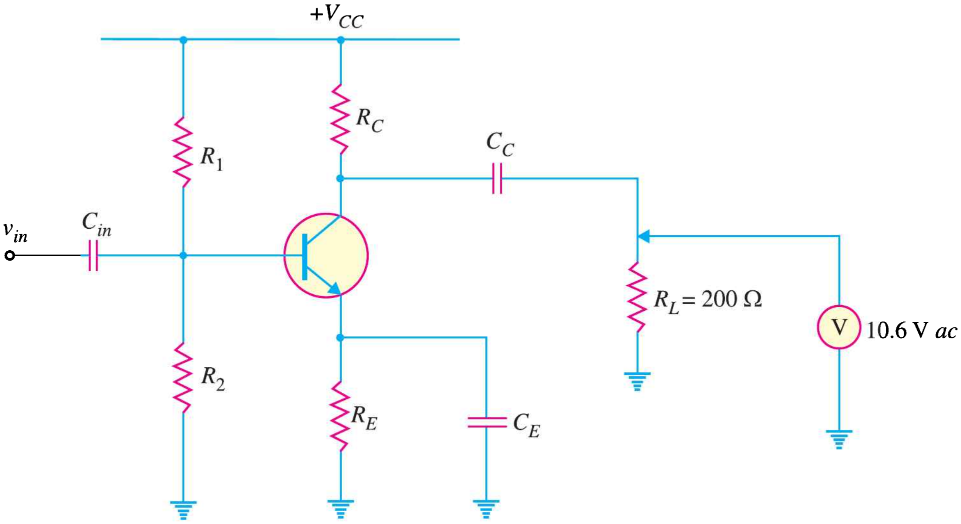


Fig. 12.3

Solution. The reading of a.c. voltmeter is 10.6V. Since a.c. voltmeters read r.m.s. voltage, we have,

$$\text{A.C. output power, } P_O = \frac{V_L^2}{R_L} = \frac{(10.6)^2}{200\ \Omega} = \mathbf{561.8\ mW}$$

Example 12.3. *In an RC coupled power amplifier, the a.c. voltage across load R_L (= 100 Ω) has a peak- to-peak value of 18V. Find the maximum possible a.c. load power.*

Solution. The peak-to-peak voltage, V_{PP} = 18V. Therefore, peak voltage (or maximum voltage) = $V_{PP}/2$ and the r.m.s value, $V_L = V_{PP}/2\sqrt{2}$.

$$\therefore \qquad P_{O\,(max)} = \frac{V_L^2}{R_L} = \frac{(V_{PP}/2\sqrt{2})^2}{R_L} = \frac{V_{PP}^2}{8\ R_L}$$

Here $\qquad V_{PP}$ = 18V and R_L = 100Ω

$$\therefore \qquad P_{O\,(max)} = \frac{(18V)^2}{(8 \times 100)\ \Omega} = 405 \times 10^{-3}\ \text{W} = \mathbf{405\ mW}$$

12.4 Difference Between Voltage and Power Amplifiers

The distinction between voltage and power amplifiers is somewhat artificial since useful power (*i.e.* product of voltage and current) is always developed in the load resistance through which current flows. The difference between the two types is really one of degree; it is a question of how much voltage and how much power. A voltage amplifier is designed to achieve maximum voltage amplification. It is, however, not important to raise the power level. On the other hand, a power amplifier is designed to obtain maximum output power.

1. Voltage amplifier. The voltage gain of an amplifier is given by :

$$A_v = \beta \times \frac{R_C}{R_{in}}$$

In order to achieve high voltage amplification, the following features are incorporated in such amplifiers :

(*i*) The transistor with high β (>100) is used in the circuit. In other words, those transistors are employed which have thin base.

(*ii*) The input resistance R_{in} of the transistor is sought to be quite low as compared to the collector load R_C.

(*iii*) A relatively high load R_C is used in the collector. To permit this condition, voltage amplifiers are always operated at low collector currents (≃ 1 mA). If the collector current is small, we can use large R_C in the collector circuit.

2. Power amplifier. A power amplifier is required to deliver a large amount of power and as such it has to handle large current. In order to achieve high power amplification, the following features are incorporated in such amplifiers :

(*i*) The size of power transistor is made considerably larger in order to dissipate the heat produced in the transistor during operation.

(*ii*) The base is made thicker to handle large currents. In other words, transistors with comparatively smaller β are used.

(*iii*) Transformer coupling is used for impedance matching.

The comparison between voltage and power amplifiers is given below in the tabular form :

S. No.	Particular	Voltage amplifier	Power amplifier
1.	β	High (> 100)	low (5 to 20)
2.	R_C	High (4 – 10 kΩ)	low (5 to 20 Ω)
3.	*Coupling*	usually $R - C$ coupling	Invariably transformer coupling
4.	*Input voltage*	low (a few mV)	High (2 – 4 V)
5.	*Collector current*	low (≃ 1 mA)	High (> 100 mA)
6.	*Power output*	low	high
7.	*Output impedance*	High (≃ 12 kΩ)	low (200 Ω)

Example 12.4. *A power amplifier operated from 12V battery gives an output of 2W. Find the maximum collector current in the circuit.*

Solution.

Let I_C be the maximum collector current.

$$\text{Power} = \text{battery voltage} \times \text{collector current}$$

$$\text{or} \quad 2 = 12 \times I_C$$

$$\therefore \quad I_C = \frac{2}{12} = \frac{1}{6}\text{ A} = \mathbf{166.7\ mA}$$

This example shows that a power amplifier handles large power as well as large current.

Example 12.5. *A voltage amplifier operated from a 12 V battery has a collector load of 4 kΩ. Find the maximum collector current in the circuit.*

Solution.

The maximum collector current will flow when the whole battery voltage is dropped across R_C.

$$\therefore \quad \text{Max. collector current} = \frac{\text{battery voltage}}{\text{collector load}} = \frac{12\text{ V}}{4\text{ k}\Omega} = \mathbf{3\ mA}$$

This example shows that a voltage amplifier handles small current.

Example 12.6. *A power amplifier supplies 50 W to an 8-ohm speaker. Find* (*i*) *a.c. output voltage* (*ii*) *a.c. output current.*

Solution.

(*i*) $P = V^2/R$

∴ a.c. output voltage, $V = \sqrt{PR} = \sqrt{50 \times 8} = \mathbf{20\ V}$

(*ii*) a.c. output current, $I = V/R = 20/8 = \mathbf{2.5\ A}$

12.5 Performance Quantities of Power Amplifiers

As mentioned previously, the prime objective for a power amplifier is to obtain maximum output power. Since a transistor, like any other electronic device has voltage, current and power dissipation limits, therefore, the criteria for a power amplifier are : ***collector efficiency, distortion*** and ***power dissipation capability.***

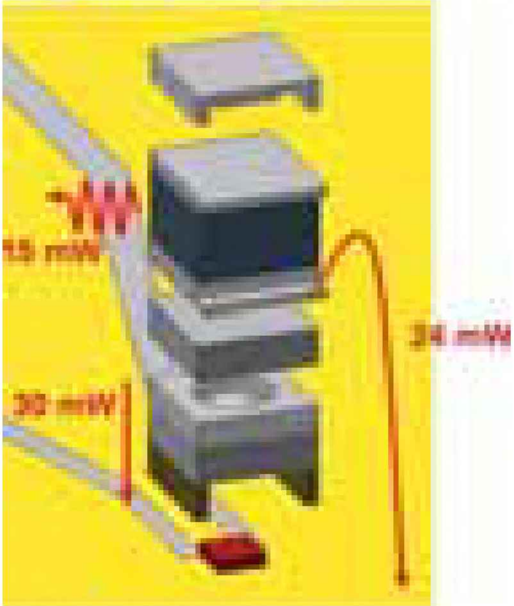
(*i*) **Collector efficiency.** The main criterion for a power amplifier is not the power gain rather it is the maximum a.c. power output. Now, an amplifier converts d.c. power from supply into a.c. power output. Therefore, the ability of a power amplifier to convert d.c. power from supply into a.c. output power is a measure of its effectiveness. This is known as collector efficiency and may be defined as under :

The ratio of a.c. output power to the zero signal power (i.e. d.c. power) supplied by the battery of a power amplifier is known as **collector efficiency.**

Collector efficiency means as to how well an amplifier converts d.c. power from the battery into a.c. output power. For instance, if the d.c. power supplied by the battery is 10W and a.c. output power is 2W, then collector efficiency is 20%. The greater the collector efficiency, the larger is the a.c. power output. It is obvious that for power amplifiers, maximum collector efficiency is the desired goal.

(*ii*) **Distortion.** *The change of output wave shape from the input wave shape of an amplifier is known as* **distortion.**

A transistor like other electronic devices, is essentially a non-linear device. Therefore, whenever a signal is applied to the input of the transistor, the output signal is not exactly like the input signal *i.e.* distortion occurs. Distortion is not a problem for small signals (*i.e.* voltage amplifiers) since transistor is a linear device for small variations about the operating point. However, a power amplifier handles large signals and, therefore, the problem of distortion immediately arises. For the comparison of two power amplifiers, the one which has the less distortion is the better. We shall discuss the method of reducing distortion in amplifiers in the chapter of negative feedback in amplifiers.



Power Dissipation Channels in a Microfabricated Atomic Clock

(*iii*) **Power dissipation capability.** *The ability of a power transistor to dissipate heat is known as* **power dissipation capability.**

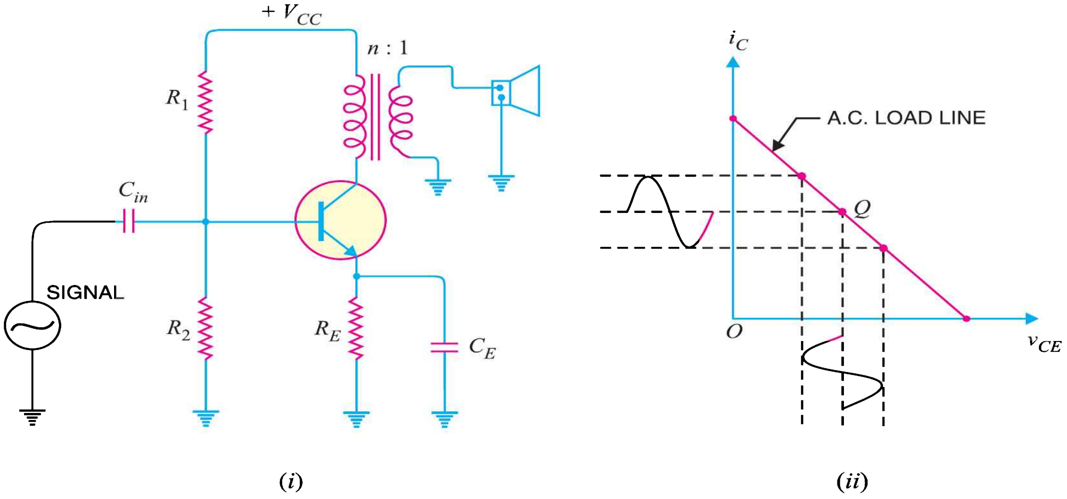
As stated before, a power transistor handles large currents and heats up during operation. As any temperature change influences the operation of transistor, therefore, the transistor must dissipate this heat to its surroundings. To achieve this, generally a *heat sink* (a metal case) is attached to a power transistor case. The increased surface area allows heat to escape easily and keeps the case temperature of the transistor within permissible limits.

12.6 Classification of Power Amplifiers

Transistor power amplifiers handle large signals. Many of them are driven so hard by the input large signal that collector current is either cut-off or is in the saturation region during a large portion of the input cycle. Therefore, such amplifiers are generally classified according to their mode of operation *i.e.* the portion of the input cycle during which the collector current is expected to flow. On this basis, they are classified as :

(*i*) class *A* power amplifier (*ii*) class *B* power amplifier (*iii*) class *C* power amplifier

(*i*) **Class A power amplifier.** *If the collector current flows at all times during the full cycle of the signal, the power amplifier is known as* **class A power amplifier.**



(*i*) (*ii*)

Fig. 12.4

Obviously, for this to happen, the power amplifier must be biased in such a way that no part of the signal is cut off. Fig. 12.4 (*i*) shows circuit of class *A* power amplifier. Note that collector has a transformer as the load which is most common for all classes of power amplifiers. The use of transformer permits impedance matching, resulting in the transference of maximum power to the load *e.g.* loudspeaker.

Fig. 12.4 (*ii*) shows the class *A* operation in terms of *a.c.* load line. The operating point *Q* is so selected that collector current flows at all times throughout the full cycle of the applied signal. As the output wave shape is exactly similar to the input wave shape, therefore, such amplifiers have least distortion. However, they have the disadvantage of low power output and low collector efficiency (about 35%).

(*ii*) **Class B power amplifier.** *If the collector current flows only during the positive half-cycle of the input signal, it is called a* **class B power amplifier.**

In class *B* operation, the transistor bias is so adjusted that zero signal collector current is zero *i.e.* no biasing circuit is needed at all. During the positive half-cycle of the signal, the input circuit is forward biased and hence collector current flows. However, during the negative half-cycle of the signal, the input circuit is reverse biased and no collector current flows. Fig. 12.5 shows the class *B* operation in terms of a.c. load line. Obviously, the operating point *Q* shall be located at collector cut off voltage. It is easy to see that output from a class *B* amplifier is amplified half-wave rectification.

In a class *B* amplifier, the negative half-cycle of the signal is cut off and hence a severe distortion occurs. However, class *B* amplifiers provide higher power output and collector efficiency (50 – 60%). Such amplifiers are mostly used for power amplification in push-pull arrangement. In such an arrangement, 2 transistors are used in class *B* operation. One transistor amplifies the positive half-cycle of the signal while the other amplifies the negative half-cycle.

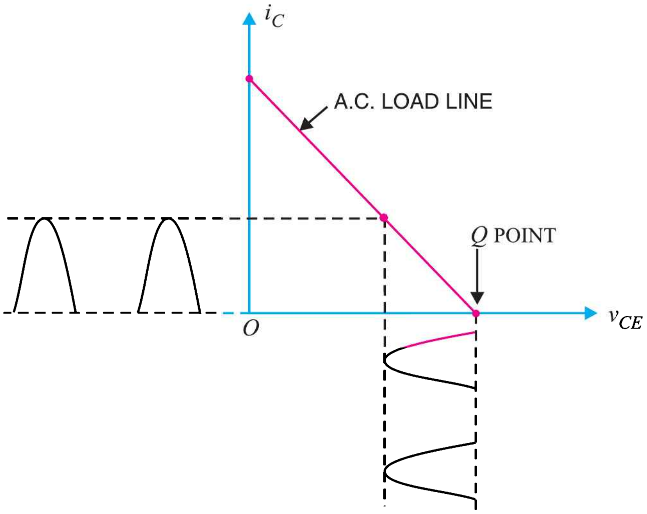


Fig. 12.5

(*iii*) **Class C power amplifier.** *If the collector current flows for less than half-cycle of the input signal, it is called* **class C power amplifier.**

In class *C* amplifier, the base is given some negative bias so that collector current does not flow just when the positive half-cycle of the signal starts. Such amplifiers are never used for power amplification. However, they are used as tuned amplifiers *i.e.* to amplify a narrow band of frequencies near the resonant frequency.

12.7 Expression for Collector Efficiency

For comparing power amplifiers, collector efficiency is the main criterion. The greater the collector efficiency, the better is the power amplifier.

Now, Collector efficiency, $\eta = \dfrac{\text{a.c. power output}}{\text{d.c. power input}}$

$$= \frac{P_o}{P_{dc}}$$

where $^*P_{dc} = V_{CC} I_C$

$$P_o = V_{ce} I_c$$

where V_{ce} is the *r.m.s.* value of signal output voltage and I_c is the *r.m.s.* value of output signal current. In terms of peak-to-peak values (which are often convenient values in load-line work), the a.c. power output can be expressed as :

---

* Note that d.c. input power to the collector circuit of power amplifier is the product of collector supply V_{CC} (and not the collector-emitter voltage) and the average (i.e. d.c.) collector current I_C.

$$*\ P_o = [(0.5 \times 0.707)\, v_{ce\,(p-p)}]\,[(0.5 \times 0.707)\, i_{c\,(p-p)}]$$

$$= \frac{v_{ce(p-p)} \times i_{c(p-p)}}{8}$$

$$\therefore \quad \text{Collector } \eta = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8\, V_{CC}\, I_C}$$

12.8. Maximum Collector Efficiency of Series-Fed Class A Amplifier

Fig. 12.6 (*i*) shows a **series – fed class *A* amplifier. This circuit is seldom used for power amplification due to its poor collector efficiency. Nevertheless, it will help the reader to understand the class *A* operation. The d.c. load line of the circuit is shown in Fig. 12.6 (*ii*). When an *ac* signal is applied to the amplifier, the output current and voltage will vary about the operating point Q. In order to achieve the maximum symmetrical swing of current and voltage (to achieve maximum output power), the Q point should be located at the centre of the *dc* load line. In that case, operating point is $I_C = V_{CC}/2R_C$ and $V_{CE} = V_{CC}/2$.

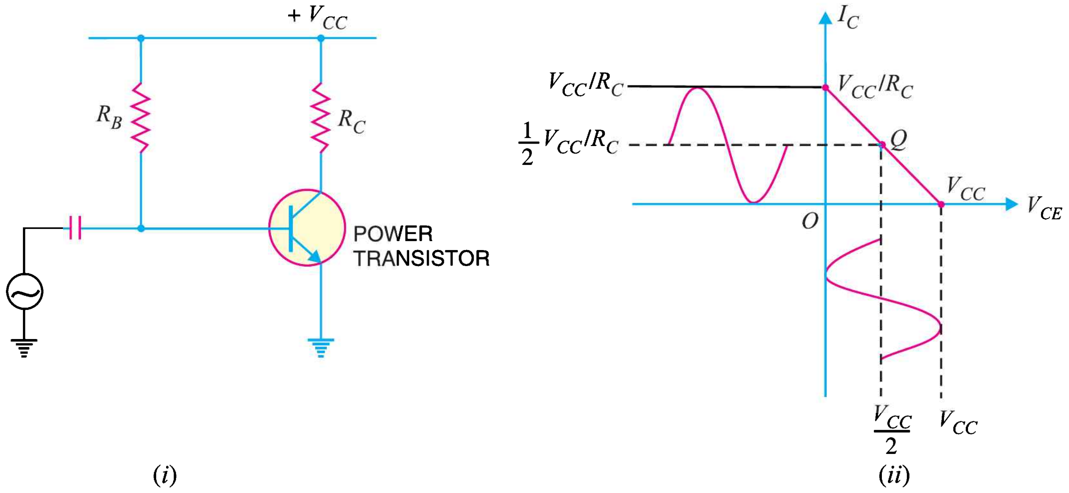


Fig. 12.6

$$\text{Maximum } v_{ce\,(p-p)} = V_{CC}$$

$$\text{Maximum } i_{c\,(p-p)} = V_{CC}/R_C$$

$$\text{Max. } ac \text{ output power,} \quad P_{o\,(max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8} = \frac{V_{CC} \times V_{CC}/R_C}{8} = \frac{V_{CC}^2}{8 R_C}$$

$$\text{D.C. power supplied, } P_{dc} = V_{CC}\, I_C = V_{CC}\left(\frac{V_{CC}}{2 R_C}\right) = \frac{V_{CC}^2}{2 R_C}$$

$$\therefore \quad \text{Maximum collector } \eta = \frac{P_{o(max)}}{P_{dc}} \times 100 = \frac{V_{CC}^2/8 R_C}{V_{CC}^2/2 R_C} \times 100 = 25\%$$

---

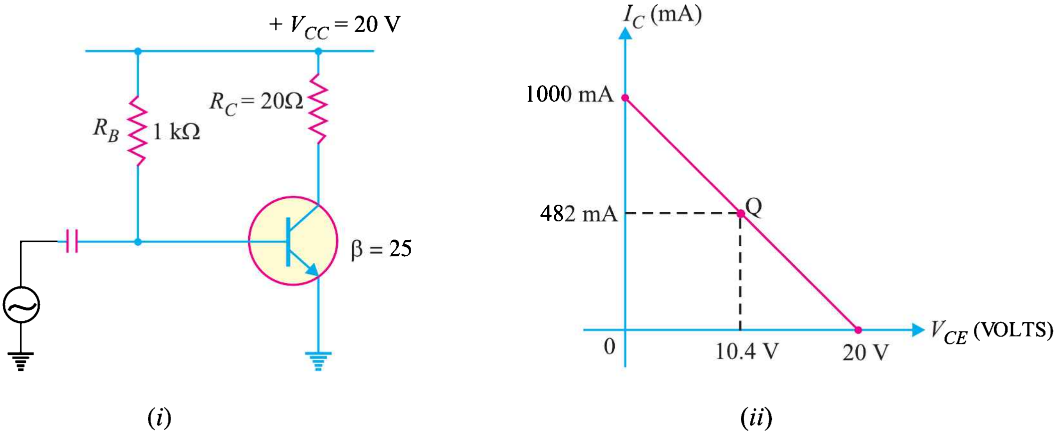
* $$\text{r.m.s. value} = \frac{1}{2}\left[\frac{\text{peak-to-peak value}}{\sqrt{2}}\right]$$

$$= 0.5 \times 0.707 \times \text{peak-to-peak value}$$

** Note that the input to this circuit is a large signal and that transistor used is a power transistor.

Thus the maximum collector efficiency of a class *A* series-fed amplifier is 25%. In actual practice, the collector efficiency is far less than this value.

Example 12.7. *Calculate the* (*i*) *output power* (*ii*) *input power and* (*iii*) *collector efficiency of the amplifier circuit shown in Fig. 12.7* (*i*). *It is given that input voltage results in a base current of 10 mA peak.*



(*i*) (*ii*)

Fig. 12.7

Solution. First draw the *d.c.* load line by locating the two end points *viz.*, $I_{C\,(sat)} = V_{CC}/R_C = 20\text{ V}/20\ \Omega = 1\text{ A} = 1000\text{ mA}$ and $V_{CE} = V_{CC} = 20$ V as shown in Fig. 12.7 (*ii*). The operating point *Q* of the circuit can be located as under :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{1\,\text{k}\Omega} = 19.3\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 25\,(19.3\text{ mA}) = 482\text{ mA}$$

Also $$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - (482\text{ mA})\,(20\ \Omega) = 10.4\text{ V}$$

The operating point *Q* (10.4 V, 482 mA) is shown on the d.c. load line.

(*i*) $i_c\text{-}(peak) = \beta\, i_b\,(peak) = 25 \times (10\text{ mA}) = 250\text{ mA}$

$$\therefore \quad P_{o\,(ac)} = \frac{i_c^2(peak)}{2} R_C = \frac{(250 \times 10^{-3})^2}{2} \times 20 = \mathbf{0.625\ W}$$

(*ii*) $P_{dc} = V_{CC}\, I_C = (20\text{ V})\,(482 \times 10^{-3}) = \mathbf{9.6\ W}$

(*iii*) $$\text{Collector } \eta = \frac{P_o(ac)}{P_{dc}} \times 100 = \frac{0.625}{9.6} \times 100 = \mathbf{6.5\ \%}$$

12.9. Maximum Collector Efficiency of Transformer Coupled Class A Power Amplifier

In class *A* power amplifier, the load can be either connected directly in the collector or it can be transformer coupled. The latter method is often preferred for two main reasons. First, transformer coupling permits impedance matching and secondly it keeps the d.c. power loss small because of the small resistance of the transformer primary winding.

Fig. 12.8 (*i*) shows the transformer coupled class *A* power amplifier. In order to determine maximum collector efficiency, refer to the output characteristics shown in Fig. 12.8 (*ii*). Under zero signal conditions, the effective resistance in the collector circuit is that of the primary winding of the transformer. The primary resistance has a very small value and is assumed zero. Therefore, d.c. load line is a vertical line rising from V_{CC} as shown in Fig. 12.8 (*ii*). When signal is applied, the collector current will vary about the operating point Q.

In order to get maximum a.c. power output (and hence maximum collector η), the peak value of collector current due to signal alone should be equal to the zero signal collector current I_C. In terms of a.c. load line, the operating point Q should be located at the centre of a.c. load line.

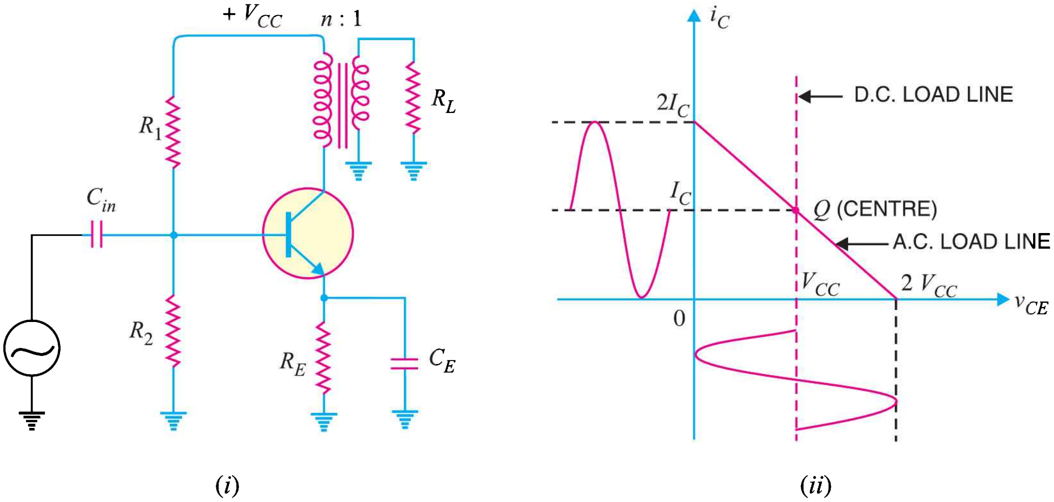


Fig. 12.8

During the peak of the positive half-cycle of the signal, the total collector current is 2 I_C and $v_{ce} = 0$. During the negative peak of the signal, the collector current is zero and *$v_{ce} = 2V_{CC}$.

∴ Peak-to-peak collector-emitter voltage is

$$v_{ce\,(p-p)} = 2V_{CC}$$

Peak-to-peak collector current, $i_{c\,(p-p)} = 2\,I_C$

$$= \frac{v_{ce(p-p)}}{R'_L} = \frac{2V_{CC}}{R'_L}$$

where R'_L is the reflected value of load R_L and appears in the primary of the transformer. If $n\ (= N_p/N_s)$ is the turn ratio of the transformer, then, $R'_L = n^2\,R_L$.

$$\text{d.c. power input, } P_{dc} = V_{CC}\,I_C$$

$$= I_C^2 R'_L \qquad (\because\ V_{CC} = I_C R'_L)$$

$$\text{Max.a.c. output power, } P_{o\,(max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8}$$

$$= \frac{2V_{CC} \times 2\,I_C}{8}$$

$$= \frac{1}{2}\,V_{CC} I_C \qquad ...(i)$$

$$= \frac{1}{2}\,I_C^2 R'_L \qquad (\because\ V_{CC} = I_C R'_L)$$

---

* This occurs at the negative peak of the signal. Under such conditions, the voltage across transformer primary is V_{CC} but in such a direction so as to reinforce the supply.

∴ $v_{ce} = 2V_{CC}$

$$\therefore \qquad \text{Max. collector } \eta = \frac{P_{o\,(max)}}{P_{dc}} \times 100$$

$$= \frac{(1/2)\, I_C^2\, R'_L}{I_C^2\, R'_L} \times 100 = 50\%$$

12.10 Important Points About Class A Power Amplifier

(*i*) A *transformer coupled class *A* power amplifier has a maximum collector efficiency of 50% *i.e.*, maximum of 50% d.c. supply power is converted into a.c. power output. In practice, the efficiency of such an amplifier is less than 50% (about 35%) due to power losses in the output transformer, power dissipation in the transistor etc.

(*ii*) The power dissipated by a transistor is given by :

$$P_{dis} = P_{dc} - P_{ac}$$

where P_{dc} = available d.c. power

P_{ac} = available a.c. power

Clearly, in class *A* operation, the transistor must dissipate less heat when signal is applied and therefore runs cooler.

(*iii*) When no signal is applied to a class *A* power amplifier, $P_{ac} = 0$.

$$\therefore \qquad P_{dis} = P_{dc}$$

Thus in class *A* operation, maximum power dissipation in the transistor occurs under zero signal conditions. Therefore, the power dissipation capability of a power transistor (for class *A* operation) must be atleast equal to the zero signal rating. For example, if the zero signal power dissipation of a transistor is 1 W, then transistor needs a rating of atleast 1W. If the power rating of the transistor is less than 1 W, it is likely to be damaged.

(*iv*) When a class *A* power amplifier is used in the final stage, it is called **single ended class A power amplifier.**

Example 12.8. *A power transistor working in class A operation has zero signal power dissipation of 10 watts. If the a.c. output power is 4 watts, find :*

(*i*) *collector efficiency* (*ii*) *power rating of transistor*

Solution.

Zero signal power dissipation, P_{dc} = 10 W

a.c. power output, P_o = 4 W

(*i*) $$\text{Collector efficiency} = \frac{P_o}{P_{dc}} \times 100 = \frac{4}{10} \times 100 = \mathbf{40\%}$$

(*ii*) The zero signal power represents the worst case *i.e.* maximum power dissipation in a transistor occurs under zero signal conditions.

∴ Power rating of transistor = **10 W**

It means to avoid damage, the transistor must have a power rating of atleast 10 W.

Example 12.9. *A class A power amplifier has a transformer as the load. If the transformer has a turn ratio of 10 and the secondary load is 100 Ω, find the maximum a.c. power output. Given that zero signal collector current is 100 mA.*

Solution.

Secondary load, $R_L = 100\,\Omega$

---

* However, resistance coupled class A power amplifier has a maximum collector efficiency of 25%.

Transformer turn ratio, $n = 10$

Zero signal collector current, $I_C = 100\text{ mA}$

Load as seen by the primary of the transformer is

$$R'_L = n^2 R_L = (10)^2 \times 100 = 10{,}000\ \Omega$$

$$\therefore \quad \text{Max. a.c. power output} = \frac{1}{2} I_C^2 R'_L = \frac{1}{2}\left(\frac{100}{1000}\right)^2 \times 10{,}000$$

$$= \mathbf{50\ W}$$

Example 12.10. *A class A transformer coupled power amplifier has zero signal collector current of 50 mA. If the collector supply voltage is 5 V, find (i) the maximum a.c. power output (ii) the power rating of transistor (iii) the maximum collector efficiency.*

Solution.

(*i*) Max. a.c. power output, $P_{o\,(max)} = \dfrac{V_{CC}\, I_C}{2}$ ...See Art. 12.9

$$= \frac{(5\text{ V}) \times (50\text{ mA})}{2} = \mathbf{125\ mW}$$

(***ii***) D.C input power, $P_{dc} = V_{CC}\, I_C$

$$= (5\text{ V}) \times (50\text{ mA}) = 250\text{ mW}$$

Since the maximum power is dissipated in the zero signal conditions,

$\therefore$ Power rating of transistor $= \mathbf{250\ mW}$

The reader may note that in class *A* operation :

$$P_{o(max)} = \frac{P_{dis}}{2}$$

or $P_{dis} = 2\,P_{o\,(max)}$

It means that power rating of the transistor is twice as great as the maximum a.c. output power. For example, if a transistor dissipates 3 W under no signal conditions, then maximum a.c. output power it can deliver is 1.5 W.

(***iii***) Max. collector $\eta = \dfrac{P_{o\,(max)}}{P_{dc}} \times 100 = \dfrac{125\text{ mW}}{250\text{ mW}} \times 100 = \mathbf{50\%}$

Example 12.11. *In a certain transistor amplifier, $i_{c\,(max)} = 160$ mA, $i_{c\,(min)} = 10$mA, $v_{ce\,(max)} = 12$V and $v_{ce\,(min)} = 2$V. Calculate the a.c. output power.*

Solution.

$$\text{A.C. output power, } P_o = \frac{v_{ce\ (p-p)} \times i_{c\,(p-p)}}{8}$$

Here $v_{ce\,(p-p)} = 12\text{V} - 2\text{V} = 10\text{V}$; $i_{c\,(p-p)} = 160\text{ mA} - 10\text{ mA} = 150\text{ mA}$

$$\therefore \quad P_o = \frac{10\text{ V} \times 150\text{ mA}}{8} = \mathbf{187.5\ mW}$$

Example 12.12. *A power transistor working in class A operation is supplied from a 12-volt battery. If the maximum collector current change is 100 mA, find the power transferred to a 5 Ω loudspeaker if it is :*

(*i*) *directly connected in the collector*

(*ii*) *transformer-coupled for maximum power transference*

Find the turn ratio of the transformer in the second case.

Solution.

Max. collector current change, $\Delta I_C = 100\,\text{mA}$

Max. collector-emitter voltage change is

$$\Delta V_{CE} = 12\,\text{V}$$

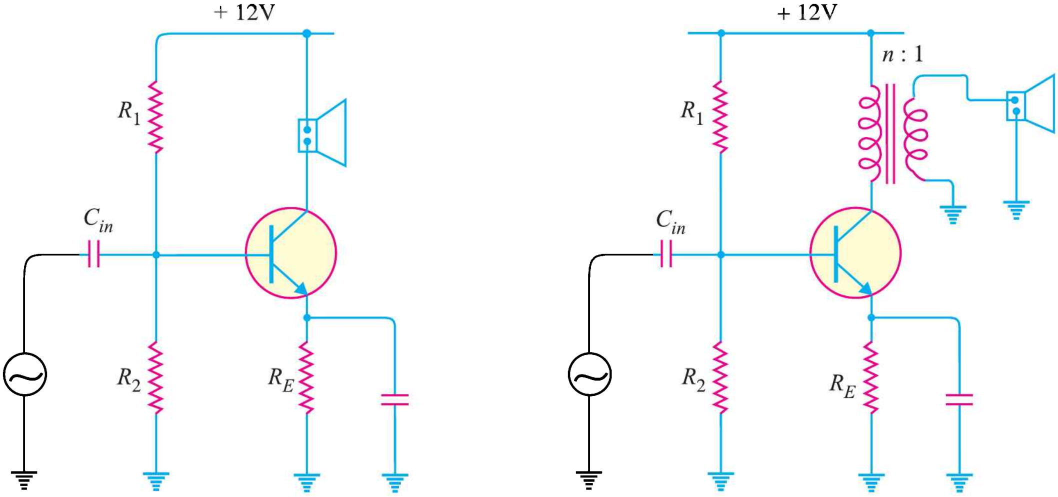
Loudspeaker resistance, $R_L = 5\,\Omega$

(*i*) **Loudspeaker directly connected.** Fig. 12.9 (*i*) shows the circuit of class *A* power amplifier with loudspeaker directly connected in the collector.

$$\text{Max. voltage across loudspeaker} = \Delta I_C \times R_L = 100\text{ mA} \times 5\ \Omega = 0.5\text{ V}$$

$$\text{Power developed in the loudspeaker} = 0.5\text{ V} \times 100\text{ mA}$$

$$= 0.05\text{ W} = \mathbf{50\ mW}$$



(*i*) (*ii*)

Fig. 12.9

Therefore, when loudspeaker is directly connected in the collector, only 50 mW of power is transferred to the loudspeaker.

(*ii*) **Loudspeaker transformer coupled.** Fig. 12.9 (*ii*) shows the class *A* power amplifier with speaker transformer coupled. As stated before, for impedance matching, step-down transformer is used.

$$\text{Output impedance of transistor} = \frac{\Delta V_{CE}}{\Delta I_C} = 12\text{ V}/100\text{ mA} = 120\ \Omega$$

In order to transfer maximum power, the primary resistance should be 120 Ω.

Now, load R'_L as seen by the primary is

$$R'_L = n^2 R_L$$

or $$120 = n^2 R_L$$

or $$n^2 = \frac{120}{5}$$

$\therefore$ $$\text{Turn ratio, } n = \sqrt{\frac{120}{5}} = \mathbf{4.9}$$

Transformer secondary voltage

$$= \frac{\text{Primary voltage}}{n} = 12/4.9 = 2.47 \text{ V}$$

$$\text{Load current, } I_L = \frac{2.47 \text{ V}}{5 \ \Omega} = 0.49 \text{ A}$$

Power transferred to the loudspeaker

$$= I_L^2 R_L$$

$$= (0.49)^2 \times 5 = 1.2 \text{ W} = \mathbf{1200 \ mW}$$

It is clear that by employing transformer coupling, we have been able to transfer a large amount of power (1200 mW) to the speaker. The main consideration in power amplifiers is the maximum power output and, therefore, transformer coupling is invariably used.

Example 12.13. *A common emitter class A transistor power amplifier uses a transistor with* $\beta = 100$. *The load has a resistance of 81.6 Ω, which is transformer coupled to the collector circuit. If the peak values of collector voltage and current are 30 V and 35 mA respectively and the corresponding minimum values are 5 V and 1 mA respectively, determine :*

(*i*) *the approximate value of zero signal collector current*

(*ii*) *the zero signal base current*

(*iii*) P_{dc} *and* P_{ac} (*iv*) *collector efficiency* (*v*) *turn ratio of the transformer.*

Solution.

In an ideal case, the minimum values of $v_{CE(min)}$ and $i_{C(min)}$ are zero. However, in actual practice, such ideal conditions cannot be realised. In the given problem, these minimum values are 5 V and 1mA respectively as shown in Fig. 12.10.

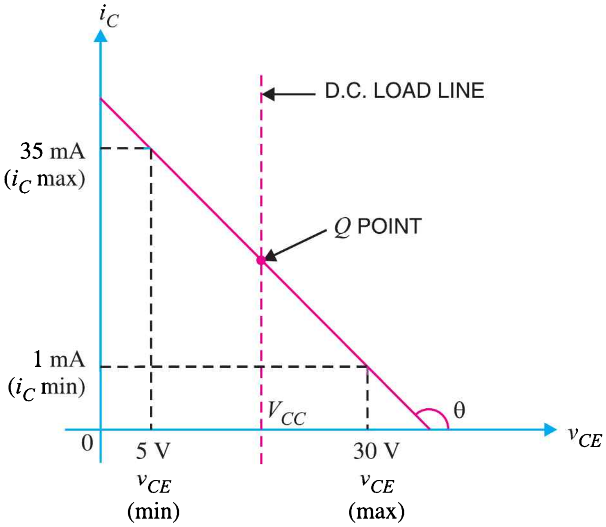


Fig. 12.10

(*i*) The zero signal collector current is approximately half-way between the maximum and minimum values of collector current *i.e.*

$$\text{Zero signal } I_C = \frac{35-1}{2} + 1 = \mathbf{18 \ mA}$$

(*ii*)

$$\text{Zero signal } I_B = I_C / \beta = 18/100 = \mathbf{0.18 \ mA}$$

(*iii*) $$\text{Zero signal } V_{CE} = \frac{30-5}{2} + 5 = 17.5 \text{ V}$$

Since the load is transformer coupled, $V_{CC} \simeq 17.5$ V.

$$\text{d.c. input power, } P_{dc} = V_{CC} I_C = 17.5 \text{ V} \times 18 \text{ mA} = \mathbf{315 \text{ mW}}$$

$$\text{a.c. output voltage, } V_{ce} = \frac{30-5}{2\sqrt{2}} = 8.84 \text{ V}$$

$$\text{a.c. output current, } I_c = \frac{35-1}{2\sqrt{2}} = 12 \text{ mA}$$

$$\therefore \quad \text{a.c. output power, } P_{ac} = V_{ce} \times I_c$$

$$= 8.84 \text{ V} \times 12 \text{ mA} = \mathbf{106 \text{ mW}}$$

(*iv*) $$\text{Collector } \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{106}{315} \times 100 = \mathbf{33.7\%}$$

(*v*) The a.c. resistance R'_L in the collector is determined from the slope of the line.

$$\text{Slope} = -\frac{1}{R'_L} = \frac{35-1}{5-30} = \frac{-34}{25} \text{ kilo mho}$$

$$\therefore \quad R'_L = \frac{25}{34} \text{ k}\Omega = \frac{25}{34} \times 1000 = 735\ \Omega$$

$$\therefore \quad \text{Turn ratio, } n = \sqrt{\frac{R'_L}{R_L}} = \sqrt{\frac{735}{81.6}} = \mathbf{3}$$

Example 12.14. *In a class A transformer coupled amplifier, the collector current alternates between 3mA and 110 mA and its quiscent value is 58 mA. The load resistance is 13Ω and when referred to primary winding, it is 325Ω. The supply voltage is 20V. Calculate (i) transformer turn ratio (ii) a.c. output power (iii) collector efficiency.*

Solution. The conditions of the problem are represented in Fig. 12.11. The zero signal $I_C = 58$ mA.

(*i*) Let $n\ (= N_p/N_s)$ be the turn ratio of the transformer.

$$\therefore \quad R'_L = n^2 R_L$$

$$\text{or} \quad n = \sqrt{\frac{R'_L}{R_L}} = \sqrt{\frac{325}{13}} = \mathbf{5}$$

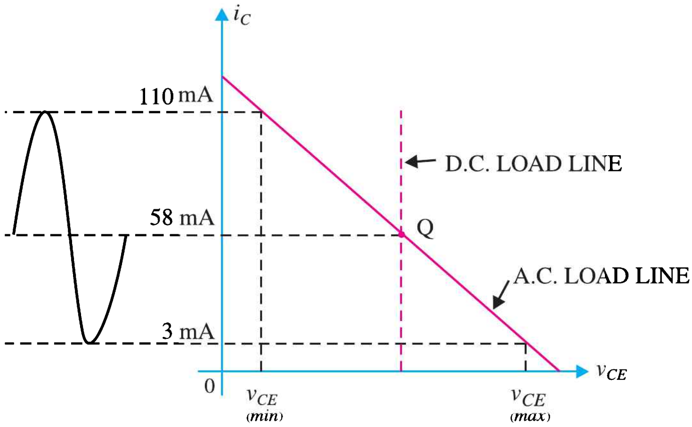


Fig. 12.11

(*ii*) $$\text{A.C. output power, } P_{ac} = \frac{1}{2} I_C^2 R'_L$$

$$= \frac{1}{2}(58\text{ mA})^2 \times 325\Omega = \mathbf{546\ mW}$$

(*iii*) D.C. input power, $P_{dc} = V_{CC} I_C = 20\text{ V} \times 58\text{ mA} = 1160\text{ mW}$

$\therefore$ Collector $\eta = \frac{546}{1160} \times 100 = \mathbf{47\%}$

12.11 Thermal Runaway

All semiconductor devices are very sensitive to temperature variations. If the temperature of a transistor exceeds the permissible limit, the transistor may be *permanently damaged. Silicon transistors can withstand temperatures upto 250°C while the germanium transistors can withstand temperatures upto 100°C.

There are two factors which determine the operating temperature of a transistor *viz.* (*i*) surrounding temperature and (*ii*) power dissipated by the transistor.

When the transistor is in operation, almost the entire heat is produced at the collector-base junction. This power dissipation causes the junction temperature to rise. This in turn increases the collector current since more electron-hole pairs are generated due to the rise in temperature. This produces an increased power dissipation in the transistor and consequently a further rise in temperature. Unless adequate cooling is provided or the transistor has built-in temperature compensation circuits to prevent excessive collector current rise, the junction temperature will continue to increase until the maximum permissible temperature is exceeded. If this situation occurs, the transistor will be permanently damaged.

The unstable condition where, owing to rise in temperature, the collector current rises and continues to increase is known as **thermal runaway.**

Thermal runaway must always be avoided. If it occurs, permanent damage is caused and the transistor must be replaced.

12.12 Heat Sink

As power transistors handle large currents, they always heat up during operation. Since transistor is a temperature dependent device, the heat generated must be dissipated to the surroundings in order to keep the temperature within permissible limits. Generally, the transistor is fixed on a metal sheet (usually aluminium) so that additional heat is transferred to the *Al* sheet.

The metal sheet that serves to dissipate the additional heat from the power transistor is known as **heat sink.**

Heat Sink

Most of the heat within the transistor is produced at the **collector junction. The heat sink increases the surface area and allows heat to escape from the collector junction easily. The result is that temperature of the transistor is sufficiently lowered. Thus heat sink is a direct practical means of combating the undesirable thermal effects *e.g.* thermal runaway.

---

* Almost the entire heat in a transistor is produced at the collector-base junction. If the temperature exceeds the permissible limit, this junction is destroyed and the transistor is rendered useless.

** Most of power is dissipated at the collector-base junction. This is because collector-base voltage is much greater than the base-emitter voltage, although currents through the two junctions are almost the same.

It may be noted that the ability of any heat sink to transfer heat to the surroundings depends upon its material, volume, area, shape, contact between case and sink and movement of air around the sink. Finned aluminium heat sinks yield the best heat transfer per unit cost.

It should be realised that the use of heat sink alone may not be sufficient to prevent thermal runaway under all conditions. In designing a transistor circuit, consideration should also be given to the choice of (*i*) operating point (*ii*) ambient temperatures which are likely to be encountered and (*iii*) the type of transistor *e.g.* metal case transistors are more readily cooled by conduction than plastic ones. Circuits may also be designed to compensate automatically for temperature changes and thus stabilise the operation of the transistor components.

12.13 Mathematical Analysis

The permissible power dissipation of the transistor is very important item for power transistors. The permissible power rating of a transistor is calculated from the following relation :

$$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta}$$

where P_{total} = total power dissipated within the transistor

$T_{J\,max}$ = maximum junction temperature. It is 90°C for *germanium* transistors and 150°C for *silicon* transistors.

T_{amb} = ambient temperature *i.e.* temperature of surrounding air

θ = *thermal resistance *i.e.* resistance to heat flow from the junction to the surrounding air

The unit of θ is °C/ watt and its value is always given in the transistor manual. A low thermal resistance means that it is easy for heat to flow from the junction to the surrounding air. The larger the transistor case, the lower is the thermal resistance and *vice-versa*. It is then clear that by using heat sink, the value of θ can be decreased considerably, resulting in increased power dissipation.

Example 12.15. *A power transistor dissipates 4 W. If* T_{Jmax} *= 90°C, find the maximum ambient temperature at which it can be operated. Given θ = 10°C/W.*

Solution.

$$P_{total} = 4\text{ W}$$

$$T_{J\,max} = 90°\text{C}$$

$$\theta = 10°\text{C/W}$$

$$\text{Now } P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta}$$

or $$4 = \frac{90 - T_{amb}}{10}$$

∴ Ambient temperature, $T_{amb} = 90 - 40 = \mathbf{50°C}$

The above example shows the effect of ambient temperature on the permissible power dissipation in a transistor. The lower the ambient temperature, the greater is the permissible power dissipation. Thus, a transistor can pass a higher collector current in winter than in summer.

Example 12.16. (*i*) *A power transistor has thermal resistance θ = 300°C/W. If the maximum junction temperature is 90°C and the ambient temperature is 30°C, find the maximum permissible power dissipation.*

---

* The path of heat flow generated at the collector-base junction is from junction to case, from case to sink and from sink to atmosphere.

(*ii*) *If a heat sink is used with the above transistor, the value of* θ *is reduced to 60°C/W. Find the maximum permissible power dissipation.*

Solution.

(*i*) *Without heat sink*

$$T_{J\,max} = 90°C$$
$$T_{amb} = 30°C$$
$$\theta = 300°C/W$$
$$\therefore \quad P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{90-30}{300} = 0.2\text{ W} = \mathbf{200\ mW}$$

(*ii*) *With heat sink*

$$T_{J\,max} = 90°C$$
$$T_{amb} = 30°C$$
$$\theta = 60°C/W$$
$$\therefore \quad P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{90-30}{60} = 1\text{ W} = \mathbf{1000\ mW}$$

It is clear from the above example that permissible power dissipation with heat sink is 5 times as compared to the case when no heat sink is used.

Example 12.17. *The total thermal resistance of a power transistor and heat sink is 20°C/W. The ambient temperature is 25°C and* $T_{J\,max}$ *= 200°C. If* V_{CE} *= 4 V, find the maximum collector current that the transistor can carry without destruction. What will be the allowed value of collector current if ambient temperature rises to 75°C ?*

Solution.

$$P_{total} = \frac{T_{Jmax} - T_{amb}}{\theta} = \frac{200-25}{20} = 8.75\text{ W}$$

This means that maximum permissible power dissipation of the transistor at ambient temperature of 25°C is 8.75 W *i.e.*

$$V_{CE} I_C = 8.75$$
$$\therefore \quad I_C = 8.75/4 = \mathbf{2.19\ A}$$

Again
$$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{200-75}{20} = 6.25\text{ W}$$
$$\therefore \quad I_C = 6.25/4 = \mathbf{1.56\ A}$$

This example clearly shows the effect of ambient temperature.

12.14 Stages of A Practical Power Amplifier

The function of a practical power amplifier is to amplify a weak signal until sufficient power is available to operate a loudspeaker or other output device. To achieve this goal, a power amplifier has generally three stages *viz. voltage amplification stage, driver stage* and *output stage.* Fig. 12.12 shows the block diagram of a practical power amplifier.

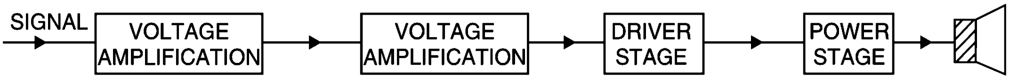


Fig. 12.12

(*i*) ***Voltage amplification stage.*** The signals found in practice have extremely low voltage level (< 10 mV). Therefore, the voltage level of the weak signal is raised by two or more voltage amplifiers. Generally, *RC* coupling is employed for this purpose.

(*ii*) ***Driver stage.*** The output from the last voltage amplification stage is fed to the driver stage. It supplies the necessary power to the output stage. The driver stage generally employs class *A* transformer coupled power amplifier. Here, concentrated effort is made to obtain *maximum power gain.*

(*iii*) ***Output stage.*** The output power from the driver stage is fed to the output stage. It is the final stage and feeds power directly to the speaker or other output device. The output stage is invariably transformer coupled and employs class *B* amplifiers in push-pull arrangement. Here, concentrated effort is made to obtain *maximum power output.*

12.15 Driver Stage

The stage that immediately precedes the output stage is called the *driver stage.* It operates as a class *A* power amplifier and supplies the drive for the output stage. Fig. 12.13 shows the driver stage. Note that transformer coupling is employed. The primary of this transformer is the collector load. The secondary is almost always centre-tapped so as to provide equal and opposite voltages to the input of push-pull amplifier (*i.e.* output stage). The driver transformer is usually a step-down transformer and facilitates impedance matching.

The output from the last voltage amplification stage forms the input to the driver stage. The driver stage renders power amplification in the usual way. It may be added that main consideration here is the maximum power gain. The output of the driver stage is taken from the centre-tapped secondary and is fed to the output stage.

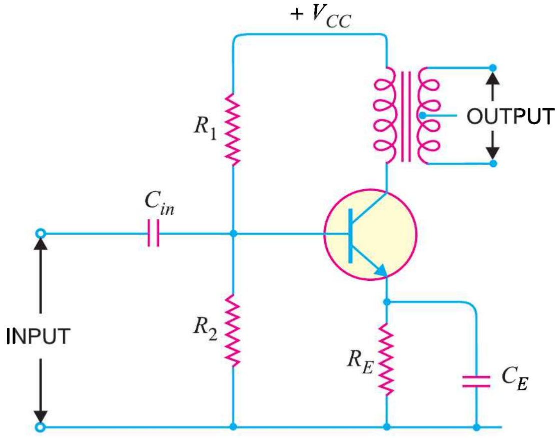


Fig. 12.13

12.16 Output Stage

The output stage essentially consists of a power amplifier and its purpose is to transfer maximum power to the output device. If a single transistor is used in the output stage, it can only be employed as class *A* amplifier for faithful amplification. Unfortunately, the power efficiency of a class *A* amplifier is very low ($\simeq$ 35%). As transistor amplifiers are operated from batteries, which is a costly source of power, therefore, such a low efficiency cannot be tolerated.

In order to obtain high output power at high efficiency, pushpull arrangement is used in the output stage. In this arrangement, we employ two transistors in class *B* operation. One transistor amplifies the positive half-cycle of the signal while the other transistor amplifies the negative half-cycle of the signal. In this way, output voltage is a complete sine wave. At the same time, the circuit delivers high output power to the load due to class *B* operation.

12.17 Push-Pull Amplifier

Push-Pull Amplifier

The push-pull amplifier is a power amplifier and is frequently employed in the output stages of electronic circuits. It is used whenever high output power at high efficiency is required. Fig. 12.14 shows the circuit of a push-pull amplifier. Two transistors T_{r1} and T_{r2} placed back to back are employed. Both transistors are operated in class *B* operation *i.e.* collector current is nearly zero in the absence of the signal. The centre-tapped secondary of driver transformer T_1 supplies equal and opposite voltages to the base circuits of two transistors.

The output transformer T_2 has the centre-tapped primary winding. The supply voltage V_{CC} is connected between the bases and this centre tap. The loudspeaker is connected across the secondary of this transformer.

Circuit operation. The input signal appears across the secondary *AB* of driver transformer. Suppose during the first half-cycle (marked 1) of the signal, end *A* becomes positive and end *B* negative. This will make the base-emitter junction of T_{r1} reverse biased and that of T_{r2} forward biased. The circuit will conduct current due to T_{r2} only and is shown by solid arrows. Therefore, this half-cycle of the signal is amplified by T_{r2} and appears in the lower half of the primary of output transformer. In the next half-cycle of the signal, T_{r1} is forward biased whereas T_{r2} is reverse biased. Therefore, T_{r1} conducts and is shown by dotted arrows. Consequently, this half-cycle of the signal is amplified by T_{r1} and appears in the upper half of the output transformer primary. The centre-tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary.

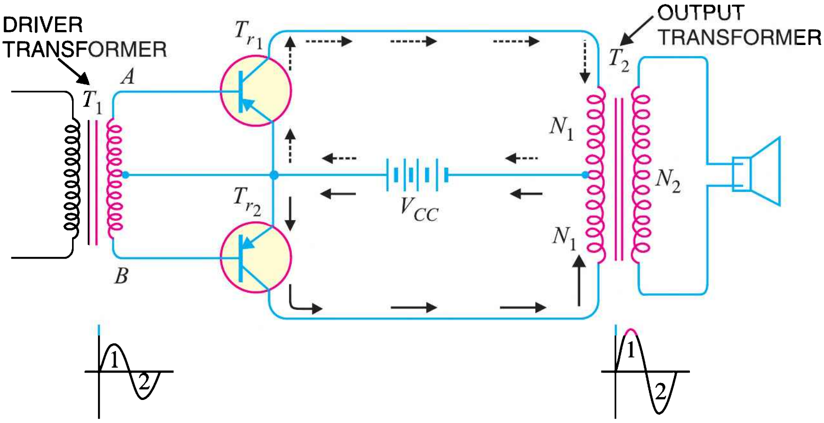


Fig. 12.14

It may be noted here that push-pull arrangement also permits a maximum transfer of power to the load through impedance matching. If R_L is the resistance appearing across secondary of output transformer, then resistance R'_L of primary shall become :

$$R'_L = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

where N_1 = Number of turns between either end of primary winding and centre-tap

N_2 = Number of secondary turns

Advantages

(*i*) The efficiency of the circuit is quite high ($\simeq$ 75%) due to class *B* operation.

(*ii*) A high a.c. output power is obtained.

Disadvantages

(*i*) Two transistors have to be used.

(*ii*) It requires two equal and opposite voltages at the input. Therefore, push-pull circuit requires the use of driver stage to furnish these signals.

(*iii*) If the parameters of the two transistors are not the same, there will be unequal amplification of the two halves of the signal.

(*iv*) The circuit gives more distortion.

(*v*) Transformers used are bulky and expensive.

12.18 Maximum Efficiency for Class B Power Amplifier

We have already seen that a push-pull circuit uses two transistors working in class *B* operation. For class *B* operation, the Q-point is located at cut-off on both d.c. and a.c. load lines. For maximum signal operation, the two transistors in class B amplifier are alternately driven from cut-off to saturation. This is shown in Fig. 12.15 (*i*). It is clear that a.c. output voltage has a peak value of V_{CE} and a.c. output current has a peak value of $I_{C\,(sat)}$. The same information is also conveyed through the a.c. load line for the circuit [See Fig. 12.15 (*ii*)].

$\therefore$ Peak a.c. output voltage $= V_{CE}$

Peak a.c. output current $= I_{C\,(sat)} = {}^{*}\dfrac{V_{CE}}{R_L} = \dfrac{V_{CC}}{2\,R_L} \qquad \left(\because V_{CE} = \dfrac{V_{CC}}{2}\right)$

Maximum average a.c. output power $P_{o\,(max)}$ is

$P_{o\,(max)}$ = Product of r.m.s. values of a.c. output voltage and a.c. output current

$$= \frac{V_{CE}}{\sqrt{2}} \times \frac{I_{C\,(sat)}}{\sqrt{2}} = \frac{V_{CE}\, I_{C\,(sat)}}{2}$$

$$= \frac{V_{CC}}{2} \times \frac{I_{C\,(sat)}}{2} = \frac{V_{CC}\, I_{C\,(sat)}}{4} \qquad \left(\because V_{CE} = \frac{V_{CC}}{2}\right)$$

$$\therefore \quad P_{o\,(max)} = 0.25\, V_{CC} I_{C\,(sat)}$$

The input d.c. power from the supply V_{CC} is

$$P_{dc} = V_{CC} I_{dc}$$

---

* Since the two transistors are identical, half the supply voltage is dropped across each transistor's collector-emitter terminals *i.e.* $V_{CE} = \dfrac{V_{CC}}{2}$

Also peak voltage across each transistor is V_{CE} and it appears across R_L.

$$\therefore I_{C\,(sat)} = \frac{V_{CE}}{R_L} = \frac{V_{CC}}{2} \times \frac{1}{R_L} = \frac{V_{CC}}{2\,R_L}$$

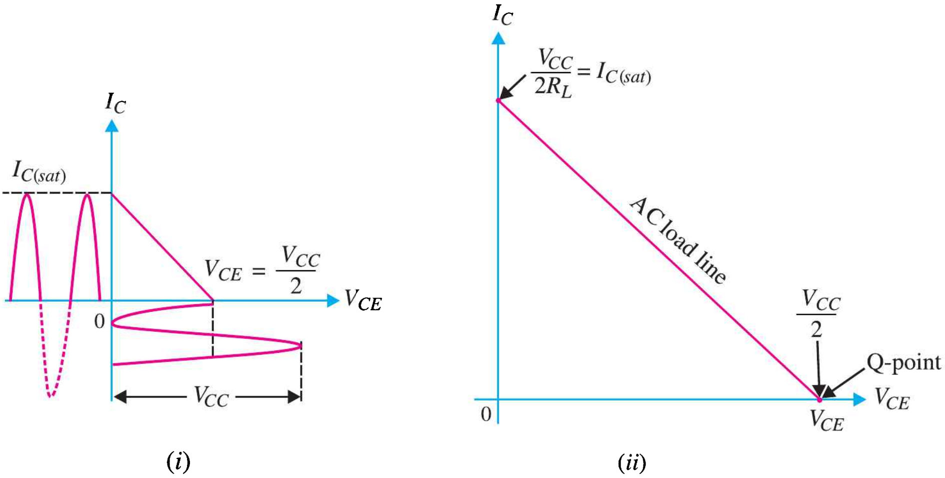


Fig. 12.15

where I_{dc} is the average current drawn from the supply V_{CC}. Since the transistor is on for alternating half-cycles, it effectively acts as a half-wave rectifier.

$$\therefore \quad I_{dc} = \frac{I_{C\,(sat)}}{\pi}$$

$$\therefore \quad P_{dc} = \frac{V_{CC}\, I_{C\,(sat)}}{\pi}$$

$$\therefore \quad \text{Max. collector}\ \eta = \frac{P_{o\,(max)}}{P_{dc}} = \frac{0.25\, V_{CC}\ I_{C\,(sat)}}{\left(V_{CC}\, I_{C\,(sat)}\right)/\pi} \times 100 = 0.25\pi \times 100 = 78.5\%$$

Thus the maximum collector efficiency of class *B* power amplifier is 78.5%. Recall that maximum collector efficiency for class A transformer coupled amplifier is 50%.

Power dissipated by transistors. The power dissipated (as heat) by the transistors in class *B* amplifier is the difference between the input power delivered by V_{CC} and the output power delivered to the load *i.e.*

$$P_{2T} = P_{dc} - P_{ac}$$

where P_{2T} = power dissipated by the two transistors

∴ Power dissipated by each transistor is

$$P_T = \frac{P_{2T}}{2} = \frac{P_{dc} - P_{ac}}{2}$$

Note. For collector efficiency of class *C* amplifiers, the reader may refer to Chapter 15 (Transistor tuned amplifiers).

Example 12.18. *For a class B amplifier using a supply of V_{CC} = 12V and driving a load of 8Ω, determine (i) maximum load power (ii) d.c. input power (iii) collector efficiency.*

Solution. $V_{CC} = 12\text{ V}\ ;\ R_L = 8\Omega$

(*i*) Maximum load power, $P_{o\,(max)} = 0.25\ V_{CC}\, I_{C\,(sat)}$

$$= 0.25\ V_{CC} \times \frac{V_{CC}}{2\,R_L} \qquad \left(\because I_{C\,(sat)} = \frac{V_{CC}}{2\,R_L}\right)$$

$$= 0.25 \times 12 \times \frac{12}{2 \times 8} = \mathbf{2.25\ W}$$

(*ii*) D.C. input power, $P_{dc} = \frac{V_{CC}\, I_{C\,(sat)}}{\pi} = \frac{V_{CC}}{\pi} \times \frac{V_{CC}}{2\,R_L}$

$$= \frac{12}{\pi} \times \frac{12}{2 \times 8} = \mathbf{2.87\ W}$$

(*iii*) Collector $\eta = \frac{P_{o\,(max)}}{P_{dc}} \times 100 = \frac{2.25}{2.87} \times 100 = \mathbf{78.4\%}$

Example 12.19. *A class B push-pull amplifier with transformer coupled load uses two transistors rated 10 W each. What is the maximum power output one can obtain at the load from the circuit?*

Solution. The power dissipation by each transistor is $P_T = 10$W. Therefore, power dissipated by two transistors is $P_{2T} = 2 \times 10 = 20$W.

Now $P_{dc} = P_{o\,(max)} + P_{2T}$; Max. $\eta = 0.785$

$\therefore$ Max $\eta = \frac{P_{o\,(max)}}{P_{dc}} = \frac{P_{o\,(max)}}{P_{o\,(max)} + P_{2T}} = \frac{P_{o\,(max)}}{P_{o\,(max)} + 20}$

or $0.785 = \frac{P_{o\,(max)}}{P_{o\,(max)} + 20}$

or $0.785\, P_{o\,(max)} + 15.7 = P_{o\,(max)}$

or $P_{o\,(max)}(1 - 0.785) = 15.7$

$\therefore$ $P_{o\,(max)} = \frac{15.7}{1 - 0.785} = \frac{15.7}{0.215} = \mathbf{73.02\ W}$

Example 12.20. *A class B push-pull amplifier has an efficiency of 60% and each transistor has a rating of 2.5W. Find the a.c. output power and d.c. input power.*

Solution. The power dissipated by each transistor is $P_T = 2.5$W.

Therefore, power dissipated by the two transistors is $P_{2T} = 2{\times}2.5 = 5$W.

Now $P_{dc} = P_{ac} + P_{2T}$; $\eta = 0.6$

$\therefore$ $\eta = \frac{P_{ac}}{P_{dc}} = \frac{P_{ac}}{P_{ac} + P_{2T}}$

or $0.6 = \frac{P_{ac}}{P_{ac} + 5}$ or $0.6\, P_{ac} + 3 = P_{ac}$

$\therefore$ $P_{ac} = \frac{3}{1 - 0.6} = \frac{3}{0.4} = \mathbf{7.5\ W}$

and $P_{dc} = P_{ac} + P_{2T} = 7.5 + 5 = \mathbf{12.5\ W}$

Example 12.21. *A class B amplifier uses V_{CC} = 10V and drives a load of 10Ω. Determine the end point values of the a.c. load line.*

Solution.

$$I_{C\,(sat)} = \frac{V_{CC}}{2R_L} = \frac{10\text{V}}{2(10\ \Omega)} = \mathbf{500\ mA}$$

This locates one end-point of the a.c. load line on the collector current axis.

$$V_{CE\,(off)} = \frac{V_{CC}}{2} = \frac{10\text{V}}{2} = \mathbf{5V}$$

This locates the second end-point of the a.c load line on the collector-emitter voltage axis. By joining these two points, the a.c. load line of the amplifier is constructed.

12.19 Complementary-Symmetry Amplifier

By complementary symmetry is meant a principle of assembling push-pull class *B* amplifier without requiring centre-tapped transformers at the input and output stages. Fig. 12.16 shows the transistor push-pull amplifier using complementary symmetry. It employs one *npn* and one *pnp* transistor and requires no centre-tapped transformers. The circuit action is as follows. During the positive-half of the input signal, transistor T_1 (the *npn* transistor) conducts current while T_2 (the *pnp* transistor) is cut off. During the negative half-cycle of the signal, T_2 conducts while T_1 is cut off. In this way, *npn* transistor amplifies the positive half-cycles of the signal while the *pnp* transistor amplifies the negative half-cycles of the signal. Note that we generally use an output transformer (not centre-tapped) for impedance matching.

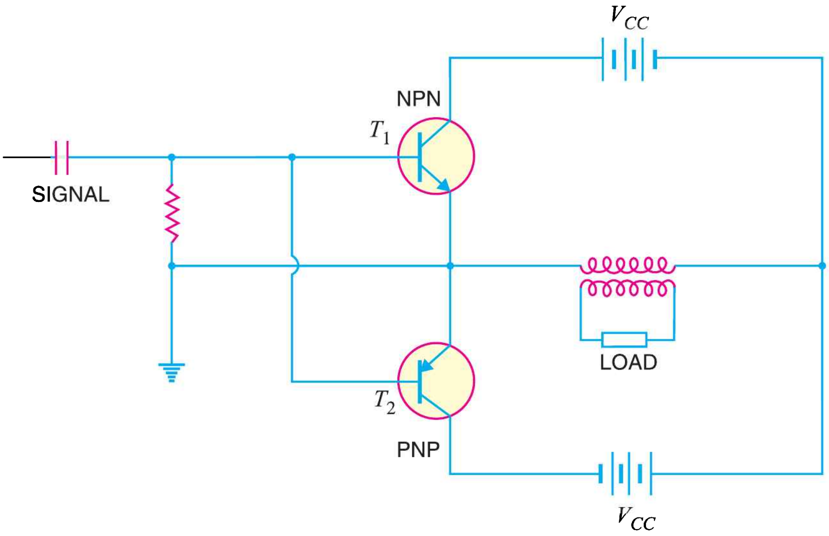


Fig.12.16

Advantages

(*i*) This circuit does not require transformer. This saves on weight and cost.

(*ii*) Equal and opposite input signal voltages are not required.

Disadvantages

(*i*) It is difficult to get a pair of transistors (*npn* and *pnp*) that have similar characteristics.

(*ii*) We require both positive and negative supply voltages.

MULTIPLE-CHOICE QUESTIONS

1. The output stage of a multistage amplifier is also called ....

(*i*) mixer stage (*ii*) power stage
(*iii*) detector stage (*iv*) R.F. stage

2. .... coupling is generally employed in power amplifiers.

(*i*) transformer (*ii*) *RC*
(*iii*) direct (*iv*) impedance

3. A class *A* power amplifier uses ....

(*i*) two transistors (*ii*) three transistors
(*iii*) one transistor (*iv*) none of the above

4. The maximum efficiency of resistance loaded class *A* power amplifier is ....

(*i*) 78.5% (*ii*) 50%
(*iii*) 30% (*iv*) 25%

5. The maximum efficiency of transformer coupled class *A* power amplifier is ....

(*i*) 30% (*ii*) 50%
(*iii*) 80% (*iv*) 45%

6. Class .... power amplifier has the highest collector efficiency.

(*i*) *C* (*ii*) *A*
(*iii*) *B* (*iv*) *AB*

7. Power amplifiers handle .... signals compared to voltage amplifiers.

(*i*) small (*ii*) very small
(*iii*) large (*iv*) none of the above

8. In class *A* operation, the operating point is generally located .... of the d.c. load line.

(*i*) at cut off point (*ii*) at the middle
(*iii*) at saturation point
(*iv*) none of the above

9. Class *C* amplifiers are used as ....

(*i*) AF amplifiers (*ii*) detectors
(*iii*) R.F. amplifiers (*iv*) none of the above

10. A power amplifier has comparatively ....β.

(*i*) small (*ii*) large
(*iii*) very large (*iv*) none of the above

11. The maximum collector efficiency of class *B* operation is ....

(*i*) 50% (*ii*) 90%
(*iii*) 60.5% (*iv*) 78.5%

12. A 2-transistor class *B* power amplifier is commonly called .... amplifier.

(*i*) dual (*ii*) push-pull
(*iii*) symmetrical (*iv*) differential

13. If a transistor is operated in such a way that output current flows for 60° of the input signal, then it is ...... operation.

(*i*) class *A* (*ii*) class *B*
(*iii*) class *C* (*iv*) none of the above

14. If the zero signal power dissipation of a transistor is 1 W, then power rating of the transistor should be atleast ....

(*i*) 0.5 W (*ii*) 0.33 W
(*iii*) 0.75 W (*iv*) 1 W

15. When a transistor is cut off, ...

(*i*) maximum voltage appears across transistor
(*ii*) maximum current flows
(*iii*) maximum voltage appears across load
(*iv*) none of the above

16. A class *A* power amplifier is sometimes called .... amplifier.

(*i*) symmetrical (*ii*) single-ended
(*iii*) reciprocating (*iv*) differential

17. Class .... operation gives the maximum distortion.

(*i*) *A* (*ii*) *B*
(*iii*) *C* (*iv*) *AB*

18. The output stage of a multistage amplifier usually employs ....

(*i*) push-pull amplifier
(*ii*) preamplifier
(*iii*) class *A* power amplifier
(*iv*) none of the above

19. The size of a power transistor is made considerably large to ....

(*i*) provide easy handling
(*ii*) dissipate heat
(*iii*) facilitate connections
(*iv*) none of the above

20. Low efficiency of a power amplifier results in ....

(*i*) low forward bias
(*ii*) less battery consumption
(*iii*) more battery consumption
(*iv*) none of the above

21. The driver stage usually employs ....

(*i*) class *A* power amplifier
(*ii*) push-pull amplifier
(*iii*) class *C* amplifier
(*iv*) none of the above

22. If the power rating of a transistor is 1 W and collector current is 100 mA, then maximum allowable collector voltage is ....

(*i*) 1 V (*ii*) 100 V
(*iii*) 20 V (*iv*) 10 V

23. When no signal is applied, the approximate collector efficiency of class *A* power amplifier is ....

(*i*) 10% (*ii*) 0%
(*iii*) 25% (*iv*) 50%

24. What will be the collector efficiency of a power amplifier having zero signal power dissipation of 5 watts and a.c. power output of 2 watts ?

(*i*) 20% (*ii*) 80%
(*iii*) 40% (*iv*) 50%

25. The output signal voltage and current of a power amplifier are 5 V and 200 mA ; the values being r.m.s. What is the power output ?

(*i*) 1 W (*ii*) 2 W
(*iii*) 4 W (*iv*) none of the above

26. The maximum a.c. power output from a class *A* power amplifier is 10 W. What should be the minimum power rating of the transistor used ?

(*i*) 10 W (*ii*) 15 W
(*iii*) 5 W (*iv*) 20 W

27. For the same a.c. power output as above, what should be the minimum power rating of transistor for class *B* operation ?

(*i*) 10 W (*ii*) 4 W
(*iii*) 8 W (*iv*) none of the above

28. The push-pull circuit must use ..... operation.

(*i*) class *A* (*ii*) class *C*
(*iii*) class *B* (*iv*) class *AB*

29. The class B push-pull circuit can deliver 100 W of a.c. output power. What should be the minimum power rating of each transistor ?

(*i*) 20 W (*ii*) 40 W
(*iii*) 10 W (*iv*) 80 W

30. What turn ratio (N_p/N_s) of transformer is required to match 4 Ω speaker to a transistor having an output impedance of 8000 Ω ?

(*i*) 35.2 (*ii*) 44.7
(*iii*) 54.3 (*iv*) none of the above

31. A transformer coupled class *A* power amplifier has a load of 100 Ω on the secondary. If the turn ratio is 10 : 1, what is the value of load appearing on the primary ?

(*i*) 5 kΩ (*ii*) 20 kΩ
(*iii*) 100 kΩ (*iv*) 10 kΩ

32. Power amplifiers generally use transformer coupling because transformer permits ....

(*i*) cooling of the circuit
(*ii*) impedance matching
(*iii*) distortionless output
(*iv*) good frequency response

33. Transformer coupling can be used in .... amplifiers.

(*i*) either power or voltage
(*ii*) only power
(*iii*) only voltage (*iv*) none of the above

34. The output transformer used in a power amplifier is a ...... transformer.

(*i*) 1 : 1 ratio (*ii*) step-up
(*iii*) step-down (*iv*) none of the above

35. The most important consideration in power amplifiers is......

(*i*) biasing the circuit
(*ii*) collector efficiency
(*iii*) to keep the transformer cool
(*iv*) none of the above

36. An *AF* amplifier is shielded to ....

(*i*) keep the amplifier cool
(*ii*) protect from rusting
(*iii*) prevent induction due to stray magnetic fields
(*iv*) none of the above

37. The pulsating d.c. applied to power amplifier causes ....

(*i*) burning of transistor
(*ii*) hum in the circuit
(*iii*) excessive forward voltage
(*iv*) none of the above

38. The disadvantage of impedance matching is that it ....

(*i*) gives distorted output

(*ii*) gives low power output

(*iii*) requires a transformer

(*iv*) none of the above

39. If the gain versus frequency curve of a transistor amplifier is not flat, then there is .... distortion.

(*i*) amplitude (*ii*) intermodulation

(*iii*) frequency (*iv*) none of the above

40. The most costly coupling is .... coupling.

(*i*) *RC* (*ii*) direct

(*iii*) impedance (*iv*) transformer.

Answers to Multiple-Choice Questions

1.	(*ii*)	**2.**	(*i*)	**3.**	(*iii*)	**4.**	(*iv*)	**5.**	(*ii*)
6.	(*i*)	**7.**	(*iii*)	**8.**	(*ii*)	**9.**	(*iii*)	**10.**	(*i*)
11.	(*iv*)	**12.**	(*ii*)	**13.**	(*iii*)	**14.**	(*iv*)	**15.**	(*i*)
16.	(*ii*)	**17.**	(*iii*)	**18.**	(*i*)	**19.**	(*ii*)	**20.**	(*iii*)
21.	(*i*)	**22.**	(*iv*)	**23.**	(*ii*)	**24.**	(*iii*)	**25.**	(*i*)
26.	(*iv*)	**27.**	(*ii*)	**28.**	(*iii*)	**29.**	(*i*)	**30.**	(*ii*)
31.	(*iv*)	**32.**	(*ii*)	**33.**	(*i*)	**34.**	(*iii*)	**35.**	(*ii*)
36.	(*iii*)	**37.**	(*ii*)	**38.**	(*i*)	**39.**	(*iii*)	**40.**	(*iv*)

Chapter Review Topics

1. What is an audio power amplifier ? What is its need ?
2. Explain the difference between a voltage and a power amplifier.
3. What do you understand by class A, class B and class C power amplifiers ?
4. Define and explain the following terms as applied to power amplifiers :
   (i) collector efficiency *(ii)* distortion *(iii)* power dissipation capability
5. Show that maximum collector efficiency of class A transformer coupled power amplifier is 50%.
6. Draw the block diagram of a practical power amplifier.
7. Explain the push-pull circuit with a neat diagram.
8. Write short notes on the following :
   (i) Heat sink *(ii)* Driver stage
   (iii) Output stage *(iv)* Complementary-symmetry amplifier

Problems

1. The resistance of the secondary of an output transformer is 100 Ω. If the output impedance is 10 kΩ, find the turn ratio of the transformer for maximum power transference. **[n = 10]**
2. A power transistor working in class A operation has zero signal power dissipation of 5 watts. If a.c. output power is 2 watts, find (*i*) collector efficiency (*ii*) power rating of transistor. **[(*i*) 40% (*ii*) 5 watts]**
3. A class A power amplifier has a maximum a.c. power output of 30 W. Find the power rating of the transistor. **[60 W]**
4. The a.c. power output of a class A power amplifier is 2 W. If the collector efficiency is 40%, find the power rating of the transistor. **[5 W]**
5. In a class A transformer coupled amplifier, collector current alternates between 3 mA and 110 mA and its quiescent value is 58 mA. The load resistance is 15 Ω and when referred to primary winding is 325 Ω. The supply voltage is 20V. Find (*i*) transformer turn ratio (*ii*) a.c. power output (*iii*) power rating of transistor.

6. A transistor has thermal resistance θ = 80°C/W. If the maximum junction temperature is 90°C and the ambient temperature is 30°C, find the maximum permissible power dissipation.

[750 mW]

7. A power transistor dissipates 4 W. If $T_{J\,max}$ = 90°C, find the maximum ambient temperature at which it can be operated. Given thermal resistance θ = 8ºC/W. **[58 °C]**

8. A class A transformer-coupled amplifier uses a 25 : 1 transformer to drive a 4Ω load. Calculate the effective a.c. load (seen by the transistor connected to the larger turns side of the transformer).

[2.5 kΩ]

9. Calculate the transformer turns ratio required to connect 4 parallel 16Ω speakers so that they appear as an 8 kΩ effective load. **[44.7]**

10. For a class B amplifier with V_{CC} = 25V driving an 8Ω load, determine :

(*i*) maximum input power

(*ii*) maximum output power

(*iii*) maximum circuit efficiency

[(*i*) 49.7W (*ii*) 39.06W (*iii*) 78.5 %]

Discussion Questions

1. Why does collector efficiency play important part in power amplifiers ?

2. Why does the problem of distortion arise in power amplifiers ?

3. Why are power amplifiers classified on the basis of mode of operation ?

4. Why does the output stage employ push-pull arrangement ?

5. Why is driver stage necessary for push-pull circuit ?

6. Why do we use transformer in the output stage ?

13

Amplifiers with Negative Feedback

13.1 Feedback

13.2 Principles of Negative Voltage Feedback In Amplifiers

13.3 Gain of Negative Voltage Feedback Amplifier

13.4 Advantages of Negative Voltage Feedback

13.5 Feedback Circuit

13.6 Principles of Negative Current Feedback

13.7 Current Gain with Negative Current Feedback

13.8 Effects of Negative Current Feedback

13.9 Emitter Follower

13.10 D.C. Analysis of Emitter Follower

13.11 Voltage Gain of Emitter Follower

13.12 Input Impedance of Emitter Follower

13.13 Output Impedance of Emitter Follower

13.14 Applications of Emitter Follower

13.15 Darlington Amplifier

INTRODUCTION

A practical amplifier has a gain of nearly one million *i.e.* its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output. There is a strong tendency in amplifiers to introduce *hum* due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output. The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible.

The noise level in amplifiers can be reduced considerably by the use of *negative feedback i.e.* by injecting a fraction of output in phase opposition to the input signal. The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

13.1 Feedback

The process of injecting a fraction of output energy of *some device back to the input is known as* **feedback**.

The principle of feedback is probably as old as the invention of first machine but it is only some 50 years ago that feedback has come into use in connection with electronic circuits. It has been found very useful in reducing noise in amplifiers and making amplifier operation stable. Depending upon whether the feedback energy aids or opposes the input signal, there are two basic types of feedback in amplifiers *viz positive feedback* and *negative feedback.*

(*i*) **Positive feedback.** When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called *positive feedback.* This is illustrated in Fig. 13.1. Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the *feedback voltage* V_f to be in phase with the input signal V_{in}.

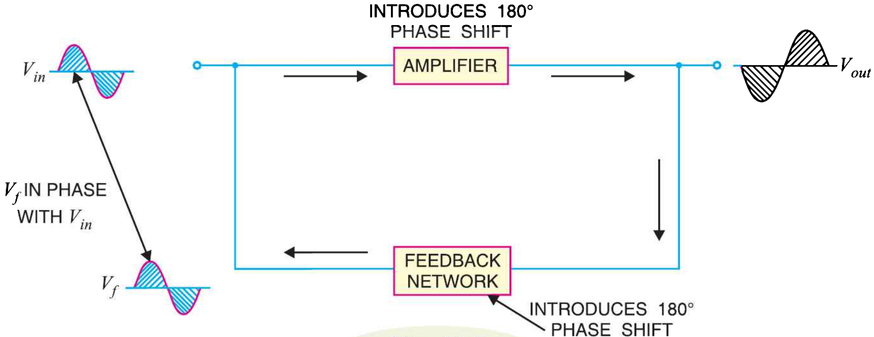

INTRODUCES 180°
PHASE SHIFT
AMPLIFIER
V_{in}
V_{out}
V_f IN PHASE
WITH V_{in}
V_f
FEEDBACK
NETWORK
INTRODUCES 180°
PHASE SHIFT

Fig. 13.1

The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is seldom employed in amplifiers. One important use of positive feedback is in oscillators. As we shall see in the next chapter, if positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

(*ii*) **Negative feedback.** When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called *negative feedback.* This is illustrated in Fig. 13.2. As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (*i.e.*, 0° phase shift). The result is that the *feedback voltage* V_f is 180° out of phase with the input signal V_{in}.

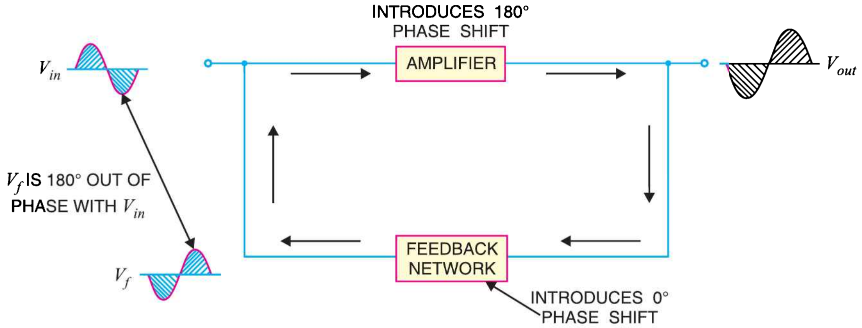

INTRODUCES 180°
PHASE SHIFT
AMPLIFIER
V_{in}
V_{out}
V_f IS 180° OUT OF
PHASE WITH V_{in}
V_f
FEEDBACK
NETWORK
INTRODUCES 0°
PHASE SHIFT

Fig. 13.2

Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances. It is due to these advantages that negative feedback is frequently employed in amplifiers.

13.2 Principles of Negative Voltage Feedback In Amplifiers

A feedback amplifier has two parts viz an amplifier and a feedback circuit. The feedback circuit usually consists of resistors and returns a fraction of output energy back to the input. Fig. 13.3 *shows the principles of negative voltage feedback in an amplifier. Typical values have been assumed to make the treatment more illustrative. The output of the amplifier is 10 V. The fraction m_v of this output *i.e.* 100 mV is fedback to the input where it is applied in series with the input signal of 101 mV. As the feedback is negative, therefore, only 1 mV appears at the input terminals of the amplifier.

Referring to Fig. 13.3, we have,

$$\text{Gain of amplifier without feedback, } A_v = \frac{10 \text{ V}}{1 \text{ mV}} = 10{,}000$$

Fig. 13.3

$$\text{Fraction of output voltage fedback, } m_v = \frac{100 \text{ mV}}{10 \text{ V}} = 0.01$$

$$\text{Gain of amplifier with negative feedback, } A_{vf} = \frac{10 \text{ V}}{101 \text{ mV}} = 100$$

The following points are worth noting :

(*i*) When negative voltage feedback is applied, the gain of the amplifier is **reduced. Thus, the gain of above amplifier without feedback is 10,000 whereas with negative feedback, it is only 100.

(*ii*) When negative voltage feedback is employed, the voltage *actually* applied to the amplifier is extremely small. In this case, the signal voltage is 101 mV and the negative feedback is 100 mV so that voltage applied at the input of the amplifier is only 1 mV.

(*iii*) In a negative voltage feedback circuit, the feedback fraction m_v is always between 0 and 1.

(*iv*) The gain with feedback is sometimes called *closed-loop gain* while the gain without feedback is called *open-loop gain*. These terms come from the fact that amplifier and feedback circuits form a "loop". When the loop is "opened" by disconnecting the feedback circuit from the input, the amplifier's gain is A_v, the "open-loop" gain. When the loop is "closed" by connecting the feedback circuit, the gain decreases to A_{vf}, the "closed-loop" gain.

---

* Note that amplifier and feedback circuits are connected in *series-parallel*. The inputs of amplifier and feedback circuits are in *series* but the outputs are in *parallel*. In practice, this circuit is widely used.

** Since with negative voltage feedback the voltage gain is decreased and current gain remains unaffected, the power gain A_p (= $A_v \times A_i$) will decrease. However, the drawback of reduced power gain is offset by the advantage of increased bandwidth.

13.3 Gain of Negative Voltage Feedback Amplifier

Consider the negative voltage feedback amplifier shown in Fig. 13.4. The gain of the amplifier without feedback is A_v. Negative feedback is then applied by feeding a fraction m_v of the output voltage e_0 back to amplifier input. Therefore, the actual input to the amplifier is the signal voltage e_g *minus* feedback voltage $m_v e_0$ *i.e.*,

$$\text{Actual input to amplifier} = e_g - m_v e_0$$

The output e_0 must be equal to the input voltage $e_g - m_v e_0$ multiplied by gain A_v of the amplifier *i.e.*,

$$(e_g - m_v e_0) A_v = e_0$$

or $$A_v e_g - A_v m_v e_0 = e_0$$

or $$e_0 (1 + A_v m_v) = A_v e_g$$

or $$\frac{e_0}{e_g} = \frac{A_v}{1 + A_v m_v}$$

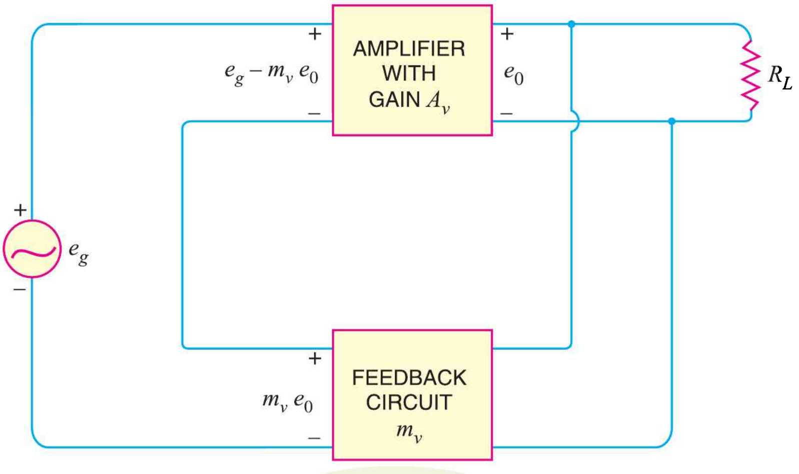


Fig. 13.4

But e_0/e_g is the voltage gain of the amplifier with feedback.

∴ Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

It may be seen that the gain of the amplifier without feedback is A_v. However, when negative voltage feedback is applied, the gain is reduced by a factor $1 + A_v m_v$. It may be noted that negative voltage feedback does not affect the current gain of the circuit.

Example 13.1. *The voltage gain of an amplifier without feedback is 3000. Calculate the voltage gain of the amplifier if negative voltage feedback is introduced in the circuit. Given that feedback fraction $m_v = 0.01$.*

Solution. $A_v = 3000, \quad m_v = 0.01$

∴ Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v} = \frac{3000}{1 + 3000 \times 0.01} = \frac{3000}{31} = \mathbf{97}$$

Example 13.2. *The overall gain of a multistage amplifier is 140. When negative voltage feedback is applied, the gain is reduced to 17.5. Find the fraction of the output that is fedback to the input.*

Solution. $A_v = 140, \quad A_{vf} = 17.5$

Let m_v be the feedback fraction. Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$17.5 = \frac{140}{1 + 140\, m_v}$$

or $$17.5 + 2450\, m_v = 140$$

$$\therefore \quad m_v = \frac{140 - 17.5}{2450} = \mathbf{\frac{1}{20}}$$

Example 13.3. *When negative voltage feedback is applied to an amplifier of gain 100, the overall gain falls to 50.*

(i) Calculate the fraction of the output voltage fedback.

(ii) If this fraction is maintained, calculate the value of the amplifier gain required if the overall stage gain is to be 75.

Solution.

(*i*) Gain without feedback, $A_v = 100$

Gain with feedback, $A_{vf} = 50$

Let m_v be the fraction of the output voltage fedback.

Now $$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$50 = \frac{100}{1 + 100\, m_v}$$

or $$50 + 5000\, m_v = 100$$

or $$m_v = \frac{100 - 50}{5000} = \mathbf{0.01}$$

(*ii*) $A_{vf} = 75\,; \quad m_v = 0.01\,; \quad A_v = ?$

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$75 = \frac{A_v}{1 + 0.01\, A_v}$$

or $$75 + 0.75\, A_v = A_v$$

$$\therefore \quad A_v = \frac{75}{1 - 0.75} = \mathbf{300}$$

Example 13.4. *With a negative voltage feedback, an amplifier gives an output of 10 V with an input of 0.5 V. When feedback is removed, it requires 0.25 V input for the same output. Calculate (i) gain without feedback (ii) feedback fraction m_v.*

Solution.

(*i*) Gain without feedback, $A_v = 10/0.25 = \mathbf{40}$

(*ii*) Gain with feedback, $A_{vf} = 10/0.5 = 20$

Now $$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$20 = \frac{40}{1 + 40\, m_v}$$

or $$20 + 800\, m_v = 40$$

or $$m_v = \frac{40 - 20}{800} = \mathbf{\frac{1}{40}}$$

Example 13.5. *The gain of an amplifier without feedback is 50 whereas with negative voltage feedback, it falls to 25. If due to ageing, the amplifier gain falls to 40, find the percentage reduction in stage gain (i) without feedback and (ii) with negative feedback.*

Solution. $$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$25 = \frac{50}{1 + 50\, m_v}$$

or $$m_v = 1/50$$

(*i*) **Without feedback.** The gain of the amplifier without feedback is 50. However, due to ageing, it falls to 40.

$$\therefore \quad \text{\%age reduction in stage gain} = \frac{50 - 40}{50} \times 100 = \mathbf{20\%}$$

(*ii*) **With negative feedback.** When the gain without feedback was 50, the gain with negative feedback was 25. Now the gain without feedback falls to 40.

$$\therefore \quad \text{New gain with negative feedback} = \frac{A_v}{1 + A_v\, m_v} = \frac{40}{1 + (40 \times 1/50)} = 22.2$$

$$\therefore \quad \text{\%age reduction in stage gain} = \frac{25 - 22.2}{25} \times 100 = \mathbf{11.2\%}$$

Example 13.6. *An amplifier has a voltage amplification A_v and a fraction m_v of its output is fedback in opposition to the input. If $m_v = 0.1$ and $A_v = 100$, calculate the percentage change in the gain of the system if A_v falls 6 db due to ageing.*

Solution. $$A_v = 100, \quad m_v = 0.1, \quad A_{vf} = ?$$

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v} = \frac{100}{1 + 100 \times 0.1} = 9.09$$

$$\text{Fall in gain} = 6db$$

Let A_{v1} be the new absolute voltage gain without feedback.

Then, $$20 \log_{10} A_v/A_{v1} = 6$$

or $$\log_{10} A_v/A_{v1} = 6/20 = 0.3$$

or $$\frac{A_v}{A_{v1}} = \text{Antilog } 0.3 = 2$$

or $$A_{v1} = A_v/2 = 100/2 = 50$$

$$\therefore \quad \text{New } A_{vf} = \frac{A_{v1}}{1 + A_{v1}\, m_v} = \frac{50}{1 + 50 \times 0.1} = 8.33$$

$$\text{\% age change in system gain} = \frac{9.09 - 8.33}{9.09} \times 100 = \mathbf{8.36\%}$$

Example 13.7. *An amplifier has a voltage gain of 500 without feedback. If a negative feedback is applied, the gain is reduced to 100. Calculate the fraction of the output fed back. If, due to ageing of components, the gain without feedback falls by 20%, calculate the percentage fall in gain with feedback.*

Solution.

$$A_v = 500 \; ; A_{vf} = 100 \; ; m_v = ?$$

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$100 = \frac{500}{1 + 500\, m_v}$$

$\therefore$ $$m_v = \mathbf{0.008}$$

Now $$A_v = \frac{80}{100} \times 500 = 400 \; ; m_v = 0.008 \; ; A_{vf} = ?$$

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v} = \frac{400}{1 + 400 \times 0.008} = \frac{400}{4.2} = 95.3$$

$\therefore$ $$\text{\% age fall in } A_{vf} = \frac{100 - 95.3}{100} \times 100 = \mathbf{4.7\%}$$

Note that without negative feedback, the change in gain is 20%. However, when negative feedback is applied, the change in gain (4.7%) is much less. This shows that negative feedback provides voltage gain stability.

Example 13.8. *An amplifier has an open-loop gain A_v = 100,000. A negative feedback of 10 db is applied. Find (i) voltage gain with feedback (ii) value of feedback fraction m_v.*

Sodlution.

(*i*) *db* voltage gain without feedback

$$= 20 \log_{10} 100{,}000 = 20 \log_{10} 10^5 = 100 \; db$$

Voltage gain with feedback $= 100 - 10 = 90 \; db$

Now $$20 \log_{10} (A_{vf}) = 90$$

or $$\log_{10} (A_{vf}) = 90/20 = 4.5$$

$\therefore$ $$A_{vf} = \text{Antilog } 4.5 = \mathbf{31622}$$

(*ii*) $$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$31622 = \frac{100{,}000}{1 + 100{,}000 \times m_v}$$

$\therefore$ $$m_v = \mathbf{2.17 \times 10^{-5}}$$

Example 13.9. *An amplifier with an open-circuit voltage gain of 1000 has an output resistance of 100 Ω and feeds a resistive load of 900 Ω. Negative voltage feedback is provided by connecting a resistive voltage divider across the output and one-fiftieth of the output voltage is fedback in series with the input signal. Determine the voltage gain with negative feedback.*

Solution. Fig. 13.5 shows the equivalent circuit of an amplifier along with the feedback circuit. Voltage gain of the amplifier without feedback is

$$A_v = \frac{A_0\, R_L}{R_{out} + R_L} \qquad \text{...See Art. 10.20}$$

$$= \frac{1000 \times 900}{100 + 900} = 900$$

$$\therefore \quad A_{vf} = \frac{A_v}{1 + A_v\, m_v} = \frac{900}{1 + 900 \times (1/50)} = \mathbf{47.4}$$

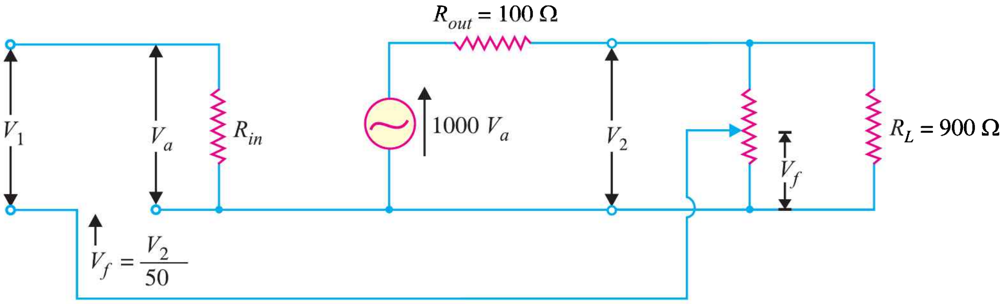


Fig. 13.5

Example 13.10. *An amplifier is required with a voltage gain of 100 which does not vary by more than 1%. If it is to use negative feedback with a basic amplifier the voltage gain of which can vary by 20%, determine the minimum voltage gain required and the feedback factor.*

Solution.

$$100 = \frac{A_v}{1 + A_v\, m_v}$$

or $\quad 100 + 100\, A_v\, m_v = A_v \qquad \ldots (i)$

Also $\quad 99 = \frac{0.8\, A_v}{1 + 0.8\, A_v\, m_v}$

or $\quad 99 + 79.2\, A_v\, m_v = 0.8\, A_v \qquad \ldots (ii)$

Multiplying eq (*i*) by 0.792, we have,

$$79.2 + 79.2\, A_v\, m_v = 0.792\, A_v \qquad \ldots (iii)$$

Subtracting [(*ii*) – (*iii*)], we have,

$$19.8 = 0.008\, A_v \quad \therefore \quad A_v = \frac{19.8}{0.008} = \mathbf{2475}$$

Putting the value of A_v (= 2475) in eq. (*i*), we have,

$$100 + 100 \times 2475 \times m_v = 2475$$

$$\therefore \quad m_v = \frac{2475 - 100}{100 \times 2475} = \mathbf{0.0096}$$

13.4 Advantages of Negative Voltage Feedback

The following are the advantages of negative voltage feedback in amplifiers :

(*i*) **Gain stability.** An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product $A_v m_v$ much greater than unity. Therefore, in the above relation, 1 can be neglected as compared to $A_v m_v$ and the expression becomes :

$$A_{vf} = \frac{A_v}{A_v m_v} = \frac{1}{m_v}$$

It may be seen that the gain now depends only upon feedback fraction m_v *i.e.*, on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

(*ii*) **Reduces non-linear distortion.** A large signal stage has non-linear distortion because its voltage gain changes at various points in the cycle. The negative voltage feedback reduces the non-linear distortion in large signal amplifiers. It can be proved mathematically that :

$$D_{vf} = \frac{D}{1 + A_v m_v}$$

where D = distortion in amplifier without feedback

D_{vf} = distortion in amplifier with negative feedback

It is clear that by applying negative voltage feedback to an amplifier, distortion is reduced by a factor $1 + A_v m_v$.

(*iii*) **Improves frequency response.** As feedback is usually obtained through a resistive network, therefore, voltage gain of the amplifier is *independent of signal frequency. The result is that voltage gain of the amplifier will be substantially constant over a wide range of signal frequency. The negative voltage feedback, therefore, improves the frequency response of the amplifier.

(*iv*) **Increases circuit stability.** The output of an ordinary amplifier is easily changed due to variations in ambient temperature, frequency and signal amplitude. This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilised or accurately fixed in value. This can be easily explained. Suppose the output of a negative voltage feedback amplifier has increased because of temperature change or due to some other reason. This means more negative feedback since feedback is being given from the output. This tends to oppose the increase in amplification and maintains it stable. The same is true should the output voltage decrease. Consequently, the circuit stability is considerably increased.

(*v*) **Increases input impedance and decreases output impedance.** The negative voltage feedback increases the input impedance and decreases the output impedance of amplifier. Such a change is profitable in practice as the amplifier can then serve the purpose of impedance matching.

(*a*) **Input impedance.** The increase in input impedance with negative voltage feedback can be explained by referring to Fig. 13.6. Suppose the input impedance of the amplifier is Z_{in} without feedback and Z'_{in} with negative feedback. Let us further assume that input current is i_1.

Referring to Fig. 13.6, we have,

$$e_g - m_v e_0 = i_1 Z_{in}$$

Now

$$\begin{aligned} e_g &= (e_g - m_v e_0) + m_v e_0 \\ &= (e_g - m_v e_0) + A_v m_v (e_g - m_v e_0) && [\because e_0 = A_v (e_g - m_v e_0)] \\ &= (e_g - m_v e_0)(1 + A_v m_v) \\ &= i_1 Z_{in} (1 + A_v m_v) && [\because e_g - m_v e_0 = i_1 Z_{in}] \end{aligned}$$

---

* $A_{vf} = 1/m_v$. Now m_v depends upon feedback circuit. As feedback circuit consists of resistive network, therefore, value of m_v is unaffected by change in signal frequency.

or $$\frac{e_g}{i_1} = Z_{in}(1 + A_v m_v)$$

But $e_g/i_1 = Z'_{in}$, the input impedance of the amplifier with negative voltage feedback.

$$\therefore \qquad Z'_{in} = Z_{in}(1 + A_v m_v)$$

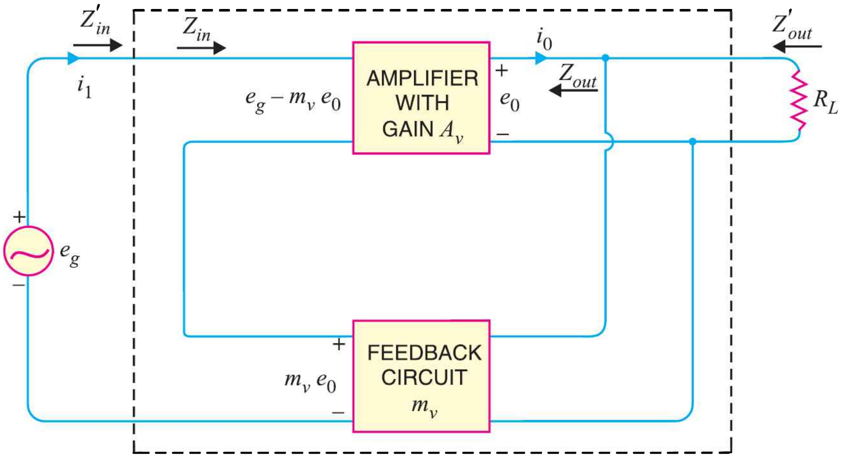


Fig. 13.6

It is clear that by applying negative voltage feedback, the input impedance of the amplifier is increased by a factor $1 + A_v m_v$. As $A_v m_v$ is much greater than unity, therefore, input impedance is increased considerably. This is an advantage, since the amplifier will now present less of a load to its source circuit.

(*b*) Output impedance. Following similar line, we can show that output impedance with negative voltage feedback is given by :

$$Z'_{out} = \frac{Z_{out}}{1 + A_v m_v}$$

where Z'_{out} = output impedance with negative voltage feedback

Z_{out} = output impedance without feedback

It is clear that by applying negative feedback, the output impedance of the amplifier is decreased by a factor $1 + A_v m_v$. This is an added benefit of using negative voltage feedback. With lower value of output impedance, the amplifier is much better suited to drive low impedance loads.

13.5 Feedback Circuit

The function of the feedback circuit is to return a fraction of the output voltage to the input of the amplifier. Fig. 13.7 shows the feedback circuit of negative voltage feedback amplifier. It is essentially a potential divider consisting of resistances R_1 and R_2. The output voltage of the amplifier is fed to this potential divider which gives the feedback voltage to the input.

Referring to Fig. 13.7, it is clear that :

$$\text{Voltage across } R_1 = \left(\frac{R_1}{R_1 + R_2}\right) e_0$$

$$\text{Feedback fraction, } m_v = \frac{\text{Voltage across } R_1}{e_0} = \frac{R_1}{R_1 + R_2}$$

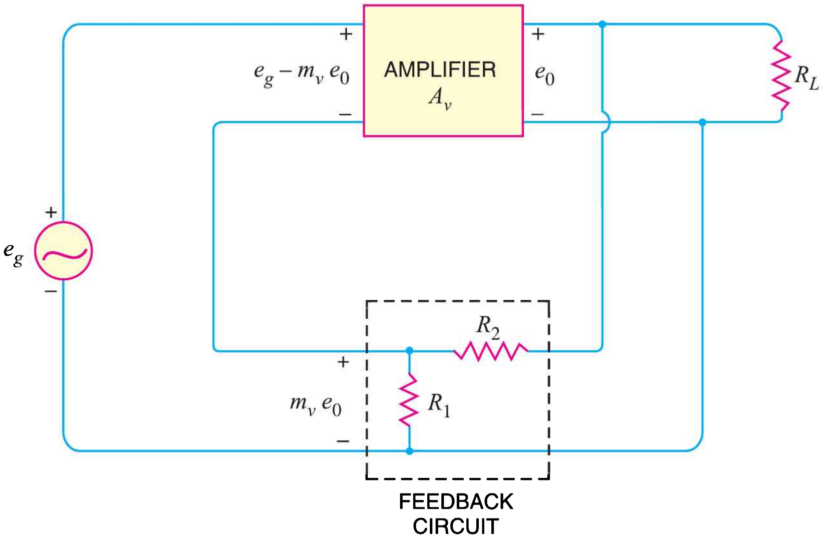

AMPLIFIER
A_v
$e_g - m_v e_0$
+
–
+
–
e_0
R_L
e_g
R_2
R_1
$m_v e_0$
FEEDBACK CIRCUIT

Fig. 13.7

Example 13.11. *Fig. 13.8 shows the negative voltage feedback amplifier. If the gain of the amplifier without feedback is 10,000, find :*

(i) feedback fraction (ii) overall voltage gain (iii) output voltage if input voltage is 1 mV.

Solution. $A_v = 10{,}000, \quad R_1 = 2\text{ k}\Omega, \quad R_2 = 18\text{ k}\Omega$

(*i*) Feedback fraction, $m_v = \dfrac{R_1}{R_1 + R_2} = \dfrac{2}{2+18} = \mathbf{0.1}$

(*ii*) Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v} = \frac{10{,}000}{1 + 10{,}000 \times 0.1} = \mathbf{10}$$

(*iii*) Output voltage $= A_{vf} \times$ input voltage

$= 10 \times 1\text{ mV} = \mathbf{10\text{ mV}}$

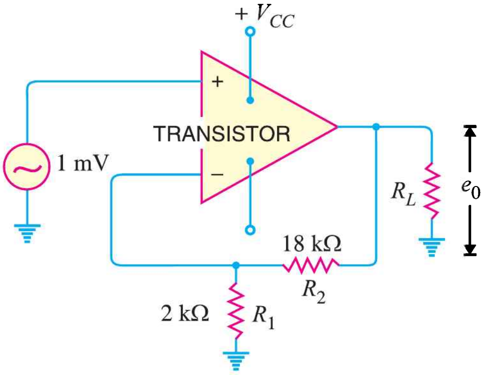

$+V_{CC}$
+
–
TRANSISTOR
1 mV
R_L
e_0
18 kΩ
R_2
2 kΩ
R_1

Fig. 13.8

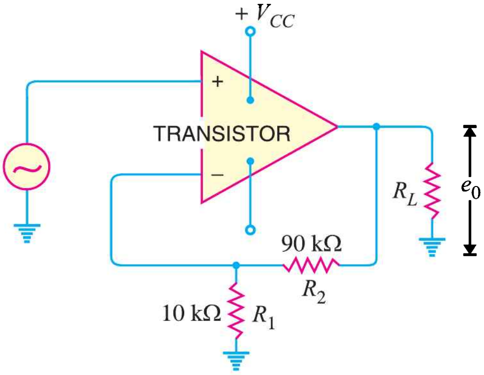

$+V_{CC}$
+
–
TRANSISTOR
R_L
e_0
90 kΩ
R_2
10 kΩ
R_1

Fig. 13.9

Example 13.12. *Fig. 13.9 shows the circuit of a negative voltage feedback amplifier. If without feedback, $A_v = 10{,}000$, $Z_{in} = 10\text{ k}\Omega$, $Z_{out} = 100\ \Omega$, find :*

(i) feedback fraction *(ii) gain with feedback*

(iii) input impedance with feedback *(iv) output impedance with feedback.*

Solution.

(*i*) Feedback fraction, $m_v = \frac{R_1}{R_1 + R_2} = \frac{10}{10 + 90} = \mathbf{0.1}$

(*ii*) Gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v} = \frac{10,000}{1 + 10,000 \times 0.1} = \mathbf{10}$$

(*iii*) With negative voltage feedback, input impedance is increased and is given by :

$$\underset{(feedback)}{Z'_{in}} = (1 + A_v m_v)\, Z_{in}$$

$$= (1 + 10,000 \times 0.1)\ 10\ \text{k}\Omega$$

$$= 1001 \times 10\ \text{k}\Omega$$

$$= \mathbf{10\ M\Omega}$$

(*iv*) With negative voltage feedback, output impedance is decreased and is given by ;

$$\underset{(feedback)}{Z'_{out}} = \frac{Z_{out}}{1 + A_v m_v} = \frac{100\ \Omega}{1 + 10,000 \times 0.1} = \frac{100}{1001} = \mathbf{0.1\ \Omega}$$

Example 13.13. *The gain and distortion of an amplifier are 150 and 5% respectively without feedback. If the stage has 10% of its output voltage applied as negative feedback, find the distortion of the amplifier with feedback.*

Solution.

Gain without feedback, $A_v = 150$

Distortion without feedback, $D = 5\% = 0.05$

Feedback fraction, $m_v = 10\% = 0.1$

If D_{vf} is the distortion with negative feedback, then,

$$D_{vf} = \frac{D}{1 + A_v m_v} = \frac{0.05}{1 + 150 \times 0.1} = 0.00313 = \mathbf{0.313\%}$$

It may be seen that by the application of negative voltage feedback, the amplifier distortion is reduced from 5% to 0.313%.

Example 13.14. *An amplifier has a gain of 1000 without feedback and cut-off frequencies are $f_1 = 1.5$ kHz and $f_2 = 501.5$ kHz. If 1% of output voltage of the amplifier is applied as negative feedback, what are the new cut-off frequencies ?*

Solution. $A_v = 1000$; $m_v = 0.01$

The new lower cut-off frequency with feedback is

$$f_{1(f)} = \frac{f_1}{1 + A_v m_v} = \frac{1.5\ \text{kHz}}{1 + 1000 \times 0.01} = \mathbf{136.4\ Hz}$$

The new upper cut-off frequency with feedback is

$$f_{2(f)} = f_2 (1 + m_v A_v) = (501.5\ \text{kHz})(1 + 1000 \times 0.01) = \mathbf{5.52\ MHz}$$

Note the effect of negative voltage feedback on the bandwidth of the amplifier. The lower cut-off frequency is decreased by a factor $(1 + m_v A_v)$ while upper cut-off frequency is increased by a factor $(1 + m_v A_v)$. In other words, the bandwidth of the amplifier is increased approximately by a factor $(1 + m_v A_v)$.

$$BW_{(f)} \simeq BW (1 + m_v A_v)$$

where BW = Bandwidth of the amplifier without feedback

$BW_{(f)}$ = Bandwidth of the amplifier with negative feedback

13.6 Principles of Negative Current Feedback

In this method, a fraction of output current is fedback to the input of the amplifier. In other words, the feedback current (I_f) is proportional to the output current (I_{out}) of the amplifier. Fig. 13.10 shows the principles of negative current feedback. This circuit is called current-shunt feedback circuit. A feedback resistor R_f is connected between input and output of the amplifier. This amplifier has a current gain of A_i without feedback. It means that a current I_1 at the input terminals of the amplifier will appear as $A_i I_1$ in the output circuit *i.e.*, $I_{out} = A_i I_1$. Now a fraction m_i of this output current is fedback to the input through R_f. The fact that arrowhead shows the feed current being fed forward is because it is *negative* feedback.

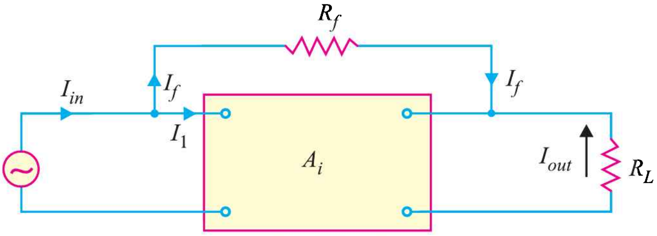


Fig. 13.10

Feedback current, $I_f = m_i I_{out}$

$$\therefore \quad \text{Feedback fraction, } m_i = \frac{I_f}{I_{out}} = \frac{\text{Feedback current}}{\text{Output current}}$$

Note that negative current feedback reduces the input current to the amplifier and hence its current gain.

13.7 Current Gain with Negative Current Feedback

Referring to Fig. 13.10, we have,

$$I_{in} = I_1 + I_f = I_1 + m_i I_{out}$$

But $I_{out} = A_i I_1$, where A_i is the current gain of the amplifier without feedback.

$$\therefore \quad I_{in} = I_1 + m_i A_i I_1 \qquad (\because I_{out} = A_i I_1)$$

∴ Current gain with negative current feedback is

$$A_{if} = \frac{I_{out}}{I_{in}} = \frac{A_i I_1}{I_1 + m_i A_i I_1}$$

or

$$A_{if} = \frac{A_i}{1 + m_i A_i}$$

This equation looks very much like that for the voltage gain of negative voltage feedback amplifier. The only difference is that we are dealing with current gain rather than the voltage gain. The following points may be noted carefully :

(*i*) The current gain of the amplifier without feedback is A_i. However, when negative current feedback is applied, the current gain is reduced by a factor $(1 + m_i A_i)$.

(*ii*) The feedback fraction (or current attenuation) m_i has a value between 0 and 1.

(*iii*) The negative current feedback does not affect the voltage gain of the amplifier.

Example 13.15. *The current gain of an amplifier is 200 without feedback. When negative current feedback is applied, determine the effective current gain of the amplifier. Given that current attenuation* $m_i = 0.012$.

Solution. $$A_{if} = \frac{A_i}{1 + m_i\, A_i}$$

Here $$A_i = 200\ ;\quad m_i = 0.012$$

$$\therefore \quad A_{if} = \frac{200}{1 + (0.012)\,(200)} = \mathbf{58.82}$$

13.8 Effects of Negative Current Feedback

The negative current feedback has the following effects on the performance of amplifiers :

(*i*) **Decreases the input impedance.** The negative current feedback decreases the input impedance of most amplifiers.

Let Z_{in} = Input impedance of the amplifier without feedback

Z'_{in} = Input impedance of the amplifier with negative current feedback

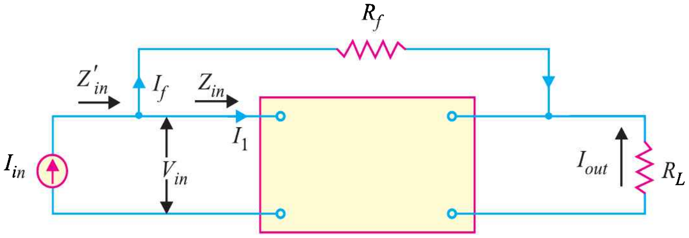


Fig. 13.11

Referring to Fig. 13.11, we have,

$$Z_{in} = \frac{V_{in}}{I_1}$$

and $$Z'_{in} = \frac{V_{in}}{I_{in}}$$

But $$V_{in} = I_1\, Z_{in} \quad \text{and} \quad I_{in} = I_1 + I_f = I_1 + m_i\, I_{out} = I_1 + m_i A_i I_1$$

$$\therefore \quad Z'_{in} = \frac{I_1\, Z_{in}}{I_1 + m_i\, A_i\, I_1} = \frac{Z_{in}}{1 + m_i\, A_i}$$

or $$Z'_{in} = \frac{Z_{in}}{1 + m_i\, A_i}$$

Thus the input impedance of the amplifier is decreased by the factor $(1 + m_i A_i)$. Note the primary difference between negative current feedback and negative voltage feedback. Negative current feedback *decreases* the input impedance of the amplifier while negative voltage feedback *increases* the input impedance of the amplifier.

(*ii*) **Increases the output impedance.** It can be proved that with negative current feedback, the output impedance of the amplifier is increased by a factor $(1 + m_i A_i)$.

$$Z'_{out} = Z_{out}\,(1 + m_i\, A_i)$$

where Z_{out} = output impedance of the amplifier without feedback

Z'_{out} = output impedance of the amplifier with negative current feedback

The reader may recall that with negative voltage feedback, the output impedance of the amplifier is decreased.

(*iii*) **Increases bandwidth.** It can be shown that with negative current feedback, the bandwidth of the amplifier is increased by the factor $(1 + m_i A_i)$.

$$BW' = BW (1 + m_i A_i)$$

where BW = Bandwidth of the amplifier without feedback

BW' = Bandwidth of the amplifier with negative current feedback

Example 13.16. *An amplifier has a current gain of 240 and input impedance of 15 kΩ without feedback. If negative current feedback (m_i = 0.015) is applied, what will be the input impedance of the amplifier ?*

Solution. $$Z'_{in} = \frac{Z_{in}}{1 + m_i A_i}$$

Here Z_{in} = 15 kΩ ; A_i = 240 ; m_i = 0.015

$$\therefore \quad Z'_{in} = \frac{15}{1 + (0.015)(240)} = \mathbf{3.26\ k\Omega}$$

Example 13.17. *An amplifier has a current gain of 200 and output impedance of 3 kΩ without feedback. If negative current feedback (m_i = 0.01) is applied; what is the output impedance of the amplifier ?*

Solution. $$Z'_{out} = Z_{out} (1 + m_i A_i)$$

Here Z_{out} = 3 kΩ ; A_i = 200 ; m_i = 0.01

$$\therefore \quad Z'_{out} = 3[1 + (0.01)(200)] = \mathbf{9\ k\Omega}$$

Example 13.18. *An amplifier has a current gain of 250 and a bandwidth of 400 kHz without feedback. If negative current feedback (m_i = 0.01) is applied, what is the bandwidth of the amplifier?*

Solution. $$BW' = BW (1 + m_i A_i)$$

Here BW = 400 kHz ; m_i = 0.01 ; A_i = 250

$$\therefore \quad BW' = 400[1 + (0.01) 250] = \mathbf{1400\ kHz}$$

13.9 Emitter Follower

It is a negative current feedback circuit. The emitter follower is a current amplifier that has no voltage gain. Its most important characteristic is that it has high input impedance and low output impedance. This makes it an ideal circuit for impedance matching.

Circuit details. Fig. 13.12 shows the circuit of an emitter follower. As you can see, it differs from the circuitry of a conventional *CE* amplifier by the absence of collector load and emitter bypass capacitor. The emitter resistance R_E itself acts as the load and a.c. output voltage (V_{out}) is taken across R_E. The biasing is generally provided by voltage-divider method or by base resistor method. The following points are worth noting about the emitter follower :

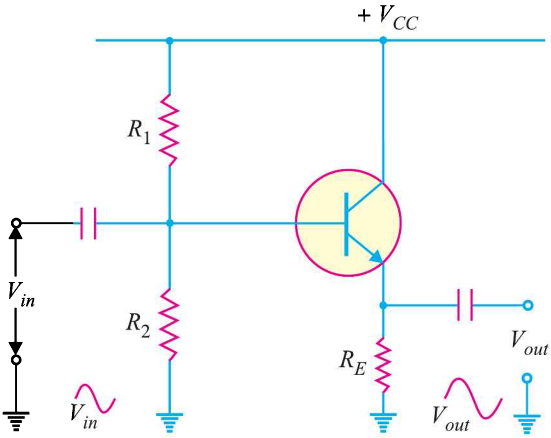


Fig. 13.12

(*i*) There is neither collector resistor in the circuit nor there is emitter bypass capacitor. These are the two circuit recognition features of the emitter follower.

(*ii*) Since the collector is at *ac* ground, this circuit is also known as *common collector* (*CC*) *amplifier.*

Operation. The input voltage is applied between base and emitter and the resulting a.c. emitter current produces an output voltage $i_e R_E$ across the emitter resistance. This voltage opposes the input voltage, thus providing negative feedback. Clearly, it is a negative current feedback circuit since the voltage fedback is proportional to the emitter current *i.e.*, output current. It is called emitter follower because the output voltage follows the input voltage.

Characteristics. The major characteristics of the emitter follower are :

(*i*) No voltage gain. In fact, the voltage gain of an emitter follower is close to 1.

(*ii*) Relatively high current gain and power gain.

(*iii*) High input impedance and low output impedance.

(*iv*) Input and output *ac* voltages are in phase.

13.10 D.C. Analysis of Emitter Follower

The d.c. analysis of an emitter follower is made in the same way as the voltage divider bias circuit of a CE amplifier. Thus referring to Fig. 13.12 above, we have,

$$\text{Voltage across } R_2,\ V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

$$\text{Emitter current, } I_E = \frac{V_E}{R_E} = \frac{V_2 - V_{BE}}{R_E}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - V_E$$

D.C. Load Line. The d.c. load line of emitter follower can be constructed by locating the two end points *viz.*, $I_{C(sat)}$ and $V_{CE(off)}$.

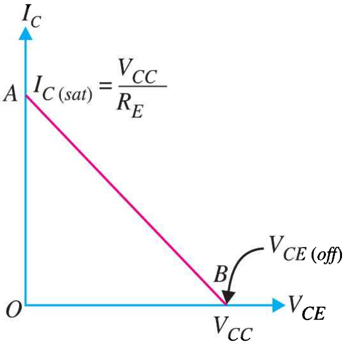


Fig. 13.13

(*i*) When the transistor is saturated, $V_{CE} = 0$.

$$\therefore \quad I_{C(sat)} = \frac{V_{CC}}{R_E}$$

This locates the point *A* ($OA = V_{CC}/R_E$) of the d.c. load line as shown in Fig. 13.13.

(*ii*) When the transistor is cut off, $I_C = 0$. Therefore, $V_{CE(off)} = V_{CC}$. This locates the point *B* ($OB = V_{CC}$) of the d.c. load line.

By joining points *A* and *B*, d.c. load line *AB* is constructed.

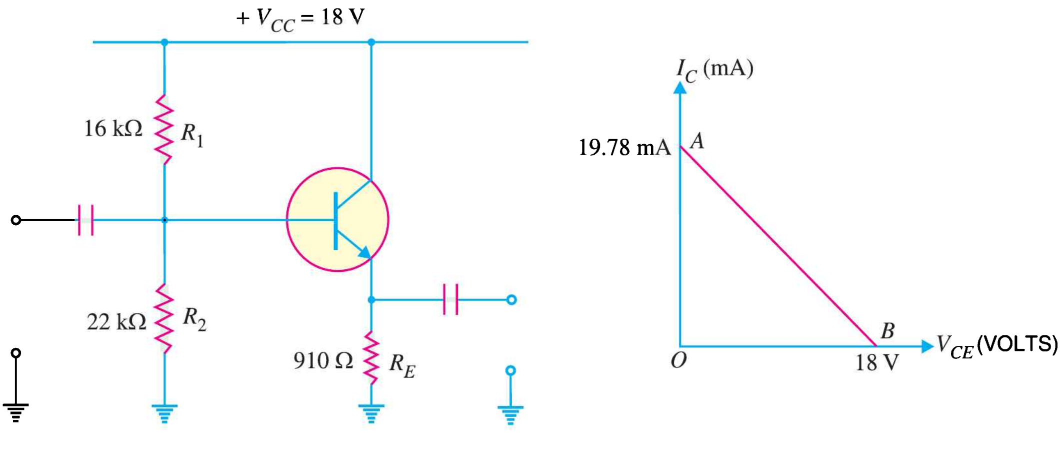
Example 13.19. *For the emitter follower circuit shown in Fig. 13.14 (i), find V_E and I_E. Also draw the dc load line for this circuit.*

Solution.

$$\text{Voltage across } R_2,\ V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{18}{16 + 22} \times 22 = 10.42 \text{ V}$$

$$\text{Voltage across } R_E,\ V_E = V_2 - V_{BE} = 10.42 - 0.7 = \mathbf{9.72\ V}$$

$$\text{Emitter current, } I_E = \frac{V_E}{R_E} = \frac{9.72 \text{ V}}{910\ \Omega} = \mathbf{10.68\ mA}$$



(*i*) (*ii*)

Fig. 13.14

D.C. load line

$$I_{C\,(sat)} = \frac{V_{CC}}{R_E} = \frac{18\text{ V}}{910\ \Omega} = 19.78\text{ mA}$$

This locates the point *A* (*OA* = 19.78 mA) of the d.c. load line.

$$V_{CE(off)} = V_{CC} = 18\text{ V}$$

This locates point *B* (*OB* = 18 V) of the d.c. load line.

By joining points *A* and *B*, d.c. load line *AB* is constructed [See Fig. 13.14 (*ii*)].

13.11 Voltage Gain of Emitter Follower

Fig. 13.15 shows the emitter follower circuit. Since the emitter resistor is not bypassed by a capacitor, the *a.c.* equivalent circuit of emitter follower will be as shown in Fig. 13.16. The ac resistance r_E of the emitter circuit is given by :

$$r_E = r'_e + R_E \qquad \text{where } r'_e = \frac{25\text{ mV}}{I_E}$$

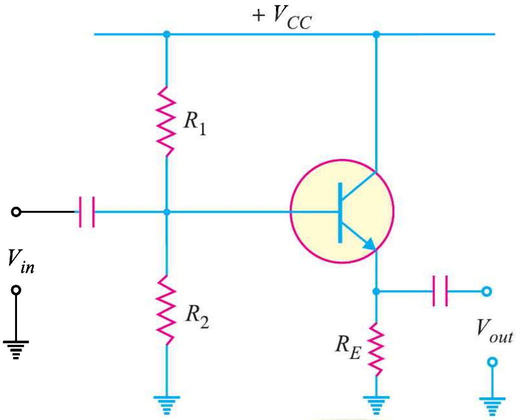


Fig. 13.15

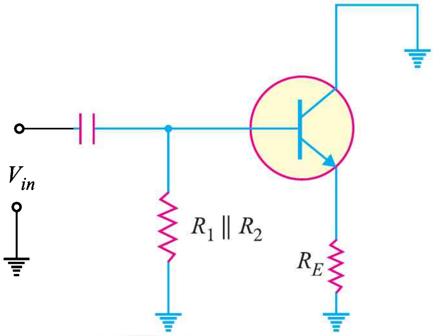


Fig. 13.16

In order to find the voltage gain of the emitter follower, let us replace the transistor in Fig. 13.16 by its equivalent circuit. The circuit then becomes as shown in Fig. 13.17.

Note that input voltage is applied across the *ac* resistance of the emitter circuit *i.e.*, (r'_e + R_E). Assuming the emitter diode to be ideal,

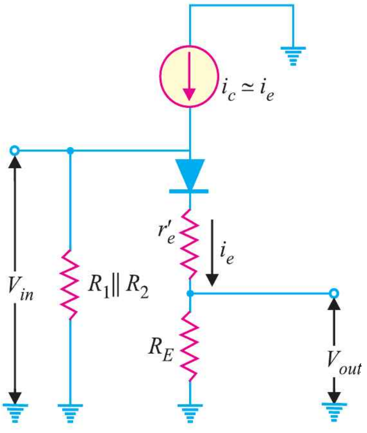


Fig. 13.17

$$\text{Output voltage,} \quad V_{out} = i_e R_E$$

$$\text{Input voltage,} \quad V_{in} = i_e (r'_e + R_E)$$

∴ Voltage gain of emitter follower is

$$A_v = \frac{V_{out}}{V_{in}} = \frac{i_e R_E}{i_e (r'_e + R_E)} = \frac{R_E}{r'_e + R_E}$$

or

$$A_v = \frac{R_E}{r'_e + R_E}$$

In most practical applications, $R_E >> r'_e$ so that $A_v \simeq 1$.

In practice, the voltage gain of an emitter follower is between 0.8 and 0.999.

Example 13.20. *Determine the voltage gain of the emitter follower circuit shown in Fig. 13.18.*

Solution.

$$\text{Voltage gain,} \quad A_v = \frac{R_E}{r'_e + R_E}$$

Now

$$r'_e = \frac{25 \text{ mV}}{I_E}$$

$$\text{Voltage across } R_2, \; V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{10}{10 + 10} \times 10 = 5 \text{ V}$$

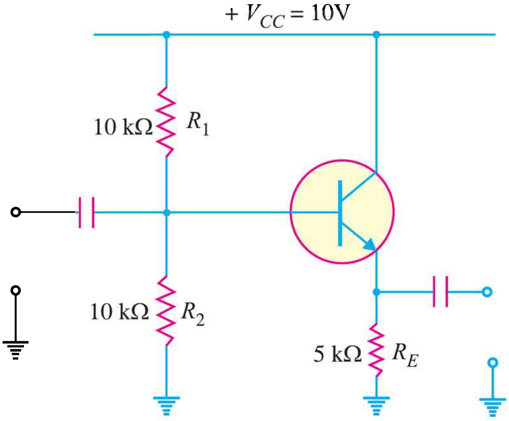


Fig. 13.18

$$\text{Voltage across } R_E, \; V_E = V_2 - V_{BE} = 5 - 0.7 = 4.3 \text{ V}$$

$$\therefore \quad \text{Emitter current,} \; I_E = \frac{V_E}{R_E} = \frac{4.3 \text{ V}}{5 \text{ k}\Omega} = 0.86 \text{ mA}$$

$$\therefore \quad r'_e = \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{0.86 \text{ mA}} = 29.1 \; \Omega$$

$$\therefore \quad \text{Voltage gain,} \; A_v = \frac{R_E}{r'_e + R_E} = \frac{5000}{29.1 + 5000} = \mathbf{0.994}$$

Example 13.21. *If in the above example, a load of 5 kΩ is added to the emitter follower, what will be the voltage gain of the circuit ?*

Solution. When a load of 5 kΩ is added to the emitter follower, the circuit becomes as shown in

Fig. 13.19. The coupling capacitor acts as a short for a.c. signal so that R_E and R_L are in parallel. Therefore, the external emitter resistance R_E changes to R'_E where

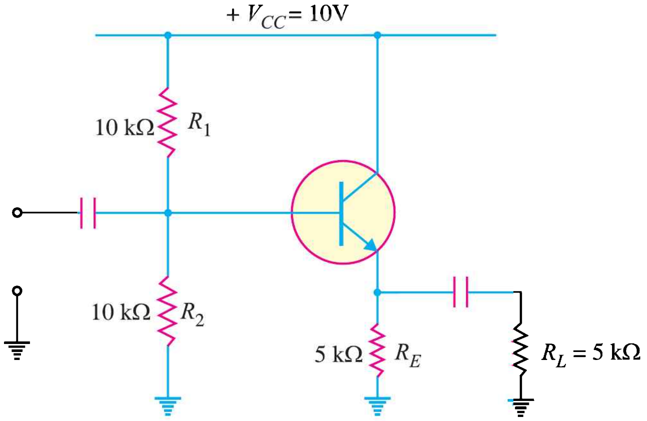


Fig. 13.19

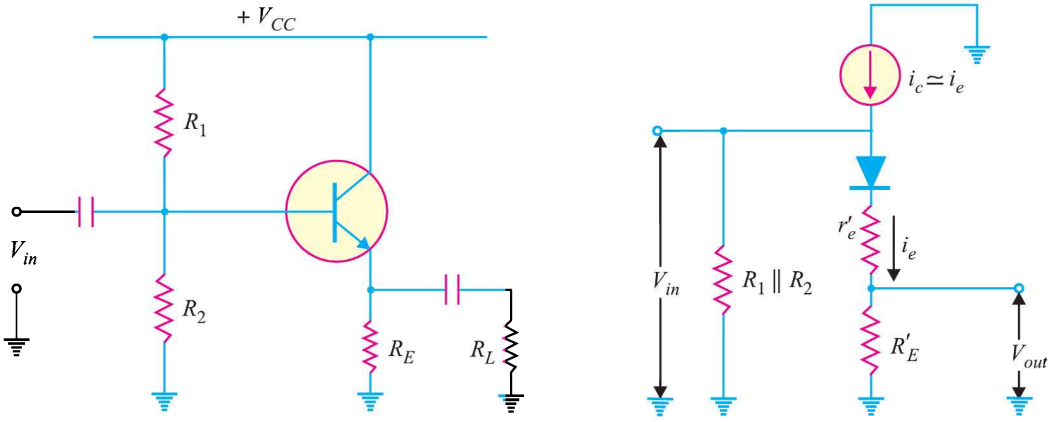
$$R'_E = R_E \parallel R_L = 5\text{ k}\Omega \parallel 5\text{ k}\Omega = 2.5\text{ k}\Omega$$

$$\text{Voltage gain, } A_v = \frac{R'_E}{r'_e + R'_E} = \frac{2500}{29.1 + 2500} = \mathbf{0.988}$$

Comments. This is the same example as example 13.20 except that load is added. Note the loading effect on the voltage gain of an emitter follower. When load is added to the emitter follower, the voltage gain drops from 0.994 to 0.988. This is really a small change. On the other hand, when a CE amplifier is loaded, there is drastic change in voltage gain. This is yet another difference between the emitter follower and CE amplifier.

13.12 Input Impedance of Emitter Follower

Fig. 13.20 (*i*) shows the circuit of a loaded emitter follower. The a.c. equivalent circuit with T model is shown in Fig. 13.20 (*ii*).



(*i*) (*ii*)

Fig. 13.20

As for CE amplifier, the input impedance of emitter follower is the combined effect of biasing resistors (R_1 and R_2) and the input impedance of transistor base [Z_{in} (*base*)]. Since these resistances are in parallel to the *ac* signal, the input impedance Z_{in} of the emitter follower is given by :

$$Z_{in} = R_1 \,||\, R_2 \,||\, Z_{in(\text{base})}$$

where $$Z_{in\,(base)} = \beta\,(r'_e + R'_E)$$

Now $$r'_e = \frac{25\text{ mV}}{I_E} \quad \text{and} \quad R'_E = R_E \,||\, R_L$$

Note. In an emitter follower, impedance of base [*i.e.*, Z_{in} (*base*)] is generally very large as compared to $R_1 \,||\, R_2$. Consequently, Z_{in} (*base*) can be ignored. As a result, approximate input impedance of the emitter follower is given by :

$$Z_{in} = R_1 \,||\, R_2$$

Example 13.22. *For the emitter follower circuit shown in Fig. 13.21, find the input impedance.*

Solution.

$$\text{Voltage across } R_2,\; V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{10}{10+10} \times 10 = 5\text{ V}$$

$$\text{Voltage across } R_E,\; V_E = V_2 - V_{BE} = 5 - 0.7 = 4.3\text{ V}$$

$$\therefore \quad \text{Emitter current, } I_E = \frac{V_E}{R_E} = \frac{4.3\text{ V}}{4.3\text{ k}\Omega} = 1\text{ mA}$$

$$\therefore \quad \text{A.C. emitter resistance, } r'_e = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{1\text{ mA}} = 25\ \Omega$$

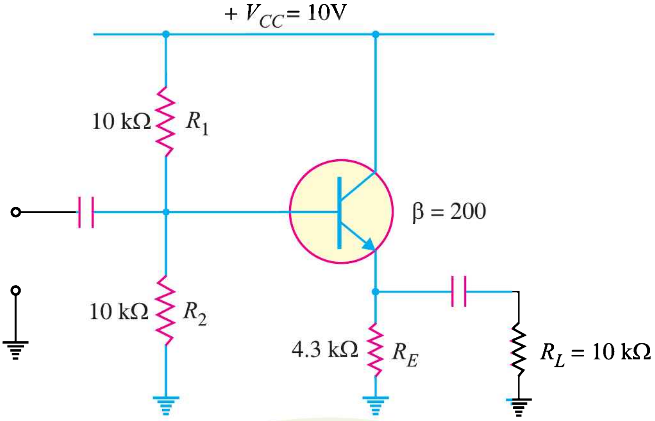


Fig. 13.21

Effective external emitter resistance is

$$R'_E = R_E \,||\, R_L = 4.3\text{ k}\Omega \,||\, 10\text{ k}\Omega = 3\text{ k}\Omega$$

$$\therefore \quad Z_{in\,(base)} = \beta\,(r'_e + R'_E) = 200\,(0.025 + 3) = 605\text{ k}\Omega$$

∴ Input impedance of the emitter follower is

$$Z_{in} = R_1 \,||\, R_2 \,||\, Z_{in\,(base)}$$
$$= 10\text{ k}\Omega \,||\, 10\text{ k}\Omega \,||\, 605\text{ k}\Omega$$
$$= 5\text{ k}\Omega \,||\, 605\text{ k}\Omega = \mathbf{4.96\text{ k}\Omega}$$

Note. Since 605 kΩ is much larger than $R_1 \,||\, R_2$ (= 5kΩ), the former can be ignored. Therefore, approximate input impedance of emitter follower is given by :

$$Z_{in} = R_1 \,||\, R_2 = 10\text{ k}\Omega \,||\, 10\text{ k}\Omega = 5\text{ k}\Omega$$

13.13 Output Impedance of Emitter Follower

The output impedance of a circuit is the impedance that the circuit offers to the load. When load is connected to the circuit, the output impedance acts as the source impedance for the load. Fig. 13.22 shows the circuit of emitter follower. Here R_s is the output resistance of amplifier voltage source.

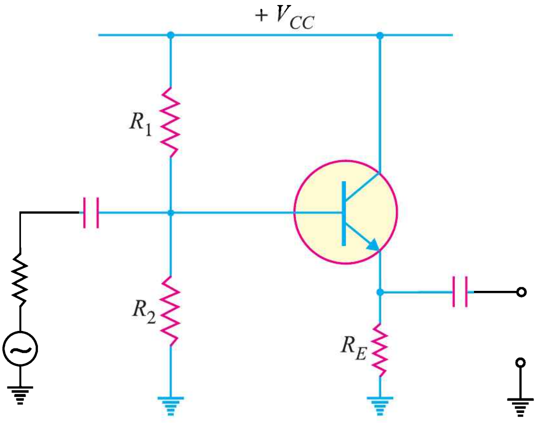


Fig. 13.22

It can be proved that the output impedance Z_{out} of the emitter follower is given by :

$$Z_{out} = R_E \parallel \left(r_e' + \frac{R_{in}'}{\beta} \right)$$

where $R_{in}' = R_1 \parallel R_2 \parallel R_s$

In practical circuits, the value of R_E is large enough to be ignored. For this reason, the output impedance of emitter follower is approximately given by :

$$Z_{out} = r_e' + \frac{R_{in}'}{\beta}$$

Example 13.23. *Determine the output impedance of the emitter follower shown in Fig. 13.23. Given that $r_e' = 20\ \Omega$.*

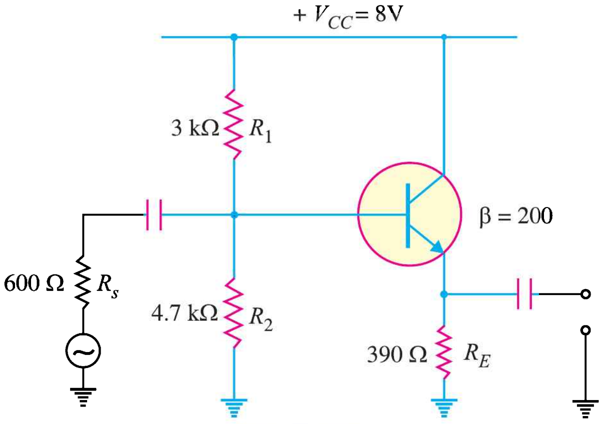


Fig. 13.23

Solution. $Z_{out} = r_e' + \dfrac{R_{in}'}{\beta}$

Now $R_{in}' = R_1 \parallel R_2 \parallel R_s$

$= 3\ \text{k}\Omega \parallel 4.7\ \text{k}\Omega \parallel 600\ \Omega = 452\ \Omega$

$\therefore$ $Z_{out} = 20 + \dfrac{452}{200} = 20 + 2.3 = \mathbf{22.3\ \Omega}$

Note that output impedance of the emitter follower is very low. On the other hand, it has high input impedance. This property makes the emitter follower a perfect circuit for connecting a low impedance load to a high-impedance source.

13.14 Applications of Emitter Follower

The emitter follower has the following principal applications :

(*i*) To provide current amplification with no voltage gain.

(*ii*) Impedance matching.

(*i*) Current amplification without voltage gain. We know that an emitter follower is a current amplifier that has no voltage gain ($A_v \simeq 1$). There are many instances (especially in digital electronics) where an increase in current is required but no increase in voltage is needed. In such a situation, an emitter follower can be used. For example, consider the two stage amplifier circuit as shown in Fig. 13.24. Suppose this 2-stage amplifier has the desired voltage gain but current gain of this multistage amplifier is insufficient. In that case, we can use an emitter follower to increase the current gain without increasing the voltage gain.

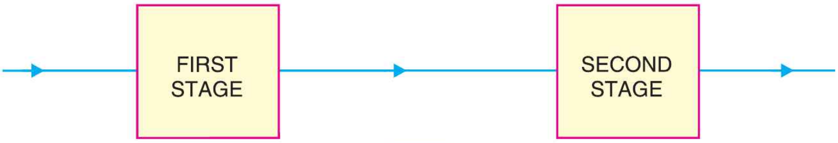


Fig. 13.24

(*ii*) Impedance matching. We know that an emitter follower has high input impedance and low output impedance. This makes the emitter follower an ideal circuit for impedance matching. Fig. 13.25 shows the impedance matching by an emitter follower. Here the output impedance of the source is 120 kΩ while that of load is 20 Ω. The emitter follower has an input impedance of 120 kΩ and output impedance of 22 Ω. It is connected between high-impedance source and low impedance load. The net result of this arrangement is that maximum power is transferred from the original source to the original load. When an emitter follower is used for this purpose, it is called a *buffer amplifier.*

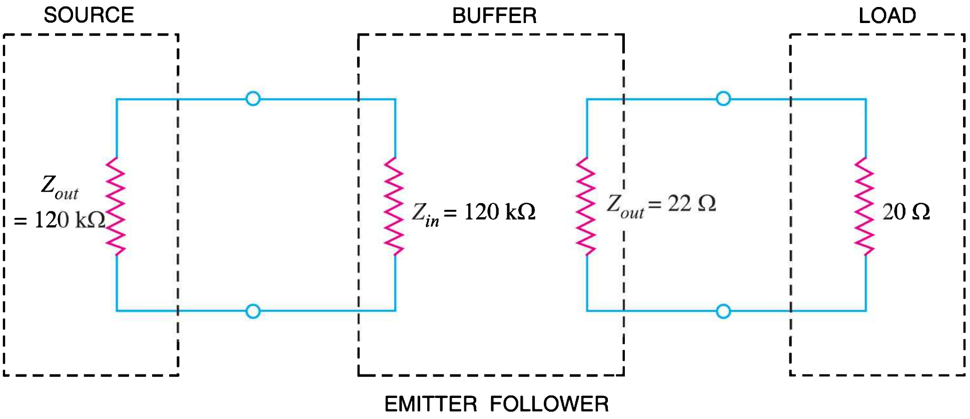


Fig. 13.25

It may be noted that the job of impedance matching can also be accomplished by a transformer. However, emitter follower is preferred for this purpose. It is because emitter follower is not only more convenient than a transformer but it also has much better frequency response *i.e.*, it works well over a large frequency range.

13.15 Darlington Amplifier

Sometimes, the current gain and input impedance of an emitter follower are insufficient to meet the requirement. In order to increase the overall values of circuit current gain (A_i) and input impedance, two transistors are connected in series in emitter follower configuration as shown in Fig. 13.26. Such a circuit is called *Darlington amplifier*. Note that emitter of first transistor is connected to the base of the second transistor and the collector terminals of the two transistors are connected together. The result is that emitter current of the first transistor is the base current of the second transistor. Therefore, the current gain of the pair is equal to product of individual current gains *i.e.*

$$^*\beta = \beta_1 \beta_2$$

Note that high current gain is achieved with a minimum use of components.

The biasing analysis is similar to that for one transistor except that two V_{BE} drops are to be considered. Thus referring to Fig. 13.26,

$$\text{Voltage across } R_2,\ V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

$$\text{Voltage across } R_E,\ V_E = V_2 - 2V_{BE}$$

$$\text{Current through } R_E,\ I_{E2} = \frac{V_2 - 2V_{BE}}{R_E}$$

Since the transistors are directly coupled, $I_{E1} = I_{B2}$. Now $I_{B2} = I_{E2}/\beta_2$.

$$\therefore \qquad I_{E1} = \frac{I_{E2}}{\beta_2}$$

Input impedance of the darlington amplifier is

$$Z_{in} = \beta_1\beta_2 R_E \text{ ... neglecting } r'_e$$

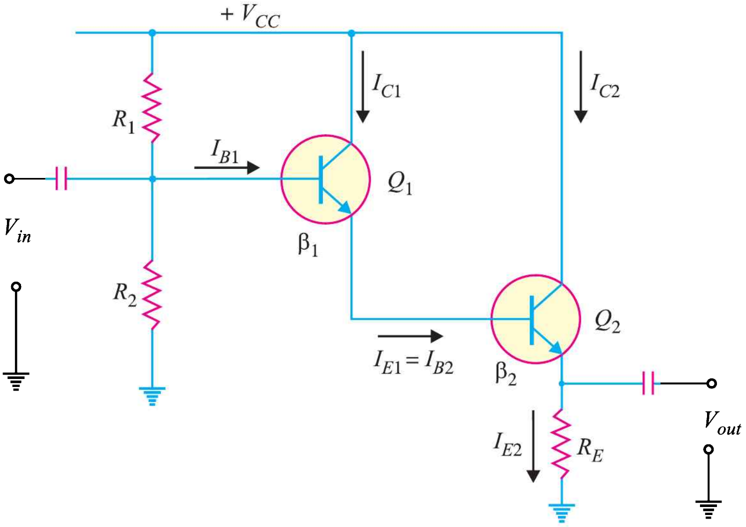


Fig. 13.26

In practice, the two transistors are put inside a single transistor housing and three terminals *E*, *B* and *C* are brought out as shown in Fig. 13.27. This three terminal device is known as a Darlington transistor. The Darlington transistor acts like a single transistor that has high current gain and high input impedance.

---

* $I_{E1} = \beta_1 I_{B1} \quad (\because I_{E1} \simeq I_{C1})$

Now I_{E1} is the base current of Q_2 *i.e.* $I_{E1} = I_{B2}$.

Now $I_{E2} = \beta_2 I_{B2} = \beta_2 I_{E1} = \beta_2 \beta_1 I_{B1}$

$$\therefore \text{ Overall current gain, } \beta = \frac{I_{E2}}{I_{B1}} = \frac{\beta_1 \beta_2 I_{B1}}{I_{B1}} = \beta_1 \beta_2$$

Characteristics. The following are the important characteristics of Darlington amplifier :

(*i*) Extremely high input impedance (MΩ).

(*ii*) Extremely high current gain (several thousands).

(*iii*) Extremely low output impedance (a few Ω).

Since the characteristics of the Darlington amplifier are basically the same as those of the emitter follower, the two circuits are used for similar applications. When you need higher input impedance and current gain and/or lower output impedance than the standard emitter follower can provide, you use a Darlington amplifier. Darlington transistors are commonly available. Like standard transistors, they have only three terminals but they have much higher values of current gain and input impedance.

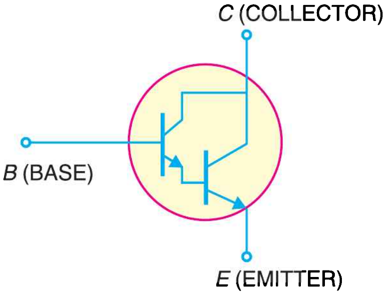


Fig. 13.27

Example 13.24. *Determine (i) d.c. value of current in R_E (ii) input impedance of the Darlington amplifier shown in Fig. 13.28.*

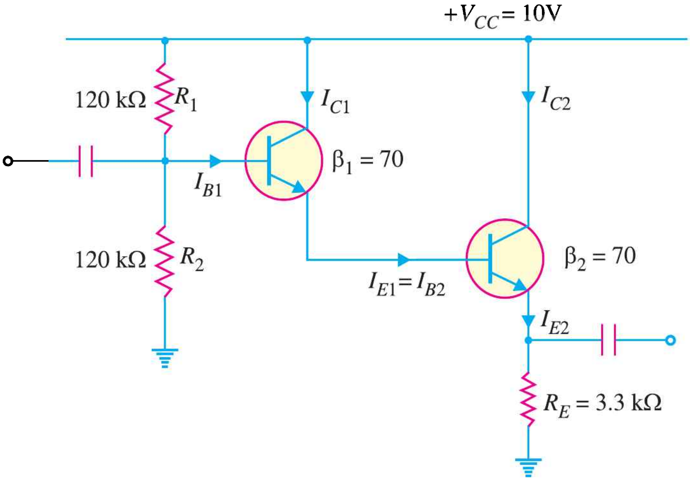


Fig. 13.28

Solution.

(*i*) Voltage across R_2, $V_2 = \dfrac{V_{CC}}{R_1 + R_2} \times R_2 = \dfrac{10V}{120\text{ k}\Omega + 120\text{ k}\Omega} \times 120\text{ k}\Omega = 5V$

D.C. current in R_E, $I_{E2} = \dfrac{V_2 - 2V_{BE}}{R_E} = \dfrac{5V - 2 \times 0.7V}{3.3\text{ k}\Omega} = \dfrac{3.6V}{3.3\text{ k}\Omega} = \mathbf{1.09\text{ mA}}$

(*ii*) Input impedance, $Z_{in} = \beta_1 \beta_2 R_E$

$= (70)(70)(3.3\text{ k}\Omega) = \mathbf{16.17\text{ M}\Omega}$

This example illustrates that the input impedance of Darlington amplifier is much higher than that of an ordinary transistor.

Example 13.25. *For the Darlington amplifier in Fig. 13.29, find (i) the d.c. levels of both the transistors and (ii) a.c. emitter resistances of both transistors.*

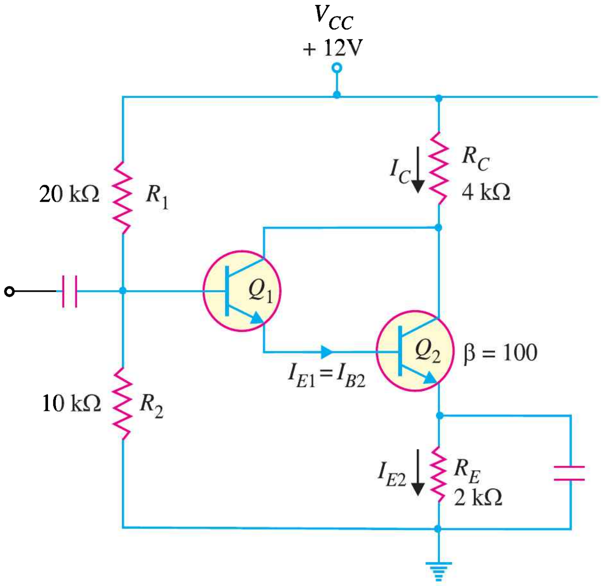


Fig. 13.29

Solution.

(*i*) **D.C. Bias Levels**

$$\text{Base voltage of } Q_1,\ V_{B1} = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{12\text{V}}{20\text{ k}\Omega + 10\text{ k}\Omega} \times 10\text{ k}\Omega = \mathbf{4V}$$

$$\text{Emitter voltage of } Q_1,\ V_{E1} = V_{B1} - V_{BE} = 4\text{V} - 0.7\text{V} = \mathbf{3.3V}$$

$$\text{Base voltage of } Q_2,\ V_{B2} = V_{E1} = \mathbf{3.3V}$$

$$\text{Emitter voltage of } Q_2,\ V_{E2} = V_{B2} - V_{BE} = 3.3\text{V} - 0.7\text{V} = \mathbf{2.6V}$$

$$\text{Emitter current of } Q_2,\ I_{E2} = \frac{V_{E2}}{R_E} = \frac{2.6\text{V}}{2\text{ k}\Omega} = \mathbf{1.3\ mA}$$

$$\text{Emitter current of } Q_1,\ I_{E1} = \frac{I_{E2}}{\beta} = \frac{1.3\text{ mA}}{100} = \mathbf{0.013\ mA}$$

(*ii*) **A.C. Analysis**

$$\text{A.C. emitter resistance of } Q_1,\ r'_{e1} = \frac{25\text{ mV}}{I_{E1}} = \frac{25\text{ mV}}{0.013\text{ mA}} = \mathbf{1923\Omega}$$

$$\text{A.C. emitter resistance of } Q_2,\ r'_{e2} = \frac{25\text{ mV}}{I_{E2}} = \frac{25\text{ mV}}{1.3\text{ mA}} = \mathbf{19.23\Omega}$$

MULTIPLE-CHOICE QUESTIONS

1. When negative voltage feedback is applied to an amplifier, its voltage gain ....

(*i*) is increased (*ii*) is reduced

(*iii*) remains the same

(*iv*) none of the above

2. The value of negative feedback fraction is always ....

(*i*) less than 1 (*ii*) more than 1

(*iii*) equal to 1 (*iv*) none of the above

3. If the output of an amplifier is 10 V and

100 mV from the output is fed back to the input, then feedback fraction is ....

(*i*) 10 (*ii*) 0.1
(*iii*) 0.01 (*iv*) 0.15

4. The gain of an amplifier without feedback is 100 *db*. If a negative feedback of 3 *db* is applied, the gain of the amplifier will become ....

(*i*) 101.5 *db* (*ii*) 300 *db*
(*iii*) 103 *db* (*iv*) 97 *db*

5. If the feedback fraction of an amplifier is 0.01, then voltage gain with negative voltage feedback is approximately ....

(*i*) 500 (*ii*) 100
(*iii*) 1000 (*iv*) 5000

6. A feedback circuit usually employs .... network.

(*i*) resistive (*ii*) capacitive
(*iii*) inductive (*iv*) none of the above

7. The gain of an amplifier with feedback is known as .... gain.

(*i*) resonant (*ii*) open loop
(*iii*) closed loop (*iv*) none of the above

8. When voltage feedback (negative) is applied to an amplifier, its input impedance ....

(*i*) is decreased (*ii*) is increased
(*iii*) remains the same
(*iv*) none of the above

9. When current feedback (negative) is applied to an amplifier, its input impedance ....

(*i*) is decreased (*ii*) is increased
(*iii*) remains the same
(*iv*) none of the above

10. Negative feedback is employed in ....

(*i*) oscillators (*ii*) rectifiers
(*iii*) amplifiers (*iv*) none of the above

11. Emitter follower is used for ....

(*i*) current gain
(*ii*) impedance matching
(*iii*) voltage gain (*iv*) none of the above

12. The voltage gain of an emitter follower is ...

(*i*) much less than 1
(*ii*) approximately equal to 1
(*iii*) greater than 1 (*iv*) none of the above

13. When current feedback (negative) is applied to an amplifier, its output impedance ......

(*i*) is increased
(*ii*) is decreased
(*iii*) remains the same
(*iv*) none of the above

14. Emitter follower is a .... circuit.

(*i*) voltage feedback
(*ii*) current feedback
(*iii*) both voltage and current feedback
(*iv*) none of the above

15. If voltage feedback (negative) is applied to an amplifier, its output impedance ....

(*i*) remains the same
(*ii*) is increased (*iii*) is decreased
(*iv*) none of the above

16. When negative voltage feedback is applied to an amplifier, its bandwidth ....

(*i*) is increased (*ii*) is decreased
(*iii*) remains the same
(*iv*) insufficient data

17. An emitter follower has ..... input impedance.

(*i*) zero (*ii*) low
(*iii*) high (*iv*) none of the above

18. If voltage gain without feedback and feedback fraction are A_v and m_v respectively, then gain with negative voltage feedback is ....

(*i*) $\dfrac{A_v}{1 - A_v\, m_v}$ (*ii*) $\dfrac{A_v}{1 + A_v\, m_v}$
(*iii*) $\dfrac{1 + A_v\, m_v}{A_v}$ (*iv*) $(1 + A_v\, m_v)\, A_v$

19. The output impedance of an emitter follower is ....

(*i*) high (*ii*) very high
(*iii*) almost zero (*iv*) low

20. The approximate voltage gain of an amplifier with negative voltage feedback (feedback fraction being m_v) is ....

(*i*) $1/m_v$ (*ii*) m_v
(*iii*) $\dfrac{1}{1 + m_v}$ (*iv*) $1 - m_v$

21. If A_v and A_{fb} are the voltage gains of an amplifier without feedback and with negative feedback respectively, then feedback fraction is ....

(*i*) $\frac{1}{A_v} - \frac{1}{A_{fb}}$ (*ii*) $\frac{1}{A_v} + \frac{1}{A_{fb}}$

(*iii*) $\frac{A_v}{A_{fb}} + \frac{1}{A_v}$ (*iv*) $\frac{1}{A_{fb}} - \frac{1}{A_v}$

22. In the expression for voltage gain with negative voltage feedback, the term $1 + A_m m_v$ is known as ....

(*i*) gain factor (*ii*) feedback factor

(*iii*) sacrifice factor (*iv*) none of the above

23. If the output impedance of an amplifier is Z_{out} without feedback, then with negative voltage feedback, its value will be ....

(*i*) $\frac{Z_{out}}{1 + A_v m_v}$ (*ii*) $Z_{out}(1 + A_v m_v)$

(*iii*) $\frac{1 + A_v m_v}{Z_{out}}$ (*iv*) $Z_{out}(1 - A_v m_v)$

24. If the input impedance of an amplifier is Z_{in} without feedback, then with negative voltage feedback, its value will be ....

(*i*) $\frac{Z_{in}}{1 + A_v m_v}$ (*ii*) $Z_{in}(1 + A_v m_v)$

(*iii*) $\frac{1 + A_v m_v}{Z_{in}}$ (*iv*) $Z_{in}(1 - A_v m_v)$

25. Feedback circuit .... frequency.

(*i*) is independent of

(*ii*) is strongly dependent on

(*iii*) is moderately dependent on

(*iv*) none of the above

26. The basic purpose of applying negative voltage feedback is to ....

(*i*) increase voltage gain

(*ii*) reduce distortion

(*iii*) keep the temperature within limits

(*iv*) none of the above

27. If the voltage gain of an amplifier without feedback is 20 and with negative voltage feedback it is 12, then feedback fraction is ....

(*i*) 5/3 (*ii*) 3/5

(*iii*) 1/5 (*iv*) 0.033

28. In an emitter follower, we employ ...... negative current feedback.

(*i*) 50% (*ii*) 25%

(*iii*) 100% (*iv*) 75%

29. An amplifier has an open loop voltage gain of 1,00,000. With negative voltage feedback, the voltage gain is reduced to 100. What is the sacrifice factor ?

(*i*) 1000 (*ii*) 100

(*iii*) 5000 (*iv*) none of the above

30. In the above question, what will happen to circuit performance ?

(*i*) distortion is increased 1000 times

(*ii*) input impedance is increased 1000 times

(*iii*) output impedance is increased 1000 times

(*iv*) none of the above

31. The non-linear distortion of an amplifier is D without feedback. The amplifier has an open-loop voltage gain of A_v and feedback fraction is m_v. With negative voltage feedback, the non-linear distortion will be ....

(*i*) $D(1 + A_v m_v)$ (*ii*) $D(1 - A_v m_v)$

(*iii*) $\frac{1 + A_v m_v}{D}$ (*iv*) $\frac{D}{1 + A_v m_v}$

32. The output and input voltages of an emitter follower have a phase difference of ....

(*i*) 180° (*ii*) 90°

(*iii*) 0° (*iv*) 270°

33. It is most necessary to control signal-to-noise ratio at ....

(*i*) initial stage (*ii*) driver stage

(*iii*) output stage (*iv*) detector stage

34. In order to obtain good gain stability in a negative voltage feedback amplifier (A_v = voltage gain without feedback ; m_v = feedback fraction), ...

(*i*) $A_v m_v = 1$ (*ii*) $A_v m_v >> 1$

(*iii*) $A_v m_v < 1$ (*iv*) none of the above

35. Emitter follower is also known as ....

(*i*) grounded emitter circuit

(*ii*) grounded base circuit

(*iii*) grounded collector circuit

(*iv*) none of the above

Answers to Multiple-Choice Questions

1.	*(ii)*	**2.**	*(i)*	**3.**	*(iii)*	**4.**	*(iv)*	**5.**	*(ii)*
6.	*(i)*	**7.**	*(iii)*	**8.**	*(ii)*	**9.**	*(i)*	**10.**	*(iii)*
11.	*(ii)*	**12.**	*(ii)*	**13.**	*(i)*	**14.**	*(ii)*	**15.**	*(iii)*
16.	*(i)*	**17.**	*(iii)*	**18.**	*(ii)*	**19.**	*(iv)*	**20.**	*(i)*
21.	*(iv)*	**22.**	*(iii)*	**23.**	*(i)*	**24.**	*(ii)*	**25.**	*(i)*
26.	*(ii)*	**27.**	*(iv)*	**28.**	*(iii)*	**29.**	*(i)*	**30.**	*(ii)*
31.	*(iv)*	**32.**	*(iii)*	**33.**	*(i)*	**34.**	*(ii)*	**35.**	*(iii)*

Chapter Review Topics

1. What do you understand by feedback ? Why is negative feedback applied in high gain amplifiers ?
2. Discuss the principles of negative voltage feedback in amplifiers with a neat diagram.
3. Derive an expression for the gain of negative voltage feedback amplifier.
4. What is a feedback circuit ? Explain how it provides feedback in amplifiers.
5. Describe the action of emitter follower with a neat diagram.
6. Derive the expressions for (*i*) voltage gain (*ii*) input impedance and (*iii*) output impedance of an emitter follower.

Problems

1. An amplifier has a gain of 2×10^5 without feedback. Determine the gain if negative voltage feedback is applied. Take feedback fraction $m_v = 0.02$. **[50]**
2. An amplifier has a gain of 10,000 without feedback. With negative voltage feedback, the gain is reduced to 50. Find the feedback fraction. **[$m_v = 0.02$]**
3. A feedback amplifier has an internal gain $A_v = 40db$ and feedback fraction $m_v = 0.05$. If the input impedance of this circuit is 12 kΩ, what would have been the input impedance if feedback were not present ? **[2kΩ]**
4. Calculate the gain of a negative voltage feedback amplifier with an internal gain $A_v = 75$ and feedback fraction $m_v = 1/15$. What will be the gain if A_v doubles ? **[12.5 ; 13.64]**
5. An amplifier with negative feedback has a voltage gain of 100. It is found that without feedback, an input signal of 50 mV is required to produce a given output, whereas with feedback, the input signal must be 0.6 V for the same output. Calculate (*i*) gain without feedback (*ii*) feedback fraction. **[(i) 1200 (ii) 0.009]**

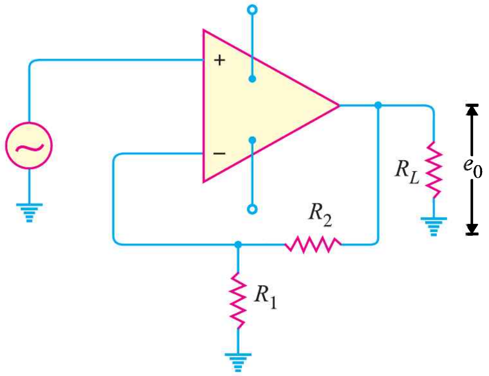


Fig. 13.30

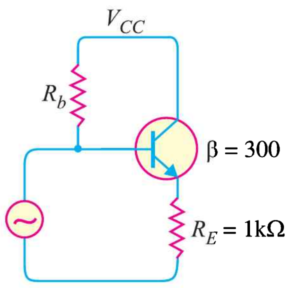


Fig. 13.31

6. Fig. 13.30 shows the negative feedback amplifier. If the gain of the amplifier without feedback is 10^5 and $R_1 = 100\ \Omega$, $R_2 = 100\ \text{k}\Omega$, find (*i*) feedback fraction (*ii*) gain with feedback. **[(i) 0.001(ii) 1000]**

7. In Fig. 13.31, if input and output impedances without feedback are 2 MΩ and 500 Ω respectively, find their values after negative voltage feedback. **[302MΩ; 1.6Ω]**
8. An amplifier has a current gain of 240 without feedback. When negative current feedback is applied, determine the effective current gain of the amplifier. Given that current attenuation $m_i = 0.015$. **[52.7]**
9. An amplifier has an open-loop gain and input impedance of 200 and 15 kΩ respectively. If negative current feedback is applied, what is the effective input impedance of the amplifier? Given that current attenuation $m_i = 0.012$. **[4.41 kΩ]**
10. An amplifier has $A_i = 200$ and $m_i = 0.012$. The open-loop output impedance of the amplifier is 2kΩ. If negative current feedback is applied, what is the effective output impedance of the amplifier ? **[6.8 kΩ]**

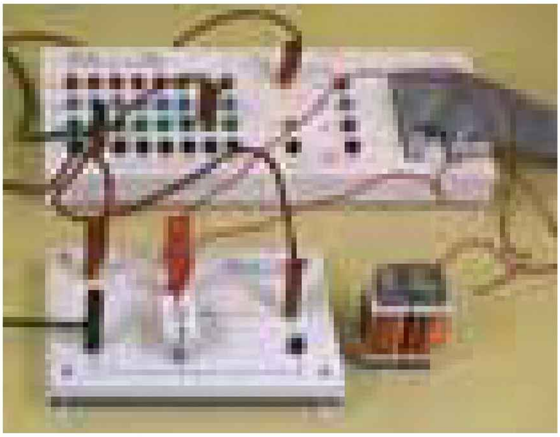
Discussion Questions

1. Why is negative voltage feedback employed in high gain amplifiers ?
2. How does negative voltage feedback increase bandwidth of an amplifier ?
3. Feedback for more than three stages is seldom employed. Explain why ?
4. Why is emitter follower preferred to transformer for impedance matching ?
5. Where is emitter follower employed practically and why ?
6. What are the practical applications of emitter follower ?

14

Sinusoidal Oscillators

14.1 Sinusoidal Oscillator
14.2 Types of Sinusoidal Oscillations
14.3 Oscillatory Circuit
14.4 Undamped Oscillations from Tank Circuit
14.5 Positive Feedback Amplifier — Oscillator
14.6 Essentials of Transistor Oscillator
14.7 Explanation of Barkhausen Criterion
14.8 Different Types of Transistor Oscillators
14.9 Tuned Collector Oscillator
14.10 Colpitt's Oscillator
14.11 Hartley Oscillator
14.12 Principle of Phase Shift Oscillators
14.13 Phase Shift Oscillator
14.14 Wien Bridge Oscillator
14.15 Limitations of LC and RC Oscillators
14.16 Piezoelectric Crystals
14.17 Working of Quartz Crystal
14.18 Equivalent Circuit of Crystal
14.19 Frequency Response of Crystal
14.20 Transistor Crystal Oscillator



INTRODUCTION

Many electronic devices require a source of energy at a specific frequency which may range from a few Hz to several MHz. This is achieved by an electronic device called an *oscillator*. Oscillators are extensively used in electronic equipment. For example, in radio and television receivers, oscillators are used to generate high frequency wave (called *carrier wave*) in the tuning stages. Audio frequency and radio-frequency signals are required for the repair of radio, television and other electronic equipment. Oscillators are also widely used in radar, electronic computers and other electronic devices.

Oscillators can produce sinusoidal or non-sinusoidal (*e.g*. square wave) waves. In this chapter, we shall confine our attention to sinusoidal oscillators *i.e*. those which produce sine-wave signals.

14.1 Sinusoidal Oscillator

An electronic device that generates sinusoidal oscillations of desired frequency is known as a ***sinusoidal oscillator.**

Although we speak of an oscillator as "generating" a frequency, it should be noted that it does not create energy, but merely acts as an energy converter. It receives d.c. energy and changes it into a.c. energy of desired frequency. The frequency of oscillations depends upon the constants of the device.

It may be mentioned here that although an alternator produces sinusoidal oscillations of 50Hz, it cannot be called an oscillator. Firstly, an alternator is a mechanical device having rotating parts whereas an oscillator is a non-rotating electronic device. Secondly, an alternator converts mechanical energy into a.c. energy while an oscillator converts d.c. energy into a.c. energy. Thirdly, an alternator cannot produce high frequency oscillations whereas an oscillator can produce oscillations ranging from a few Hz to several MHz.

Advantages

Although oscillations can be produced by mechanical devices (*e.g.* alternators), but electronic oscillators have the following advantages :

(*i*) An oscillator is a non-rotating device. Consequently, there is little wear and tear and hence longer life.

(*ii*) Due to the absence of moving parts, the operation of an oscillator is quite silent.

(*iii*) An oscillator can produce waves from small (20 Hz) to extremely high frequencies (> 100 MHz).

(*iv*) The frequency of oscillations can be easily changed when desired.

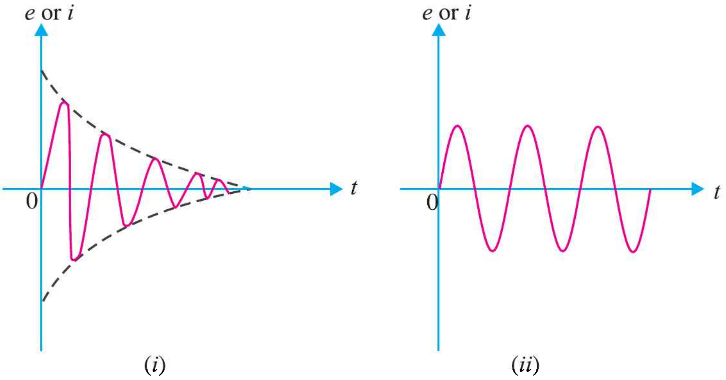
(*v*) It has good frequency stability *i.e.* frequency once set remains constant for a considerable period of time.

(*vi*) It has very high efficiency.

14.2 Types of Sinusoidal Oscillations

Sinusoidal electrical oscillations can be of two types *viz damped oscillations* and *undamped oscillations*.

(*i*) **Damped oscillations.** The electrical oscillations whose amplitude goes on decreasing with time are called *damped oscillations*. Fig. 14.1 (*i*) shows waveform of damped electrical oscillations. Obviously, the electrical system in which these oscillations are generated has losses and some energy is lost during each oscillation. Further, no means are provided to compensate for the losses and consequently the amplitude of the generated wave decreases gradually. It may be noted that frequency of oscillations remains unchanged since it depends upon the constants of the electrical system.



(*i*) (*ii*)

Fig. 14.1

---

* Note that oscillations are produced without any external signal source. The only input power to an oscillator is the d.c. power supply.

(*ii*) **Undamped oscillations.** The electrical oscillations whose amplitude remains constant with time are called *undamped oscillations*. Fig. 14.1 (*ii*) shows waveform of undamped electrical oscillations. Although the electrical system in which these oscillations are being generated has also losses, but now right amount of energy is being supplied to overcome the losses. Consequently, the amplitude of the generated wave remains constant. It should be emphasised that an oscillator is required to produce undamped electrical oscillations for utilising in various electronics equipment.

14.3 Oscillatory Circuit

A circuit which produces electrical oscillations of any desired frequency is known as an **oscillatory circuit** *or* **tank circuit.**

A simple oscillatory circuit consists of a capacitor (*C*) and inductance coil (*L*) in parallel as shown in Fig. 14.2. This electrical system can produce electrical oscillations of frequency determined by the values of *L* and *C*. To understand how this comes about, suppose the capacitor is charged from a d.c. source with a polarity as shown in Fig. 14.2 (*i*).

(*i*) In the position shown in Fig. 14.2 (*i*), the upper plate of capacitor has deficit of electrons and the lower plate has excess of electrons. Therefore, there is a voltage across the capacitor and the capacitor has electrostatic energy.

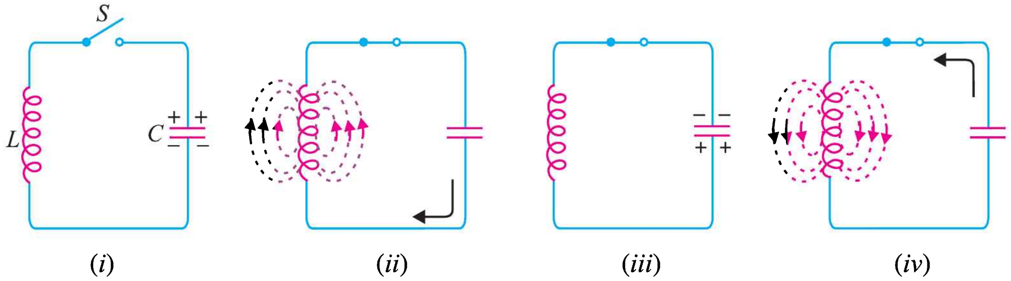


Fig. 14.2

(*ii*) When switch *S* is closed as shown in Fig. 14.2 (*ii*) , the capacitor will discharge through inductance and the electron flow will be in the direction indicated by the arrow. This current flow sets up magnetic field around the coil. Due to the inductive effect, the current builds up slowly towards a maximum value. The circuit current will be maximum when the capacitor is fully discharged. At this instant, electrostatic energy is zero but because electron motion is greatest (*i.e.* maximum current), the magnetic field energy around the coil is maximum. This is shown in Fig. 14.2 (*ii*). Obviously, the electrostatic energy across the capacitor is completely converted into magnetic field energy around the coil.

(*iii*) Once the capacitor is discharged, the magnetic field will begin to collapse and produce a counter e.m.f. According to Lenz's law, the counter e.m.f. will keep the current flowing in the same direction. The result is that the capacitor is now charged with opposite polarity, making upper plate of capacitor negative and lower plate positive as shown in Fig. 14.2 (*iii*).

(*iv*) After the collapsing field has recharged the capacitor, the capacitor now begins to discharge; current now flowing in the opposite direction. Fig. 14.2 (*iv*) shows capacitor fully discharged and maximum current flowing.

The sequence of charge and discharge results in alternating motion of electrons or an oscillating current. The energy is alternately stored in the electric field of the capacitor (*C*) and the magnetic field of the inductance coil (*L*). This interchange of energy between *L* and *C* is repeated over and again resulting in the production of oscillations.

Waveform. If there were no losses in the tank circuit to consume the energy, the interchange of energy between *L* and *C* would continue indefinitely. In a practical tank circuit, there are resistive and radiation losses in the coil and dielectric losses in the capacitor. During each cycle, a small part of the originally imparted energy is used up to overcome these losses. The result is that the amplitude of oscillating current decreases gradually and eventually it becomes zero when all the energy is consumed as losses. Therefore, the tank circuit by itself will produce *damped oscillations* as shown in Fig. 14.3.

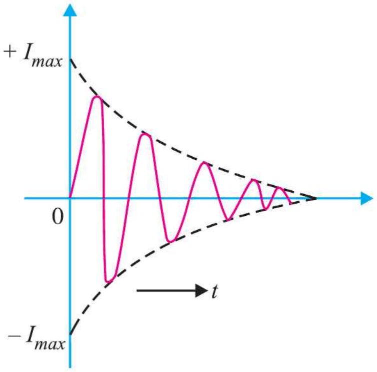


Fig. 14.3

Frequency of oscillations. The frequency of oscillations in the tank circuit is determined by the constants of the circuit *viz* *L* and *C*. The actual frequency of oscillations is the resonant frequency (or natural frequency) of the tank circuit given by :

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

It is clear that frequency of oscillations in the tank circuit is inversely proportional to *L* and *C*. This can be easily explained. If a large value of capacitor is used, it will take longer for the capacitor to charge fully and also longer to discharge. This will lengthen the period of oscillations in the tank circuit, or equivalently lower its frequency. With a large value of inductance, the opposition to change in current flow is greater and hence the time required to complete each cycle will be longer. Therefore, the greater the value of inductance, the longer is the period or the lower is the frequency of oscillations in the tank circuit.

14.4. Undamped Oscillations from Tank Circuit

As discussed before, a tank circuit produces damped oscillations. However, in practice, we need continuous undamped oscillations for the successful operation of electronics equipment. In order to make the oscillations in the tank circuit undamped, it is necessary to supply correct amount of energy to the tank circuit at the proper time intervals to meet the losses. Thus referring back to Fig. 14.2, any energy which would be applied to the circuit must have a polarity conforming to the existing polarity at the instant of application of energy. If the applied energy is of opposite polarity, it would oppose the energy in the tank circuit, causing stoppage of oscillations. Therefore, in order to make the oscillations in the tank circuit undamped, the following conditions must be fulfilled :

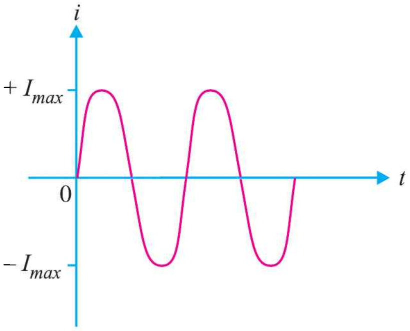


Fig. 14.4

(*i*) The amount of energy supplied should be such so as to meet the losses in the tank circuit and the a.c. energy removed from the circuit by the load. For instance, if losses in *LC* circuit amount to 5 mW and a.c. output being taken is 100 mW, then power of 105 mW should be continuously supplied to the circuit.

(*ii*) The applied energy should have the same frequency as that of the oscillations in the tank circuit.

(*iii*) The applied energy should be in phase with the oscillations set up in the tank circuit *i.e.* it should aid the tank circuit oscillations.

If these conditions are fulfilled, the circuit will produce continuous undamped output as shown in Fig. 14.4.

14.5. Positive Feedback Amplifier — Oscillator

A transistor amplifier with *proper* positive feedback can act as an oscillator *i.e.*, it can generate oscillations without any external signal source. Fig. 14.5 shows a transistor amplifier with positive feedback. Remember that a positive feedback amplifier is one that produces a feedback voltage (V_f) that *is in phase* with the original input signal. As you can see, this condition is met in the circuit shown in Fig. 14.5. A phase shift of 180° is produced by the amplifier and a further phase shift of 180° is introduced by feedback network. Consequently, the signal is shifted by 360° and fed to the input *i.e.*, feedback voltage is in phase with the input signal.

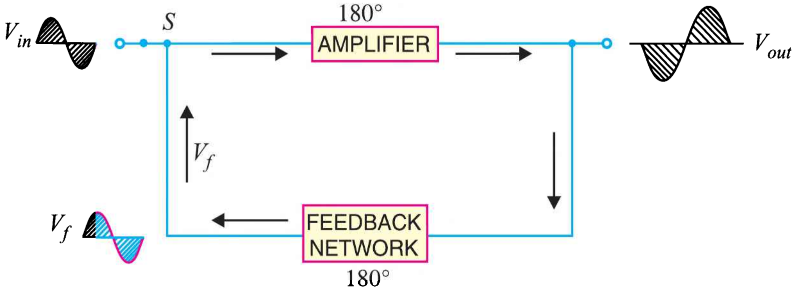


Fig. 14.5

(*i*) We note that the circuit shown in Fig. 14.5 is producing oscillations in the output. However, this circuit has an input signal. This is inconsistent with our definition of an oscillator *i.e.*, an oscillator is a circuit that produces oscillations without any external signal source.

Positive Feedback Amplifier

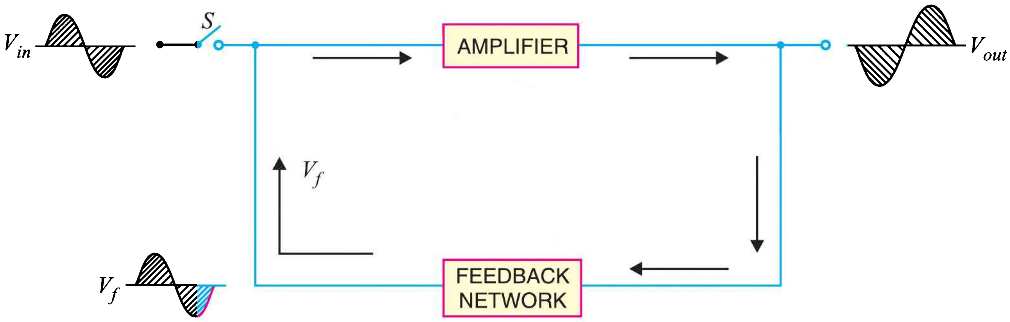


Fig. 14.6

(*ii*) When we open the switch *S* of Fig. 14.5, we get the circuit shown in Fig. 14.6. This means the input signal (V_{in}) is removed. However, V_f (which is in phase with the original signal) is still applied to the input signal. The amplifier will respond to this signal in the same way that it did to V_{in} *i.e.*, V_f will be amplified and sent to the output. The feedback network sends a portion of the output back to the input. Therefore, the amplifier receives another input cycle and another output cycle is produced. This process will continue so long as the amplifier is turned on. Therefore, the amplifer will produce sinusoidal output with no external signal source. The following points may be noted carefully :

(*a*) A transistor amplifer with proper *positive* feedback will work as an oscillator.

(*b*) The circuit needs only a quick trigger signal to start the oscillations. Once the oscillations have started, no external signal source is needed.

(*c*) In order to get continuous undamped output from the circuit, the following condition must be met :

$$m_v A_v = 1$$

where A_v = voltage gain of amplifer without feedback

m_v = feedback fraction

This relation is called *Barkhausen criterion*. This condition will be explained in the Art. 14.7.

14.6 Essentials of Transistor Oscillator

Fig. 14.7 shows the block diagram of an oscillator. Its essential components are :

(*i*) ***Tank circuit.*** It consists of inductance coil (*L*) connected in parallel with capacitor (*C*). The frequency of oscillations in the circuit depends upon the values of inductance of the coil and capacitance of the capacitor.

(*ii*) ***Transistor amplifier.*** The transistor amplifier receives d.c. power from the battery and changes it into a.c. power for supplying to the tank circuit. The oscillations occurring in the tank circuit are applied to the input of the transistor amplifier. Because of the amplifying properties of the transistor, we get increased output of these oscillations.

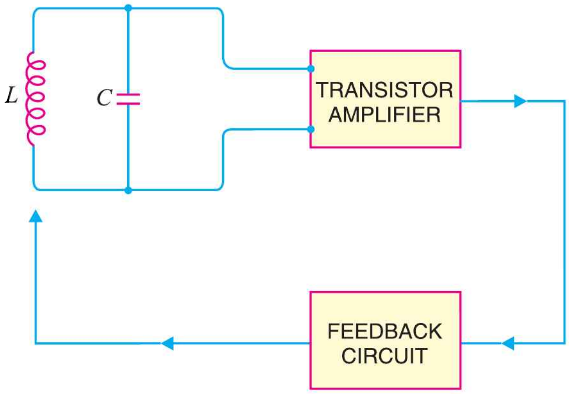


Fig. 14.7

This amplified output of oscillations is due to the d.c. power supplied by the battery. The output of the transistor can be supplied to the tank circuit to meet the losses.

(*iii*) Feedback circuit. The feedback circuit supplies a part of collector energy to the tank circuit in correct phase to aid the oscillations *i.e.* it provides positive feedback.

14.7 Explanation of Barkhausen Criterion

Barkhausen criterion is that in order to produce continuous undamped oscillations at the output of an amplifier, the positive feedback should be such that :

$$m_v A_v = 1$$

Once this condition is set in the positive feedback amplifier, continuous undamped oscillations can be obtained at the output immediately after connecting the necessary power supplies.

(*i*) **Mathematical explanation.** The voltage gain of a positive feedback amplifier is given by;

$$A_{vf} = \frac{A_v}{1 - m_v \, A_v}$$

$$\text{If } m_v \, A_v = 1, \quad \text{then} \quad A_{vf} \to \infty.$$

We know that we cannot achieve infinite gain in an amplifier. So what does this result infer in physical terms ? It means that a vanishing small input voltage would give rise to finite (*i.e.*, a definite amount of) output voltage even when the input signal is zero. Thus once the circuit receives the input trigger, it would become an oscillator, generating oscillations with no external signal source.

(*ii*) **Graphical Explanation.** Let us discuss the condition $m_v A_v = 1$ graphically. Suppose the voltage gain of the amplifier without positive feedback is 100. In order to produce continuous undamped oscillations, $m_v A_v = 1$ or $m_v \times 100 = 1$ or $m_v = 0.01$. This is illustrated in Fig. 14.8. Since the condition $m_v A_v = 1$ is met in the circuit shown in Fig. 14.8, it will produce sustained oscillations.

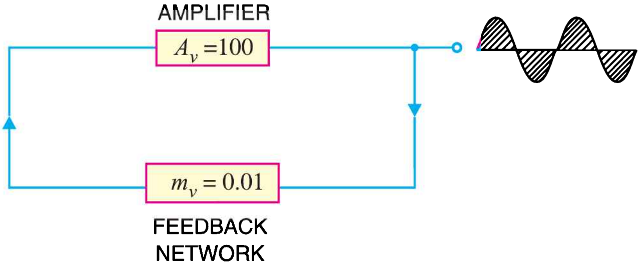


Fig. 14.8

Suppose the initial triggering voltage is 0.1V peak. Starting with this value, circuit ($A_v = 100$; $m_v = 0.01$) will progress as follows.

Cycle	V_{in}	V_{out}	V_f
1.	0.1Vpk	10Vpk	0.1Vpk
2.	0.1Vpk	10Vpk	0.1Vpk

The same thing will repeat for 3rd, 4th cycles and so on. Note that during each cycle, V_f = 0.1Vpk and V_{out} = 10 Vpk. Clearly, the oscillator is producing continuous undamped oscillations.

Note. The relation $m_v \, A_v = 1$ holds good for true ideal circuits. However, practical circuits need an $m_v \, A_v$ product that is slightly greater than 1. This is to compensate for power loss (*e.g.*, in resistors) in the circuit.

14.8 Different Types of Transistor Oscillators

A transistor can work as an oscillator to produce continuous undamped oscillations of any desired frequency if tank and feedback circuits are properly connected to it. All oscillators under different names have similar function *i.e.*, they produce continuous undamped output. However, the major difference between these oscillators lies in the method by which energy is supplied to the tank circuit to meet the losses. The following are the transistor oscillators commonly used at various places in electronic circuits :

(*i*) Tuned collector oscillator
(*ii*) Colpitt's oscillator
(*iii*) Hartley oscillator
(*iv*) Phase shift oscillator
(*v*) Wien Bridge oscillator
(*vi*) Crystal oscillator

14.9 Tuned Collector Oscillator

Fig.14.9 shows the circuit of tuned collector oscillator. It contains tuned circuit L_1-C_1 in the collector and hence the name. The frequency of oscillations depends upon the values of L_1 and C_1 and is given by :

$$f = \frac{1}{2\pi\sqrt{L_1 C_1}} \qquad ...(i)$$

The feedback coil L_2 in the base circuit is magnetically coupled to the tank circuit coil L_1. In practice, L_1 and L_2 form the primary and secondary of the transformer respectively. The biasing is provided by potential divider arrangement. The capacitor C connected in the base circuit provides low reactance path to the oscillations.

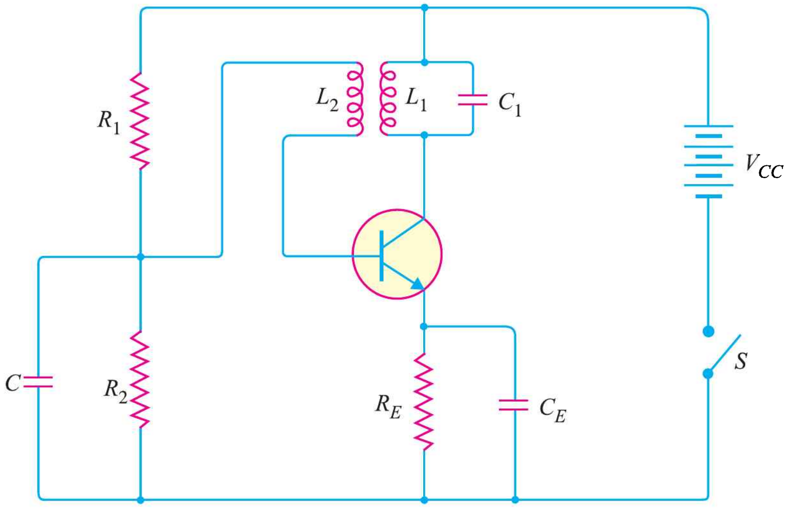


Fig. 14.9

Circuit operation. When switch S is closed, collector current starts increasing and charges the capacitor C_1. When this capacitor is fully charged, it discharges through coil L_1, setting up oscillations of frequency determined by exp. (i). These oscillations induce some voltage in coil L_2 by mutual induction. The frequency of voltage in coil L_2 is the same as that of tank circuit but its magnitude depends upon the number of turns of L_2 and coupling between L_1 and L_2. The voltage across L_2 is applied between base and emitter and appears in the amplified form in the collector circuit, thus overcoming the losses occurring in the tank circuit. The number of turns of L_2 and coupling between L_1 and L_2 are so adjusted that oscillations across L_2 are amplified to a level just sufficient to supply losses to the tank circuit.

It may be noted that the phase of feedback is correct *i.e.* energy supplied to the tank circuit is in phase with the generated oscillations. A phase shift of 180° is created between the voltages of L_1 and L_2 due to transformer *action. A further phase shift of 180° takes place between base-emitter and collector circuit due to transistor properties. As a result, the energy fedback to the tank circuit is in phase with the generated oscillations.

Example 14.1. *The tuned collector oscillator circuit used in the local oscillator of a radio*

---

* All transformers introduce a phase shift of 180° between primary and secondary.

receiver makes use of an LC tuned circuit with L_1 = 58.6 μH and C_1 = 300 pF. Calculate the frequency of oscillations.

Solution.

$$L_1 = 58.6\ \mu\text{H} = 58.6 \times 10^{-6}\ \text{H}$$

$$C_1 = 300\ \text{pF} = 300 \times 10^{-12}\ \text{F}$$

Frequency of oscillations,
$$f = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

$$= \frac{1}{2\pi\sqrt{58.6 \times 10^{-6} \times 300 \times 10^{-12}}}\ \text{Hz}$$

$$= 1199 \times 10^3\ \text{Hz} = \mathbf{1199\ kHz}$$

Example 14.2. *Find the capacitance of the capacitor required to build an LC oscillator that uses an inductance of L_1 = 1 mH to produce a sine wave of frequency 1 GHz (1 GHz = 1 × 10^{12} Hz).*

Solution.

Frequency of oscillations is given by ;

$$f = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

or
$$C_1 = \frac{1}{L_1 (2\pi f)^2} = \frac{1}{(1 \times 10^{-3})\ (2\pi \times 1 \times 10^{12})^2}$$

$$= 2{\cdot}53 \times 10^{-23}\ \text{F} = \mathbf{2{\cdot}53 \times 10^{-11}\ pF}$$

The LC circuit is often called *tuned circuit* or *tank circuit.*

14.10 Colpitt's Oscillator

Fig. 14.10 shows a Colpitt's oscillator. It uses two capacitors and placed across a common inductor *L* and the centre of the two capacitors is tapped. The tank circuit is made up of C_1, C_2 and *L*. The frequency of oscillations is determined by the values of C_1, C_2 and *L* and is given by ;

$$f = \frac{1}{2\pi\sqrt{LC_T}} \qquad \text{....}(i)$$

where
$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

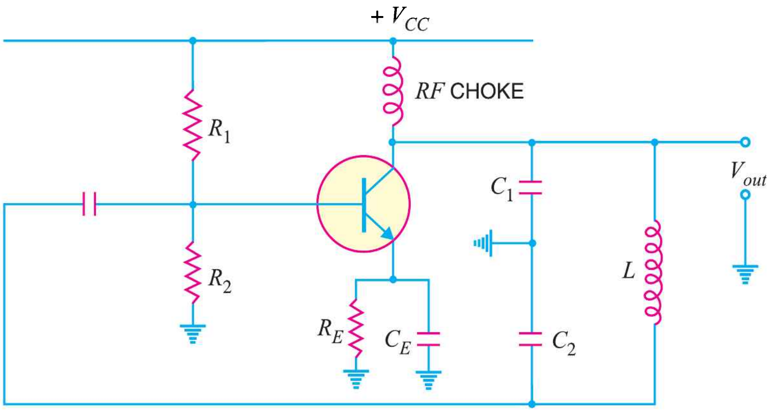


Fig. 14.10

*Note that $C_1 - C_2 - L$ is also the feedback circuit that produces a phase shift of 180°.

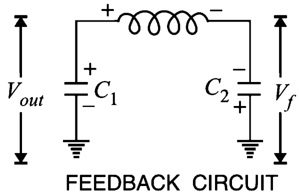


Fig. 14.11

Circuit operation. When the circuit is turned on, the capacitors C_1 and C_2 are charged. The capacitors discharge through L, setting up oscillations of frequency determined by exp.** (*i*). The output voltage of the amplifier appears across C_1 and feedback voltage is developed across C_2. The voltage across it is 180° out of phase with the voltage developed across C_1 (V_{out}) as shown in Fig. 14.11. It is easy to see that voltage fedback (voltage across C_2) to the transistor provides positive feedback. A phase shift of 180° is produced by the transistor and a further phase shift of 180° is produced by $C_1 - C_2$ voltage divider. In this way, feedback is properly phased to produce continuous undamped oscillation.

Feedback fraction m_v. The amount of feedback voltage in Colpitt's oscillator depends upon feedback fraction m_v of the circuit. For this circuit,

$$\text{Feedback fraction, } m_v = \frac{V_f}{V_{out}} = \frac{X_{c2}}{X_{c1}} = \frac{C_1}{C_2}^{***}$$

$$\text{or} \qquad m_v = \frac{C_1}{C_2}$$

Example 14.3. *Determine the (i) operating frequency and (ii) feedback fraction for Colpitt's oscillator shown in Fig. 14.12.*

Solution.

(*i*) **Operating Frequency.** The operating frequency of the circuit is always equal to the resonant frequency of the feedback network. As noted previously, the capacitors C_1 and C_2 are in series.

$$\therefore \qquad C_T = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.001 \times 0.01}{0.001 + 0.01} = 9.09 \times 10^{-4}\ \mu\text{F}$$

$$= 909 \times 10^{-12}\ \text{F}$$

$$L = 15\ \mu\text{H} = 15 \times 10^{-6}\ \text{H}$$

$$\therefore \quad \text{Operating frequency, } f = \frac{1}{2\pi\sqrt{LC_T}}$$

$$= \frac{1}{2\pi\sqrt{15 \times 10^{-6} \times 909 \times 10^{-12}}}\ \text{Hz}$$

$$= 1361 \times 10^3\ \text{Hz} = \mathbf{1361\ kHz}$$

(*ii*) **Feedback fraction**

$$m_v = \frac{C_1}{C_2} = \frac{0.001}{0.01} = \mathbf{0.1}$$

---

* The RF choke decouples any ac signal on the power lines from affecting the output signal.

** Referring to Fig. 14.11, it is clear that C_1 and C_2 are in series. Therefore, total capacitance C_T is given by;

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

*** Referring to Fig. 14.11, the circulating current for the two capacitors is the same. Futher, capacitive reactance is inversely proportional to capacitance.

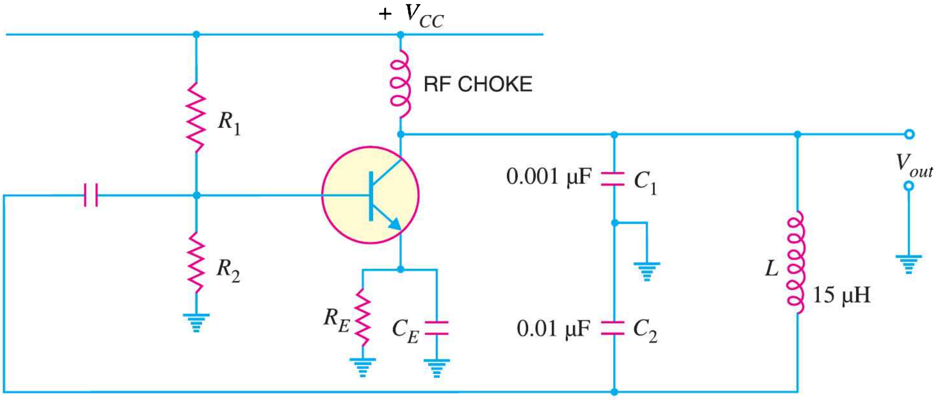


Fig. 14.12

Example 14.4. *A 1 mH inductor is available. Choose the capacitor values in a Colpitts oscillator so that f = 1 MHz and* $m_v = 0.25$.

Solution.

Feedback fraction, $$m_v = \frac{C_1}{C_2}$$

or $$0.25 = \frac{C_1}{C_2} \qquad \therefore\ C_2 = 4C_1$$

Now $$f = \frac{1}{2\pi\sqrt{LC_T}}$$

or $$C_T = \frac{1}{L(2\pi f)^2} = \frac{1}{(1\times10^{-3})\,(2\pi\times1\times10^{6})^2} = 25.\ 3\times10^{-12}\,\text{F}$$

$$= 25.3\ \text{pF}$$

or $$\frac{C_1 C_2}{C_1 + C_2} = 25.3\ \text{pF} \qquad \left[\because\ C_T = \frac{C_1 C_2}{C_1 + C_2}\right]$$

or $$\frac{C_2}{1 + \frac{C_2}{C_1}} = 25.3$$

or $$\frac{C_2}{1+4} = 25.3 \qquad \therefore\ C_2 = 25.3 \times 5 = \mathbf{126.5\ pF}$$

and $$C_1 = C_2/4 = 126.5/4 = \mathbf{31.6\ pF}$$

14.11 Hartley Oscillator

The Hartley oscillator is similar to Colpitt's oscillator with minor modifications. Instead of using tapped capacitors, two inductors L_1 and L_2 are placed across a common capacitor *C* and the centre of the inductors is tapped as shown in Fig. 14.13. The tank circuit is made up of L_1, L_2 and *C*. The frequency of oscillations is determined by the values of L_1, L_2 and *C* and is given by :

$$f = \frac{1}{2\pi\sqrt{CL_T}} \qquad ...(i)$$

where $L_T = L_1 + L_2 + 2M$

Here M = mutual inductance between L_1 and L_2

Note that $L_1 - L_2 - C$ is also the feedback network that produces a phase shift of 180°.

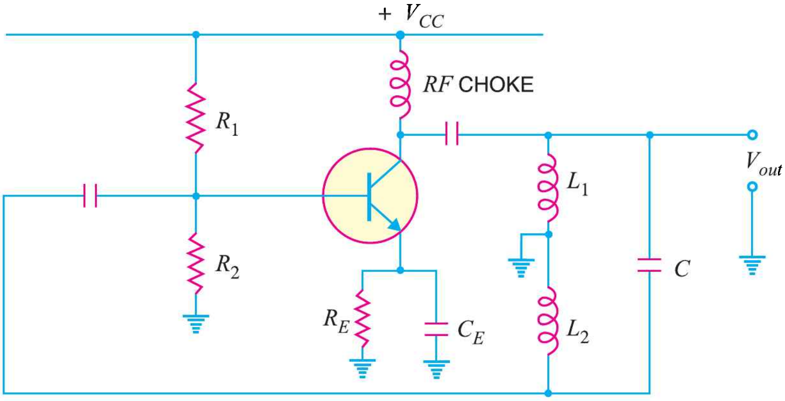


Fig. 14.13

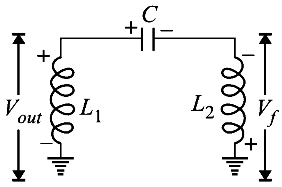


Fig. 14.14

Circuit operation. When the circuit is turned on, the capacitor is charged. When this capacitor is fully charged, it discharges through coils L_1 and L_2 setting up oscillations of frequency determined by *exp. (*i*). The output voltage of the amplifier appears across L_1 and feedback voltage across L_2. The voltage across L_2 is 180° out of phase with the voltage developed across L_1 (V_{out}) as shown in Fig. 14.14. It is easy to see that voltage fedback (*i.e.*, voltage across L_2) to the transistor provides positive feedback. A phase shift of 180° is produced by the transistor and a further phase shift of 180° is produced by $L_1 - L_2$ voltage divider. In this way, feedback is properly phased to produce continuous undamped oscillations.

Feedback fraction m_v. In Hartley oscillator, the feedback voltage is across L_2 and output voltage is across L_1.

$$\therefore \quad \text{Feedback fraction, } m_v = \frac{V_f}{V_{out}} = \frac{X_{L_2}}{X_{L_1}} = {}^{**}\frac{L_2}{L_1}$$

$$\text{or} \quad m_v = \frac{L_2}{L_1}$$

Example 14.5. *Calculate the (i) operating frequency and (ii) feedback fraction for Hartley oscillator shown in Fig. 14.15. The mutual inductance between the coils, M = 20 μH.*

Solution.

$$(i) \quad L_1 = 1000\,\mu\text{H}\,; \quad L_2 = 100\,\mu\text{H}\,; \quad M = 20\,\mu\text{H}$$

$$\therefore \quad \text{Total inductance, } L_T = L_1 + L_2 + 2M$$

$$= 1000 + 100 + 2 \times 20 = 1140\,\mu\text{H} = 1140 \times 10^{-6}\,\text{H}$$

$$\text{Capacitance, } C = 20\text{ pF} = 20 \times 10^{-12}\text{ F}$$

---

* Referring to Fig. 14.14, it is clear that L_1 and L_2 are in series. Therefore, total inductance L_T is given by : $L_T = L_1 + L_2 + 2M$

** Referring to Fig. 14.14, the circulating current for the two inductors is the same. Further, inductive reactance is directly proportional to inductance.

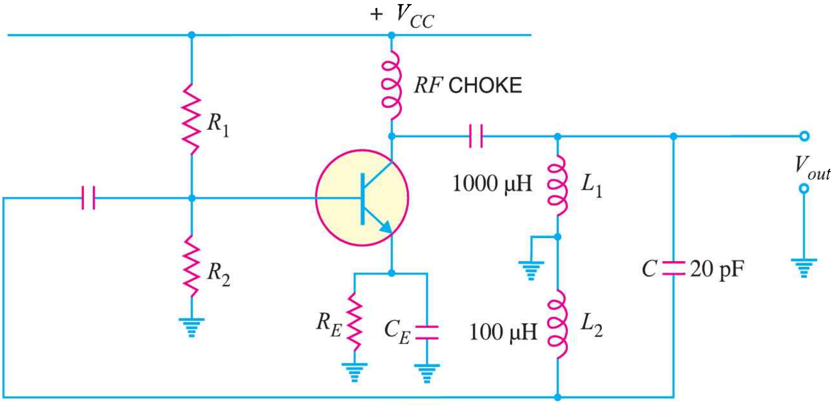


Fig. 14.15

$$\therefore \quad \text{Operating frequency, } f = \frac{1}{2\pi\sqrt{L_T C}} = \frac{1}{2\pi\sqrt{1140 \times 10^{-6} \times 20 \times 10^{-12}}} \text{ Hz}$$

$$= 1052 \times 10^3 \text{ Hz} = \mathbf{1052\ kHz}$$

$$(ii) \quad \text{Feedback fraction, } m_v = \frac{L_2}{L_1} = \frac{100\ \mu H}{1000\ \mu H} = \mathbf{0.1}$$

Example 14.6. *A 1 pF capacitor is available. Choose the inductor values in a Hartley oscillator so that f = 1 MHz and m_v = 0.2.*

Solution.

$$\text{Feedback fraction, } m_v = \frac{L_2}{L_1}$$

$$\text{or} \quad 0.2 = \frac{L_2}{L_1} \qquad \therefore \; L_1 = 5L_2$$

$$\text{Now} \quad f = \frac{1}{2\pi\sqrt{L_T C}}$$

$$\text{or} \quad L_T = \frac{1}{C(2\pi f)^2} = \frac{1}{(1 \times 10^{-12})(2\pi \times 1 \times 10^6)^2}$$

$$= 25.3 \times 10^{-3} \text{ H} = 25.3 \text{ mH}$$

$$\text{or} \quad L_1 + L_2 = 25.3 \text{ mH} \qquad (\because \; L_T = L_1 + L_2)$$

$$\text{or} \quad 5L_2 + L_2 = 25.3 \qquad \therefore \; L_2 = 25.3/6 = \mathbf{4.22\ mH}$$

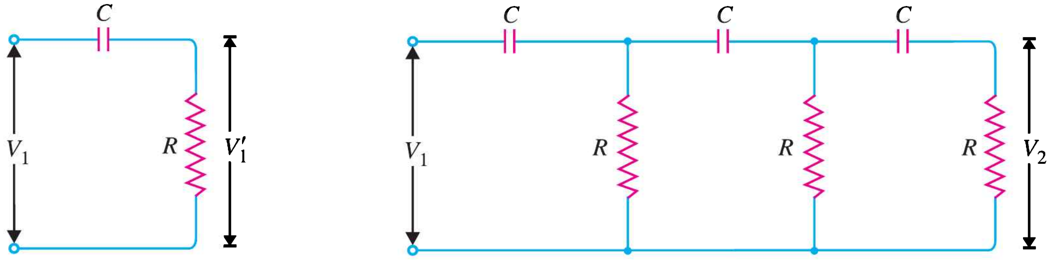
$$\text{and} \quad L_1 = 5\,L_2 = 5 \times 4.22 = \mathbf{21.1\ mH}$$

14.12 Principle of Phase Shift Oscillators

One desirable feature of an oscillator is that it should feed back energy of correct phase to the tank circuit to overcome the losses occurring in it. In the oscillator circuits discussed so far, the tank circuit employed inductive (*L*) and capacitive (*C*) elements. In such circuits, a phase shift of 180° was obtained due to inductive or capacitive coupling and a further phase shift of 180° was obtained due to transistor properties. In this way, energy supplied to the tank circuit was in phase with the generated oscillations. The oscillator circuits employing *L-C* elements have two general drawbacks. Firstly, they suffer from frequency instability and poor waveform. Secondly, they cannot be used for very low frequencies because they become too much bulky and expensive.

Good frequency stability and waveform can be obtained from oscillators employing resistive and capacitive elements. Such amplifiers are called *R-C* or *phase shift oscillators* and have the additional advantage that they can be used for very low frequencies. In a phase shift oscillator, a phase shift of 180° is obtained with a phase shift circuit instead of inductive or capacitive coupling. A further phase shift of 180° is introduced due to the transistor properties. Thus, energy supplied back to the tank circuit is assured of correct phase.

Phase shift circuit. A phase-shift circuit essentially consists of an *R-C* network. Fig. 14.16 (*i*) shows a single section of *RC* network. From the elementary theory of electrical engineering, it can be shown that alternating voltage V_1' across *R* leads the applied voltage V_1 by ϕ°. The value of ϕ depends upon the values of *R* and *C*. If resistance *R* is varied, the value of ϕ also changes. If *R* were reduced to zero, V_1' will lead V_1 by 90° *i.e.* $\phi = 90°$. However, adjusting *R* to zero would be impracticable because it would lead to no voltage across *R*. Therefore, in practice, *R* is varied to such a value that makes V_1' to lead V_1 by 60°.



(*i*) (*ii*)

Fig. 14.16

Fig. 14.16 (*ii*) shows the three sections of *RC* network. Each section produces a phase shift of 60°. Consequently, a total phase shift of 180° is produced *i.e.* voltage V_2 leads the voltage V_1 by 180°.

14.13 Phase Shift Oscillator

Fig.14.17 shows the circuit of a phase shift oscillator. It consists of a conventional single transistor amplifier and a *RC* phase shift network. The phase shift network consists of three sections R_1C_1, R_2C_2 and R_3C_3. At some particular frequency f_0, the phase shift in each *RC* section is 60° so that the total phase-shift produced by the *RC* network is 180°. The frequency of oscillations is given by :

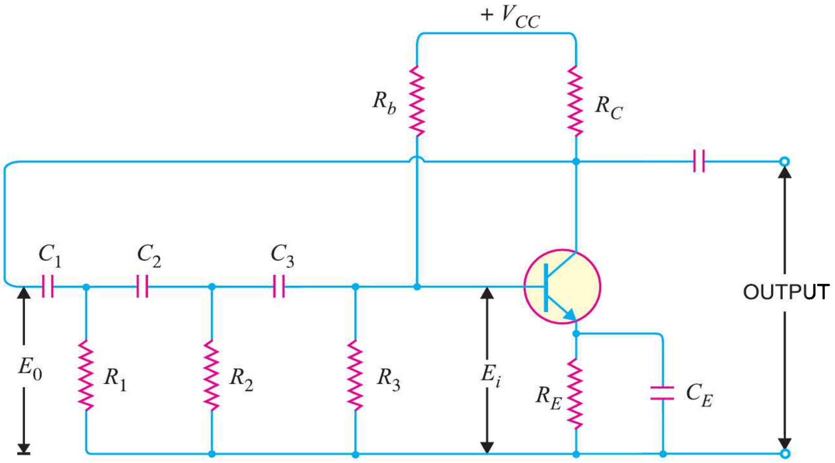


Fig. 14.17

$$f_0 = \frac{1}{2\pi RC\sqrt{6}} \qquad \ldots(i)$$

where

$$R_1 = R_2 = R_3 = R$$
$$C_1 = C_2 = C_3 = C$$

Circuit operation. When the circuit is switched on, it produces oscillations of frequency determined by exp. (*i*). The output E_0 of the amplifier is fed back to *RC* feedback network. This network produces a phase shift of 180° and a voltage E_i appears at its output which is applied to the transistor amplifier.

Obviously, the feedback fraction $m = E_i/E_0$. The feedback phase is correct. A phase shift of 180° is produced by the transistor amplifier. A further phase shift of 180° is produced by the *RC* network. As a result, the phase shift around the entire loop is 360°.

Advantages

(*i*) It does not require transformers or inductors.

(*ii*) It can be used to produce very low frequencies.

(*iii*) The circuit provides good frequency stability.

Disadvantages

(*i*) It is difficult for the circuit to start oscillations as the feedback is generally small.

(*ii*) The circuit gives small output.

Example 14.7. *In the phase shift oscillator shown in Fig. 14.17,* $R_1 = R_2 = R_3 = 1 M\Omega$ *and* $C_1 = C_2 = C_3 = 68\, pF$. *At what frequency does the circuit oscillate ?*

Solution.

$$R_1 = R_2 = R_3 = R = 1\, M\Omega = 10^6\, \Omega$$
$$C_1 = C_2 = C_3 = C = 68\, pF = 68 \times 10^{-12}\, F$$

Frequency of oscillations is

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$
$$= \frac{1}{2\pi \times 10^6 \times 68 \times 10^{-12}\sqrt{6}}\ \text{Hz}$$
$$= \mathbf{954\ Hz}$$

Example 14.8. *A phase shift oscillator uses 5 pF capacitors. Find the value of R to produce a frequency of 800 kHz.*

Solution.

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

or

$$R = \frac{1}{2\pi f_o C\sqrt{6}} = \frac{1}{2\pi \times 800 \times 10^3 \times 5 \times 10^{-12} \times \sqrt{6}}$$
$$= 16.2 \times 10^3\, \Omega = \mathbf{16.2\ k\Omega}$$

14.14 Wien Bridge Oscillator

The Wien-bridge oscillator is the standard oscillator circuit for all frequencies in the range of 10 Hz to about 1 MHz. It is the most frequently used type of audio oscillator as the output is free from circuit fluctuations and ambient temperature. Fig. 14.18 shows the circuit of Wien bridge oscillator. It is essentially a two-stage amplifier with *R-C* bridge circuit. The bridge circuit has the arms R_1C_1,

R_3, R_2C_2 and tungsten lamp L_p. Resistances R_3 and L_p are used to stabilise the amplitude of the output. The transistor T_1 serves as an oscillator and amplifier while the other transistor T_2 serves as an inverter (*i.e.* to produce a phase shift of 180°). The circuit uses positive and negative feedbacks. The positive feedback is through R_1C_1, C_2R_2 to the transistor T_1. The negative feedback is through the voltage divider to the input of transistor T_2. The frequency of oscillations is determined by the series element R_1C_1 and parallel element R_2C_2 of the bridge.

$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

If $R_1 = R_2 = R$

and $C_1 = C_2 = C$, then,

$$f = \frac{1}{2\pi RC} \qquad \text{...}(i)$$

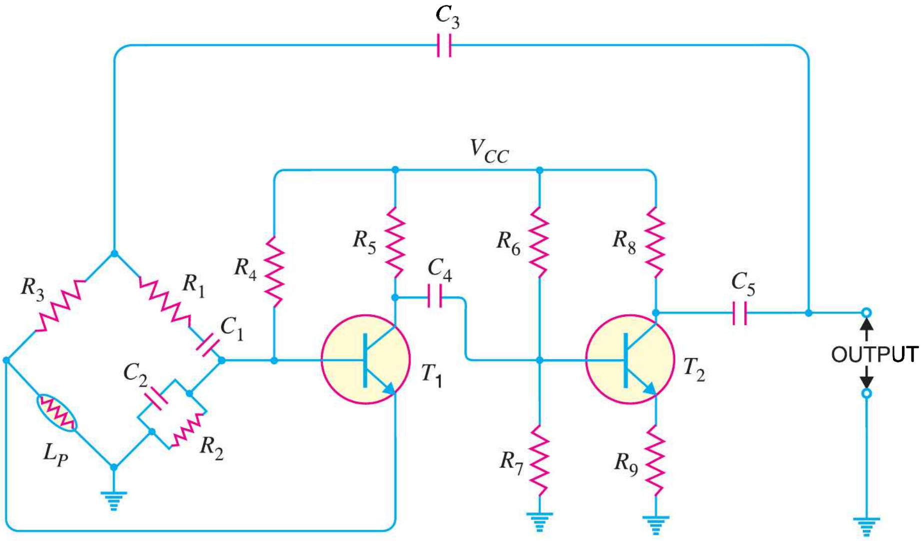


Fig. 14.18

When the circuit is started, bridge circuit produces oscillations of frequency determined by exp. (*i*). The two transistors produce a total phase shift of 360° so that proper positive feedback is ensured. The negative feedback in the circuit ensures constant output. This is achieved by the temperature sensitive tungsten lamp L_p. Its resistance increases with current. Should the amplitude of output tend to increase, more current would provide more negative feedback. The result is that the output would return to original value. A reverse action would take place if the output tends to decrease.

Advantages

(*i*) It gives constant output.

(*ii*) The circuit works quite easily.

(*iii*) The overall gain is high because of two transistors.

(*iv*) The frequency of oscillations can be easily changed by using a potentiometer.

Disadvantages

(*i*) The circuit requires two transistors and a large number of components.

(*ii*) It cannot generate very high frequencies.

Example 14.9. *In the Wien bridge oscillator shown in Fig. 14.18,* $R_1 = R_2 = 220\ k\Omega$ *and* $C_1 = C_2 = 250\ pF$*. Determine the frequency of oscillations.*

Solution.

$$R_1 = R_2 = R = 220\ \text{k}\Omega = 220 \times 10^3\ \Omega$$

$$C_1 = C_2 = C = 250\ \text{pF} = 250 \times 10^{-12}\ \text{F}$$

Frequency of oscillations,

$$f = \frac{1}{2\pi RC}$$

$$= \frac{1}{2\pi \times 220 \times 10^3 \times 250 \times 10^{-12}}\ \text{Hz}$$

$$= \mathbf{2892\ Hz}$$

14.15 Limitations of LC and RC Oscillators

The *LC* and *RC* oscillators discussed so far have their own limitations. The major problem in such circuits is that their operating frequency does not remain strictly constant. There are two principal reasons for it *viz.*,

(*i*) As the circuit operates, it will warm up. Consequently, the values of resistors and inductors, which are the frequency determining factors in these circuits, will change with temperature. This causes the change in frequency of the oscillator.

(*ii*) If any component in the feedback network is changed, it will shift the operating frequency of the oscillator.

However, in many applications, it is desirable and necessary to maintain the frequency constant with extreme low tolerances. For example, the frequency tolerance for a broadcasting station should not exceed 0.002% *i.e.* change in frequency due to any reason should not be more than 0.002% of the specified frequency. The broadcasting stations have frequencies which are quite close to each other. In fact, the frequency difference between two broadcasting stations is less than 1%. It is apparent that if we employ *LC* or *RC* circuits, a change of temperature may cause the frequencies of adjacent broadcasting stations to overlap.

In order to maintain constant frequency, *piezoelectric crystals* are used in place of *LC* or *RC* circuits. Oscillators of this type are called *crystal oscillators*. The frequency of a crystal oscillator changes by less than 0.1% due to temperature and other changes. Therefore, such oscillators offer the most satisfactory method of stabilising the frequency and are used in great majority of electronic applications.

14.16 Piezoelectric Crystals

Certain crystalline materials, namely, Rochelle salt, quartz and tourmaline exhibit the *piezoelectric effect i.e.*, when we apply an a.c. voltage across them, they vibrate at the frequency of the applied voltage. Conversely, when they are compressed or placed under mechanical strain to vibrate, they produce an a.c. voltage. Such crystals which exhibit piezoelectric effect are called *piezoelectric crystals*. Of the various piezoelectric crystals, quartz is most commonly used because it is inexpensive and readily available in nature.

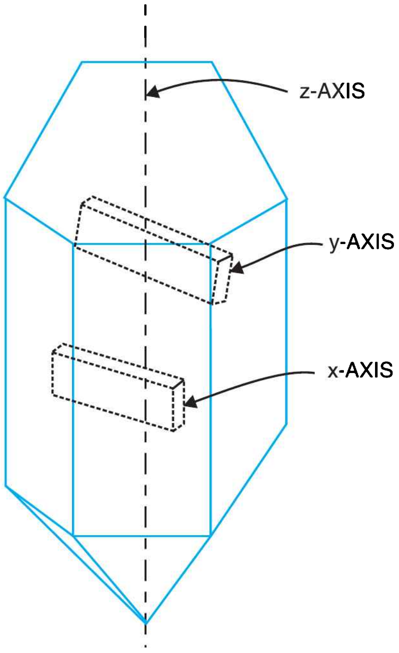


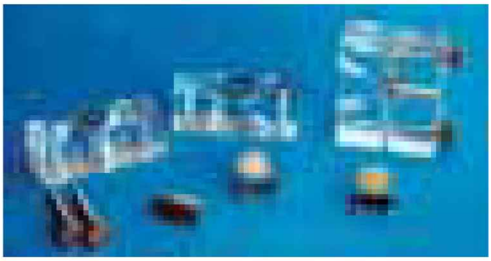
Fig. 14.19

Quartz crystal. Quartz crystals are generally used in crystal oscillators because of their great mechanical strength and simplicity of manufacture. The natural shape of quartz crystal is hexagonal as shown in Fig. 14.19. The three axes are shown : the *z-axis* is called the *optical axis*, the *x-axis* is called the *electrical axis* and *y-axis* is called the *mechanical axis*. Quartz crystal can be cut in different ways. Crystal cut perpendicular to the *x-axis* is called *x-cut crystal* whereas that cut perpendicular to *y-axis* is called *y-cut crystal*. The piezoelectric properties of a crystal depend upon its cut.

Frequency of crystal. Each crystal has a natural frequency like a pendulum. The natural frequency f of a crystal is given by :

$$f = \frac{K}{t}$$

where K is a constant that depends upon the cut and t is the thickness of the crystal. It is clear that frequency is inversely proportional to crystal thickness. The thinner the crystal, the greater is its natural frequency and *vice-versa*. However, extremely thin crystal may break because of vibrations. This puts a limit to the frequency obtainable. In practice, frequencies between *25 kHz* to *5 MHz* have been obtained with crystals.



Piezoelectric Crystals

14.17 Working of Quartz Crystal

In order to use crystal in an electronic circuit, it is placed between two metal plates. The arrangement then forms a capacitor with crystal as the dielectric as shown in Fig. 14.20. If an a.c. voltage is applied across the plates, the crystal will start vibrating at the frequency of applied voltage. However, if the frequency of the applied voltage is made equal to the natural frequency of the crystal, resonance takes place and crystal vibrations reach a maximum value. This natural frequency is almost constant. Effects of temperature change can be eliminated by mounting the crystal in a temperature-controlled oven as in radio and television transmitters.

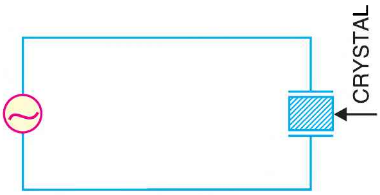


Fig. 14.20

14.18 Equivalent Circuit of Crystal

Although the crystal has electromechanical resonance, we can represent the crystal action by an equivalent electrical circuit.

(*i*) When the crystal is not vibrating, it is equivalent to capacitance C_m because it has two metal plates separated by a dielectric [See Fig. 14.21 (*i*)]. This capacitance is known as *mounting capacitance*.

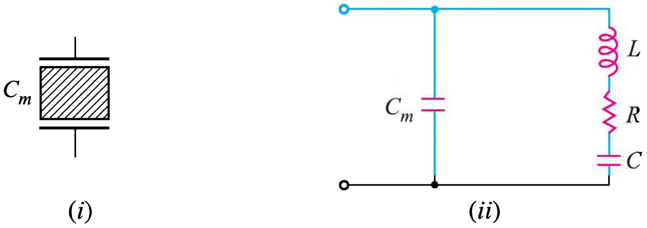
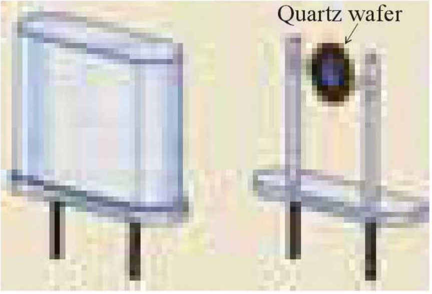


Fig. 14.21

(*ii*) When a crystal vibrates, *it is equivalent to $R - L - C$ series circuit. Therefore, the equivalent circuit of a vibrating crystal is $R - L - C$ series circuit shunted by the mounting capacitance C_m as shown in Fig. 14.21 (*ii*).

C_m = mounting capacitance

$R–L–C$ = electrical equivalent of vibrational characteristic of the crystal



A quartz crystal

Typical values for a 4 MHz crystal are :

L = 100 mH ; R = 100 Ω

C = 0.015 pF ; C_m = 5 pF

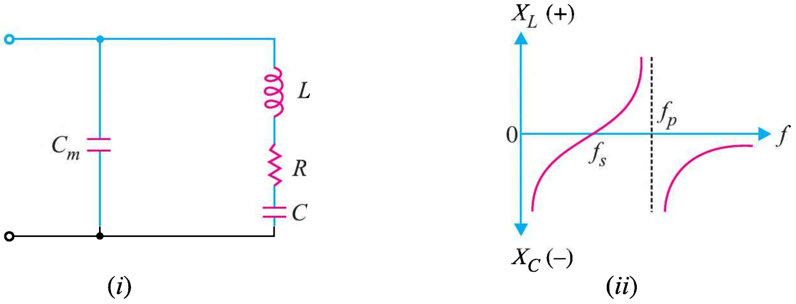
$$\therefore \qquad Q\text{-factor of crystal} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

$$= \frac{1}{100}\sqrt{\frac{100 \times 10^{-3}}{0.015 \times 10^{-12}}} = 26{,}000$$

Note that Q of crystal is very high. The extremely high Q of a crystal leads to frequency **stability.

14.19 Frequency Response of Crystal

When the crystal is vibrating, its equivalent electrical circuit is as shown in Fig. 14.22 (*i*). The capacitance values of C and C_m are relatively low (less than 1 pF for C and 4–40 pF for C_m). Note that the value of C is much lower than that of C_m.



(*i*) (*ii*)

Fig. 14.22

(*i*) At low frequencies, the impedance of the crystal is controlled by extremely high values of X_{C_m} and X_C. In other words, at low frequencies, the impedance of the network is high and capacitive as shown in Fig. 14.22 (*ii*).

(*ii*) As the frequency is increased, $R - L - C$ branch approaches its resonant frequency. At some definite frequency, the reactance X_L will be equal to X_C. The crystal now acts as a series-resonant circuit. For this condition, the impedance of the crystal is very low; being equal to *R*. The frequency at which the vibrating crystal behaves as a series-resonant circuit is called *series-resonant frequency* f_s. Its value is given by:

---

* When the crystal is vibrating , L is the electrical equivalent of crystal mass, C is the electrical equivalent of elasticity and R is electrical equivalent of mechanical friction.

** When Q is high, frequency is primarily determined by L and C of the crystal. Since these values remain fixed for a crystal, the frequency is stable. However, in ordinary LC tank circuit, the values of L and C have large tolerances.

$$f_s = \frac{1}{2\pi\sqrt{LC}} \text{ Hz}$$

where *L* is in henry and *C* is in farad.

(***iii***) At a slightly higher frequency, the net reactance of branch $R - L - C$ becomes inductive and equal to X_{C_m}. The crystal now acts as a parallel-resonant circuit. For this condition, the crystal offers a very high impedance. The frequency at which the vibrating crystal behaves as a parallel-resonant circuit is called *parallel-resonant frequency* f_p.

$$f_p = \frac{1}{2\pi\sqrt{LC_T}}$$

where $$C_T = \frac{C \times C_m}{C + C_m}$$

Since C_T is less than C, f_p is always greater than f_s. Note that frequencies f_s and f_p are very close to each other.

(***iv***) At frequencies greater than f_p, the value of X_{C_m} drops and eventually the crystal acts as a short circuit.

Conclusion. The above discussion leads to the following conclusions :

(***i***) At f_s, the crystal will act as a series-resonant circuit.

(***ii***) At f_p, the crystal will act as a parallel-resonant circuit.

Therefore, we can use a crystal in place of a series *LC* circuit or in place of parallel *LC* circuit. If we use it in place of series *LC* circuit, the oscillator will operate at f_s. However if we use the crystal in place of parallel *LC* circuit, the oscillator will operate at f_p. In order to use the crystal properly, it must be connected in a cricuit so that its low impedance in the series resonant operating mode or high impedance in the parallel resonant operating mode is selected.

14.20 Transistor Crystal Oscillator

Fig. 14.23 shows the transistor crystal oscillator. Note that it is a Collpit's oscillator modified to act as a crystal oscillator. The only change is the addition of the crystal (*Y*) in the feedback network. The crystal will act as a parallel-tuned circuit. As you can see in this circuit that instead of

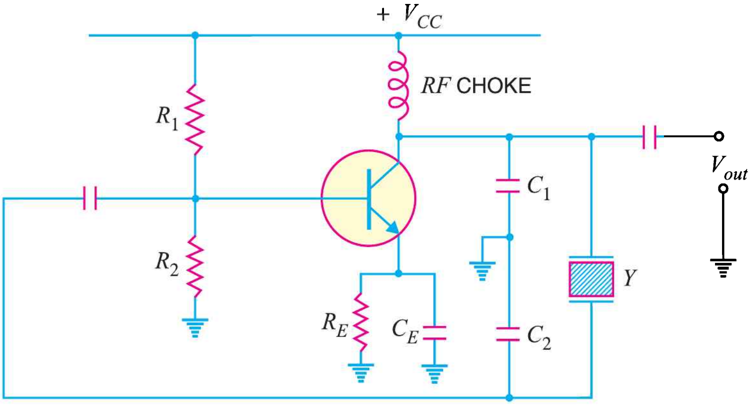


Fig. 14.23

resonance caused by L and $(C_1 + C_2)$, we have the parallel resonance of the crystal. At parallel resonance, the impedance of the crystal is maximum. This means that there is a maximum voltage drop across C_1. This in turn will allow the maximum energy transfer through the feedback network at f_p.

Note that feedback is positive. A phase shift of 180° is produced by the transistor. A further phase shift of 180° is produced by the capacitor voltage divider. This oscillator will oscillate only at f_p. Even the smallest deviation from f_p will cause the oscillator to act as an effective short. Consequently, we have an extremely stable oscillator.

Advantages

(*i*) They have a high order of frequency stability.

(*ii*) The quality factor (Q) of the crystal is very high. The Q factor of the crystal may be as high as 10,000 compared to about 100 of L-C tank.

Disadvantages

(*i*) They are fragile and consequently can only be used in low power circuits.

(*ii*) The frequency of oscillations cannot be changed appreciably.

Example 14.10. *A crystal has a thickness of t mm. If the thickness is reduced by 1%, what happens to frequency of oscillations ?*

Solution. Frequency, $f = \frac{K}{t}$

or $f \propto \frac{1}{t}$

If the thickness of the crystal is reduced by 1%, the frequency of oscillations will increase by 1%.

Example 14.11. *The ac equivalent circuit of a crystal has these values: L = 1H, C = 0.01 pF, R = 1000 Ω and C_m = 20 pF. Calculate f_s and f_p of the crystal.*

Solution.

$$L = 1\text{ H}$$

$$C = 0.01\text{ pF} = 0.01 \times 10^{-12}\text{ F}$$

$$C_m = 20\text{ pF} = 20 \times 10^{-12}\text{ F}$$

$$\therefore \quad f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{1 \times 0.01 \times 10^{-12}}}\text{ Hz}$$

$$= 1589 \times 10^3\text{ Hz} = \mathbf{1589\text{ kHz}}$$

Now

$$C_T = \frac{C \times C_m}{C + C_m} = \frac{0.01 \times 20}{0.01 + 20} = 9.99 \times 10^{-3}\text{ pF}$$

$$= 9.99 \times 10^{-15}\text{ F}$$

$$\therefore \quad f_p = \frac{1}{2\pi\sqrt{LC_T}}$$

$$= \frac{1}{2\pi\sqrt{1 \times 9.99 \times 10^{-15}}}\text{ Hz}$$

$$= 1590 \times 10^3\text{ Hz} = \mathbf{1590\text{ kHz}}$$

If this crystal is used in an oscillator, the frequency of oscillations will lie between 1589 kHz and 1590 kHz.

MULTIPLE-CHOICE QUESTIONS

1. An oscillator converts ....
- (*i*) a.c. power into d.c. power
- (*ii*) d.c. power into a.c. power
- (*iii*) mechanical power into a.c. power
- (*iv*) none of the above

2. In an LC transistor oscillator, the active device is ....
- (*i*) LC tank circuit (*ii*) biasing circuit
- (*iii*) transistor (*iv*) none of the above

3. In an LC circuit, when the capacitor energy is maximum, the inductor energy is ....
- (*i*) minimum (*ii*) maximum
- (*iii*) half-way between maximum and minimum
- (*iv*) none of the above

4. In an *LC* oscillator, the frequency of oscillator is .... *L* or *C*.
- (*i*) proportional to square of
- (*ii*) directly proportional to
- (*iii*) independent of the values of
- (*iv*) inversely proportional to square root of

5. An oscillator produces .... oscillations.
- (*i*) damped (*ii*) undamped
- (*iii*) modulated (*iv*) none of the above

6. An oscillator employs .... feedback.
- (*i*) positive (*ii*) negative
- (*iii*) neither positive nor negative
- (*iv*) data insufficient

7. An LC oscillator cannot be used to produce .... frequencies.
- (*i*) high (*ii*) audio
- (*iii*) very low (*iv*) very high

8. Hartley oscillator is commonly used in ....
- (*i*) radio receivers (*ii*) radio transmitters
- (*iii*) TV receivers (*iv*) none of the above

9. In a phase shift oscillator,we use .... *RC* sections.
- (*i*) two (*ii*) three
- (*iii*) four (*iv*) none of the above

10. In a phase shift oscillator, the frequency determining elements are ....
- (*i*) L and C (*ii*) R, L and C
- (*iii*) R and C (*iv*) none of the above

11. A Wien bridge oscillator uses .... feedback.
- (*i*) only positive (*ii*) only negative
- (*iii*) both positive and negative
- (*iv*) none of the above

12. The piezoelectric effect in a crystal is ....
- (*i*) a voltage developed because of mechanical stress
- (*ii*) a change in resistance because of temperature
- (*iii*) a change of frequency because of temperature
- (*iv*) none of the above

13. If the crystal frequency changes with temperature, we say that crystal has .... temperature coefficient.
- (*i*) positive (*ii*) zero
- (*iii*) negative (*iv*) none of the above

14. The crystal oscillator frequency is very stable due to .... of the crystal.
- (*i*) rigidity (*ii*) vibrations
- (*iii*) low *Q* (*iv*) high *Q*

15. The application where one would most likely find a crystal oscillator is ....
- (*i*) radio receiver (*ii*) radio transmitter
- (*iii*) AF sweep generator
- (*iv*) none of the above

16. An oscillator differs from an amplifer because it ....
- (*i*) has more gain
- (*ii*) requires no input signal
- (*iii*) requires no d.c. supply
- (*iv*) always has the same input

17. One condition for oscillation is ....
- (*i*) a phase shift around the feedback loop of 180°
- (*ii*) a gain around the feedback loop of one-third

(*iii*) a phase shift around the feedback loop of 0°

(*iv*) a gain around the feedback loop of less than 1

18. A second condition for oscillations is ....

(*i*) a gain of 1 around the feedback loop

(*ii*) no gain around the feedback loop

(*iii*) the attenuation of the feedback circuit must be one-third

(*iv*) the feedback circuit must be capacitive

19. In a certain oscillator, $A_v = 50$. The attenuation of the feedback circuit must be ....

(*i*) 1 (*ii*) 0.01

(*iii*) 10 (*iv*) 0.02

20. For an oscillator to properly start, the gain around the feedback loop must initially be ....

(*i*) 1 (*ii*) greater than 1

(*iii*) less than 1

(*iv*) equal to attenuation of feedback circuit

21. In a Wien-bridge oscillator, if the resistances in the positive feedback circuit are decreased, the frequency ....

(*i*) remains the same

(*ii*) decreases

(*iii*) increases

(*iv*) insufficient data

22. In a Colpitt's oscillator, feedback is obtained ....

(*i*) by magnetic induction

(*ii*) by a tickler coil

(*iii*) from the centre of split capacitors

(*iv*) none of the above

23. The Q of a crystal is of the order of ....

(*i*) 100 (*ii*) 1000

(*iii*) 50 (*iv*) more than 10,000

24. Quartz crystal is most commonly used in crystal oscillators because ....

(*i*) it has superior electrical properties

(*ii*) it is easily available

(*iii*) it is quite inexpensive

(*iv*) none of the above

25. In LC oscillators, the frequency of oscillations is given by ....

(*i*) $\frac{2\pi}{\sqrt{LC}}$ (*ii*) $\frac{1}{2\pi\sqrt{LC}}$

(*iii*) $\frac{\sqrt{LC}}{2\pi}$ (*iv*) $\frac{2\pi L}{\sqrt{LC}}$

26. The operating frequency of a Wien-bridge oscillator is given by ....

(*i*) $\frac{1}{2\pi\sqrt{LC}}$ (*ii*) $\frac{1}{4\pi\sqrt{LC}}$

(*iii*) $\frac{1}{2\pi RC}$ (*iv*) $\frac{1}{29\,RC}$

27. .... is a fixed frequency oscillator.

(*i*) Phase-shift oscillator

(*ii*) Hartley oscillator

(*iii*) Colpitt's oscillator

(*iv*) Crystal oscillator

28. In an LC oscillator, if the value of L is increased four times, the frequency of oscillations is ....

(*i*) increased 2 times

(*ii*) decreased 4 times

(*iii*) increased 4 times

(*iv*) decreased 2 times

29. An important limitation of a crystal oscillator is ....

(*i*) its low output (*ii*) its high Q

(*iii*) less availability of quartz crystal

(*iv*) its high output

30. The signal generator generally used in the laboratories is .... oscillator.

(*i*) Wien-bridge (*ii*) Hartley

(*iii*) Crystal (*iv*) Phase shift

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iii*)	**3.** (*i*)	**4.** (*iv*)	**5.** (*ii*)
6. (*i*)	**7.** (*iii*)	**8.** (*i*)	**9.** (*ii*)	**10.** (*iii*)
11. (*iii*)	**12.** (*i*)	**13.** (*i*)	**14.** (*iv*)	**15.** (*ii*)
16. (*ii*)	**17.** (*iii*)	**18.** (*i*)	**19.** (*iv*)	**20.** (*ii*)
21. (*iii*)	**22.** (*iii*)	**23.** (*iv*)	**24.** (*i*)	**25.** (*ii*)
26. (*iii*)	**27.** (*iv*)	**28.** (*iv*)	**29.** (*i*)	**30.** (*i*)

Chapter Review Topics

1. What is an oscillator ? What is its need ? Discuss the advantages of oscillators.
2. What do you understand by damped and undamped electrical oscillations ? Illustrate your answer with examples.
3. Explain the operation of a tank circuit with neat diagrams.
4. What is the nature of oscillations produced by tank circuit ?
5. How will you get undamped oscillations from a tank circuit ?
6. Discuss the essentials of an oscillator.
7. Discuss the circuit operation of tuned collector oscillator.
8. With a neat diagram, explain the action of Hartley and Colpitt's oscillators.
9. What are the drawbacks of LC oscillators ?
10. Write short notes on the following :

    (*i*) *RC* oscillators (*ii*) Wien bridge oscillators (*iii*) Crystal oscillator

Problems

1. Figure 14.24 shows the Colpitt's oscillator. Determine the (*i*) operating frequency and (*ii*) feedback fraction. **[(*i*) 24.5 kHz (*ii*) 0.1]**

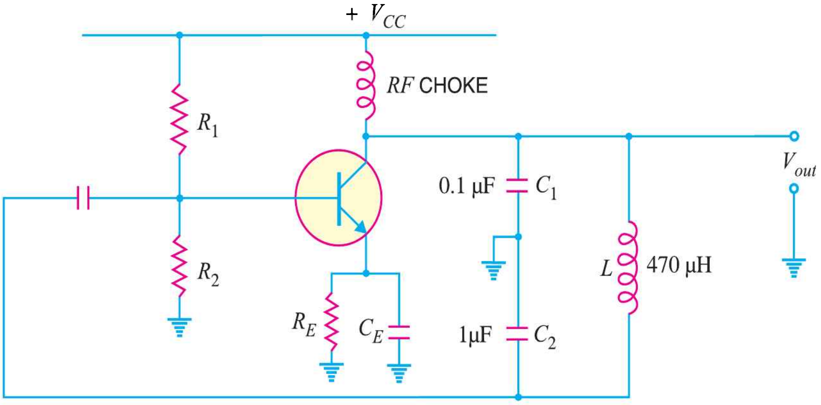


Fig. 14.24

2. Figure 14.25 shows the Hartley oscillator. If L_1 = 1000 µH, L_2 = 100 µH and C = 20 pF, find the (*i*) operating frequency and (*ii*) feedback fraction. **[(*i*) 1052 kHz (*ii*) 0.1]**
3. For the Colpitt's oscillator shown in Fig. 14.24, C_1= 750 pF, C_2 = 2500 pF and L = 40 µH. Determine (*i*) the operating frequency and (*ii*) feedback fraction. **[(*i*) 1050 kHz (*ii*) 0.3]**

4. For the Hartley oscillator shown in Fig. 14.25, $C = 250$ pF, $L_1 = 1.5$ mH, $L_2 = 1.5$ mH and $M = 0.58$ mH. Determine the operating frequency. **[159.2 kHz]**

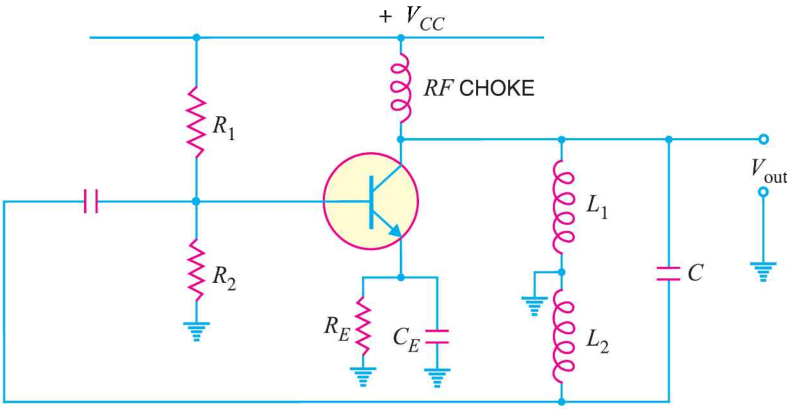


Fig. 14.25

5. A crystal has $L = 3H$, $C = 0.05$ pF, $R = 2$ kΩ and $C_m = 10$ pF. Calculate the series-resonant and parallel-resonant frequencies of the crystal. **[411 kHz ; 412 kHz]**

Discussion Questions

1. Why is amplifier circuit necessary in an oscillator ?
2. Why is crystal oscillator used in radio transmitter ?
3. Why do you use three *RC* sections in *RC* oscillator ?
4. Why is negative feedback provided in Wien bridge oscillators ?
5. Why is quartz crystal commonly used in crystal oscillators ?

15

Transistor Tuned Amplifiers

15.1 Tuned Amplifiers
15.2 Distinction between Tuned Amplifiers and other Amplifiers
15.3 Analysis of Parallel Tuned Circuit
15.4 Characteristics of Parallel Resonant Circuit
15.5 Advantages of Tuned Amplifiers
15.6 Why not Tuned Circuits for Low Frequency Amplification?
15.7 Frequency Response of Tuned Amplifier
15.8 Relation between *Q* and Bandwidth
15.9 Single Tuned Amplifier
15.10 Analysis of Tuned Amplifier
15.11 A.C. Equivalent Circuit of Tuned Amplifier
15.12 Double Tuned Amplifier
15.13 Bandwidth of Double-Tuned Circuit
15.14 Practical Application of Double Tuned Amplifier
15.15 Tuned Class C Amplifier
15.16 Class C Operation
15.17 D.C. and A.C. Loads
15.18 Maximum A.C. Output Power

INTRODUCTION

Most of the audio amplifiers we have discussed in the earlier chapters will also work at radio frequencies *i.e.* above 50 kHz. However, they suffer from two major drawbacks. First, they become less efficient at radio frequency. Secondly, such amplifiers have mostly resistive loads and consequently their gain is independent of signal frequency over a large bandwidth. In other words, an audio amplifier amplifies a wide band of frequencies equally well and does not permit the selection of a particular desired frequency while rejecting all other frequencies.

However, sometimes it is desired that an amplifier should be selective *i.e.* it should select a desired frequency or narrow band of frequencies for amplification. For instance, radio and television transmission are carried on a specific radio frequency assigned to the broadcasting station. The radio receiver is required to pick up and amplify the radio frequency desired while discriminating all others. To achieve this, the simple resistive load is replaced by a parallel tuned circuit whose impedance strongly depends upon frequency. Such a tuned circuit becomes very selective and amplifies very strongly signals of resonant frequency and narrow band on either side. Therefore, the use of tuned circuits in conjunction with a transistor makes possible the selection and efficient amplification of a particular desired radio frequency. Such an amplifier is called a *tuned amplifier*. In this chapter, we shall focus our attention on transistor tuned amplifiers and their increasing applications in high frequency electronic circuits.

15.1 Tuned Amplifiers

Amplifiers which amplify a specific frequency or narrow band of frequencies are called **tuned amplifiers.**

Tuned amplifiers are mostly used for the amplification of high or radio frequencies. It is because radio frequencies are generally single and the tuned circuit permits their selection and efficient amplification. However, such amplifiers are not suitable for the amplification of audio frequencies as they are mixture of frequencies from 20 Hz to 20 kHz and not single. Tuned amplifiers are widely used in radio and television circuits where they are called upon to handle radio frequencies.

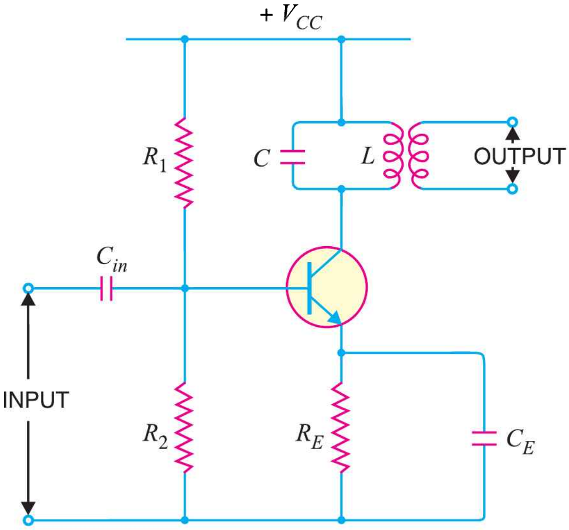


Fig. 15.1

Fig. 15.1 shows the circuit of a simple transistor tuned amplifier. Here, instead of load resistor, we have a parallel tuned circuit in the collector. The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance at *resonant frequency* and very small impedance at all other frequencies. If the signal has the same frequency as the resonant frequency of *LC* circuit, large amplification will result due to high impedance of *LC* circuit at this frequency. When signals of many frequencies are present at the input of tuned amplifier, it will select and strongly amplify the signals of resonant frequency while *rejecting all others. Therefore, such amplifiers are very useful in radio receivers to select the signal from one particular broadcasting station when signals of many other frequencies are present at the receiving aerial.

15.2 Distinction between Tuned Amplifiers and other Amplifiers

We have seen that amplifiers (*e.g.*, voltage amplifier, power amplifier *etc.*) provide the constant gain over a limited band of frequencies *i.e.*, from lower cut-off frequency f_1 to upper cut-off frequency f_2. Now bandwidth of the amplifier, $BW = f_2 - f_1$. The reader may wonder, then, what distinguishes a tuned amplifier from other amplifiers? The difference is that tuned amplifiers are designed to have specific, usually narrow bandwidth. This point is illustrated in in Fig. 15.2. Note that BW_S is the bandwidth of standard frequency response while BW_T is the bandwidth of the tuned amplifier. In many applications, the narrower the bandwidth of a tuned amplifier, the better it is.

---

* For all other frequencies, the impedance of LC circuit will be very small. Consequently, little amplification will occur for these frequencies.

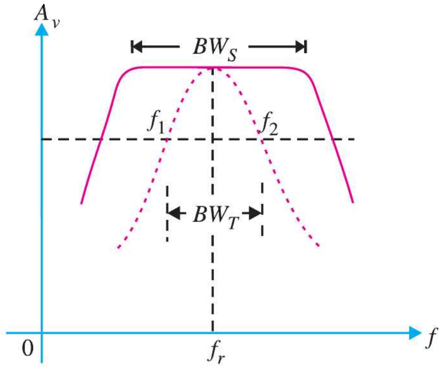


Fig. 15.2

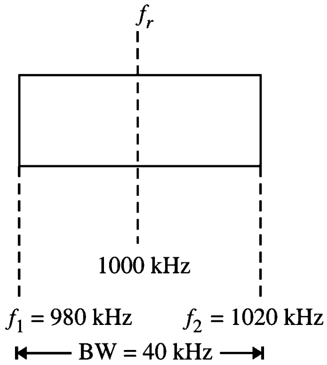


Fig. 15.3

Illustration. Consider a tuned amplifier that is designed to amplify only those frequencies that are within ± 20 kHz of the central frequency of 1000 kHz (*i.e.*, f_r = 1000 kHz). Here [See Fig. 15.3],

$f_1 = 980$ kHz, $f_r = 1000$ kHz, $f_2 = 1020$ kHz, $BW = 40$ kHz

This means that so long as the input signal is within the range of 980 – 1020 kHz, it will be amplified. If the frequency of input signal goes out of this range, amplification will be drastically reduced.

15.3 Analysis of Parallel Tuned Circuit

A parallel tuned circuit consists of a capacitor C and inductor L in parallel as shown in Fig. 15.4 (*i*). In practice, some resistance R is always present with the coil. If an alternating voltage is applied across this parallel circuit, the frequency of oscillations will be that of the applied voltage. However, if the frequency of applied voltage is equal to the natural or resonant frequency of LC circuit, then *electrical resonance* will occur. Under such conditions, the impedance of the tuned circuit becomes maximum and the line current is minimum. The circuit then draws just enough energy from a.c. supply necessary to overcome the losses in the resistance R.

Parallel resonance. A parallel circuit containing reactive elements (L and C) is *resonant when the circuit power factor is unity *i.e.* applied voltage and the supply current are in phase. The phasor diagram of the parallel circuit is shown in Fig. 15. 4 (*ii*). The coil current I_L has two rectangular components *viz* active component $I_L \cos \phi_L$ and reactive component $I_L \sin \phi_L$. This parallel circuit will resonate when the circuit power factor is unity. This is possible only when the net reactive component of the circuit current is zero *i.e.*

$$I_C - I_L \sin \phi_L = 0$$

or

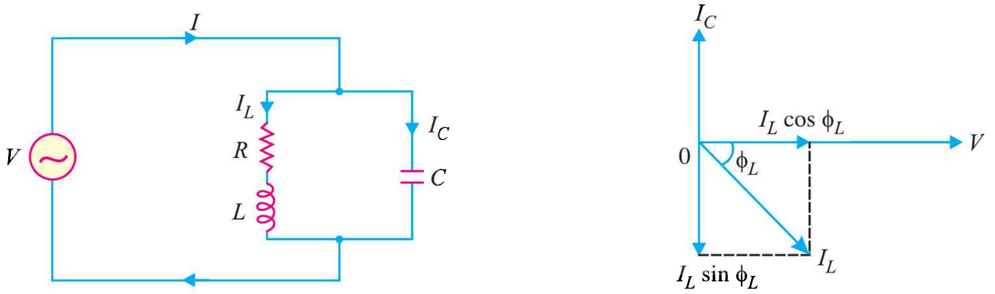
$$I_C = I_L \sin \phi_L$$

Resonance in parallel circuit can be obtained by changing the supply frequency. At some frequency f_r (called resonant frequency), $I_C = I_L \sin \phi_L$ and resonance occurs.

---

* Resonance means to be in step with. In an a.c. circuit if applied voltage and supply current are in phase (*i.e.*, in step with), resonance is said to occur. If this happens in a parallel a.c. circuit, it is called parallel resonance.

Resonant frequency. The frequency at which parallel resonance occurs (*i.e.* reactive component of circuit current becomes zero) is called the *resonant frequency* f_r.



(*i*) (*ii*)

Fig. 15.4

At parallel resonance, we have, $I_C = I_L \sin \phi_L$

Now $I_L = V/Z_L$; $\sin \phi_L = X_L/Z_L$ and $I_C = V/X_C$

$$\therefore \quad \frac{V}{X_C} = \frac{V}{Z_L} \times \frac{X_L}{Z_L}$$

$$\text{or} \quad X_L X_C = Z_L^2$$

$$\text{or} \quad \frac{\omega L}{\omega C} = Z_L^2 = R^2 + X_L^2 \qquad \ldots(i)$$

$$\text{or} \quad \frac{L}{C} = R^2 + (2\pi f_r L)^2$$

$$\text{or} \quad (2\pi f_r L)^2 = \frac{L}{C} - R^2$$

$$\text{or} \quad 2\pi f_r L = \sqrt{\frac{L}{C} - R^2}$$

$$\text{or} \quad f_r = \frac{1}{2\pi L}\sqrt{\frac{L}{C} - R^2}$$

$$\therefore \quad \text{Resonant frequency, } f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}} \qquad \ldots(ii)$$

If coil resistance R is small (as is generally the case), then,

$$f_r = \frac{1}{2\pi\sqrt{LC}} \qquad \ldots(iii)$$

The resonant frequency will be in Hz if R, L and C are in ohms, henry and farad respectively.

Note. If in the problem, the value of R is given, then eq. (*ii*) should be used to find f_r. However, if R is not given, then eq. (*iii*) may be used to find f_r.

15.4 Characteristics of Parallel Resonant Circuit

It is now desirable to discuss some important characteristics of parallel resonant circuit.

(*i*) **Impedance of tuned circuit.** The impedance offered by the parallel LC circuit is given by the supply voltage divided by the line current *i.e.*, V/I. Since at resonance, line current is minimum, therefore, impedance is maximum at resonant frequency. This fact is shown by the impedance-frequency curve of Fig 15.5. It is clear from impedance-frequency curve that impedance rises to a steep peak at resonant frequency f_r. However, the impedance of the circuit decreases rapidly when the frequency is changed above or below the resonant frequency. This characteristic of parallel tuned circuit provides it the selective properties *i.e.* to select the resonant frequency and reject all others.

$$\text{Line current, } I = I_L \cos \phi_L$$

$$\text{or} \quad \frac{V}{Z_r} = \frac{V}{Z_L} \times \frac{R}{Z_L}$$

$$\text{or} \quad \frac{1}{Z_r} = \frac{R}{Z_L^2}$$

$$\text{or} \quad \frac{1}{Z_r} = \frac{R}{L/C} = \frac{CR}{L}$$

$$\left[\because Z_L^2 = \frac{L}{C} \text{ from eq. } (i)\right]$$

$$\therefore \quad \text{Circuit impedance, } Z_r = \frac{L}{CR}$$

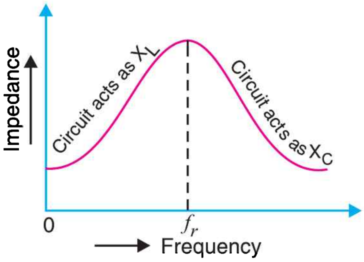


Fig. 15.5

Thus at parallel resonance, the circuit impedance is equal to *L/CR. It may be noted that Z_r will be in ohms if R, L and C are measured in ohms, henry and farad respectively.

(*ii*) Circuit Current. At parallel resonance, the circuit or line current I is given by the applied voltage divided by the circuit impedance Z_r *i.e.*,

$$\text{Line current, } I = \frac{V}{Z_r} \qquad \text{where } Z_r = \frac{L}{CR}$$

Because Z_r is very high, the line current I will be very small.

(*iii*) Quality factor Q. It is desired that resonance curve of a parallel tuned circuit should be as sharp as possible in order to provide selectivity. The sharp resonance curve means that impedance falls rapidly as the frequency is varied from the resonant frequency. The smaller the resistance of coil, the more sharp is the resonance curve. This is due to the fact that a small resistance consumes less power and draws a relatively small line current. The ratio of inductive reactance and resistance of the coil at resonance, therefore, becomes a measure of the quality of the tuned circuit. This is called *quality factor* and may be defined as under :

The ratio of inductive reactance of the coil at resonance to its resistance is known as ****quality factor Q*** *i.e.*,

$$Q = \frac{X_L}{R} = \frac{2\pi f_r L}{R}$$

The quality factor Q of a parallel tuned circuit is very important because the sharpness of resonance curve and hence selectivity of the circuit depends upon it. The higher the value of Q, the more selective is the tuned circuit. Fig. 15.6 shows the effect of resistance R of the coil on the sharpness of

---

* Two things are worth noting. First, Z_r (= L/CR) is a pure resistance because there is no frequency term present. Secondly, the value of Z_r is very high because the ratio L/C is very large at parallel resonance.

** Strictly speaking, the Q of a tank circuit is defined as the ratio of the energy stored in the circuit to the energy lost in the circuit *i.e.*,

$$Q = \frac{\text{Energy stored}}{\text{Energy lost}} = \frac{\text{Reactive Power}}{\text{Resistive Power}} = \frac{I_L^2 X_L}{I_L^2 R} \quad \text{or} \quad Q = \frac{X_L}{R}$$

the resonance curve. It is clear that when the resistance is small, the resonance curve is very sharp. However, if the coil has large resistance, the resonance curve is less sharp. It may be emphasised that where high selectivity is desired, the value of Q should be very large.

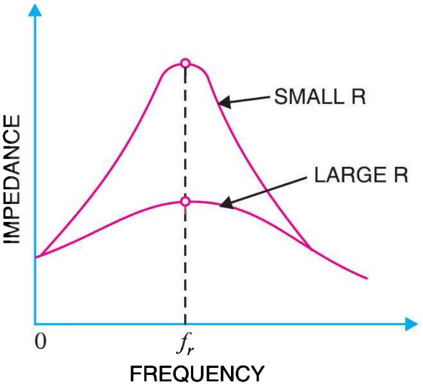


Fig. 15.6

Example 15.1. *A parallel resonant circuit has a capacitor of 250pF in one branch and inductance of 1.25mH plus a resistance of 10Ω in the parallel branch. Find (i) resonant frequency (ii) impedance of the circuit at resonance (iii) Q-factor of the circuit.*

Solution.

$R = 10\Omega\,;\, L = 1.25 \times 10^{-3}\text{H};\, C = 250 \times 10^{-12}\,\text{F}$

(*i*) Resonant frequency of the circuit is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{1.25 \times 10^{-3} \times 250} - \frac{10^2}{(1.25 \times 10^{-3})^2}}\ \text{Hz}$$

$$= 284.7 \times 10^3\ \text{Hz} = \mathbf{284.7\ kHz}$$

(*ii*) Impedance of the circuit at resonance is

$$Z_r = \frac{L}{C\,R} = \frac{1.25 \times 10^{-3}}{250 \times 10^{-12} \times 10} = 500 \times 10^3\ \Omega$$

$$= \mathbf{500\ k\Omega}$$

(*iii*) Quality factor of the circuit is

$$Q = \frac{2\pi f_r L}{R} = \frac{2\pi\,(284.7 \times 10^3) \times 1.25 \times 10^{-3}}{10} = \mathbf{223.6}$$

Example 15.2. *A parallel resonant circuit has a capacitor of 100 pF in one branch and inductance of 100 μH plus a resistance of 10 Ω in parallel branch. If the supply voltage is 10 V, calculate (i) resonant frequency (ii) impedance of the circuit and line current at resonance.*

Solution.

$R = 10\ \Omega,\ L = 100 \times 10^{-6}\text{H}\,;\, C = 100 \times 10^{-12}\,\text{F}$

(*i*) Resonant frequency of the circuit is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{100 \times 10^{-6} \times 100} - \frac{10^2}{(100 \times 10^{-6})^2}}\ \text{Hz}$$

$$= 1592.28 \times 10^3\ \text{Hz} = \mathbf{1592.28\ kHz}$$

(*ii*) Impedance of the circuit at resonance is

$$Z_r = \frac{L}{C\,R} = \frac{L}{C} \times \frac{1}{R} = \frac{100 \times 10^{-6}}{100 \times 10^{-12}} \times \frac{1}{R}$$

$$= 10^6 \times \frac{1}{R} = 10^6 \times \frac{1}{10} = 10^5\ \Omega = \mathbf{0.1\ M\Omega}$$

Note that the circuit impedance Z_r is very high at resonance. It is because the ratio L/C is very large at resonance.

Line current at resonance is

$$I = \frac{V}{Z_r} = \frac{10\ \text{V}}{10^5\ \Omega} = \mathbf{100\ \mu A}$$

Example 15.3. *The *dynamic impedance of a parallel resonant circuit is 500 kΩ. The circuit consists of a 250 pF capacitor in parallel with a coil of resistance 10Ω. Calculate (i) the coil inductance (ii) the resonant frequency and (iii) Q-factor of the circuit.*

Solution.

(*i*) Dynamic impedance, $Z_r = \dfrac{L}{CR}$

∴ Inductance of coil, $L = Z_r CR = (500 \times 10^3) \times (250 \times 10^{-12}) \times 10$

$= 1.25 \times 10^{-3}\ \text{H} = \mathbf{1.25\ mH}$

(*ii*) Resonant frequency, $f_r = \dfrac{1}{2\pi}\sqrt{\dfrac{1}{LC} - \dfrac{R^2}{L^2}}$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{1.25 \times 10^{-3} \times 250} - \frac{10^2}{(1.25 \times 10^{-3})^2}}$$

$= 284.7 \times 10^3\ \text{Hz} = \mathbf{284.7\ kHz}$

(*iii*) Q-factor of the circuit $= \dfrac{2\pi f_r L}{R} = \dfrac{2\pi \times (284.7 \times 10^3) \times (1.25 \times 10^{-3})}{10} = \mathbf{223.6}$

15.5 Advantages of Tuned Amplifiers

In high frequency applications, it is generally required to amplify a single frequency, rejecting all other frequencies present. For such purposes, tuned amplifiers are used. These amplifiers use tuned parallel circuit as the collector load and offer the following advantages :

(*i*) **Small power loss.** A tuned parallel circuit employs reactive components L and C. Consequently, the power loss in such a circuit is quite low. On the other hand, if a resistive load is used in the collector circuit, there will be considerable loss of power. Therefore, tuned amplifiers are highly efficient.

(*ii*) **High selectivity.** A tuned circuit has the property of selectivity *i.e.* it can select the desired frequency for amplification out of a large number of frequencies simultaneously impressed upon it. For instance, if a mixture of frequencies including f_r is fed to the input of a tuned amplifier, then maximum amplification occurs for f_r. For all other frequencies, the tuned circuit offers very low impedance and hence these are amplified to a little extent and may be thought as rejected by the circuit. On the other hand, if we use resistive load in the collector, all the frequencies will be amplified equally well *i.e.* the circuit will not have the ability to select the desired frequency.

(*iii*) **Smaller collector supply voltage.** Because of little resistance in the parallel tuned circuit, it requires small collector supply voltage V_{CC}. On the other hand, if a high load resistance is used in the collector for amplifying even one frequency, it would mean large voltage drop across it due to zero signal collector current. Consequently, a higher collector supply will be needed.

---

* Impedance of parallel resonant circuit at ressonance is called dynamic impedance.

15.6 Why not Tuned Circuits for Low Frequency Amplification ?

The tuned amplifiers are used to select and amplify a specific high frequency or narrow band of frequencies. The reader may be inclined to think as to why tuned circuits are not used to amplify low frequencies. This is due to the following reasons :

(*i*) *Low frequencies are never single.* A tuned amplifier selects and amplifies a single frequency. However, the low frequencies found in practice are the audio frequencies which are a mixture of frequencies from 20 Hz to 20 kHz and are not single. It is desired that all these frequencies should be equally amplified for proper reproduction of the signal. Consequently, tuned amplifiers cannot be used for the purpose.

(*ii*) *High values of L and C.* The resonant frequency of a parallel tuned circuit is given by;

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

For low frequency amplification, we require large values of L and C. This will make the tuned circuit bulky and expensive. It is worthwhile to mention here that R-C and transformer coupled amplifiers, which are comparatively cheap, can be conveniently used for low frequency applications.

15.7 Frequency Response of Tuned Amplifier

The voltage gain of an amplifier depends upon β, input impedance and effective collector load. In a tuned amplifier, tuned circuit is used in the collector. Therefore, voltage gain of such an amplifier is given by :

$$\text{Voltage gain} = \frac{\beta Z_C}{Z_{in}}$$

where Z_C = effective collector load

Z_{in} = input impedance of the amplifier

The value of Z_C and hence gain strongly depends upon frequency in the tuned amplifier. As Z_C is maximum at resonant frequency, therefore, voltage gain will be maximum at this frequency. The value of Z_C and gain decrease as the frequency is varied above and below the resonant frequency. Fig. 15.7 shows the frequency response of a tuned amplifier. It is clear that voltage gain is maximum at resonant frequency and falls off as the frequency is varied in either direction from resonance.

Bandwidth. The range of frequencies at which the voltage gain of the tuned amplifier falls to 70.7 % of the maximum gain is called its *bandwidth.* Referring to Fig. 15.7, the bandwidth of tuned amplifier is $f_1 - f_2$. The amplifier will amplify nicely any signal in this frequency range. The bandwidth of tuned amplifier depends upon the value of Q of LC circuit *i.e.* upon the sharpness of the frequency response. The greater the value of Q of tuned circuit, the lesser is the bandwidth of the amplifier and *vice-versa.* In practice, the value of Q of LC circuit is made such so as to permit the amplification of desired narrow band of high frequencies.

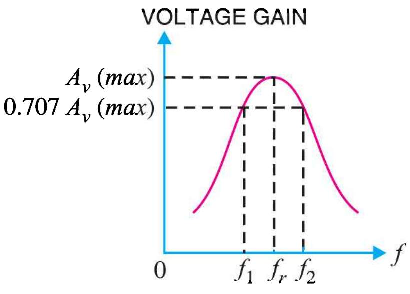


Fig. 15.7

The practical importance of bandwidth of tuned amplifiers is found in communication system. In radio and TV transmission, a very high frequency wave, called *carrier wave* is used to carry the audio or picture signal. In radio transmission, the audio signal has a frequency range of 10 kHz. If the carrier wave frequency is 710 kHz, then the resultant radio wave has a frequency range *between (710 –5) kHz and (710 +5) kHz. Consequently, the tuned amplifier must have a bandwidth of 705 kHz to 715 kHz (*i.e.* 10 kHz). The Q of the tuned circuit should be such that bandwidth of the amplifier lies in this range.

15.8 Relation between *Q* and Bandwidth

The quality factor Q of a tuned amplifier is equal to the ratio of resonant frequency (f_r) to bandwidth (BW) *i.e.*,

$$Q = \frac{f_r}{BW}$$

The Q of an amplifier is determined by the circuit component values. It may be noted here that Q of a tuned amplifier is generally greater than 10. When this condition is met, the resonant frequency at parallel resonance is approximately given by:

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Example 15.4. *The Q of a tuned amplifier is 60. If the resonant frequency for the amplifier is 1200 kHz, find (i) bandwidth and (ii) cut-off frequencies.*

Solution.

(*i*) $$BW = \frac{f_r}{Q} = \frac{1200 \text{ kHz}}{60} = \mathbf{20\ kHz}$$

(*ii*) Lower cut-off frequency, $f_1 = 1200 - 10 = \mathbf{1190\ kHz}$

Upper cut-off frequency, $f_2 = 1200 + 10 = \mathbf{1210\ kHz}$

Example 15.5. *A tuned amplifier has maximum voltage gain at a frequency of 2 MHz and the bandwidth is 50 kHz. Find the Q factor.*

Solution. The maximum voltage gain occurs at the resonant frequency. Therefore, $f_r = 2$ MHz $= 2 \times 10^6$ Hz and BW = 50 kHz $= 50 \times 10^3$ Hz.

Now $$BW = \frac{f_r}{Q}$$

$$\therefore \quad Q = \frac{f_r}{BW} = \frac{2 \times 10^6}{50 \times 10^3} = \mathbf{40}$$

Example 15.6. *Draw the frequency response of an ideal tuned amplifier and discuss its characteristics.*

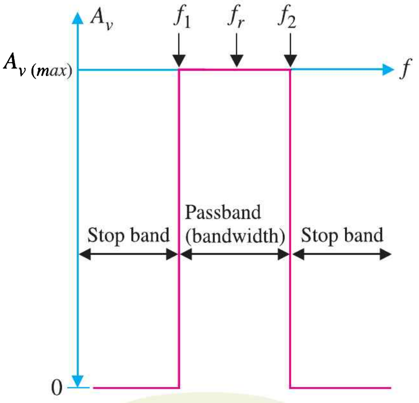


Fig. 15.8

---

* See chapter on modulation and demodulation.

Solution. Fig. 15.8 shows the frequency response of an ideal tuned amplifier. The ideal tuned amplifier has zero gain for all frequencies from 0 Hz up to the lower cut-off frequency f_1. At this point, the gain *instantly* jumps to the maximum value $[A_{v\,(max)}]$. The gain stays at the maximum value until f_2 is reached. At this time, the gain *instantly* drops back to zero. Thus all the frequencies within the bandwidth (f_1 to f_2) of the amplifier would be *passed* by the circuit while all others would be effectively stopped. This is where the terms *pass band* and *stop band* come from. The pass band is the range of frequencies that is passed (amplified) by a tuned amplifier. On the other hand, the stop band is the range of frequencies that is outside the amplifier's pass band.

In practice, the ideal characteristics of the tuned amplifier cannot be achieved. In a practical frequency response (refer back to Fig. 15.7), the gain falls gradually from maximum value as the frequency goes outside the f_1 or f_2 limits. However, the closer the frequency response of a tuned amplifier to that of the ideal, the better.

15.9 Single Tuned Amplifier

A single tuned amplifier consists of a transistor amplifier containing a parallel tuned circuit as the collector load. The values of capacitance and inductance of the tuned circuit are so selected that its resonant frequency is equal to the frequency to be amplified. The output from a single tuned amplifier can be obtained either (*a*) by a coupling capacitor C_C as shown in Fig. 15.9 (*i*) or (*b*) by a secondary coil as shown in Fig. 15.9 (*ii*).

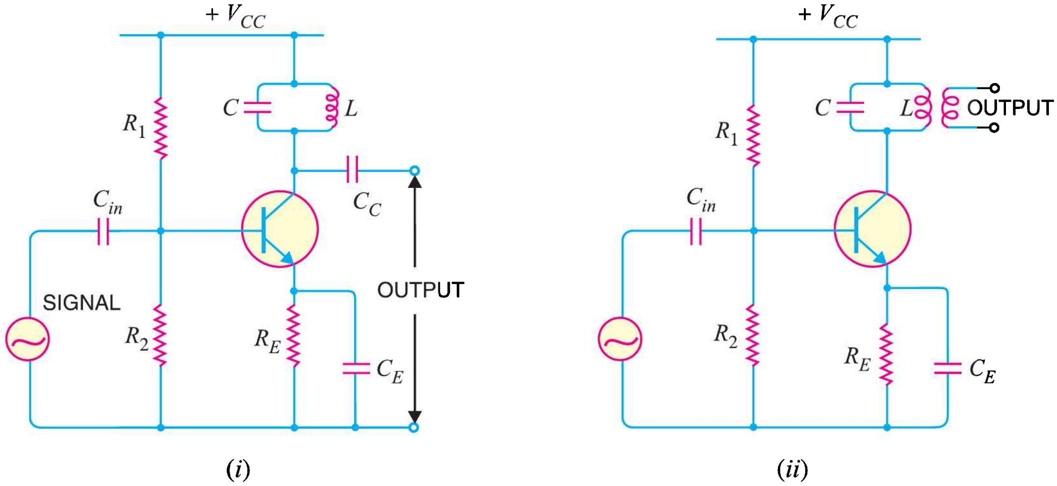


Fig. 15.9

Operation. The high frequency signal to be amplified is given to the input of the amplifier. The resonant frequency of parallel tuned circuit is made equal to the frequency of the signal by changing the value of C. Under such conditions, the tuned circuit will offer very high impedance to the signal frequency. Hence a large output appears across the tuned circuit. In case the input signal is complex containing many frequencies, only that frequency which corresponds to the resonant frequency of the tuned circuit will be amplified. All other frequencies will be rejected by the tuned circuit. In this way, a tuned amplifier selects and amplifies the desired frequency.

Note. The fundamental difference between *AF* and tuned (*RF*) amplifiers is the bandwidth they are expected to amplify. The *AF* amplifiers amplify a major portion of *AF* specturm (20 Hz to 20 kHz) equally well throughout. The tuned amplifiers amplify a relatively narrow portion of *RF* spectrum, rejecting all other frequencies.

15.10 Analysis of Tuned Amplifier

Fig. 15.10 (*i*) shows a single tuned amplifier. Note the presence of the parallel *LC* circuit in the collector circuit of the transistor. When the circuit has a high *Q*, the parallel resonance occurs at a frequency f_r given by:

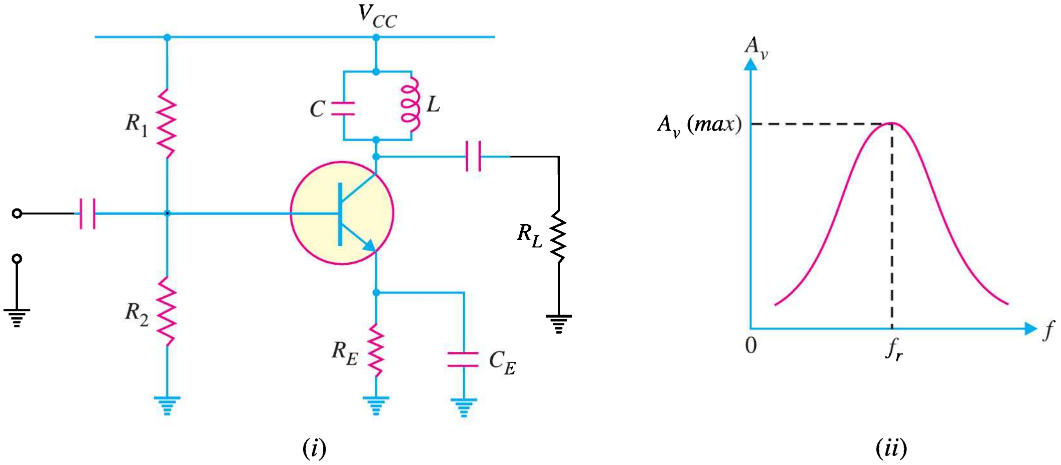


Fig. 15.10

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

At the resonant frequency, the impedance of the parallel resonant circuit is very high and is purely resistive. Therefore, when the circuit is tuned to resonant frequency, the voltage across R_L is maximum. In other words, the voltage gain is maximum at f_r. However, above and below the resonant frequency, the voltage gain decreases rapidly. The higher the *Q* of the circuit, the faster the gain drops off on either side of resonance [See Fig. 15.10 (*ii*)].

15.11 A.C. Equivalent Circuit of Tuned Amplifier

Fig. 15.11 (*i*) shows the *ac* equivalent circuit of the tuned amplifier. Note the tank circuit components are not shorted. In order to completely understand the operation of this circuit, we shall see its behaviour at three frequency conditions *viz.*,

(*i*) $f_{in} = f_r$ (*ii*) $f_{in} < f_r$ (*iii*) $f_{in} > f_r$

(*i*) **When input frequency equals** f_r (*i.e.*, $f_{in} = f_r$). When the frequency of the input signal is equal to f_r, the parallel *LC* circuit offers a very high impedance *i.e.*, it acts as an open. Since R_L represents the only path to ground in the collector circuit, all the ac collector current flows through R_L. Therefore, voltage across R_L is maximum *i.e.*, the voltage gain is maximum as shown in Fig. 15.11 (*ii*).

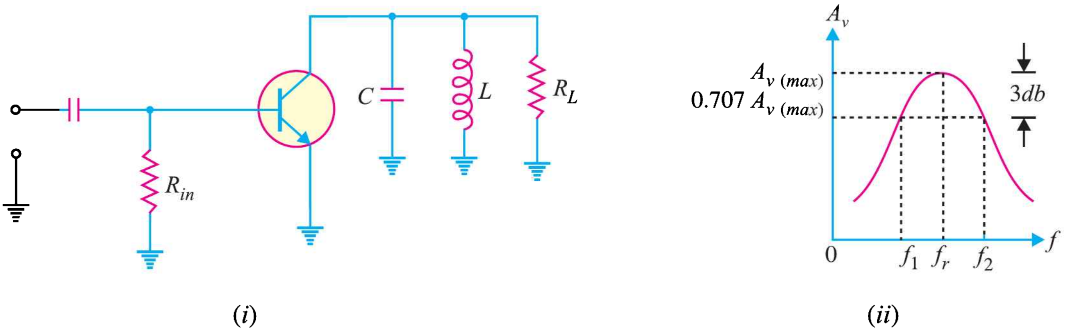


Fig. 15.11

(*ii*) **When input frequency is less than** f_r (*i.e.*, $f_{in} < f_r$). When the input signal frequency is less than f_r, the circuit is effectively* inductive. As the frequency decreases from f_r, a point is reached when $X_C - X_L = R_L$. When this happens, the voltage gain of the amplifier falls by 3 *db*. In other words, the lower cut-off frequency f_1 for the circuit occurs when $X_C - X_L = R_L$.

(*iii*) **When input frequency is greater than** f_r (*i.e.*, $f_{in} > f_r$). When the input signal frequency is greater than f_r, the circuit is effectively capacitive. As f_{in} is increased beyond f_r, a point is reached when $X_L - X_C = R_L$. When this happens, the voltage gain of the amplifier will again fall by 3*db*. In other words, the upper cut-off frequency for the circuit will occur when $X_L - X_C = R_L$.

Example 15.7. *For the tuned amplifier shown in Fig. 15.12, determine (i) the resonant frequency (ii) the Q of tank circuit and (iii) bandwidth of the amplifier.*

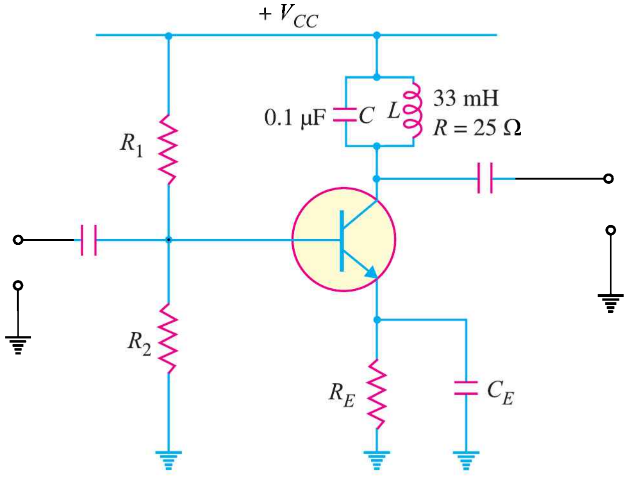


Fig. 15.12

Solution.

(*i*) Resonant frequency,
$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{33\times10^{-3}\times0.1\times10^{-6}}}$$
$$= 2.77\times10^3 \text{ Hz} = \textbf{2.77 kHz}$$

(*ii*) $X_L = 2\pi f_r L = 2\pi\times(2.77\times10^3)\times33\times10^{-3} = 574\ \Omega$

$$\therefore \quad Q = \frac{X_L}{R} = \frac{574}{25} = \textbf{23}$$

(*iii*)
$$BW = \frac{f_r}{Q} = \frac{2.77\text{ kHz}}{23} = \textbf{120 Hz}$$

15.12 Double Tuned Amplifier

Fig. 15.13 shows the circuit of a double tuned amplifier. It consists of a transistor amplifier containing two tuned circuits ; one (L_1C_1) in the collector and the other (L_2C_2) in the output as shown. The high frequency signal to be amplified is applied to the input terminals of the amplifier. The resonant frequency of tuned circuit L_1C_1 is made equal to the signal frequency. Under such conditions, the

---

* At frequencies below f_r, $X_C > X_L$ or $I_L > I_C$. Therefore, the circuit will be inductive.

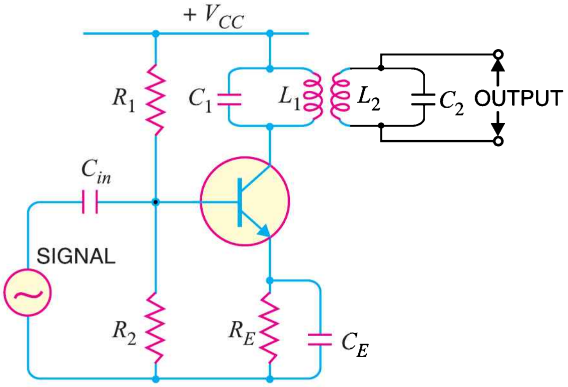


Fig. 15.13

tuned circuit offers very high impedance to the signal frequency. Consequently, large output appears across the tuned circuit L_1C_1. The output from this tuned circuit is transferred to the second tuned circuit L_2C_2 through mutual induction. Double tuned circuits are extensively used for coupling the various circuits of radio and television receivers.

Frequency response. The frequency response of a double tuned circuit depends upon the degree of coupling *i.e.* upon the amount of mutual inductance between the two tuned circuits. When coil L_2 is coupled to coil L_1 [See Fig. 15.14 (*i*)], a portion of load resistance is coupled into the primary tank circuit L_1C_1 and affects the primary circuit in exactly the same manner as though a resistor had been added in series with the primary coil L_1.

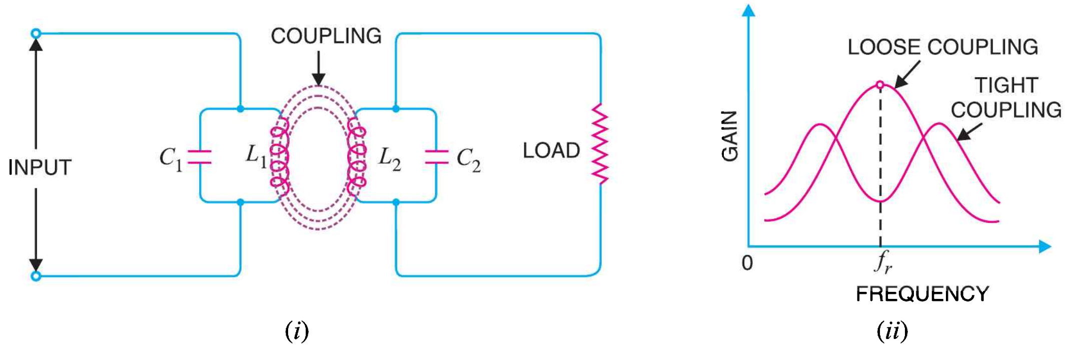


Fig.15.14

When the coils are spaced apart, all the primary coil L_1 flux will not link the secondary coil L_2. The coils are said to have *loose coupling*. Under such conditions, the resistance reflected from the load (*i.e.* secondary circuit) is small. The resonance curve will be sharp and the circuit Q is high as shown in Fig. 15.14 (*ii*). When the primary and secondary coils are very close together, they are said to have *tight coupling*. Under such conditions, the reflected resistance will be large and the circuit Q is lower. Two positions of gain maxima, one above and the other below the resonant frequency, are obtained.

15.13 Bandwidth of Double-Tuned Circuit

If you refer to the frequency response of double-tuned circuit shown in Fig. 15.14 (*ii*), it is clear that bandwidth increases with the degree of coupling. Obviously, the determining factor in a double-tuned circuit is not Q but the coupling. For a given frequency, the tighter the coupling, the greater is the bandwidth.

$$BW_{dt} = k f_r$$

The subscript *dt* is used to indicate double-tuned circuit. Here *k* is coefficient of coupling.

Example 15.8. *It is desired to obtain a bandwidth of 200 kHz at an operating frequency of 10 MHz using a double tuned circuit. What value of co-efficient of coupling should be used ?*

Solution.

$$BW_{dt} = k f_r$$

∴ Co-efficient of coupling, $k = \dfrac{BW_{dt}}{f_r} = \dfrac{200\text{ kHz}}{10 \times 10^3\text{ kHz}} = \mathbf{0.02}$

15.14 Practical Application of Double Tuned Amplifier

Double tuned amplifiers are used for amplifying radio-frequency (*RF*) signals. One such application is in the radio receiver as shown in Fig. 15.15. This is the IF stage using double tuned resonant circuits. Each resonant circuit is tuned to *455 kHz. The critical coupling occurs when the coefficient of coupling is

$$k_{cirtical} = \frac{1}{\sqrt{Q_1 Q_2}}$$

where Q_1 = quality factor of primary resonant circuit ($L_1 C_1$)

Q_2 = quality factor of secondary resonant circuit ($L_2 C_2$)

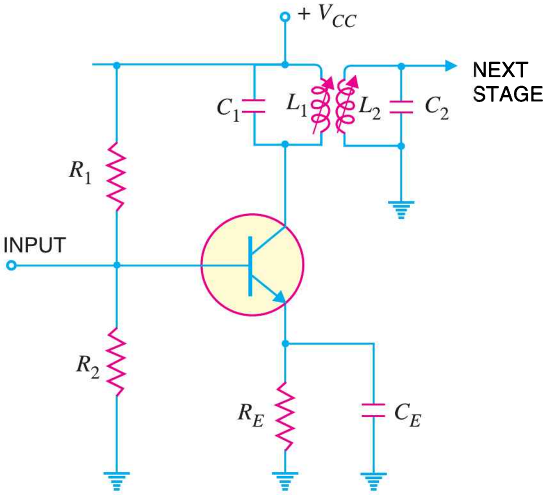


Fig. 15.15

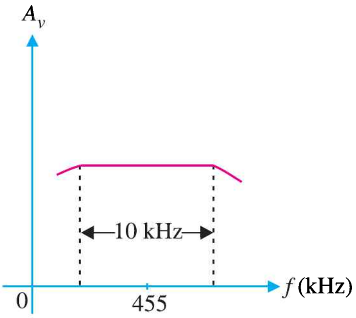


Fig. 15.16

When two resonant circuits are critically coupled, the frequency response becomes flat over a considerable range of frequencies as shown in Fig. 15.16. In other words, the double tuned circuit has better frequency response as compared to that of a single tuned circuit. The use of double tuned circuit offers the following advantages :

(*i*) Bandwidth is increased.

(*ii*) Sensitivity (*i.e.* ability to receive weak signals) is increased.

(*iii*) Selectivity (*i.e.* ability to discriminate against signals in adjacent bands) is increased.

15.15 Tuned Class C Amplifier

So far we have confined our attention to tuned class *A* amplifiers. Such amplifiers are used where *RF* signal has low power level *e.g.* in radio receivers, small signal applications in transmitters. However, owing to low efficiency of class *A* operation, these amplifiers are not employed where large *RF* (radio frequency) power is involved *e.g.* to excite transmitting antenna. In such situations, tuned class *C* power amplifiers are used. Since a class *C* amplifier has a very high efficiency, it can deliver more load power than a class *A* amplifier.

---

* In a radio receiver, the *IF* (intermediate frequency) of 455 kHz is obtained from the mixer circuit regardless of radio station to which the receiver is tuned (See Chapter 16).

Class C operation means that collector current flows for less than 180°. In a practical tuned class C amplifier, the collector current flows for much less than 180° ; the current looks like narrow pulses as shown in Fig. 15.17. As we shall see later, when narrow current pulses like these drive a high-Q resonant (*i.e.* LC) circuit, the voltage across the circuit is almost a perfect sine wave. One very important advantage of class C operation is its *high efficiency. Thus 10 W supplied to a class A amplifier may produce only about 3.5 W of a.c. output (35 % efficiency). The same transistor biased to class C may be able to produce 7 W output (70 % efficiency). Class C power amplifiers normally use RF power transistors. The power ratings of such transistors range from 1 W to over 100 W.

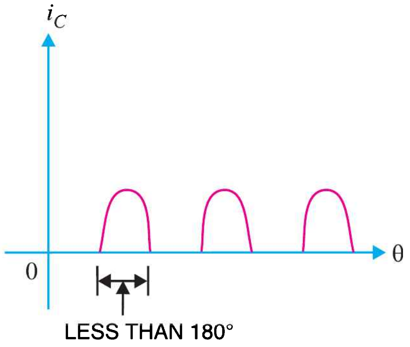
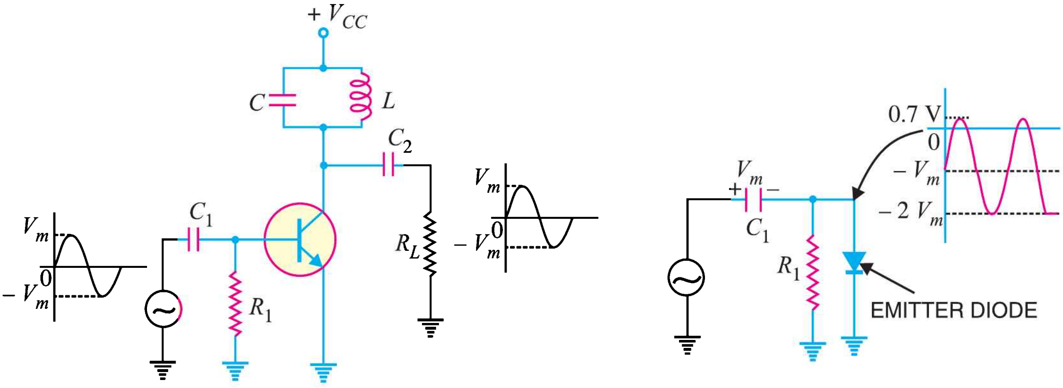


Fig. 15.17

15.16 Class C Operation

Fig. 15.18 (*i*) shows the circuit of tuned class C amplifier. The circuit action is as under:

(*i*) When no a.c. input signal is applied, no collector current flows because the emitter diode (*i.e.* base-emitter junction) is unbiased.



(*i*) (*ii*)

Fig. 15.18

(*ii*) When an a.c. signal is applied, *clamping action* takes place as shown in Fig. 15.18 (*ii*). The voltage across the emitter diode varies between + 0.7 V (during positive peaks of input signal) to about $-2V_m$ (during negative peaks of input signal). This means that conduction of the transistor occurs only for a short period during positive peaks of the signal. This results in the pulsed output *i.e.* collector current waveform is a train of narrow pulses (Refer back to Fig. 15.17).

(*iii*) When this pulsed output is fed to the LC circuit, **sine-wave output is obtained. This can be easily explained. Since the pulse is narrow, inductor looks like high impedance and the capacitor like a low impedance. Consequently, most of the current charges the capacitor as shown in Fig. 15.19.

---

* Class C amplifier has a relatively long duration between the pulses, allowing the transistor to rest for a major portion of each input cycle. In other words, very little power is dissipated by the transistor. For this reason, class C amplifier has high efficiency.

** There is another explanation for it. The pulsed output is actually the sum of an infinite number of sine waves at frequencies in multiples of the input frequency. If the LC tank circuit is set up to resonate at the input frequency, it will result in sine-wave output of just the input frequency.

When the capacitor is fully charged, it will discharge through the coil and the load resistor, setting up oscillations just as an oscillatory circuit does. Consequently, sine-wave output is obtained.

(iv) If only a single current pulse drives the *LC* circuit, we will get damped sine-wave output. However, if a train of narrow pulses drive the *LC* circuit, we shall get undamped sine-wave output.

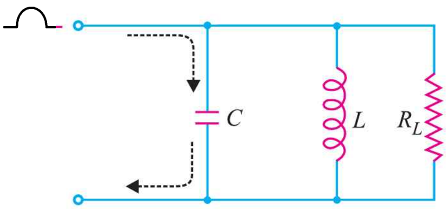


Fig. 15.19

15.17 D.C. and A.C. Loads

Fig. 15.20 shows the circuit of tuned class *C* amplifier. We shall determine the d.c. and a.c. load of the circuit.

(*i*) The d.c. load of the circuit is just the d.c. resistance *R* of the inductor because the capacitor looks like an open to d.c.

$\therefore$ D.C. load, R_{dc} = d.c. resistance of the inductor = R

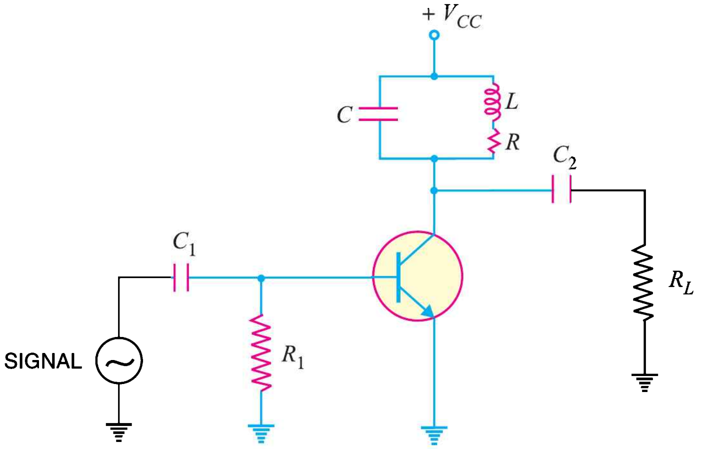


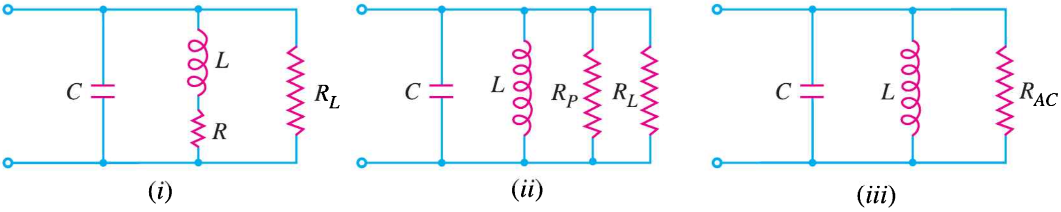
Fig. 15.20

(*ii*) The a.c. load is a parallel combination of capacitor, coil and load resistance R_L as shown in Fig. 15.21 (*i*). The series resistance *R* of the inductor can be replaced by its equivalent parallel resistance R_P as shown in Fig. 15.21 (*ii*) where

$$R_P = Q_{coil} \times X_L$$

The a.c. load resistance R_{AC} is the equivalent resistance of the parallel combination of R_P and R_L *i.e.*

$$R_{AC} = R_P \,||\, R_L = \frac{R_P \times R_L}{R_P + R_L}$$



(*i*) (*ii*) (*iii*)

Fig. 15.21

Example 15.9. *In the circuit shown in Fig. 15.20, C = 500 pF and the coil has L = 50.7 μH and R = 10Ω and R_L = 1 MΩ. Find (i) the resonant frequency (ii) d.c. load and a.c. load.*

Solution.

(*i*) Resonant frequency, $f_r \simeq \dfrac{1}{2\pi\sqrt{LC}} = \dfrac{10^9}{2\pi\sqrt{50.7 \times 500}} = \mathbf{106\ Hz}$

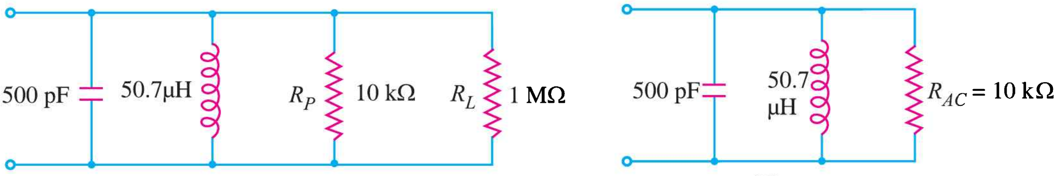
(*ii*) D.C. load, $R_{dc} = R = \mathbf{10\ \Omega}$

$$X_L = 2\pi f_r L = 2\pi \times (10^6) \times (50.7 \times 10^{-6}) = 318\ \Omega$$

$$Q_{coil} = \frac{X_L}{R} = \frac{318}{10} = 31.8$$

The series resistance R (= 10 Ω) of the inductor can be replaced by its equivalent parallel resistance R_P where,

$$R_P = Q_{coil} \times X_L = 31.8 \times 318 = 10^4\ \Omega = 10\ \text{k}\Omega$$



(*i*) (*ii*)

Fig. 15.22

The equivalent circuit is shown in Fig. 15.22 (*i*). This further reduces to the circuit shown in Fig. 15.22 (*ii*).

$$\therefore \quad R_{AC} = R_P \parallel R_L = 10\ \text{k}\Omega \parallel 1\ \text{M}\Omega \simeq \mathbf{10\ k\Omega}$$

15.18 Maximum A.C. Output Power

Fig. 15.23 (*i*) shows tuned class *C* amplifier. When no signal is applied, the collector-emitter voltage is *V_{CC} *i.e.*

$$v_{CE} = V_{CC}$$

When signal is applied, it causes the total collector-emitter voltage to swing above and below this voltage. The collector-emitter voltage can have a maximum value of $2V_{CC}$ and minimum value 0 (ideally) as shown in Fig. 15.23 (*ii*).

Referring to Fig. 15.23 (*ii*), output voltage has a peak value of V_{CC}. Therefore, the maximum a.c. output power is :

$$P_{o(max)} = \frac{V_{r.m.s.}^2}{R_{AC}} = \frac{\left(V_{CC}/\sqrt{2}\right)^2}{R_{AC}} = \frac{V_{CC}^2}{2R_{AC}}$$

where R_{AC} = a.c. load

Maximum efficiency. The d.c. input power (P_{dc}) from the supply is :

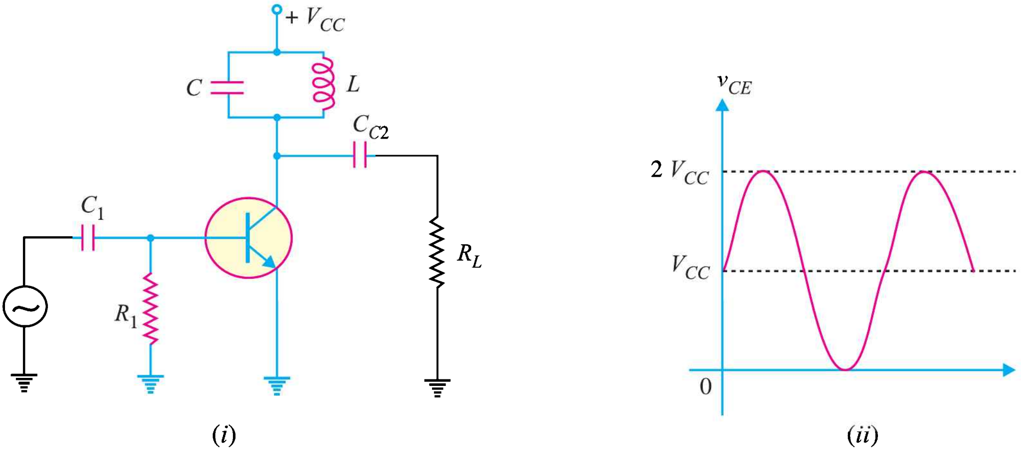
$$P_{dc} = P_{o(max)} + P_D$$

where P_D = power dissipation of the transistor

$$\therefore \quad \text{Max. collector } \eta = \frac{P_{o(max)}}{P_{o(max)} + P_D}$$

---

* Because the drop in *L* due to d.c. component is negligible.



(i) (ii)

Fig. 15.23

As discussed earlier, P_D in class *C* operation is very small because the transistor remains biased off during most of the input signal cycle. Consequently, P_D may be neglected as compared to $P_{o(max)}$.

$$\therefore \qquad \text{Maximum } \eta \simeq \frac{P_{o(max)}}{P_{o(max)}} \simeq 100\ \%$$

It is worthwhile to give a passing reference about the maximum efficiencies of class *A*, class *B* and class *C* amplifiers. *A* class *A* amplifier (transformer-coupled) has a maximum efficiency of 50%, class *B* of 78.5% and class *C* nearly 100%. It is emphasised here that class *C* operation is suitable only for *resonant *RF* applications.

Example 15.10. *Calculate (i) a.c. load (ii) maximum load power in the circuit shown in Fig. 15.24.*

Solution.

(*i*) A.C. load, R_{AC} = Reflected load resistance seen by the collector

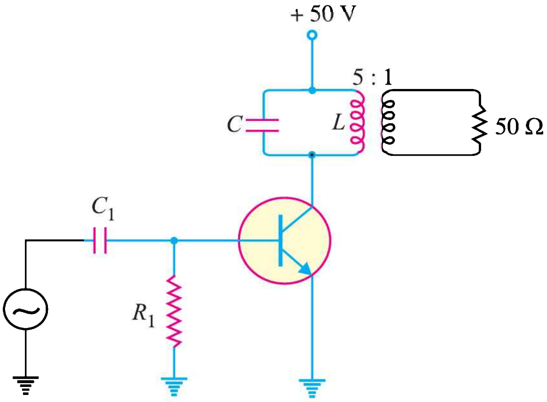


Fig. 15.24

---

* Because power losses are very small (less than 1 %) in high - *Q* resonant circuits. An extremely narrow pulse will compensate the losses.

$$= (N_p/N_s)^2 \times 50 = (5/1)^2 \times 50 = \mathbf{1250\ \Omega}$$

(*ii*) Max. load power, $$P_{o(max)} = \frac{V_{CC}^2}{2R_{AC}} = \frac{(50)^2}{2\times 1250} = \mathbf{1\ W}$$

Example 15.11. *In the above example, if power dissipation of the transistor is 4 mW, find the maximum collector efficiency.*

Solution.

$$P_{o\,(max)} = 1\text{W};\ P_D = 4\text{mW} = 4 \times 10^{-3}\ \text{W}$$

$$\therefore \quad \text{Max. collector } \eta = \frac{P_{o\,(\max)}}{P_{o(\max)} + P_D} \times 100$$

$$= \frac{1}{1 + 4\times 10^{-3}} \times 100 = \mathbf{99.6\%}$$

Note that maximum collector efficiency is very close to the ideal case of 100% efficiency. Therefore, we can neglect P_D in circuit calculations with reasonable accuracy.

MULTIPLE-CHOICE QUESTIONS

1. A tuned amplifier uses .... load.
(*i*) resistive (*ii*) capacitive
(*iii*) LC tank (*iv*) inductive

2. A tuned amplifier is generally operated in .... operation.
(*i*) class A (*ii*) class C
(*iii*) class B (*iv*) none of the above

3. A tuned amplifier is used in .... applications.
(*i*) radio frequency
(*ii*) low frequency
(*iii*) audio frequency
(*iv*) none of the above

4. Frequencies above .... kHz are called radio frequencies.
(*i*) 2 (*ii*) 10
(*iii*) 50 (*iv*) 200

5. At series or parallel resonance, the circuit power factor is ....
(*i*) 0 (*ii*) 0.5
(*iii*) 1 (*iv*) 0.8

6. The voltage gain of a tuned amplifier is .... at resonant frequency.
(*i*) minimum (*ii*) maximum
(*iii*) half-way between maximum and minimum
(*iv*) zero

7. At parallel resonance, the line current is ....
(*i*) minimum (*ii*) maximum
(*iii*) quite large (*iv*) none of the above

8. At series resonance, the circuit offers .... impedance.
(*i*) zero (*ii*) maximum
(*iii*) minimum (*iv*) none of the above

9. A resonant circuit contains .... elements.
(*i*) *R* and *L* only (*ii*) *R* and *C* only
(*iii*) only *R* (*iv*) *L* and *C*

10. At series or parallel resonance, the circuit behaves as a .... load.
(*i*) capacitive (*ii*) resistive
(*iii*) inductive (*iv*) none of the above

11. At series resonance, voltage across *L* is .... voltage across *C*.
(*i*) equal to but opposite in phase to
(*ii*) equal to but in phase with
(*iii*) greater than but in phase with
(*iv*) less than but in phase with

12. When either *L* or *C* is increased, the resonant frequency of *LC* circuit ....
(*i*) remains the same
(*ii*) increases (*iii*) decreases
(*iv*) insufficient data

13. At parallel resonance, the net reactive component of circuit current is ....

(*i*) capacitive (*ii*) zero
(*iii*) inductive (*iv*) none of the above

14. At parallel resonance, the circuit impedance is ....

(*i*) $\frac{C}{LR}$ (*ii*) $\frac{R}{LC}$
(*iii*) $\frac{CR}{L}$ (*iv*) $\frac{L}{CR}$

15. In a parallel LC circuit, if the input signal frequency is increased above resonant frequency, then ....

(*i*) X_L increases and X_C decreases
(*ii*) X_L decreases and X_C increases
(*iii*) both X_L and X_C increase
(*iv*) both X_L and X_C decrease

16. The Q of an LC circuit is given by ....

(*i*) $2\pi f_r \times R$ (*ii*) $\frac{R}{2\pi\, f_r L}$
(*iii*) $\frac{2\pi\, f_r L}{R}$ (*iv*) $\frac{R^2}{2\pi\, f_r L}$

17. If Q of an LC circuit increases, then bandwidth ....

(*i*) increases (*ii*) decreases
(*iii*) remains the same
(*iv*) insufficient data

18. At series resonance, the net reactive component of circuit current is ....

(*i*) zero (*ii*) inductive
(*iii*) capacitive (*iv*) none of the above

19. The dimensions of L/CR are that of ....

(*i*) farad (*ii*) henry
(*iii*) ohm (*iv*) none of the above

20. If L/C ratio of a parallel LC circuit is increased, the Q of the circuit ....

(*i*) is decreased (*ii*) is increased
(*iii*) remains the same
(*iv*) none of the above

21. At series resonance, the phase angle between applied voltage and circuit current is ....

(*i*) 90° (*ii*) 180°
(*iii*) 0° (*iv*) none of the above

22. At parallel resonance, the ratio L/C is ....

(*i*) very large (*ii*) zero
(*iii*) small (*iv*) none of the above

23. If the resistance of a tuned circuit is increased, the Q of the circuit ....

(*i*) is increased (*ii*) is decreased
(*iii*) remains the same
(*iv*) none of the above

24. The Q of a tuned circuit refers to the property of ....

(*i*) sensitivity (*ii*) fidelity
(*iii*) selectivity (*iv*) none of the above

25. At parallel resonance, the phase angle between the applied voltage and circuit current is ....

(*i*) 90° (*ii*) 180°
(*iii*) 0° (*iv*) none of the above

26. In a parallel LC circuit, if the signal frequency is decreased below the resonant frequency, then ....

(*i*) X_L decreases and X_C increases
(*ii*) X_L increases and X_C decreases
(*iii*) line current becomes minimum
(*iv*) none of the above

27. In series resonance, there is ....

(*i*) voltage amplification
(*ii*) current amplification
(*iii*) both voltage and current amplification
(*iv*) none of the above

28. The Q of a tuned amplifier is generally ....

(*i*) less than 5 (*ii*) less than 10
(*iii*) more than 10 (*iv*) none of the above

29. The Q of a tuned amplifier is 50. If the resonant frequency for the amplifier is 1000 kHz, then bandwidth is ....

(*i*) 10 kHz (*ii*) 40 kHz
(*iii*) 30 kHz (*iv*) 20 kHz

30. In the above question, what are the values of cut-off frequencies ?

(*i*) 140 kHz, 60 kHz
(*ii*) 1020 kHz, 980 kHz
(*iii*) 1030 kHz, 970 kHz
(*iv*) none of the above

31. For frequencies above the resonant frequency, a parallel LC circuit behaves as a .... load.

(*i*) capacitive
(*ii*) resistive
(*iii*) inductive
(*iv*) none of the above

32. In parallel resonance, there is ....
- (*i*) both voltage and current amplification
- (*ii*) voltage amplification
- (*iii*) current amplification
- (*iv*) none of the above

33. For frequencies below resonant frequency, a series *LC* circuit behaves as a .... load.
- (*i*) resistive
- (*ii*) capacitive
- (*iii*) inductive
- (*iv*) none of the above

34. If a high degree of selectivity is desired, then double-tuned circuit should have .... coupling.
- (*i*) loose
- (*ii*) tight
- (*iii*) critical
- (*iv*) none of the above

35. In the double tuned circuit, if the mutual inductance between the two tuned circuits is decreased, the level of resonance curve ....
- (*i*) remains the same
- (*ii*) is lowered
- (*iii*) is raised
- (*iv*) none of the above

36. For frequencies above the resonant frequency, a series *LC* circuit behaves as a .... load.
- (*i*) resistive
- (*ii*) inductive
- (*iii*) capacitive
- (*iv*) none of the above

37. Double tuned circuits are used in .... stages of a radio receiver
- (*i*) IF
- (*ii*) audio
- (*iii*) output
- (*iv*) none of the above

38. A class C amplifier always drives .... load.
- (*i*) a pure resistive
- (*ii*) a pure inductive
- (*iii*) a pure capacitive
- (*iv*) a resonant tank

39. Tuned class C amplifiers are used for RF signals of ....
- (*i*) low power
- (*ii*) high power
- (*iii*) very low power
- (*iv*) none of the above

40. For frequencies below the resonant frequency, a parallel LC circuit behaves as a .... load.
- (*i*) inductive
- (*ii*) resistive
- (*iii*) capacitive
- (*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*iii*)	**2.** (*ii*)	**3.** (*i*)	**4.** (*iv*)	**5.** (*iii*)
6. (*ii*)	**7.** (*i*)	**8.** (*iii*)	**9.** (*iv*)	**10.** (*ii*)
11. (*i*)	**12.** (*iii*)	**13.** (*ii*)	**14.** (*iv*)	**15.** (*i*)
16. (*iii*)	**17.** (*ii*)	**18.** (*i*)	**19.** (*iii*)	**20.** (*ii*)
21. (*iii*)	**22.** (*i*)	**23.** (*ii*)	**24.** (*iii*)	**25.** (*iii*)
26. (*i*)	**27.** (*i*)	**28.** (*iii*)	**29.** (*iv*)	**30.** (*ii*)
31. (*i*)	**32.** (*iii*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*iii*)
36. (*ii*)	**37.** (*i*)	**38.** (*iv*)	**39.** (*iv*)	**40.** (*i*)

Chapter Review Topics

1. What are tuned amplifiers and where are they used ?
2. Discuss parallel tuned circuit with special reference to resonant frequency, circuit impedance and frequency response.
3. What do you understand by quality factor *Q* of parallel tuned circuit ?
4. Discuss the advantages of tuned amplifiers.
5. Discuss the circuit operation of a single tuned amplifier.
6. Write short notes on the following :
    (*i*) Double tuned amplifier (*ii*) Bandwidth of tuned amplifier

Problems

1. A parallel circuit has a capacitor of 100 pF in one branch and an inductance of 100 μH plus a resistance of 10 Ω in the second branch. The line voltage is 100V. Find (*i*) resonant frequency (*ii*) circuit impedance at resonance and (*iii*) line current at resonance. **[(*i*) 1590 kHz (*ii*) 100 kΩ (*iii*) 100 mA]**

2. A tuned amplifier is designed to have a resonant frequency of 1000 kHz and a bandwidth of 40 kHz. What is the *Q* of this amplifier ? **[25]**

3. The *Q* of a tuned amplifier is 25. If the resonant frequency of the circuit is 1400 kHz, what is its bandwidth? **[56 kHz]**

4. A tuned amplifier has parallel *LC* circuit. One branch of this parallel circuit has a capacitor of 100 pF and the other branch has an inductance of 1mH plus a resistance of 25 Ω. Determine (*i*) the resonant frequency and (*ii*) *Q* of the tank circuit. **[(*i*) 503.3 kHz (*ii*) 126.5]**

5. It is desired to obtain a bandwidth of 12 kHz at an operating frequency of 800 kHz, using a double-tuned circuit. What value of co-efficient of coupling should be used ? **[0.015]**

Discussion Questions

1. Why are tuned circuits not used for low frequency applications ?
2. Why is tuned amplifier operated in class *C* operation ?
3. How does coupling affect the gain of tuned amplifiers ?
4. What is the effect of *Q* on the resonance curve ?
5. What are the practical applications of tuned amplifiers ?

16

Modulation and Demodulation

16.1 Radio Broadcasting, Transmission and Reception
16.2 Modulation
16.3 Types of Modulation
16.4 Amplitude Modulation
16.5 Modulation Factor
16.6 Analysis of Amplitude Modulated Wave
16.7 Sideband Frequencies in AM Wave
16.8 Transistor AM Modulator
16.9 Power in AM Wave
16.10 Limitations of Amplitude Modulation
16.11 Frequency Modulation
16.12 Theory of Frequency Modulation
16.13 Comparison of FM and AM
16.14 Demodulation
16.15 Essentials in Demodulation
16.16 A.M. Diode Detector
16.17 A.M. Radio Receivers
16.18 Types of A. M. Radio Receivers
16.19 Stages of Superhetrodyne Radio Receiver
16.20 Advantages of Superhetrodyne Circuit
16.21 FM Receiver
16.22 Difference Between FM And AM Receivers

INTRODUCTION

In radio transmission, it is necessary to send audio signal (*e.g.* music, speech etc.) from a broadcasting station over great distances to a receiver. This communication of audio signal does not employ any wire and is sometimes called *wireless*. The audio signal cannot be sent directly over the air for appreciable distance. Even if the audio signal is converted into electrical signal, the latter cannot be sent very far without employing large amount of power. The energy of a wave is directly proportional to its frequency. At audio frequencies (20 Hz to 20 kHz), the signal power is quite small and radiation is not practicable.

The radiation of electrical energy is practicable only at high frequencies *e.g.* above 20 kHz. The high frequency signals can be sent thousands of miles even with comparatively small power. Therefore, if audio signal is to be transmitted properly, some means must be devised which will permit transmission to occur at high frequencies while it simultaneously allows the carrying of audio signal. This is achieved by superimposing electrical audio signal on high frequency carrier. The resultant waves are known *as modulated waves* or *radio waves* and the process is called *modulation.* At the radio receiver, the audio signal is extracted from the modulated wave by the process called *demodulation.* The signal is then amplified and reproduced into sound by the loudspeaker. In this chapter, we shall focus our attention on the various aspects of modulation and demodulation.

16.1 Radio Broadcasting, Transmission and Reception

Radio communication means the radiation of radio waves by the transmitting station, the propagation of these waves through space and their reception by the radio receiver. Fig. 16.1 shows the general principles of radio broadcasting, transmission and reception. As a matter of convenience, the entire arrangement can be divided into three parts *viz. transmitter, transmission of radio waves* and *radio receiver.*

1. Transmitter. Transmitter is an extremely important equipment and is housed in the broadcasting station. Its purpose is to produce radio waves for transmission into space. The important components of a transmitter are microphone, audio amplifiers, oscillator and modulator (See Fig. 16.1).

(*i*) ***Microphone.*** A microphone is a device which converts sound waves into electrical waves. When the speaker speaks or a musical instrument is played, the varying air pressure on the microphone generates an audio electrical signal which corresponds in frequency to the original signal. The output of microphone is fed to a multistage audio amplifier for raising the strength of weak signal.

(*ii*) ***Audio amplifier.*** The audio signal from the microphone is quite weak and requires amplification. This job is accomplished by cascaded audio amplifiers. The amplified output from the last audio amplifier is fed to the modulator for rendering the process of modulation.

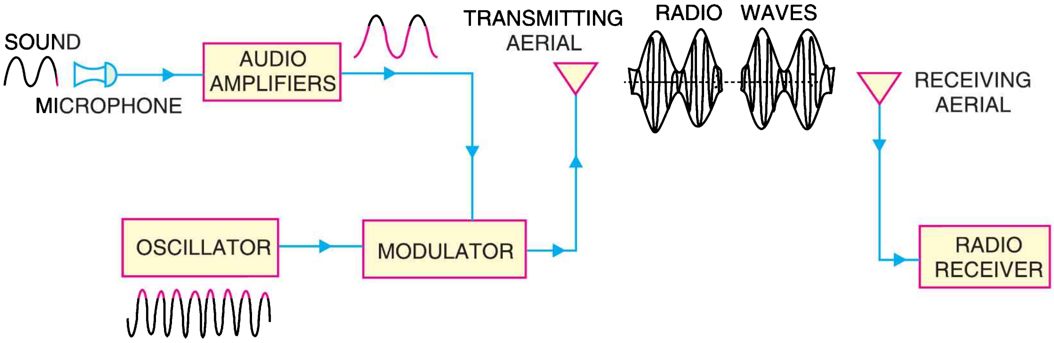


Fig. 16.1

(*iii*) ***Oscillator.*** The function of oscillator is to produce a high frequency signal, called a *carrier wave.* Usually, a crystal oscillator is used for the purpose. The power level of the carrier wave is raised to a sufficient level by radio frequency amplifier stages (not shown in Fig. 16.1). Most of the broadcasting stations have carrier wave power of several kilowatts. Such high power is necessary for transmitting the signal to the required distances.

(*iv*) ***Modulator.*** The amplified audio signal and carrier wave are fed to the modulator. Here, the audio signal is superimposed on the carrier wave in a suitable manner. The resultant waves are called *modulated waves or radio waves* and the process is called *modulation.* The process of modulation permits the transmission of audio signal at the carrier frequency. As the carrier frequency is very high, therefore, the audio signal can be transmitted to large distances. The radio waves from the transmitter are fed to the transmitting antenna or aerial from where these are radiated into space.

2. Transmission of radio waves. The transmitting antenna radiates the radio waves in space in all directions. These radio waves travel with the velocity of light *i.e.* 3×10^8 m/sec. The radio waves are electromagnetic waves and possess the same general properties. These are similar to light and heat waves except that they have longer wavelengths. It may be emphasised here that radio waves are sent without employing any wire. It can be easily shown that at high frequency, electrical energy can be radiated into space.

3. Radio receiver. On reaching the receiving antenna, the radio waves induce tiny e.m.f. in it. This small voltage is fed to the radio receiver. Here, the radio waves are first amplified and then signal is extracted from them by the process of *demodulation*. The signal is amplified by audio amplifiers and then fed to the speaker for reproduction into sound waves.

16.2 Modulation

As discussed earlier, a high frequency carrier wave is used to carry the audio signal. The question arises how the audio signal should be "added" to the carrier wave. The solution lies in changing some characteristic of carrier wave in accordance with the signal. Under such conditions, the audio signal will be contained in the resultant wave. This process is called modulation and may be defined as under :

The process of changing some characteristic (e.g. amplitude, frequency or phase) of a carrier wave in accordance with the intensity of the signal is known as **modulation**.

Modulation means to "change". In modulation, some characteristic of carrier wave is changed in accordance with the intensity (*i.e.* amplitude) of the signal. The resultant wave is called modulated wave or radio wave and contains the audio signal. Therefore, modulation permits the transmission to occur at high frequency while it simultaneously allows the carrying of the audio signal.

Need for modulation. Modulation is extremely necessary in communication system due to the following reasons :

(*i*) ***Practical antenna length.*** Theory shows that in order to transmit a wave effectively, the length of the transmitting antenna should be approximately equal to the wavelength of the wave.

$$\text{Now,} \qquad \text{wavelength} = \frac{\text{velocity}}{\text{frequency}} = \frac{3 \times 10^8}{\text{frequency (Hz)}} \text{ metres}$$

As the audio frequencies range from 20 Hz to 20 kHz, therefore, if they are transmitted directly into space, the length of the transmitting antenna required would be extremely large. For instance, to radiate a frequency of 20 kHz directly into space, we would need an antenna length of $3 \times 10^8/20 \times 10^3$ = 15,000 metres. This is too long antenna to be constructed practically. For this reason, it is impracticable to radiate audio signal directly into space. On the other hand, if a carrier wave say of 1000 kHz is used to carry the signal, we need an antenna length of 300 metres only and this size can be easily constructed.

(*ii*) ***Operating range.*** The energy of a wave depends upon its frequency. The greater the frequency of the wave, the greater the energy possessed by it. As the audio signal frequencies are small, therefore, these cannot be transmitted over large distances if radiated directly into space. The only practical solution is to modulate a high frequency carrier wave with audio signal and permit the transmission to occur at this high frequency (*i.e.* carrier frequency).

(*iii*) ***Wireless communication.*** One desirable feature of radio transmission is that it should be carried without wires *i.e.* radiated into space. At audio frequencies, radiation is not practicable because the efficiency of radiation is poor. However, efficient radiation of electrical energy is possible at high frequencies (> 20 kHz). For this reason, modulation is always done in communication systems.

16.3 Types of Modulation

As you will recall, modulation is the process of changing amplitude or frequency or phase of a carrier wave in accordance with the intensity of the signal. Accordingly, there are three basic types of modulation, namely ;

(*i*) amplitude modulation (*ii*) frequency modulation (*iii*) phase modulation

In India, amplitude modulation is used in radio broadcasting. However, in television transmission, frequency modulation is used for sound signal and amplitude modulation for picture signal. Therefore, our attention in this chapter shall be confined to the first two most important types of modulation.

16.4 Amplitude Modulation

When the amplitude of high frequency carrier wave is changed in accordance with the intensity of the signal, it is called **amplitude modulation**.

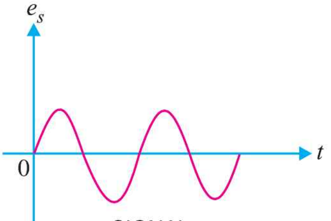
In amplitude modulation, only the amplitude of the carrier wave is changed in accordance with the intensity of the signal. However, the frequency of the modulated wave remains the same *i.e.* carrier frequency. Fig. 16.2 shows the principle of amplitude modulation. Fig. 16.2 (*i*) shows the audio electrical signal whereas Fig. 16.2 (*ii*) shows a carrier wave of constant amplitude. Fig. 16.2 (*iii*) shows the amplitude modulated (AM) wave. Note that the amplitudes of both positive and negative half-cycles of carrier wave are changed in accordance with the signal. For instance, when the signal is increasing in the positive sense, the amplitude of carrier wave also increases. On the other hand, during negative half-cycle of the signal, the amplitude of carrier wave decreases. Amplitude modulation is done by an electronic circuit called *modulator.*

The following points are worth noting in amplitude modulation :

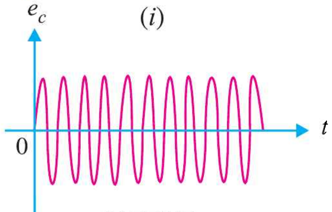
(*i*) The amplitude of the carrier wave changes according to the intensity of the signal.

(*ii*) The amplitude variations of the carrier wave is at the signal frequency f_s.

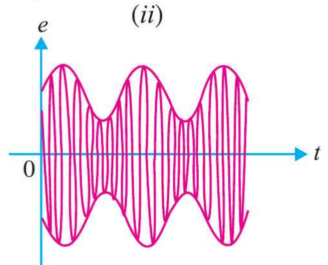
(*iii*) The frequency of the amplitude modulated wave remains the same *i.e.* carrier frequency f_c.



SIGNAL
(*i*)



CARRIER
(*ii*)



A.M. WAVE
(*iii*)

Fig. 16.2

16.5 Modulation Factor

An important consideration in amplitude modulation is to describe the depth of modulation *i.e.* the extent to which the amplitude of carrier wave is changed by the signal. This is described by a factor called modulation factor which may be defined as under :

The ratio of change of amplitude of carrier wave to the amplitude of normal carrier wave is called the **modulation factor** *m i.e.*

$$\text{Modulation factor, } m = \frac{\text{Amplitude change of carrier wave}}{\text{Normal carrier amplitude (unmodulated)}}$$

The value of modulation factor depends upon the amplitudes of carrier and signal. Fig. 16.3 shows amplitude modulation for different values of modulation factor *m*.

(*i*) When signal amplitude is zero, the carrier wave is not modulated as shown in Fig. 16.3 (*i*). The amplitude of carrier wave remains unchanged.

Amplitude change of carrier $= 0$

Amplitude of normal carrier $= A$

$\therefore$ Modulation factor, $m = 0/A = 0$ or 0%

(*ii*) When signal amplitude is equal to the carrier amplitude as shown in Fig. 16.3 (*ii*), the amplitude of carrier varies between 2A and zero.

Amplitude change of carrier $= 2A - A = A$

$$\therefore \quad \text{Modulation factor, } m = \frac{\text{Amplitude change of carrier}}{\text{Amplitude of normal carrier}} = A/A = 1 \text{ or } 100\ \%$$

In this case, the carrier is said to be 100% modulated.

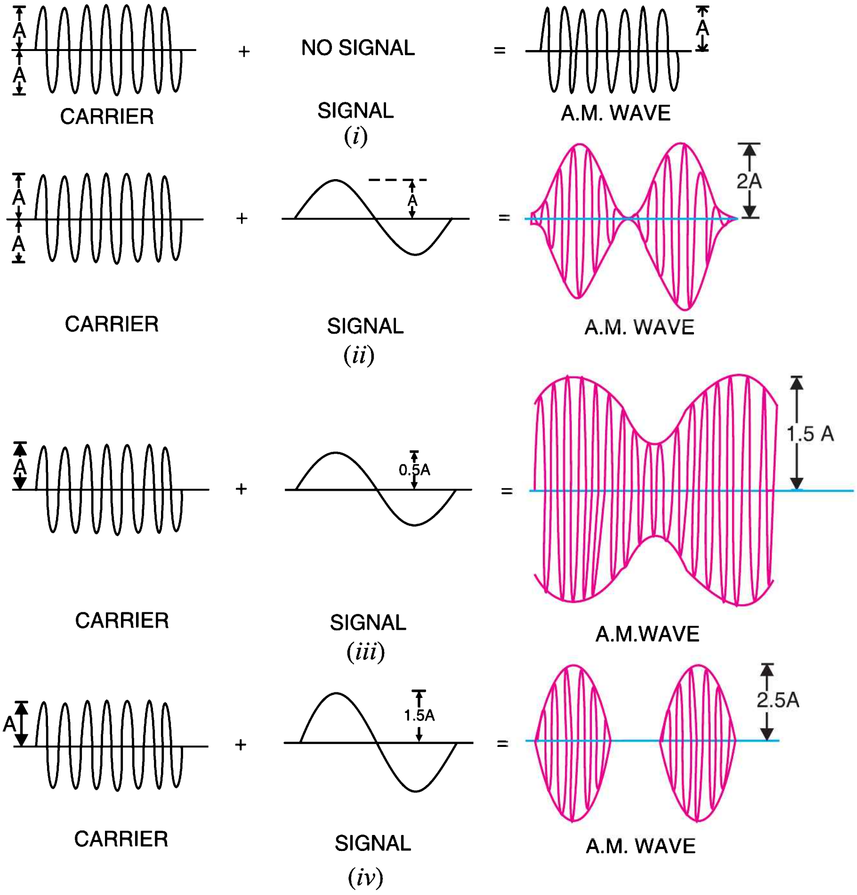

A
A
CARRIER
+
NO SIGNAL
=
A
SIGNAL
(i)
A.M. WAVE
A
A
CARRIER
+
A
SIGNAL
(ii)
=
2A
A.M. WAVE
A
CARRIER
+
0.5A
SIGNAL
(iii)
=
1.5 A
A.M.WAVE
A
CARRIER
+
1.5A
SIGNAL
(iv)
=
2.5A
A.M. WAVE

Fig. 16.3

(*iii*) When the signal amplitude is one-half the carrier amplitude as shown in Fig. 16.3 (*iii*), the amplitude of carrier wave varies between 1.5 A and 0.5 A.

Amplitude change of carrier $= 1.5\,A - A = 0.5\,A$

$\therefore$ Modulation factor, $m = 0.5\,A/A = 0.5$ or $50\ \%$

In this case, the carrier is said to be 50% modulated.

(*iv*) When the signal amplitude is 1.5 times the carrier amplitude as shown in Fig. 16.3 (*iv*), the maximum value of carrier wave becomes 2.5 *A*.

Amplitude change of carrier wave $= 2.5\,A - A = 1.5\,A$

$$\therefore \qquad \text{Modulation factor, } m = \frac{1.5\,A}{A} = 1.5 \text{ or } 150\ \%$$

In this case, the carrier is said to be 150% modulated *i.e.* over-modulated.

Importance of modulation factor. Modulation factor is very important since it determines the strength and quality of the transmitted signal. In an AM wave, the signal is contained in the variations of the carrier amplitude. When the carrier is modulated to a small degree (*i.e.* small m), the amount of carrier amplitude variation is small. Consequently, the audio signal being transmitted will not be very strong. The greater the degree of modulation (*i.e.* m), the stronger and clearer will be the audio signal. It may be emphasised here that if the carrier is overmodulated (*i.e.* $m > 1$), distortion will occur during reception. This condition is shown in Fig. 16.3 (*iv*). The AM waveform is clipped and the envelope is discontinuous. Therefore, degree of modulation should never exceed 100%.

Example 16.1. *If the maximum and minimum voltage of an AM wave are V_{max} and V_{min} respectively, then show that modulation factor m is given by :*

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

Solution. Fig. 16.4 shows the waveform of amplitude modulated wave. Let the amplitude of the normal carrier wave be E_C. Then, it is clear from Fig. 16.4 that :

$$E_C = \frac{V_{max} + V_{min}}{2}$$

If E_S is the signal amplitude, then it is clear from Fig. 16.4 that :

$$E_S = \frac{V_{max} - V_{min}}{2}$$

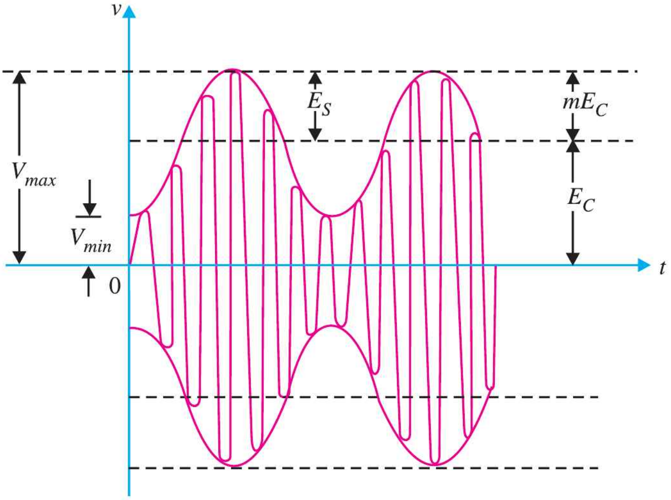


Fig. 16.4

But $$E_S = m\,E_C$$

or $$\frac{V_{max} - V_{min}}{2} = m\,\frac{V_{max} + V_{min}}{2} \quad \text{or} \quad m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

Example 16.2. *The maximum peak-to-peak voltage of an AM wave is 16 mV and the minimum peak-to-peak voltage is 4 mV. Calculate the modulation factor.*

Solution. Fig. 16.5 shows the conditions of the problem.

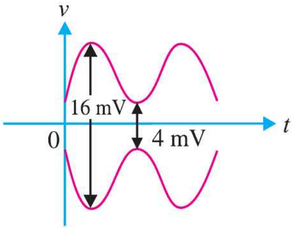


Fig. 16.5

Maximum voltage of AM wave is

$$V_{max} = \frac{16}{2} = 8 \text{ mV}$$

Minimum voltage of AM wave is

$$V_{min} = \frac{4}{2} = 2 \text{ mV}$$

$$\therefore \quad \text{Modulation factor, } m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

$$= \frac{8-2}{8+2} = \frac{6}{10} = \mathbf{0.6}$$

Example 16.3. *A carrier of 100V and 1200 kHz is modulated by a 50 V, 1000 Hz sine wave signal. Find the modulation factor.*

Solution.

$$\text{Modulation factor, } m = \frac{E_S}{E_C} = \frac{50 \text{ V}}{100 \text{ V}} = \mathbf{0.5}$$

16.6 Analysis of Amplitude Modulated Wave

A carrier wave may be represented by :

$$e_c = E_C \cos \omega_c t$$

where e_c = instantaneous voltage of carrier

E_C = amplitude of carrier

$\omega_c = 2\pi f_c$

= angular velocity at carrier frequency f_c

In amplitude modulation, the amplitude E_C of the carrier wave is varied in accordance with the intensity of the signal as shown in Fig. 16.6. Suppose the modulation factor is m. It means that signal produces a maximum change of $m\,E_C$ in the carrier amplitude. Obviously, the amplitude of signal is $m\,E_C$. Therefore, the signal can be represented by :

$$e_s = m\,E_C \cos \omega_s t$$

where e_s = instantaneous voltage of signal

$m\,E_C$ = amplitude of signal

$\omega_s = 2\pi f_s$ = angular velocity at signal frequency f_s

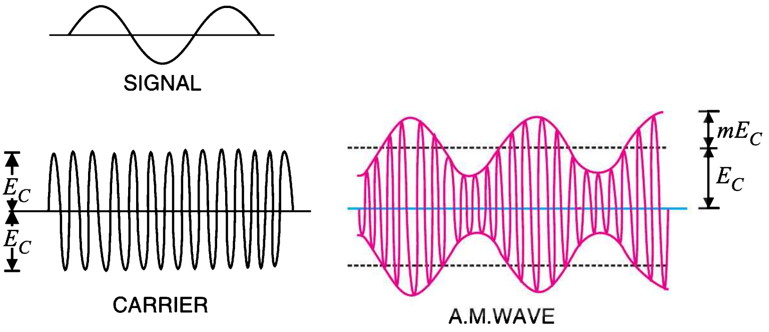


Fig. 16.6

The amplitude of the carrier wave varies at signal frequency f_s. Therefore, the amplitude of AM wave is given by :

$$\text{Amplitude of AM wave} = E_C + m\,E_C \cos \omega_s t = E_C (1 + m \cos \omega_s t)$$

The instantaneous voltage of AM wave is :

$$\begin{aligned} e &= \text{Amplitude} \times \cos \omega_c t \\ &= E_C (1 + m \cos \omega_s t) \cos \omega_c t \\ &= E_C \cos \omega_c t + m\,E_C \cos \omega_s t \cos \omega_c t \\ &= E_C \cos \omega_c t + \frac{mE_C}{2} (2 \cos \omega_s t \cos \omega_c t) \\ &= E_C \cos \omega_c t + \frac{mE_C}{2} [\cos (\omega_c + \omega_s) t + \cos (\omega_c - \omega_s) t]^* \\ &= E_C \cos \omega_c t + \frac{mE_C}{2} \cos (\omega_c + \omega_s) t + \frac{mE_C}{2} \cos (\omega_c - \omega_s) t \end{aligned}$$

The following points may be noted from the above equation of amplitude modulated wave:

(*i*) The AM wave is equivalent to the summation of three sinusoidal waves; one having amplitude E_C and frequency **f_c, the second having amplitude $mE_C/2$ and frequency $(f_c + f_s)$ and the third having amplitude $mE_C/2$ and frequency $f_c - f_s$.

(*ii*) The AM wave contains three frequencies *viz* $f_c, f_c + f_s$ and $f_c - f_s$. The first frequency is the carrier frequency. Thus, the process of modulation does not change the original carrier frequency but produces two new frequencies $(f_c + f_s)$ and $(f_c - f_s)$ which are called sideband frequencies.

(*iii*) The sum of carrier frequency and signal frequency *i.e.* $(f_c + f_s)$ is called *upper sideband frequency*. The *lower sideband frequency* is $f_c - f_s$ *i.e.* the difference between carrier and signal frequencies.

16.7 Sideband Frequencies in AM Wave

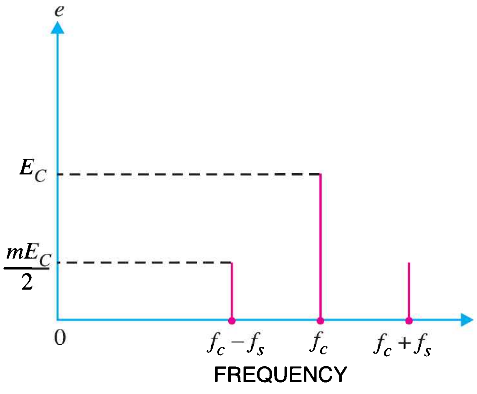


Fig. 16.7

In an amplitude modulated wave, the sideband frequencies are of our interest. It is because the signal frequency f_s is contained in the sideband frequencies. Fig. 16.7 shows the frequency spectrum of an amplitude modulated wave. The frequency components in the AM wave are shown by vertical lines. The height of each vertical line is equal to the amplitude of the components present. It may be added here that in practical radio transmission, carrier frequency f_c is many times greater than signal frequency f_s. Hence, the sideband frequencies are generally close to the carrier frequency. It may be seen that a carrier modulated by a single frequency is equivalent to three simultaneous signals; the car-

---

* From trigonometry, we have the expansion formula :

$$2 \cos A \cos B = \cos (A + B) + \cos (A - B)$$

** $f_c = \frac{\omega_c}{2\pi}$, $f_c + f_s = \frac{\omega_c + \omega_s}{2\pi}$, $f_c - f_s = \frac{\omega_c - \omega_s}{2\pi}$

rier itself and two other steady frequencies *i.e.* $f_c + f_s$ and $f_c - f_s$.

Let us illustrate sideband frequencies with an example. Suppose the carrier frequency is 400 kHz and the signal frequency is 1 kHz. The AM wave will contain three frequencies *viz* 400 kHz, 401 kHz and 399 kHz. It is clear that upper sideband frequency (401 kHz) and lower sideband frequency (399 kHz) are very close to the carrier frequency (400 kHz).

Bandwidth. In an AM wave, the bandwidth is from $(f_c - f_s)$ to $(f_c + f_s)$ *i.e.*, $2f_s$. Thus in the above example, bandwidth is from 399 to 401 kHz or 2 kHz which is twice the signal frequency. Therefore, we arrive at a very important conclusion that *in amplitude modulation, bandwidth is twice the signal frequency.* The tuned amplifier which is called upon to amplify the modulated wave must have the required bandwidth to include the sideband frequencies. If the tuned amplifier has insufficient bandwidth, the upper sideband frequencies may not be reproduced by the radio receiver.

Example 16.4. *A 2500 kHz carrier is modulated by audio signal with frequency span of 50 – 15000 Hz. What are the frequencies of lower and upper sidebands ? What bandwidth of RF amplifier is required to handle the output ?*

Solution. The modulating signal (*e.g.* music) has a range of 0.05 to 15 kHz. The sideband frequencies produced range from f_c ± 0.05 kHz to f_c ± 15 kHz. Therefore, upper sideband ranges from 2500.05 to 2515 kHz and lower sideband ranges from 2499.95 to 2485 kHz.

The sideband frequencies produced can be approximately expressed as 2500 ± 15 kHz. Therefore, bandwidth requirement = 2515 – 2485 = 30 kHz. Note that bandwidth of *RF* amplifier required is twice the frequency of highest modulating signal frequency.

16.8 Transistor AM *Modulator

Fig. 16.8 shows the circuit of a simple AM modulator. It is essentially a *CE* amplifier having a voltage gain of A. The carrier signal is the input to the amplifier. The modulating signal is applied in the emitter resistance circuit.

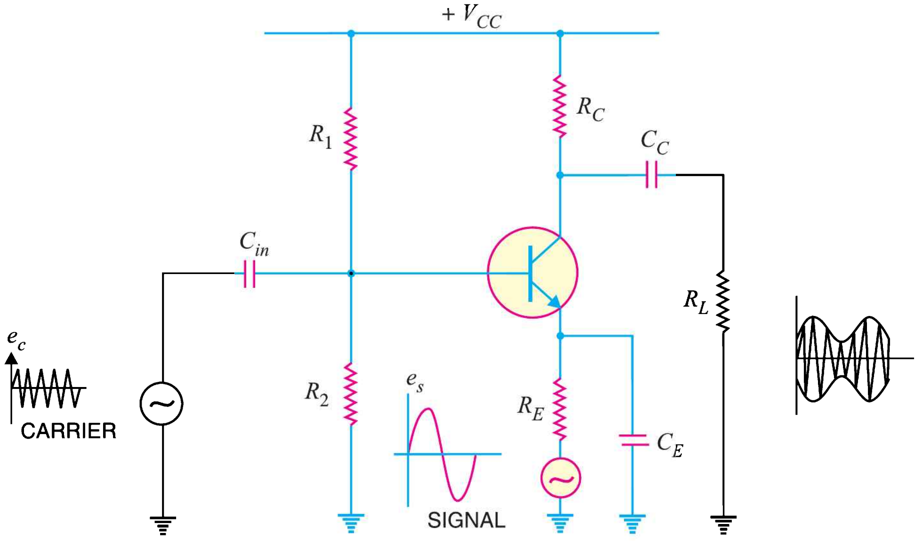


Fig. 16.8

---

* A circuit which does amplitude modulation is called AM modulator.

Working. The carrier e_c is applied at the input of the amplifier and the modulating signal e_s is applied in the emitter resistance circuit. The amplifier circuit amplifies the carrier by a factor "*A*" so that the output is Ae_c. Since the modulating signal is a part of the biasing circuit, it produces low-frequency variations in the emitter circuit. This in turn causes *variations in "*A*". The result is that amplitude of the carrier varies in accordance with the strength of the signal. Consequently, amplitude modulated output is obtained across R_L. It may be noted that carrier should not influence the voltage gain A; only the modulating signal should do this. To achieve this objective, carrier should have a small magnitude and signal should have a large magnitude.

Example 16.5. *An AM wave is represented by the expression :*

$$v = 5\,(1 + 0.6 \cos 6280\, t) \sin 211 \times 10^4\, t \text{ volts}$$

(*i*) *What are the minimum and maximum amplitudes of the AM wave ?*

(*ii*) *What frequency components are contained in the modulated wave and what is the amplitude of each component?*

Solution.

The AM wave equation is given by : $v = 5\,(1 + 0.6 \cos 6280\, t) \sin 211 \times 10^4\, t$ volts ...(*i*)

Compare it with standard AM wave eq., $v = E_C\,(1 + m \cos \omega_s t) \sin \omega_c t$ ...(*ii*)

From eqs. (*i*) and (*ii*), we get,

$$\begin{aligned} E_C &= \text{carrier amplitude} = 5 \text{ V} \\ m &= \text{modulation factor} = 0.6 \\ f_s &= \text{signal frequency} = \omega_s/2\pi = 6280/2\pi = 1 \text{ kHz} \\ f_c &= \text{carrier frequency} = \omega_c/2\pi = 211 \times 10^4/2\pi = 336 \text{ kHz} \end{aligned}$$

(*i*) Minimum amplitude of AM wave $= E_C - mE_C = 5 - 0.6 \times 5 = \mathbf{2\ V}$

Maximum amplitude of AM wave $= E_C + mE_C = 5 + 0.6 \times 5 = \mathbf{8\ V}$

(*ii*) The AM wave will contain three frequencies *viz.*

$$\begin{array}{llll} & f_c - f_s, & f_c, & f_c + f_s \\ \text{or} & 336 - 1, & 336, & 336 + 1 \\ \text{or} & \mathbf{335\ kHz,} & \mathbf{336\ kHz,} & \mathbf{337\ kHz} \end{array}$$

The amplitudes of the three components of AM wave are :

$$\begin{array}{llll} & \dfrac{mE_C}{2}, & E_C, & \dfrac{mE_C}{2} \\ \text{or} & \dfrac{0.6 \times 5}{2}, & 5, & \dfrac{0.6 \times 5}{2} \\ \text{or} & \mathbf{1.5\ V,} & \mathbf{5\ V,} & \mathbf{1.5\ V} \end{array}$$

Example 16.6. *A sinusoidal carrier voltage of frequency 1 MHz and amplitude 100 volts is amplitude modulated by sinusoidal voltage of frequency 5 kHz producing 50% modulation. Calculate the frequency and amplitude of lower and upper sideband terms.*

Solution.

$$\begin{aligned} \text{Frequency of carrier, } f_c &= 1 \text{ MHz} = 1000 \text{ kHz} \\ \text{Frequency of signal, } f_s &= 5 \text{ kHz} \\ \text{Modulation factor, } m &= 50\% = 0.5 \end{aligned}$$

---

* The principle of this circuit is to change the gain A (and hence the amplitude of carrier) by the modulating signal.

Amplitude of carrier, $E_C = 100$ V

The lower and upper sideband frequencies are :

$f_c - f_s$ and $f_c + f_s$

or (1000 – 5) kHz and (1000 + 5) kHz

or **995 kHz** and **1005 kHz**

$$\text{Amplitude of each sideband term} = \frac{mE_C}{2} = \frac{0.5 \times 100}{2} = \mathbf{25\ V}$$

Example 16.7. *A carrier wave of frequency 10 MHz and peak value 10V is amplitude modulated by a 5- kHz sine wave of amplitude 6V. Determine (i) modulation factor (ii) sideband frequencies and (iii) amplitude of sideband components. Draw the frequency spectrum.*

Solution.

Carrier amplitude, E_C = 10V

Signal amplitude, E_S = 6V

Carrier frequency, f_c = 10 MHz

Signal frequency, f_s = 5 kHz = 0.005 MHz

(*i*) $$\text{Modulation factor, } m = \frac{E_S}{E_C} = \frac{6}{10} = \mathbf{0.6}$$

(*ii*) Sideband frequencies are :

$f_c - f_s$; $f_c + f_s$

10 – 0.005 ; 10 + 0.005

9.995 MHz ; 10.005 MHz

(*iii*) $$\text{Amplitude of each sideband} = \frac{m\,E_C}{2} = \frac{0.6 \times 10}{2} = \mathbf{3V}$$

Fig. 16.9 shows the frequency spectrum of the A.M. wave.

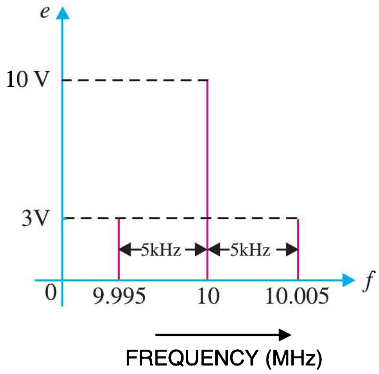


Fig. 16.9

16.9 Power in AM Wave

The power dissipated in any circuit is a function of the square of voltage across the circuit and the effective resistance of the circuit. Equation of AM wave reveals that it has three components of amplitude E_C, $m\,E_C/2$ and $m\,E_C/2$. Clearly, power output must be distributed among these components.

$$\text{Carrier power, } P_C = \frac{^*\left(E_C/\sqrt{2}\right)^2}{R} = \frac{E_C^2}{2R} \qquad \text{...}(i)$$

$$\text{Total power of sidebands, } P_S = \frac{\left(m\,E_C/2\sqrt{2}\right)^2}{R} + \frac{\left(m\,E_C/2\sqrt{2}\right)^2}{R}$$

$$= \frac{m^2 E_C^2}{8R} + \frac{m^2 E_C^2}{8R} = \frac{m^2 E_C^2}{4R} \qquad \text{...}(ii)$$

$$\text{Total power of AM wave, } P_T = P_C + P_S$$

---

* r.m.s. values are considered.

$$= \frac{E_C^2}{2R} + \frac{m^2 E_C^2}{4R} = \frac{E_C^2}{2R}\left[1 + \frac{m^2}{2}\right]$$

or $$P_T = \frac{E_C^2}{2R}\frac{\left[2 + m^2\right]}{2} \qquad ...(iii)$$

Fraction of total power carried by sidebands is

$$\frac{P_S}{P_T} = \frac{\text{Exp. }(ii)}{\text{Exp. }(iii)} = \frac{m^2}{2 + m^2} \qquad ....(iv)$$

As the signal is contained in the sideband frequencies, therefore, useful power is in the sidebands. Inspection of exp. (*iv*) reveals that sideband power depends upon the modulation factor *m*. The greater the value of *m*, the greater is the useful power carried by the sidebands. This emphasises the importance of modulation factor.

(*i*) When $m = 0$, power carried by sidebands $= 0^2/2 + 0^2 = 0$

(*ii*) When $m = 0.5$, power carried by sidebands

$$= \frac{(0.5)^2}{2 + (0.5)^2} = 11.1\ \%\text{ of total power of AM wave}$$

(*iii*) When $m = 1$, power carried by sidebands

$$= \frac{(1)^2}{2 + (1)^2} = 33.3\%\text{ of total power of AM wave}$$

As an example, suppose the total power of an AM wave is 600 watts and modulation is 100%. Then sideband power is 600/3 = 200 watts and carrier power will be 600 – 200 = 400 watts.

The sideband power represents the signal content and the carrier power is that power which is required as the means of transmission.

Note. $$P_C = \frac{E_C^2}{2R} \text{ and } P_S = \frac{m^2 E_C^2}{4R}$$

∴ $$\frac{P_S}{P_C} = \frac{1}{2}m^2$$

or $$P_S = \frac{1}{2}m^2 P_C \qquad ...(v)$$

Expression (*v*) gives the relation between total sideband power (P_S) and carrier power (P_C).

16.10 Limitations of Amplitude Modulation

Although theoretically highly effective, amplitude modulation suffers from the following drawbacks:

(*i*) ***Noisy reception.*** In an AM wave, the signal is in the amplitude variations of the carrier. Practically all the natural and man made noises consist of electrical amplitude disturbances. As a radio receiver cannot distinguish between amplitude variations that represent noise and those that contain the desired signal, therefore, reception is generally noisy.

(*ii*) ***Low efficiency.*** In amplitude modulation, useful power is in the sidebands as they contain the signal. As discussed before, an AM wave has low sideband power. For example, if modulation is 100%, the sideband power is only one-third of the total power of AM wave. Hence the efficiency of this type of modulation is low.

(*iii*) ***Small operating range.*** Due to low efficiency of amplitude modulation, transmitters employing this method have a small operating range *i.e.* messages cannot be transmitted over larger distances.

(*iv*) ***Lack of audio quality.*** This is a distinct disadvantage of amplitude modulation. In order to attain high-fidelity reception, all audio frequencies up to 15 kHz must be reproduced. This necessitates bandwidth of 30 kHz since both sidebands must be reproduced. But AM broadcasting stations are assigned bandwidth of only 10 kHz to minimise the interference from adjacent broadcasting stations. This means that the highest modulating frequency can be 5 kHz which is hardly sufficient to reproduce the music properly.

Example 16.8. *A carrier wave of 500 watts is subjected to 100% amplitude modulation. Determine :*

(*i*) *power in sidebands* (*ii*) *power of modulated wave.*

Solution.

(*i*) Sideband power, $P_S = \frac{1}{2}m^2P_C = \frac{1}{2} \times 500 = \mathbf{250\ W}$

Thus there are 125 W in upper sideband and 125 W in lower sideband.

(*ii*) Power of AM wave, $P_T = P_C + P_S = 500 + 250 = \mathbf{750\ W}$

Example 16.9. *A 50 kW carrier is to be modulated to a level of* (*i*) *80%* (*ii*) *10%. What is the total sideband power in each case ?*

Solution. (*i*) $P_S = \frac{1}{2}m^2P_C = \frac{1}{2}(0.8)^2 \times 50 = \mathbf{16\ kW}$

(*ii*) $P_S = \frac{1}{2}m^2P_C = \frac{1}{2}(0.1)^2 \times 50 = \mathbf{0.25\ kW}$

Note the effect of modulation factor on the magnitude of sideband power. In the first case ($m = 80\%$), we generated and transmitted 50 kW carrier in order to send 16 kW of intelligence. In the second case ($m = 10\%$), the same carrier level — 50 kW — is used to send merely 250 W of intelligence. Clearly, the efficiency of operation decreases rapidly as modulation factor decreases. For this reason, in amplitude modulation, the value of m is kept as close to unity as possible.

Example 16.10. *A 40kW carrier is to be modulated to a level of 100%.*

(*i*) *What is the carrier power after modulation ?*

(*ii*) *How much audio power is required if the efficiency of the modulated RF amplifier is 72% ?*

Solution. Fig. 16.10 shows the block diagram indicating the power relations.

(*i*) Since the carrier itself is unaffected by the modulating signal, there is no change in the carrier power level.

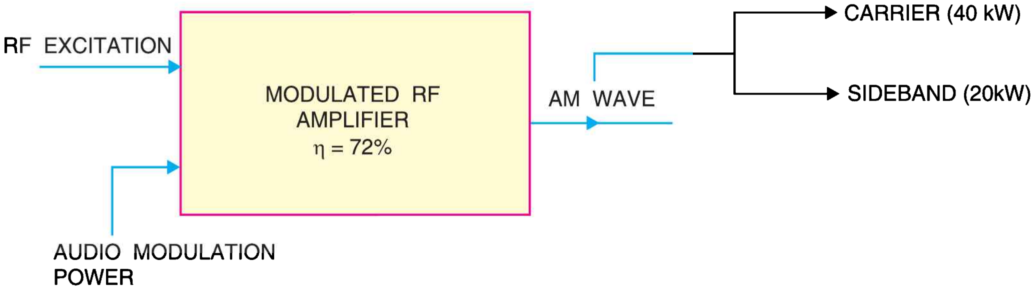


Fig. 16.10

$$\therefore \quad P_C = \mathbf{40\ kW}$$

(*ii*) $$P_S = \frac{1}{2}m^2 P_C = \frac{1}{2}(1)^2 \times 40 = 20\text{ kW}$$

$$\therefore \quad P_{audio} = \frac{P_S}{0.72} = \frac{20}{0.72} = \mathbf{27.8\ kW}$$

Example 16.11. *An audio signal of 1 kHz is used to modulate a carrier of 500 kHz. Determine (i) sideband frequencies (ii) bandwidth required.*

Solution. Carrier frequency, f_c = 500 kHz

Signal frequency, f_s = 1 kHz

(*i*) As discussed in Art. 16.6, the *AM* wave has sideband frequencies of $(f_c + f_s)$ and $(f_c - f_s)$.

∴ Sideband frequencies = (500 + 1) kHz and (500 − 1) kHz

= **501 kHz** and **499 kHz**

(*ii*) Bandwidth required = 499 kHz to 501 kHz = **2 kHz**

Example 16.12. *The load current in the transmitting antenna of an unmodulated AM transmitter is 8A. What will be the antenna current when modulation is 40% ?*

Solution.

$$P_S = \frac{1}{2}m^2 P_C$$

$$P_T = P_C + P_S = P_C\left(1 + \frac{m^2}{2}\right)$$

$$\therefore \quad \frac{P_T}{P_C} = 1 + \frac{m^2}{2}$$

or $$\left(\frac{I_T}{I_C}\right)^2 = 1 + \frac{m^2}{2}$$

Given that $I_C = 8\text{A};\ m = 0.4$

$$\therefore \quad \left(\frac{I_T}{8}\right)^2 = 1 + \frac{(0.4)^2}{2}$$

or $$(I_T/8)^2 = 1.08$$

or $$I_T = 8\sqrt{1.08} = \mathbf{8.31\ A}$$

Example 16.13. *The antenna current of an AM transmitter is 8A when only carrier is sent but it increases to 8.93A when the carrier is sinusoidally modulated. Find the % age modulation.*

Solution. As shown in example 16.12,

$$\left(\frac{I_T}{I_C}\right)^2 = 1 + \frac{m^2}{2}$$

Given that $I_T = 8.93\text{ A};\ I_C = 8\text{ A};\ m = ?$

$$\therefore \quad \left(\frac{8.93}{8}\right)^2 = 1 + \frac{m^2}{2}$$

or $$1.246 = 1 + m^2/2$$

or $$m^2/2 = 0.246$$

or $$m = \sqrt{2 \times 0.246} = 0.701 = \mathbf{70.1\%}$$

Example 16.14. *The r.m.s. value of carrier voltage is 100 V. After amplitude modulation by a sinusoidal a.f. voltage, the r.m.s. value becomes 110 V. Calculate the modulation index.*

Solution.

$$\frac{P_T}{P_C} = 1 + \frac{m^2}{2}$$

or

$$\left(\frac{V_T}{V_C}\right)^2 = 1 + \frac{m^2}{2}$$

Given that $V_T = 110\text{ V}$; $V_C = 100\text{ V}$; $m = ?$

$\therefore$

$$\left(\frac{110}{100}\right)^2 = 1 + \frac{m^2}{2}$$

or

$$1.21 = 1 + \frac{m^2}{2}$$

or

$$m^2/2 = 0.21$$

or

$$m = \sqrt{0.21 \times 2} = \mathbf{0.648}$$

Example 16.15. *An AM wave consists of the following components :*

Carrier component = 5 V peak value
Lower sideband component = 2.5 V peak value
Upper sideband component = 2.5 V peak value

If the AM wave drives a 2 kΩ resistor, find the power delivered to the resistor by (i) carrier (ii) lower sideband component and (iii) upper sideband component. What is the total power delivered?

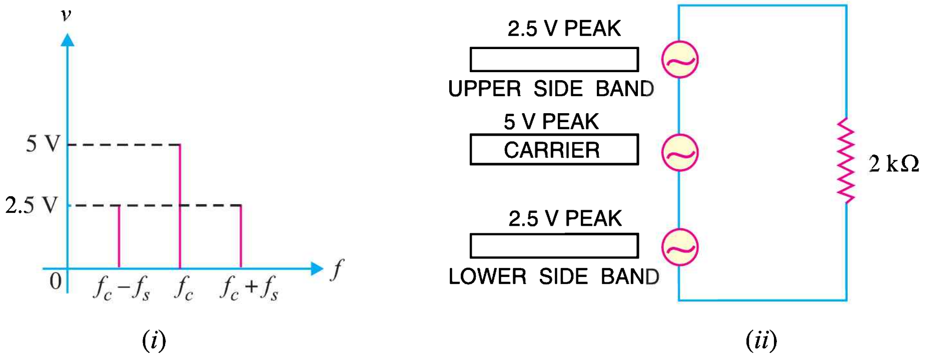
Solution. Fig. 16.11 (*i*) shows the frequency spectrum of AM wave whereas Fig. 16.11 (*ii*) shows the equivalent circuit.

$$\text{Power} = \frac{(\text{r.m.s. voltage})^2}{R} = \frac{(0.707 \times \text{peak value})^2}{R}$$

(*i*) Power delivered by the carrier, $P_C = \dfrac{(0.707 \times 5)^2}{2000} = \mathbf{6.25\ mW}$

(*ii*) Power delivered by lower sideband component is

$$P_{lower} = \frac{(0.707 \times 2.5)^2}{2000} = \mathbf{1.562\ mW}$$



(*i*) (*ii*)

Fig. 16.11

(*iii*) Power delivered by upper sideband component is

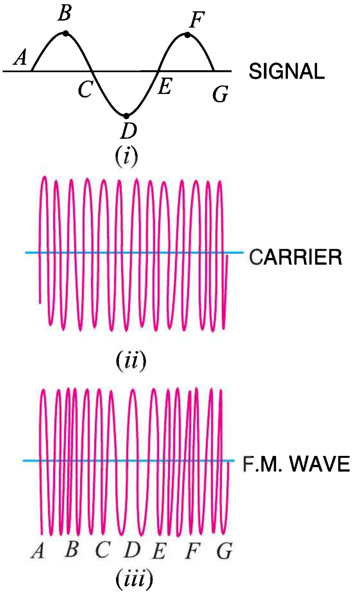
$$P_{upper} = \frac{(0.707 \times 2.5)^2}{2000} = \mathbf{1.562\ mW}$$

Total power delivered by the *AM* wave = 6.25 + 1.562 + 1.562 = **9.374 mW**

16.11 Frequency Modulation (FM)

When the frequency of carrier wave is changed in accordance with the intensity of the signal, it is called **frequency modulation (FM)**.

In frequency modulation, only the frequency of the carrier wave is changed in accordance with the signal. However, the amplitude of the modulated wave remains the same *i.e.* carrier wave amplitude. The frequency variations of carrier wave depend upon the instantaneous amplitude of the signal as shown in Fig. 16.12 (*iii*). When the signal voltage is zero as at *A*, *C*, *E* and *G*, the carrier frequency is unchanged. When the signal approaches its positive peaks as at *B* and *F*, the carrier frequency is increased to maximum as shown by the closely spaced cycles. However, during the negative peaks of signal as at *D*, the carrier frequency is reduced to minimum as shown by the widely spaced cycles.



(*i*)

(*ii*)

(*iii*)

Fig. 16.12

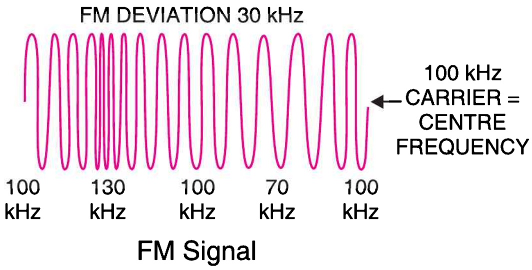


Fig. 16.13

Illustration. The process of frequency modulation (FM) can be made more illustrative if we consider numerical values. Fig. 16.13 shows the FM signal having carrier frequency f_c = 100 kHz. Note that FM signal has constant amplitude but varying frequencies above and below the carrier frequency of 100 kHz (=f_c). For this reason, f_c (= 100 kHz) is called *centre frequency*. The changes in the carrier frequency are produced by the audio-modulating signal. The amount of change in frequency from f_c (= 100 kHz) or *frequency deviation* depends upon the amplitude of the audio-modulating signal. The frequency deviation increases with the increase in the modulating signal and vice-versa. Thus the peak audio voltage will produce maximum frequency deviation. Referring to Fig. 16.13, the centre frequency is 100 kHz and the maximum frequency deviation is 30 kHz. The following points about frequency modulation (FM) may be noted carefully :

(*a*) The frequency deviation of FM signal depends on the amplitude of the modulating signal.

(*b*) The centre frequency is the frequency without modulation or when the modulating voltage is zero.

(*c*) The audio frequency (*i.e.* frequency of modulating signal) does not determine frequency deviation.

Advantages **:** The following are the advantages of FM over AM :

(*i*) It gives noiseless reception. As discussed before, noise is a form of amplitude variations and a FM receiver will reject such signals.

(*ii*) The operating range is quite large.

(*iii*) It gives high-fidelity reception.

(*iv*) The efficiency of transmission is very high.

16.12 Theory of Frequency Modulation (FM)

In frequency modulation (FM), the amplitude of the carrier is kept constant but the frequency f_c of the carrier is varied by the modulating signal. The carrier frequency f_c varies at the rate of the [*]signal frequency f_s ; the frequency deviation being proportional to the instantaneous amplitude of the modulating signal. Note that maximum frequency deviation is $(f_{c\,(max)} - f_c)$ and occurs at the peak voltage of the modulating signal. Suppose we modulate a 100 MHz carrier by 1V, 1 kHz modulating signal and the maximum frequency deviation is 25 kHz. This means that the carrier frequency will vary sinusoidally between (100 + 0.025) MHz and (100 – 0.025) MHz at the rate of 1000 times per second. If the amplitude of the modulating signal is increased to 2V, then the maximum frequency deviation will be 50 kHz and the carrier frequency will vary between (100 + 0.05) MHz and (100 – 0.05) MHz at the rate of 1000 times per second.

Suppose a modulating sine-wave signal e_s $(= E_s \cos \omega_s t)$ is used to vary the carrier frequency f_c. Let the change in carrier frequency be ke_s where k is a constant known as the *frequency deviation constant.* The instantaneous carrier frequency f_i is given by ;

$$\begin{aligned} f_i &= f_c + k\,e_s \\ &= f_c + k\,E_s \cos \omega_s t \end{aligned}$$

A graph of f_i versus time is shown in Fig. 16.14. It is important to note that it is frequency-time curve and not amplitude-time curve. The factor $k\,E_s$ represents the maximum frequency deviation and is denoted by Δf *i.e.*

Max. frequency deviation, $\Delta f = {}^{**}\,k\,E_s$

$\therefore \qquad f_i = f_c + \Delta f \cos \omega_s t$

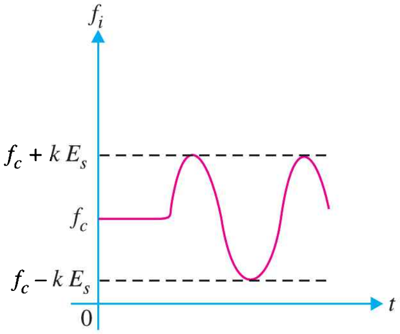


Fig. 16.14

Equation of FM wave. In frequency modulation, the carrier frequency is varied sinusoidally at signal frequency. The instantaneous deviation in frequency from the carrier is proportional to the instantaneous amplitude of the modulating signal. Thus the instantaneous angular frequency of FM is given by ;

$$\omega_i = \omega_c + \Delta\omega_c \cos \omega_s t$$

Total phase angle $\theta = \omega t$ so that if ω is variable, then,

$$\begin{aligned} \theta &= \int_0^t \omega_i \, dt \\ &= \int_0^t (\omega_c + \Delta\omega_c \cos \omega_s t)\, dt \end{aligned}$$

---

[*] Note this point. It means that modulating frequency is the rate of frequency of deviations in the *RF* carrier. For example, all signals having the same amplitude will deviate the carrier frequency by the same amount, say 50 kHz, no matter what their frequencies. On similar lines, all signals of the same frequency, say, 3 kHz, will deviate the carrier at the same rate of 3000 times per second, no matter what their individual amplitudes.

[**] Note that k is in kHz or MHz per volt.

$$\therefore \qquad \theta = \omega_c t + \frac{\Delta\omega_c}{\omega_s} \sin \omega_s t$$

The term $\frac{\Delta\omega_c}{\omega_s}$ is called *modulation index* m_f.

$$\therefore \qquad \theta = \omega_c t + m_f \sin \omega_s t$$

The instantaneous value of FM voltage wave is given by ;

$$e = E_c \cos \theta$$

or
$$e = E_c \cos(\omega_c t + m_f \sin \omega_s t) \qquad ...(i)$$

Exp. (*i*) is the general voltage equation of a FM wave. The following points may be noted carefully :

(*i*) The modulation index m_f is the ratio of maximum frequency deviation (Δf) to the frequency ($= f_s$) of the modulating signal *i.e.*

$$\text{Modulation index, } m_f = \frac{\Delta\omega_c}{\omega_s} = \frac{f_{c\,(max)} - f_c}{f_s} = \frac{\Delta f}{f_s}$$

(*ii*) Unlike amplitude modulation, the modulation index (m_f) for frequency modulation can be greater than unity.

Frequency Spectrum. It requires advanced mathematics to derive the spectrum of FM wave. We will give only the results without derivation. If f_c and f_s are the carrier and signal frequencies respectively, then FM spectrum will have the following frequencies :

f_c ; $f_c \pm f_s$; $f_c \pm 2f_s$; $f_c \pm 3f_s$ and so on.

Note that $f_c + f_s$, $f_c + 2f_s$, $f_c + 3f_s$ ...... are the upper sideband frequencies while $f_c - f_s$, $f_c - 2f_s$, $f_c - 3f_s$ ...... are the lower sideband frequencies.

Example 16.16. *A frequency modulated voltage wave is given by the equation :*

$$e = 12 \cos(6 \times 10^8 t + 5 \sin 1250\, t)$$

Find (i) carrier frequency (ii) signal frequency (iii) modulation index (iv) maximum frequency deviation (v) power dissipated by the FM wave in 10-ohm resistor.

Solution. The given FM voltage wave is

$$e = 12 \cos(6 \times 10^8 t + 5 \sin 1250\, t) \qquad ...(i)$$

The equation of standard FM voltage wave is

$$e = E_c \cos(\omega_c t + m_f \sin \omega_s t) \qquad ...(ii)$$

Comparing eqs. (*i*) and (*ii*), we have,

(*i*) Carrier frequency, $f_c = \frac{\omega_c}{2\pi} = \frac{6 \times 10^8}{2\pi} = \mathbf{95.5 \times 10^6\ Hz}$

(*ii*) Signal frequency, $f_s = \frac{\omega_s}{2\pi} = \frac{1250}{2\pi} = \mathbf{199\ Hz}$

(*iii*) Modulation index, $m_f = \mathbf{5}$

(*iv*) Max. frequency deviation, $\Delta f = m_f \times f_s = 5 \times 199 = \mathbf{995\ Hz}$

(*v*) Power dissipated, $P = \frac{E_{r.m.s.}^2}{R} = \frac{(12/\sqrt{2})^2}{10} = \mathbf{7.2W}$

Example 16.17. *A 25 MHz carrier is modulated by a 400 Hz audio sine wave. If the carrier voltage is 4V and the maximum frequency deviation is 10 kHz, write down the voltage equation of the FM wave.*

Solution. The voltage equation of the FM wave is

$$e = E_c \cos(\omega_c t + m_f \sin \omega_s t)$$

Here $\omega_c = 2\pi f_c = 2\pi \times 25 \times 10^6 = 1.57 \times 10^8$ rad/s

$\omega_s = 2\pi f_s = 2\pi \times 400 = 2513$ rad/s

$$m_f = \frac{\Delta f}{f_s} = \frac{10 \text{ kHz}}{400 \text{ Hz}} = \frac{10 \times 10^3 \text{ Hz}}{400\text{Hz}} = 25$$

$\therefore$ $e = 4 \cos (1.57 \times 10^8 t + 25 \sin 2513t)$ **Ans.**

Example 16.18. *Calculate the modulation index for an FM wave where the maximum frequency deviation is 50 kHz and the modulating frequency is 5 kHz.*

Solution.

Max. frequency deviation, Δf = 50 kHz

Modulating frequency, f_s = 5 kHz

$\therefore$ Modulation index, $m_f = \dfrac{\Delta f}{f_s} = \dfrac{50 \text{ kHz}}{5 \text{ kHz}} = \mathbf{10}$

Example 16.19. *The carrier frequency in an FM modulator is 1000 kHz. If the modulating frequency is 15 kHz, what are the first three upper sideband and lower sideband frequencies?*

Solution.

Carrier frequency, f_c = 1000 kHz

Modulating frequency, f_s = 15 kHz

Upper sideband frequencies

$f_c + f_s$; $f_c + 2f_s$; $f_c + 3f_s$

1000 + 15 ; 1000 + 2 × 15 ; 1000 + 3 × 15

1015 kHz ; **1030 kHz** ; **1045 kHz**

Lower sideband frequencies

$f_c - f_s$; $f_c - 2f_s$; $f_c - 3f_s$

1000 – 15 ; 1000 – 2 × 15 ; 1000 – 3 × 15

985 kHz ; **970 kHz** ; **955 kHz**

Example 16.20. *The carrier and modulating frequencies of an FM transmitter are 100 MHz and 15 kHz respectively. If the maximum frequency deviation is 75 kHz, find the bandwidth of FM signal.*

Solution. To calculate the exact bandwidth of an FM signal, it requires the use of advanced mathematics (Bessel functions) which is beyond the level of this book. However, the bandwidth of an FM signal is approximately given by ;

Bandwidth, $BW = 2 [\Delta f + f_s] = 2 [75 + 15] = \mathbf{180 \text{ kHz}}$

Example 16.21. *In a frequency modulated wave, frequency deviation constant is 75 kHz/volt and the signal amplitude is 2V. Find the maximum frequency deviation.*

Solution.

Frequency deviation constant, k = 75 kHz/V

Amplitude of signal, E_s = 2V

$\therefore$ Max. frequency deviation, $\Delta f = k E_s = 75 \times 2 = \mathbf{150 \text{ kHz}}$

Example 16.22. *In an FM system, when the audio frequency (AF) is 500 Hz and the AF voltage is 2.4V, the frequency deviation is 4.8 kHz. If the AF voltage is now increased to 7.2V, what is the new frequency deviation? If the AF voltage is raised to 10V while the AF is dropped to 200 Hz, what is the deviation? Find the modulation index in each case.*

Solution.

We know that :

$$\text{Frequency deviation, } \Delta f_1 = k\,E_s$$

$$\therefore \quad \text{Frequency deviation constant, } k = \frac{\Delta f_1}{E_s} = \frac{4.8}{2.4} = 2 \text{ kHz/V}$$

For $E_s = 7.2\text{V}$, $\Delta f_2 = 2 \times 7.2 =$ **14.4 kHz**

For $E_s = 10\text{V}$, $\Delta f_3 = 2 \times 10 =$ **20 kHz**

The answer of **20 kHz** shows that deviation is independent of modulating frequency.

The modulation indices in the three cases are :

$$m_{f1} = \frac{\Delta f_1}{f_{s1}} = \frac{4.8}{0.5} = \mathbf{9.6}$$

$$m_{f2} = \frac{\Delta f_2}{f_{s1}} = \frac{14.4}{0.5} = \mathbf{28.8}$$

$$m_{f3} = \frac{\Delta f_3}{f_{s2}} = \frac{20}{0.2} = \mathbf{100}$$

It is important to note that for calculating modulation index, the modulating frequency change had to be taken into account in the third case.

16.13 Comparison of FM and AM

The comparison of FM and AM is given in the table below.

S. No	FM	AM
1.	The amplitude of carrier remains constant with modulation.	The amplitude of carrier changes with modulation.
2.	The carrier frequency changes with modulation.	The carrier frequency remains constant with modulation.
3.	The carrier frequency changes according to the strength of the modulating signal.	The carrier amplitude changes according to the strength of the modulating signal.
4.	The value of modulation index (m_f) can be more than 1.	The value of modulation factor (m) cannot be more than 1 for distortionless AM signal.

16.14 Demodulation

The process of recovering the audio signal from the modulated wave is known as **demodulation** *or* **detection.**

At the broadcasting station, modulation is done to transmit the audio signal over larger distances to a receiver. When the modulated wave is picked up by the radio receiver, it is necessary to recover the audio signal from it. This process is accomplished in the radio receiver and is called demodulation.

Necessity of demodulation. It was noted previously that amplitude modulated wave consists of carrier and sideband frequencies. The audio signal is contained in the sideband frequencies which are radio frequencies. If the modulated wave after amplification is directly fed to the speaker as shown in Fig. 16.15, no sound will be heard. It is because diaphragm of the speaker is not at all able to respond to such high frequencies. Before the diaphragm is able to move in one direction, the rapid reversal of current tends to move it in the opposite direction i.e. diaphragm will not move at all. Consequently, no sound will be heard.

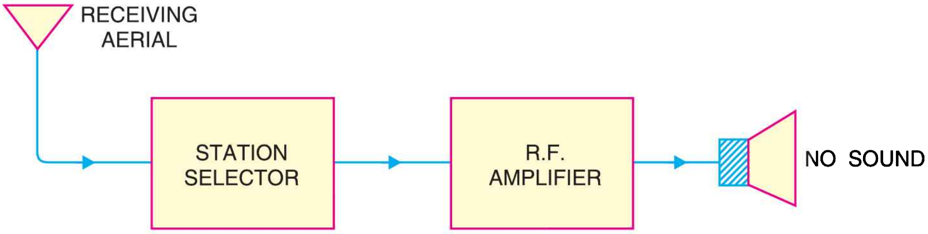


Fig. 16.15

From the above discussion, it follows that audio signal must be separated from the carrier at a suitable stage in the receiver. The recovered audio signal is then amplified and fed to the speaker for conversion into sound.

16.15 Essentials in Demodulation

In order that a modulated wave is audible, it is necessary to change the nature of modulated wave. This is accomplished by a circuit called *detector.* A detector circuit performs the following two functions :

(*i*) ***It rectifies the modulated wave i.e.*** negative half of the modulated wave is eliminated. As shown in Fig. 16.16 (*i*), a modulated wave has positive and negative halves exactly equal. Therefore, average current is zero and speaker cannot respond. If the negative half of this modulated wave is eliminated as shown in Fig. 16.16 (*ii*), the average value of this wave will not be zero since the resultant pulses are now all in one direction. The average value is shown by the dotted line in Fig. 16.16 (*ii*). Therefore, the diaphragm will have definite displacement corresponding to the average value of the wave. It may be seen that shape of the average wave is similar to that of the modulation envelope. As the signal is of the same shape as the envelope, therefore, average wave shape is of the same form as the signal.

(*ii*) ***It separates the audio signal from the carrier.*** The rectified modulated wave contains the audio signal and the carrier. It is desired to recover the audio signal. This is achieved by a filter circuit which removes the carrier frequency and allows the audio signal to reach the load *i.e.*speaker.

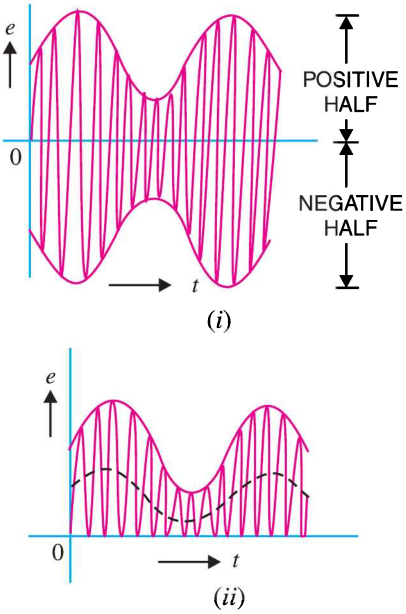


Fig. 16.16

16.16 A.M. Diode Detector

Fig. 16.17 shows a simple detector circuit employing vacuum diode and filter circuit. The modulated wave of desired frequency is selected by the parallel tuned circuit L_1C_1 and is applied to the vacuum diode. During the positive half-cycles of modulated wave, the diode conducts while during negative half-cycles, it does not. The result of this rectifying action is that output of the diode consists of positive half-cycles of modulated wave as shown.

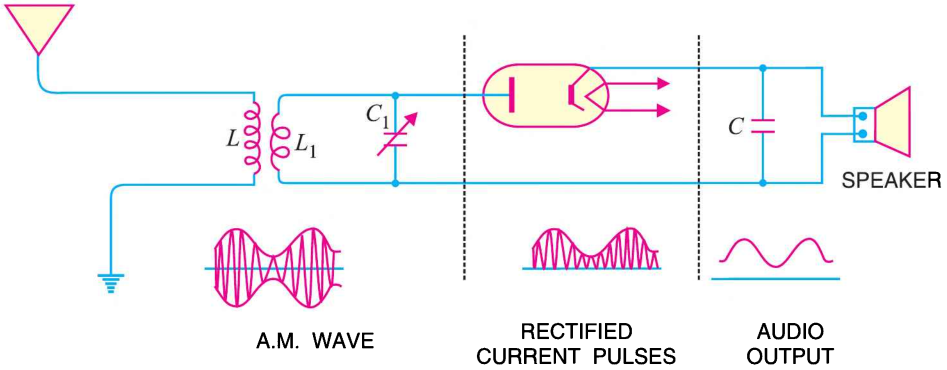


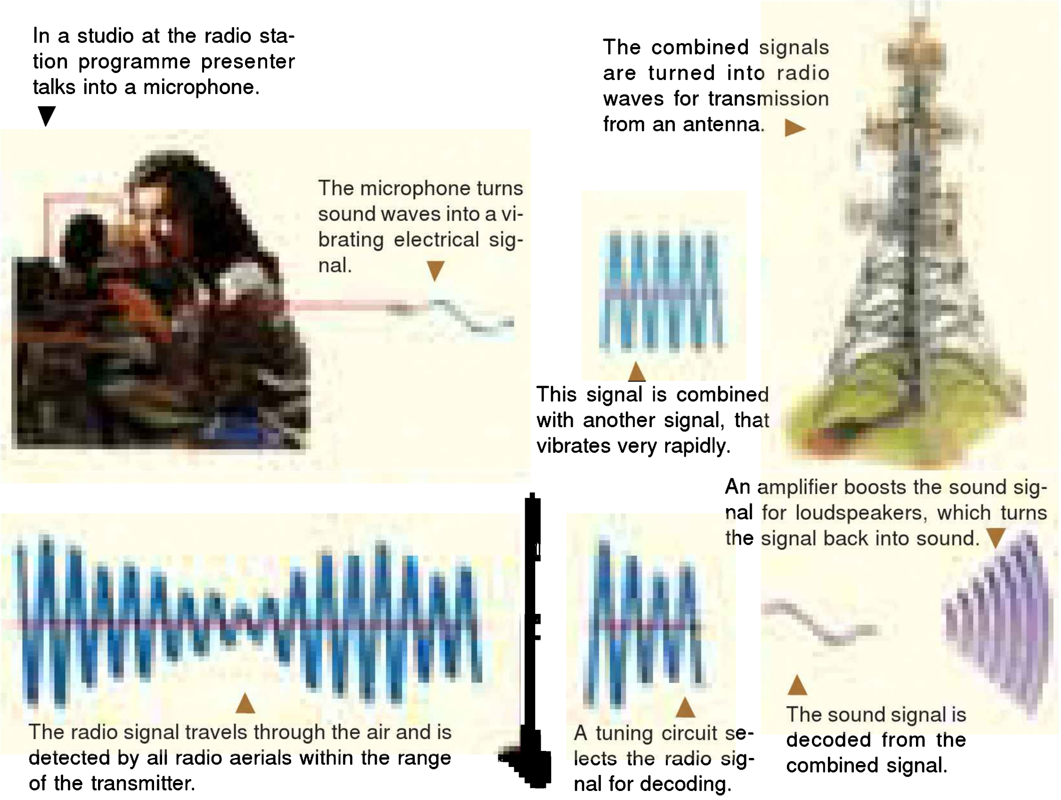
Fig. 16.17

The rectified modulated wave contains radio frequency and the signal and cannot be fed to the speaker for sound reproduction. If done so, no sound will be heard due to the inertia of speaker diaphragm. The *r.f.* component is filtered by the capacitor *C* shunted across the speaker. The value of this capacitor is sufficiently large to present low reactance to the r.f. component while presenting a relatively high reactance to the audio signal. The result is that the r.f. component is bypassed by the capacitor *C* and the signal is passed on to the speaker for sound reproduction.

Note. If vacuum diode is replaced by a crystal diode, the circuit becomes crystal diode detector.

16.17 A.M. Radio Receivers

A radio receiver is a device which reproduces the modulated or radio waves into sound waves. In India, only amplitude modulation is used for radio transmission and reception. Therefore, such radio



In a studio at the radio station programme presenter talks into a microphone.

The microphone turns sound waves into a vibrating electrical signal.

This signal is combined with another signal, that vibrates very rapidly.

The combined signals are turned into radio waves for transmission from an antenna.

The radio signal travels through the air and is detected by all radio aerials within the range of the transmitter.

A tuning circuit selects the radio signal for decoding.

The sound signal is decoded from the combined signal.

An amplifier boosts the sound signal for loudspeakers, which turns the signal back into sound.

receivers are called A.M. radio receivers. In order to reproduce the A.M. wave into sound waves, every radio receiver must perform the following functions :

(*i*) The receiving aerial must intercept a portion of the passing radio waves.

(*ii*) The radio receiver must select the desired radio wave from a number of radio waves intercepted by the receiving aerial. For this purpose, tuned parallel *LC* circuits must be used. These circuits will select only that radio frequency which is in resonant with them.

(*iii*) The selected radio wave must be amplified by the tuned frequency amplifiers.

(*iv*) The audio signal must be recovered from the amplified radio wave.

(*v*) The audio signal must be amplified by suitable number of audio-amplifiers.

(*vi*) The amplified audio signal should be fed to the speaker for sound reproduction.

16.18 Types of A.M. Radio Receivers

A.M. radio receivers can be broadly classified into two types *viz.*, *straight radio receiver* and *superhetrodyne radio receiver.* The former was used in the early days of radio communication. However at present, all radio receivers are of superhetrodyne type.

1. Straight radio receiver. Fig. 16.18 shows the block diagram of a straight radio receiver. The aerial is receiving radio waves from different broadcasting stations. The desired radio wave is selected by the R.F. amplifier which employs a tuned parallel circuit. The selected radio wave is amplified by the tuned r.f. amplifiers. The amplified radio wave is fed to the detector circuit. This circuit extracts the audio signal from the radio wave. The output of the detector is the audio signal which is amplified by one or more stages of audio-amplification. The amplified audio signal is fed to the speaker for sound reproduction.

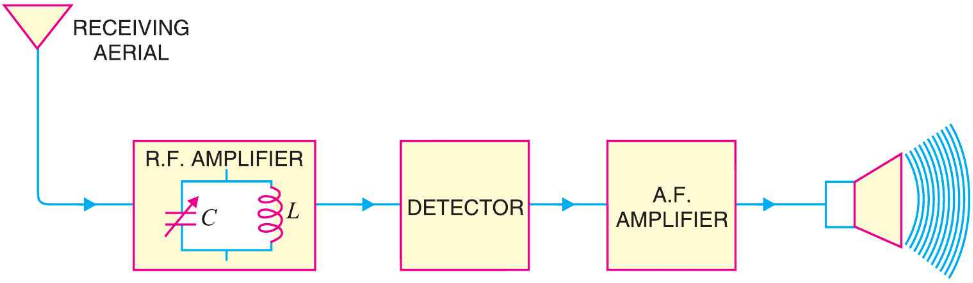


Fig. 16.18

Limitations.

(*i*) In straight radio receivers, tuned circuits are used. As it is necessary to change the value of variable capacitors (gang capacitors) for tuning to the desired station, therefore, there is a considerable variation of *Q* between the closed and open positions of the variable capacitors. This changes the sensitivity and selectivity of the radio receivers.

(*ii*) There is too much interference of adjacent stations.

2. Superhetrodyne receiver. The shortcomings of straight radio receiver were overcome by the invention of superhetrodyne receiver by Major Edwin H. Armstrong during the First World War. At present, all modern receivers utilise the superhetrodyne circuit. In this type of radio receiver, the selected radio frequency is converted to a fixed lower value, called *intermediate frequency* (*IF*). This is achieved by a special electronic circuit called *mixer circuit.* There is a local oscillator in the radio receiver itself. This oscillator produces high frequency waves. The selected radio frequency is mixed with the high frequency wave by the mixer circuit. In this process, beats are produced and the *mixer produces a frequency equal to the difference between local oscillator and radio wave fre-*

quency. As explained later, the circuit is so designed that oscillator always produces a frequency 455 kHz above the selected radio frequency. Therefore, the mixer will always produce an intermediate frequency of 455 kHz regardless of the station to which the receiver is tuned. For instance, if 600 kHz station is tuned, then local oscillator will produce a frequency of 1055 kHz. Consequently, the output from the mixer will have a frequency of 455 kHz. Fig. 16.19 shows the superhetrodyne principle with a block diagram. The selected radio frequency f_1 is mixed with a frequency f_2 from a local oscillator. The output from the mixer is a difference (*i.e.* $f_2 - f_1$) and is always 455 kHz regardless of the station to which the receiver is tuned.

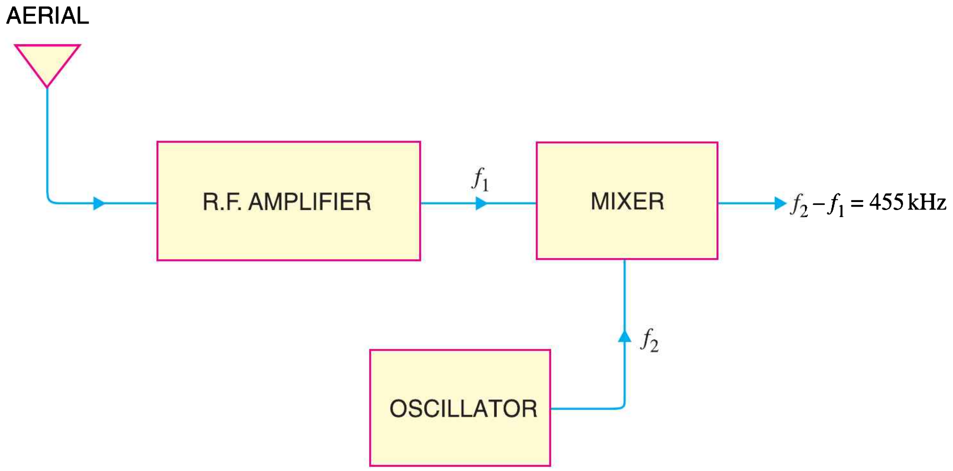


Fig. 16.19

The production of fixed intermediate frequency (455 kHz) is the salient feature of superhetrodyne circuit. At this fixed intermediate frequency, the amplifier circuits operate with maximum stability, selectivity and sensitivity. As the conversion of incoming radio frequency to the intermediate frequency is achieved by *heterodyning* or beating the local oscillator against radio frequency, therefore, this circuit is called *superhetrodyne circuit.

16.19 Stages of Superhetrodyne Radio Receiver

Fig. 16.20 shows the block diagram of a superhetrodyne receiver. It may be seen that R.F. amplifier stage, mixer stage and oscillator stage use tuned parallel circuits with variable capacitors. These capacitors are ganged together as shown by the dotted interconnecting lines. The rotation of the common shaft simultaneously changes the capacitance of these tuned circuits.

(*i*) **R.F. amplifier stage.** The R.F. amplifier stage uses a tuned parallel circuit L_1C_1 with a variable capacitor C_1. The radio waves from various broadcasting stations are intercepted by the receiving aerial and are coupled to this stage. This stage selects the desired radio wave and raises the strength of the wave to the desired level.

(*ii*) **Mixer stage.** The amplified output of R.F. amplifier is fed to the mixer stage where it is combined with the output of a local oscillator. The two frequencies beat together and produce an intermediate frequency (*IF*). The intermediate frequency is the difference between oscillator frequency and radio frequency *i.e.*

$$I.F. = \text{Oscillator frequency} - \text{Radio frequency}$$

---

* In a super-hetrodyne receiver, the hetrodyne principle is used to produce an intermediate frequency which is higher than that can be heard *i.e.*, supersonic. Superhetrodyne is short for supersonic hetrodyne.

The *IF* is always 455 kHz regardless of the frequency to which the receiver is tuned. The reason why the mixer will always produce 455 kHz frequency above the radio frequency is that oscillator always produces a frequency 455 kHz *above the selected radio frequency. This is achieved by making C_3 smaller than C_1 and C_2. By making C_3 smaller, oscillator will tune to a higher frequency. In practice, capacitance of C_3 is designed to tune the oscillator to a frequency higher than radio wave frequency by 455 kHz. This frequency difference (*i.e.* 455 kHz) will always be maintained because when C_1 and C_2 are varied, C_3 will also vary proportionally. It may be noted that in mixer stage, the carrier frequency is reduced. The *IF* still contains the audio signal.

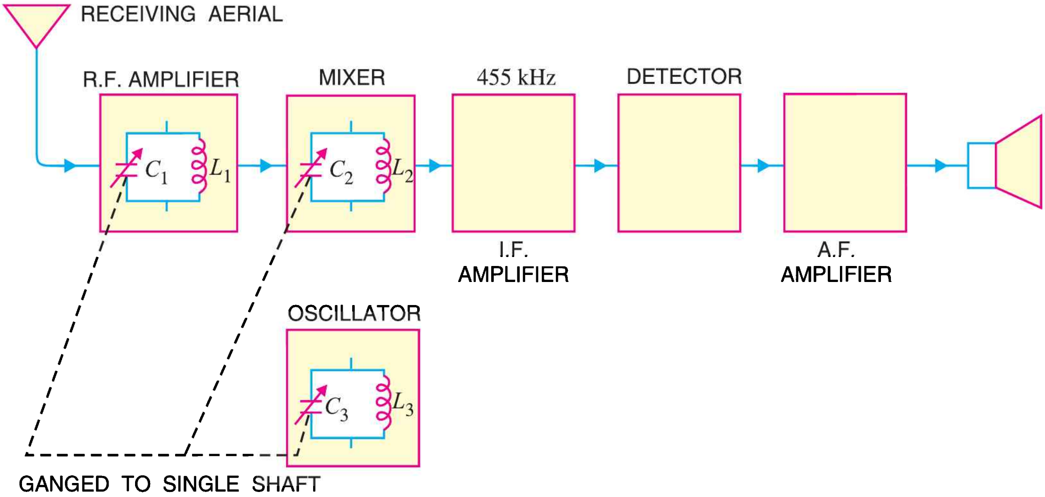
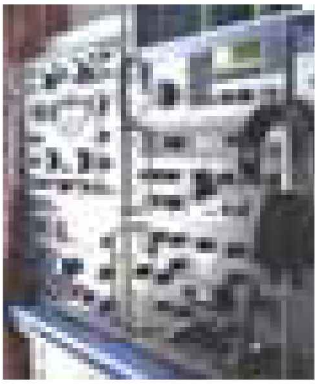


Fig. 16.20

(*iii*) **I.F. amplifier stage.** The output of mixer is always 455 kHz and is fed to fixed tuned I.F. amplifiers. These amplifiers are tuned to one frequency (*i.e.* 455 kHz) and render nice amplification.

(*iv*) **Detector stage.** The output from the last IF amplifier stage is coupled to the input of the detector stage. Here, the audio signal is extracted from the IF output. Usually, diode detector circuit is used because of its low distortion and excellent audio fidelity.

(*v*) **A.F. amplifier stage.** The audio signal output of detector stage is fed to a multistage audio amplifier. Here, the signal is amplified until it is sufficiently strong to drive the speaker. The speaker converts the audio signal into sound waves corresponding to the original sound at the broadcasting station.



Superhetrodyne Receiver

16.20 Advantages of Superhetrodyne Circuit

The basic principle involved in superhetrodyne circuit is to obtain a fixed intermediate frequency with the help of a mixer circuit and local oscillator. The superhetrodyne principle has the following advantages :

---

* The reason that the oscillator is designed to produce a frequency 455 kHz above and not below the selected frequency is as follows. A radio receiver is required to tune over 550 to 1600 kHz frequency. To provide IF of 455 kHz, the oscillator frequency must vary from 1005 to 2055 kHz. If the oscillator is designed to produce a frequency 455 kHz below the selected frequency (of course IF will be still 455 kHz), then the frequency range of the oscillator will have to be 95 to 1145 kHz. This frequency ratio is too high to be covered in a single band.

(*i*) ***High r.f. amplification.*** The superhetrodyne principle makes it possible to produce an intermediate frequency (*i.e.* 455 kHz) which is much less than the radio frequency. R.F. amplification at low frequencies is more stable since feedback through stray and interelectrode capacitance is reduced.

(*ii*) ***Improved selectivity.*** Losses in the tuned circuits are lower at intermediate frequency. Therefore, the quality factor Q of the tuned circuits is increased. This makes the amplifier circuits to operate with maximum selectivity.

(*iii*) ***Lower cost.*** In a superhetrodyne circuit, a fixed intermediate frequency is obtained regardless of the radio wave selected. This permits the use of fixed R.F. amplifiers. The superhetrodyne receiver is thus cheaper than other radio receivers.

16.21 FM Receiver

The FM receiver is more complicated and, therefore, more expensive than the normal AM receiver. As we shall see, an FM receiver also uses superheterodyne principle. The FM broadcast signals lie in the frequency range between 88 MHz and 108 MHz. The IF (intermediate frequency) of an FM receiver is 10.7 MHz—much *higher than the IF value of 455 kHz in AM receivers. Fig. 16.21 shows the block diagram of an FM receiver. In the interest of understanding, we shall discuss the various sections of the FM receiver.

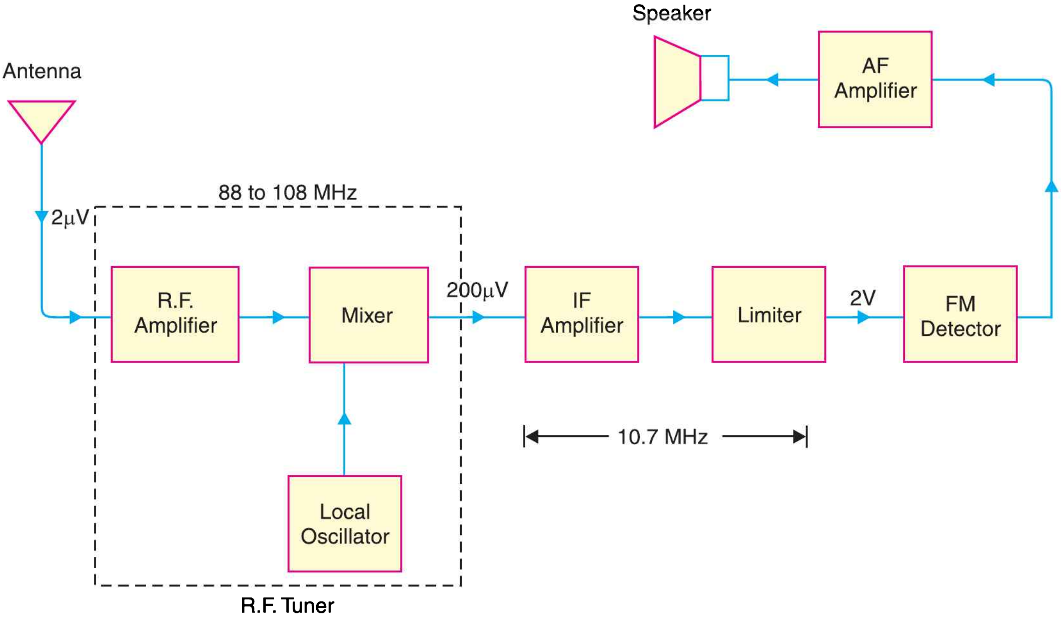


Fig. 16.21

1. **R.F. Tuner.** The FM signals are in the frequency range of 88 to 108 MHz. The weak FM signal (say 2 μV) is picked up by the antenna and is fed to the R.F. tuner. The R.F. tuner consists of (*i*) R.F. amplifier (*ii*) Mixer and (*iii*) local oscillator. The R.F. amplifier amplifies the selected FM signal (to 200 μV in the present case). The output from the RF amplifier is fed to the mixer stage where it is combined with the output signal from a local oscillator. The two frequencies beat together and produce an intermediate frequency (IF). The intermediate frequency (IF) is equal to the difference between oscillator frequency and the RF frequency.

---

* It is because the RF carrier frequencies for FM radio broadcasting are in the 88 to 108 MHz band.

The IF is always 10.7 MHz (Recall IF in AM receiver is 455 kHz) regardless of the frequency to which the FM receiver is tuned.

2. **IF Amplifier Stage.** The output signal from the mixer always has a frequency of 10.7 MHz and is fed to the IF amplifiers. Since IF amplifiers are tuned to IF (= 10.7 MHz), they render nice amplification. Note that bandwidth of IF amplifiers is about 200 kHz or 0.2 MHz. The IF gain is very large (assumed 10,000 in this case) so that output is 2V.

3. **Limiter Stage.** The output from IF stage is fed to the limiter. This circuit is an IF amplifier tuned to 10.7 MHz but its main function is to remove AM interference from the FM signal. Fig. 16.22 shows how the limiter removes AM interference from the FM signal. The input is an FM signal, but it has different amplitude levels because of AM interference has been added. However, the limiter circuit keeps the output level constant for different input levels.

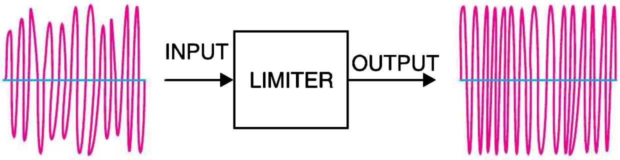


Fig. 16.22

4. **FM Detector.** After the removal of amplitude modulation from the FM signal by the limiter, the IF signal drives the input of the FM detector. An FM detector is a circuit that converts frequency variations to amplitude variations. The FM detector is also called a *discriminator* because it can distinguish between different frequencies in the input to provide different output voltages. The resultant amplitude modulated signal is then rectified and amplified for feeding to speaker for sound reproduction.

16.22 Difference Between FM and AM Receivers

Both FM and AM receivers employ superheterodyne principle. However, the following are the points of differences between the two types of receivers :

(*i*) An FM receiver has two additional stages *viz.* limiter and discriminator, which are quite different from an AM receiver.

(*ii*) FM broadcast signals lie in the frequency range between 88 and 108 MHz whereas AM broadcast signals lie in the frequency range from 540 kHz to 1600 kHz.

(*iii*) FM receivers are free from interference and this means that much weaker signals can be successfully handled.

(*iv*) FM bandwidth is about 200 kHz compared to 10 kHz bandwidth for AM.

(*v*) The IF for FM receivers is 10.7 MHz whereas IF for AM receivers is 455 kHz.

MULTIPLE-CHOICE QUESTIONS

1. Modulation is done in ....
(*i*) transmitter
(*ii*) radio receiver
(*iii*) between transmitter and radio receiver
(*iv*) none of the above

2. In a transmitter, ... oscillator is used.
(*i*) Hartley (*ii*) RC phase-shift
(*iii*) Wien-bridge (*iv*) crystal

3. In India, ... modulation is used for radio transmission.
(*i*) frequency (*ii*) amplitude
(*iii*) phase (*iv*) none of the above

4. In an AM wave, useful power is carried by ....
(*i*) carrier
(*ii*) sidebands
(*iii*) both sidebands and carrier
(*iv*) none of the above

5. In amplitude modulation, bandwidth is .... the audio signal frequency.

(*i*) thrice (*ii*) four times
(*iii*) twice (*iv*) none of the above

6. In amplitude modulation, the .... of carrier is varied according to the strength of the signal.
(*i*) amplitude (*ii*) frequency
(*iii*) phase (*iv*) none of the above

7. Overmodulation (amplitude) occurs when signal amplitude is .... carrier amplitude.
(*i*) equal to (*ii*) greater than
(*iii*) less than (*iv*) none of the above

8. In an AM wave, the majority of the power is in ....
(*i*) lower sideband
(*ii*) upper sideband
(*iii*) carrier
(*iv*) none of the above

9. At 100 % modulation, the power in each sideband is .... of that of carrier.
(*i*) 50 % (*ii*) 40 %
(*iii*) 60 % (*iv*) 25 %

10. Overmodulation results in ....
(*i*) weakening of the signal
(*ii*) excessive carrier power
(*iii*) distortion
(*iv*) none of the above

11. If modulation is 100 %, then signal amplitude is .... carrier amplitude.
(*i*) equal to (*ii*) greater than
(*iii*) less than (*iv*) none of the above

12. As the modulation level is increased, the carrier power ....
(*i*) is increased (*ii*) remains the same
(*iii*) is decreased (*iv*) none of the above

13. Demodulation is done in ....
(*i*) receiving antenna
(*ii*) transmitter
(*iii*) radio receiver
(*iv*) transmitting antenna

14. A high Q tuned circuit will permit an amplifier to have high ....
(*i*) fidelity (*ii*) frequency range
(*iii*) sensitivity (*iv*) selectivity

15. In radio transmission, the medium of transmission is ....
(*i*) space (*ii*) an antenna
(*iii*) cable (*iv*) none of the above

16. If level of modulation is increased .... power is increased.
(*i*) carrier
(*ii*) sideband
(*iii*) carrier as well as sideband
(*iv*) none of the above

17. In TV transmission, picture signal is .... modulated.
(*i*) frequency (*ii*) phase
(*iii*) amplitude (*iv*) none of the above

18. In a radio receiver, noise is generally developed at ....
(*i*) IF stage (*ii*) receiving antenna
(*iii*) audio stage (*iv*) RF stage

19. Man made noises are .... variations.
(*i*) amplitude
(*ii*) frequency
(*iii*) phase
(*iv*) both phase and frequency

20. The signal voltage induced in the aerial of a radio receiver is of the order of ....
(*i*) mV (*ii*) μV
(*iii*) V (*iv*) none of the above

21. Superhetrodyne principle refers to ....
(*i*) using a large number of amplifier stages
(*ii*) using a push-pull circuit
(*iii*) obtaining lower fixed intermediate frequency
(*iv*) none of the above

22. If a radio receiver amplifies all the signal frequencies equally well, it is said to have high ....
(*i*) sensitivity (*ii*) selectivity
(*iii*) distortion (*iv*) fidelity

23. Most of the amplification in a superhetrodyne receiver occurs at .... stage.
(*i*) IF (*ii*) RF amplifier
(*iii*) audio amplifier (*iv*) detector

24. The letters AVC stand for ....
(*i*) audio voltage control
(*ii*) abrupt voltage control
(*iii*) automatic volume control
(*iv*) automatic voltage control

25. The superhetrodyne principle provides selectivity at .... stage.
(*i*) RF (*ii*) IF
(*iii*) audio (*iv*) before RF

26. In superhetrodyne receiver, the input at the mixer stage is ....
(*i*) IF and RF
(*ii*) RF and AF

(*iii*) IF and AF
(*iv*) RF and local oscillator signal

27. The major advantage of FM over AM is ....
(*i*) reception is less noisy
(*ii*) higher carrier frequency
(*iii*) smaller bandwidth
(*iv*) small frequency deviation

28. When the modulating signal controls the frequency of the carrier, we get, ...
(*i*) phase modulation
(*ii*) amplitude modulation
(*iii*) frequency modulation
(*iv*) may be any one of the above

29. Modulation refers to a low-frequency signal controlling the ....
(*i*) amplitude of the carrier
(*ii*) frequency of the carrier
(*iii*) phase of the carrier
(*iv*) may be any of the above

30. The IF is 455 kHz. If the radio receiver is tuned to 855 kHz, the local oscillator frequency is ....
(*i*) 455 kHz (*ii*) 1310 kHz
(*iii*) 1500 kHz (*iv*) 1520 kHz

31. If $A_{min} = 40$ and $A_{max} = 60$, what is the percentage modulation ?
(*i*) 20 % (*ii*) 40 %
(*iii*) 50 % (*iv*) 10 %

32. The function of ferrite antenna is to ....
(*i*) reduce stray capacitance
(*ii*) stabilise d.c. bias
(*iii*) increase the Q of tuned circuit
(*iv*) reduce noise

33. In a radio receiver, we generally use .... oscillator as a local oscillator.
(*i*) crystal (*ii*) Wien-bridge
(*iii*) phase-shift (*iv*) Hartley

34. A 100 V carrier is made to vary between 160 V and 40 V by the signal. What is the modulation factor ?
(*i*) 0.3 (*ii*) 0.6
(*iii*) 0.5 (*iv*) none of the above

35. A 50 kW carrier is to be amplitude modulated to a level of 85 %. What is the carrier power after modulation ?
(*i*) 50 kW (*ii*) 42.5 kW
(*iii*) 58.8 kW (*iv*) 25 kW

36. In the above question, what is the power in sidebands ?
(*i*) 7.8 kW (*ii*) 11.6 kW
(*iii*) 19.06 kW (*iv*) 15.9 kW

37. In a superhetrodyne receiver, the difference frequency is chosen as the IF rather than the sum frequency because ....
(*i*) the difference frequency is closer to oscillator frequency
(*ii*) lower frequencies are easier to amplify
(*iii*) only the difference frequency can be modulated
(*iv*) none of the above

38. The diode detector in an AM radio receiver is usually found ....
(*i*) before the first RF stage
(*ii*) after the first RF stage
(*iii*) after several stages of amplification
(*iv*) none of the above

39. In a TRF radio receiver, the RF and detection stages are tuned to ....
(*i*) radio frequency
(*ii*) IF
(*iii*) audio frequency
(*iv*) none of the above

40. In TV transmission, sound signal is .... modulated
(*i*) amplitude (*ii*) frequency
(*iii*) phase (*iv*) none of the above

Answers to Multiple-Choice Questions

1.	(*i*)	**2.**	(*iv*)	**3.**	(*ii*)	**4.**	(*ii*)	**5.**	(*iii*)
6.	(*i*)	**7.**	(*ii*)	**8.**	(*iii*)	**9.**	(*iv*)	**10.**	(*iii*)
11.	(*i*)	**12.**	(*ii*)	**13.**	(*iii*)	**14.**	(*iv*)	**15.**	(*i*)
16.	(*ii*)	**17.**	(*iii*)	**18.**	(*iv*)	**19.**	(*i*)	**20.**	(*ii*)
21.	(*iii*)	**22.**	(*iv*)	**23.**	(*i*)	**24.**	(*iii*)	**25.**	(*ii*)
26.	(*iv*)	**27.**	(*i*)	**28.**	(*iii*)	**29.**	(*iv*)	**30.**	(*ii*)
31.	(*i*)	**32.**	(*iii*)	**33.**	(*iv*)	**34.**	(*ii*)	**35.**	(*i*)
36.	(*iii*)	**37.**	(*ii*)	**38.**	(*iii*)	**39.**	(*i*)	**40.**	(*ii*)

Chapter Review Topics

1. Explain the general principles of radio broadcasting, transmission and reception.
2. What is modulation ? Why is modulation necessary in communication system ?
3. Explain amplitude modulation. Derive the voltage equation of an AM wave.
4. What do you understand by modulation factor ? What is its significance ?
5. Draw the waveform of AM wave for the following values of modulation factor :
   (*i*) 0 (*ii*) 0.5 (*iii*) 1 (*iv*) 1.5
6. What do you understand by sideband frequencies in an AM wave ?
7. Derive an expression for the fraction of total power carried by the sidebands in amplitude modulation.
8. What are the limitations of amplitude modulation ?
9. What do you understand by frequency modulation ? Explain its advantages over amplitude modulation.
10. What is demodulation ? What are essentials in demodulation ?
11. Draw the diode detector circuit and explain its action.
12. What is superhetrodyne principle ? Explain the function of each stage of superhetrodyne receiver with the help of a block diagram.

Problems

1. The maximum peak-to-peak voltage of an AM wave is 16 mV while the minimum peak-to-peak voltage is 8 mV. Find the percentage modulation. **[60%]**
2. A carrier of peak voltage 0.05 V and frequency 200 kHz is amplitude modulated by a signal of peak voltage 10 V and frequency 1 kHz. Find (*i*) frequencies in the output spectrum and (*ii*) the peak values of output components if $m = 0.5$ and voltage gain $A = 100$.
   [(*i*) 199 kHz, 200 kHz, 201 kHz (*ii*) 1.25 V, 5 V, 1.25 V]
3. An AM transmitter supplies 10kW to the antenna when unmodulated. Determine the total power radiated by the transmitter when modulated to 30%. **[10.45 kW]**
4. A certain AM transmitter radiates 8kW with carrier unmodulated and 9kW when the carrier is modulated. Find the percentage modulation. **[50%]**
5. A transmitter radiates a total power of 10 kW. The carrier is modulated to a depth of 60% . Calculate (*i*) the power in the carrier and (*ii*) power in each sideband. **[(*i*) 8.47kW (*ii*) 0.765kW]**
6. A carrier of 100 V and 1500 kHz is modulated by 60V, 1200 Hz sinusoidal signal. Calculate modulation factor and express this as percentage. **[0.6; 60%]**
7. A carrier with an amplitude of 140 V is modulated by a signal with an amplitude of 80V. What is the percentage modulation ? What is the amplitude of lower sideband frequency ? **[57% ; 40V]**
8. A 50 kW carrier is to be modulated to a level of 85%. What is the carrier power after modulation ? What is sideband power ? **[50 kW ; 19.06 kW]**
9. The r.m.s. antenna current of a radio transmitter is 10 A when unmodulated, rising to 12 A when the carrier is sinusoidally modulated. What is the modulation index ? **[0.94]**
10. The r.m.s. antenna current of an AM transmitter increases by 15% over the unmodulated value when sinusoidal modulation is applied. Determine the modulation index. **[0.8]**
11. A 500 Hz modulating voltage produces a frequency deviation of 2.25 kHz. What is the modulation index ? If the amplitude of the modulation voltage is kept constant, but its frequency is raised to 6 kHz, what is the new deviation ? **[4.5 ; 54 kHz]**
12. When the modulating frequency in an FM system is 400 Hz and the modulation voltage is 2.4V, the modulation index is 60. Calculate the maximum deviation. What is the modulation index when the modulating frequency is reduced to 250 Hz and the modulating voltage is simultaneously raised to 3.2V ? **[24 kHz ; 128]**

Discussion Questions

1. Why cannot electrical energy be radiated at low frequencies (< 20 kHz) ?
2. Why is radio transmission carried at high frequencies ?
3. Why does amplitude modulation give noisy reception ?
4. Why do we always design the oscillator to produce a frequency of 455 kHz above and not below the incoming radio wave ?
5. What is the importance of modulation factor in communication system ?
6. Why is superhetrodyne principle employed in radio receivers ?
7. Why is AM and not FM employed for radio transmission in India ?
8. Why does frequency modulation give noiseless reception ?
9. Why have we selected *IF* as 455 kHz ?
10. What is the importance of sideband frequencies ?

17

Regulated D.C. Power Supply

17.1 Ordinary D.C. Power Supply
17.2 Important Terms
17.3 Regulated Power Supply
17.4 Types of Voltage Regulators
17.5 Zener Diode Voltage Regulator
17.6 Conditions for Proper Operation of Zener Regulator
17.7 Transistor Series Voltage Regulator
17.8 Series Feedback Voltage Regulator
17.9 Short-Circuit Protection
17.10 Transistor Shunt Voltage Regulator
17.11 Shunt Feedback Voltage Regulator
17.12 Glow-Tube Voltage Regulator
17.13 Series Triode Voltage Regulator
17.14 Series Double Triode Voltage Regulator
17.15 IC Voltage Regulators
17.16 Fixed Positive Voltage Regulators
17.17 Fixed Negative Voltage Regulators
17.18 Adjustable Voltage Regulators
17.19 Dual-Tracking Voltage Regulators

INTRODUCTION

In general, electronic circuits using tubes or transistors require a source of d.c. power. For example, in tube amplifiers, d.c. voltage is needed for plate, screen grid and control grid. Similarly, the emitter and collector bias in a transistor must also be direct current. Batteries are rarely used for this purpose as they are costly and require frequent replacement. In practice, d.c. power for electronic circuits is most conveniently obtained from commercial a.c. lines by using rectifier-filter system, called a *d.c. power supply.*

The rectifier-filter combination constitutes an ordinary d.c. power supply. The d.c. voltage from an ordinary power supply remains constant so long as a.c. mains voltage or load is unaltered. However, in many electronic applications, it is desired that d.c. voltage should remain constant irrespective of changes in a.c. mains or load. Under such situations, *voltage regulating devices* are used with ordinary power supply. This constitutes *regulated d.c. power supply* and keeps the d.c. voltage at fairly constant value. In this chapter, we shall focus our attention on the various voltage regulating circuits used to obtain regulated power supply.

17.1 Ordinary D.C. Power Supply

An ordinary or unregulated d.c. power supply contains a rectifier and a filter circuit as shown in Fig. 17.1. The output from the rectifier is pulsating d.c. These pulsations are due to the presence of a.c. component in the rectifier output. The filter circuit removes the a.c. component so that steady d.c. voltage is obtained across the load.

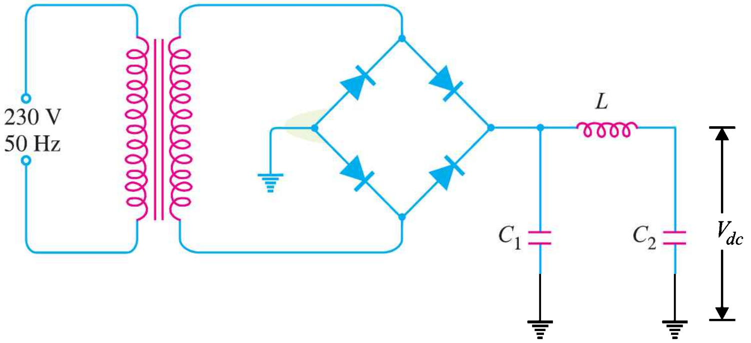


Fig. 17.1

Limitations. An ordinary d.c. power supply has the following drawbacks :

(*i*) The d.c. output voltage changes directly with input a.c. voltage. For instance, a 5% increase in input a.c. voltage results in approximately 5% increase in d.c. output voltage.

(*ii*) The d.c. output voltage decreases as the load current increases. This is due to voltage drop in (*a*) transformer windings (*b*) rectifier and (*c*) filter circuit.

These variations in d.c. output voltage may cause inaccurate or erratic operation or even malfunctioning of many electronic circuits. For example, in an oscillator, the frequency will shift and in transmitters, distorted output will result. Therefore, ordinary power supply is unsuited for many electronic applications and is being replaced by regulated power supply.

17.2 Important Terms

For comparison of different types of power supplies, the following terms are commonly used :

(*i*) **Voltage regulation.** The d.c.voltage available across the output terminals of a given power supply depends upon load current. If the load current I_{dc} is increased by decreasing R_L (See Fig. 17.2), there is greater voltage drop in the power supply and hence smaller d.c. output voltage will be available. Reverse will happen if the load current decreases. The variation of output voltage w.r.t. the amount of load current drawn from the power supply is known as *voltage regulation* and is expressed by the following relation :

$$\%\text{ Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

where V_{NL} = d.c. output voltage at no-load

V_{FL} = d.c. output voltage at full-load

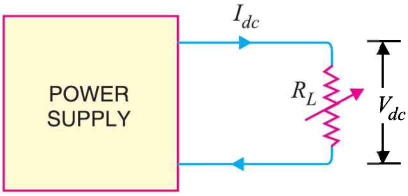


Fig. 17.2

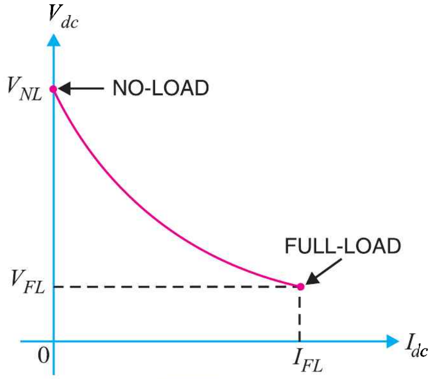


Fig. 17.3

In a well designed power supply, the full-load voltage is only slightly less than no-load voltage *i.e.* voltage regulation approaches zero. Therefore, lower the voltage regulation, the lesser the difference between full-load and no-load voltages and better is the power supply. Power supplies used in practice have a voltage regulation of 1% *i.e.* full-load voltage is within 1% of the no-load voltage. Fig. 17.3 shows the change of d.c. output voltage with load current. This is known as *voltage regulation curve*.

Note. The above voltage regulation is called *load regulation* because it indicates the change in output voltage due to the change in load current. There is another type of voltage regulation, called *line regulation* and indicates the change in output voltage due to the change in input voltage.

(*ii*) **Minimum load resistance.** The change of load connected to a power supply varies the load current and hence the d.c. output voltage. In order that a power supply gives the rated output voltage and current, there is minimum load resistance allowed. For instance, if a power supply is required to deliver a full-load current I_{FL} at full-load voltage V_{FL}, then,

$$R_{L(min)} = \frac{V_{FL}}{I_{FL}}$$

Thus, if a data sheet specifies that a power supply will give an output voltage of 100V at a maximum rated current of 0.4A, then minimum load resistance you can connect across supply is $R_{min} = 100/0.4 = 250\ \Omega$. If any attempt is made to decrease the value of R_L below this value, the rated d.c. output voltage will not be available.

Example 17.1. *If the d.c. output voltage is 400V with no-load attached to power supply but decreases to 300V at full-load, find the percentage voltage regulation.*

Solution.

$$V_{NL} = 400\text{ V}\ ;\quad V_{FL} = 300\text{ V}$$

$$\therefore \quad \%\text{ Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{400 - 300}{300} \times 100 = \mathbf{33.33\ \%}$$

Example 17.2. *A power supply has a voltage regulation of 1%. If the no-load voltage is 30V, what is the full-load voltage ?*

Solution. Let V_{FL} be the full-load voltage.

$$\%\text{ Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$$\text{or} \quad 1 = \frac{30 - V_{FL}}{V_{FL}} \times 100$$

$$\therefore \quad V_{FL} = \mathbf{29.7\ V}$$

Example 17.3. *Two power supplies A and B are available in the market. Power supply A has no-load and full-load voltages of 30V and 25V respectively whereas these values are 30V and 29V for power supply B. Which is better power supply ?*

Solution. That power supply is better which has lower voltage regulation.

Power supply A

$$V_{NL} = 30\text{ V},\quad V_{FL} = 25\text{ V}$$

$$\therefore \quad \%\text{ Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{30-25}{25} \times 100 = 20\%$$

Power supply B

$$V_{NL} = 30\text{ V},\quad V_{FL} = 29\text{ V}$$

$$\therefore \quad \%\text{ Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{30-29}{29} \times 100 = 3.45\ \%$$

Therefore, power supply B is better than power supply A.

Example 17.4. *Fig. 17.4 shows the regulation curve of a power supply. Find (i) voltage regulation and (ii) minimum load resistance.*

Solution. Referring to the regulation curve shown in Fig. 17.4, it is clear that :

$$V_{NL} = 500\text{ V};\quad V_{FL} = 300\text{ V}$$

$$I_{FL} = 120\text{ mA};\quad R_{L\,(min)} = ?$$

(*i*) Regulation

$$= \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{500-300}{300} \times 100 = \mathbf{66.7\ \%}$$

(*ii*)

$$R_{L\,(min)} = \frac{V_{FL}}{I_{FL}} = \frac{300\text{ V}}{120\text{ mA}} = \mathbf{2.5\ k\Omega}$$

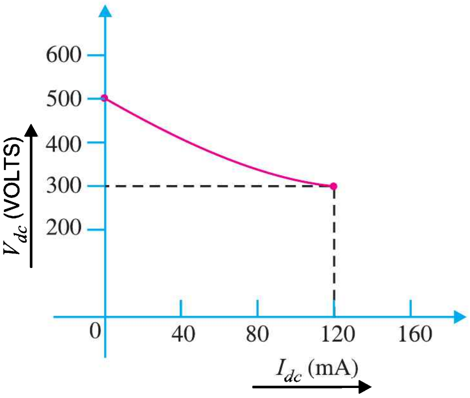


Fig. 17.4

Example 17.5. *In adding 1A load to an existing 1A load, the output voltage of a power supply drops from 10.5V to 10V. Calculate (i) output impedance of power supply and (ii) no-load voltage of power supply.*

Solution. All practical power supplies always have some internal impedance (often called output impedance) which is denoted by Z_o as shown in Fig. 17.5. It is given by the ratio of change in load voltage to the corresponding change in load current *i.e.*

$$Z_o = \frac{\Delta V_L}{\Delta I_L}$$

(*i*) Output impedance of power supply is

$$Z_o = \frac{\Delta V_L}{\Delta I_L} = \frac{10.5\text{V} - 10\text{V}}{1\text{A}} = \mathbf{0.5\Omega}$$

(*ii*) Now

$$Z_o = \frac{\Delta V_L}{\Delta I_L}$$

or

$$0.5 = \frac{V_{NL} - 10.5}{1\text{A}}$$

$$\therefore \quad V_{NL} = 0.5 \times 1 + 10.5 = \mathbf{11V}$$

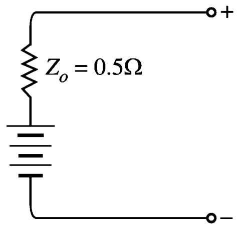


Fig. 17.5

Example 17.6. *A d.c. power supply is delivering 10V (normally) to a load that is varying sinusoidally between 0.5A and 1 A at a rate of 10 kHz. If the output impedance of the power supply is 0.01Ω at 10 kHz, determine the fluctuations in the output voltage caused by this periodic load change.*

Solution. For rapidly changing load levels—the normal situation in electronic systems—the output impedance of power supply varies with the frequency of the load change. This change with frequency occurs because of the impedance of the power supply.

Output impedance of power supply is

$$Z_o = \frac{\Delta V_L}{\Delta I_L}$$

or $$\Delta V_L = Z_o \times \Delta I_L = 0.01 \times (1 - 0.5) = 0.005\text{V} = 5\text{mV}$$

Therefore, the *output voltage will have 5mV p–p fluctuations at a rate of 10 kHz.*

Note. The power supply not only acts as a voltage source but also includes an output impedance. When specifying a power supply, output impedance is an important consideration. The smaller the output impedance of a power supply, the better it is.

Example 17.7. *A voltage regulator experiences a 10 μV change in its output voltage when its input voltage changes by 5V. Determine the value of line regulation for the circuit.*

Solution. In practice, a change in input voltage to a voltage regulator will cause a change in its output voltage. The *line regulation* of a voltage regulator indicates the change in output voltage that will occur per unit change in the input voltage *i.e.*

$$\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

$$= \frac{10\,\mu\text{V}}{5\text{V}} = \mathbf{2\,\mu V/V}$$

The 2 μV/V rating of the voltage regulator means that the output voltage will change by 2 μV for every 1V change in the regulator's input voltage.

17.3 Regulated Power Supply

A d.c. power supply which maintains the output voltage constant irrespective of a.c. mains fluctuations or load variations is known as **regulated d.c. power supply.**

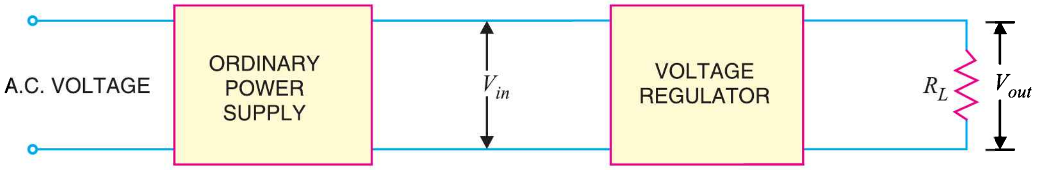


Fig. 17.6

A regulated power supply consists of an ordinary power supply and voltage regulating device. Fig. 17.6 shows the block diagram of a regulated power supply. The output of ordinary power supply is fed to the voltage regulator which produces the final output. The output voltage remains constant whether the load current changes or there are fluctuations in the input a.c. voltage.

Fig. 17.7 shows the complete circuit of a regulated power supply using zener diode as a voltage regulating device. As you can see, the regulated power supply is a combination of three circuits *viz.*, (*i*) bridge rectifier (*ii*) a capacitor filter *C* and (*iii*) zener voltage regulator. The bridge rectifier converts the transformer secondary a.c. voltage (point *P*) into pulsating voltage (point *Q*). The pulsating d.c. voltage is applied to the capacitor filter. This filter reduces the pulsations in the rectifier d.c. output voltage (point *R*). Finally, the zener voltage regulator performs two functions. Firstly, it reduces the variations in the filtered output voltage. Secondly, it keeps the output voltage (V_{out}) nearly constant whether the load current changes or there is change in input a.c. voltage. Fig. 17.8 shows the waveforms at various stages of regulated power supply. Note that bridge rectifier and capacitor filter constitute an ordinary power supply. However, when voltage regulating device is added to this ordinary power supply, it turns into a regulated power supply.

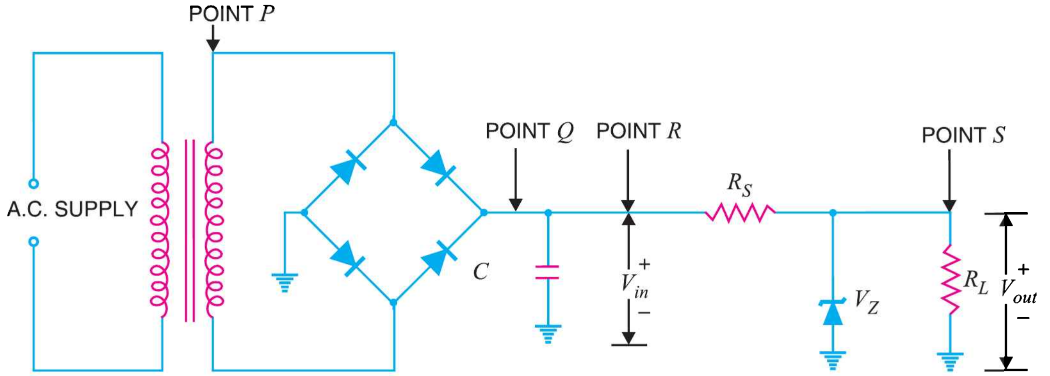

POINT *P*
A.C. SUPPLY
POINT *Q*
POINT *R*
POINT *S*
R_S
C
+
V_{in}
−
V_Z
R_L
+
V_{out}
−

Fig. 17.7

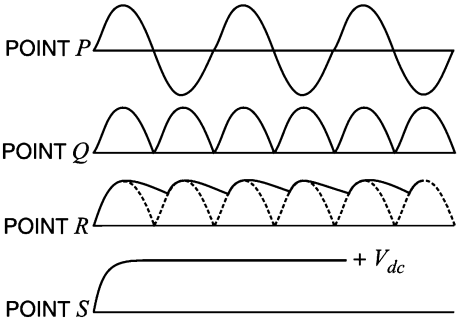


Fig. 17.8

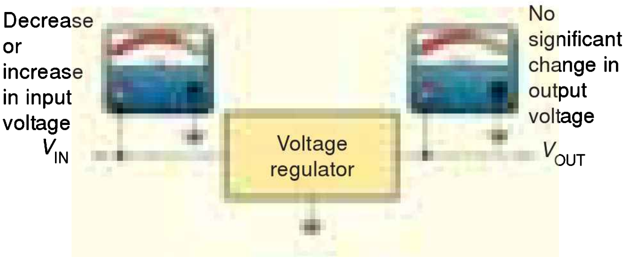
Note. In practice, this type of regulator is rarely used. The primary problem with the simple zener regulator is the fact that the zener wastes a tremendous amount of power. Practical voltage regulators contain a number of discrete and/or integrated active devices. Nevertheless, this circuit gives an idea about the regulated power supply.

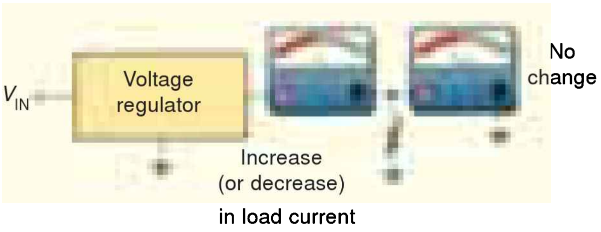
Need of Regulated Power Supply

In an ordinary power supply, the voltage regulation is poor *i.e.* d.c. output voltage changes appreciably with load current. Moreover, output voltage also changes due to variations in the input a.c. voltage. This is due to the following reasons :

(*i*) In practice, there are considerable variations in a.c. line voltage caused by outside factors beyond our control. This changes the d.c. output voltage. Most of the electronic circuits will refuse to work satisfactorily on such output voltage fluctuations. This necessitates to use regulated d.c. power supply.

(*ii*) The internal resistance of ordinary power supply is relatively large (> 30 Ω). Therefore, output voltage is markedly affected by the amount of load current drawn from the supply. These variations in d.c. voltage may cause erratic operation of electronic circuits. Therefore, regulated d.c. power supply is the only solution in such situations.


Decrease or increase in input voltage
V_{IN}
Voltage regulator
No significant change in output voltage
V_{OUT}


V_{IN}
Voltage regulator
No change
Increase (or decrease) in load current

17.4 Types of Voltage Regulators

A device which maintains the output voltage of an ordinary power supply constant irrespective of load variations or changes in input a.c. voltage is known as a *voltage regulator.* A voltage regulator generally employs electronic devices to achieve this objective. There are basic two types of voltage regulators *viz.*, (*i*) series voltage regulator (*ii*) shunt voltage regulator.

The series regulator is placed in series with the load as shown in Fig. 17.9 (*i*). On the other hand, the shunt regulator is placed in parallel with the load as shown in Fig. 17.9 (*ii*). Each type of regulator provides an output voltage that remains constant even if the input voltage varies or the load current changes.

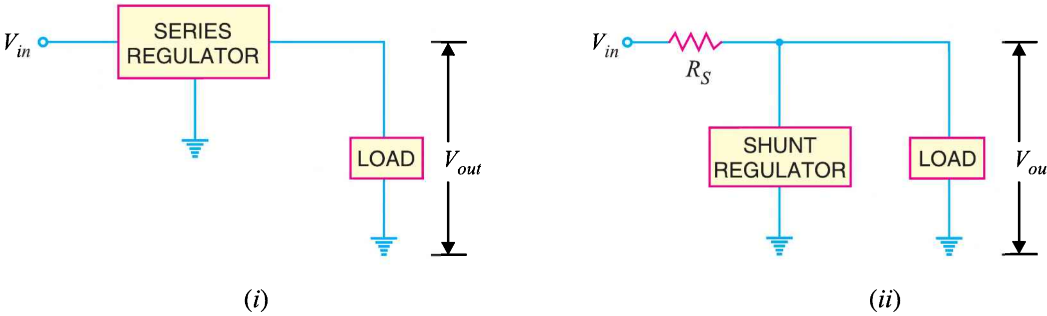


Fig. 17.9

1. For low voltages. For low d.c. output voltages (upto 50V), either zener diode alone or zener in conjunction with transistor is used. Such supplies are called transistorised power supplies. A transistor power supply can give only low stabilised voltages because the safe value of V_{CE} is about 50 V and if it is increased above this value, the breakdown of the junction may occur.

2. For high voltages. For voltages greater than 50 V, glow tubes are used in conjunction with vacuum tube amplifiers. Such supplies are generally called tube power supplies and are extensively used for the proper operation of vacuum valves.

Voltage Regulator

17.5 Zener Diode Voltage Regulator

As discussed in chapter 6, when the zener diode is operated in the breakdown or zener region, the voltage across it is substantially constant for a large change of current through it. This characteristic permits it to be used as a voltage regulator. Fig. 17.10 shows the circuit of a zener diode regulator. As long as input voltage V_{in} is greater than zener voltage V_Z, the zener operates in the breakdown region and maintains constant voltage across the load. The series limiting resistance R_S limits the input current.

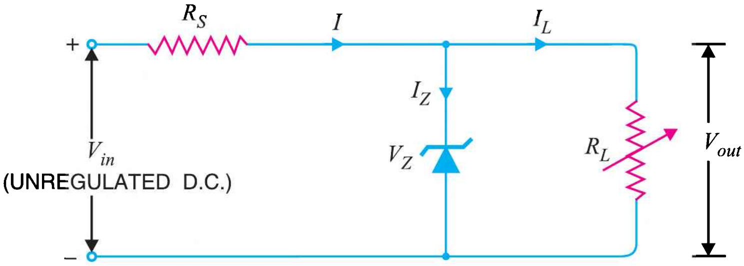
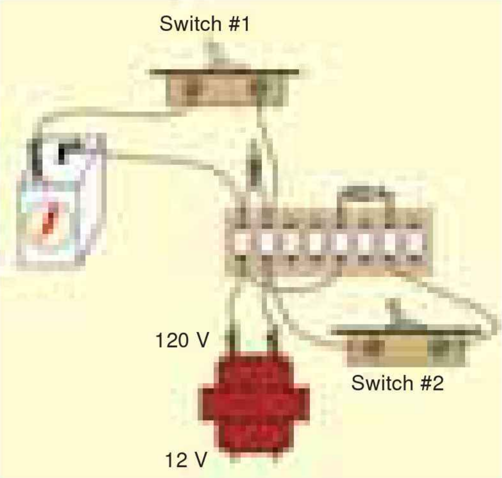


Fig. 17.10



Operation. The zener will maintain constant voltage across the load inspite of changes in load current or input voltage. As the load current increases, the zener current decreases so that current through resistance R_S is constant. As output voltage = $V_{in} - IR_S$, and I is constant, therefore, output voltage remains unchanged. The reverse would be true should the load current decrease. The circuit will also correct for the changes in input voltages. Should the input voltage V_{in} increase, more current will flow through the zener, the voltage drop across R_S will increase but load voltage would remain constant. The reverse would be true should the input voltage decrease.

Limitations. A zener diode regulator has the following drawbacks :

(*i*) It has low efficiency for heavy load currents. It is because if the load current is large, there will be considerable power loss in the series limiting resistance.

(*ii*) The output voltage slightly changes due to zener impedance as $V_{out} = V_Z + I_Z Z_Z$. Changes in load current produce changes in zener current. Consequently, the output voltage also changes. Therefore, the use of this circuit is limited to only such applications where variations in load current and input voltage are small.

17.6 Conditions for Proper Operation of Zener Regulator

When a zener diode is connected in a circuit for voltage regulation, the following conditions must be satisfied :

(*i*) The zener must operate in the breakdown region or regulating region *i.e.* between $I_{Z(max)}$ and $I_{Z(min)}$. The current $I_{Z(min)}$ (generally 10 mA) is the minimum zener current to put the zener diode in the *ON state i.e.* regulating region. The current $I_{Z(max)}$ is the maximum zener current that zener diode can conduct without getting destroyed due to excessive heat.

(*ii*) The zener should not be allowed to exceed maximum dissipation power otherwise it will be destroyed due to excessive heat. If maximum power dissipation of a zener is $P_{Z(max)}$ and zener voltage is V_Z, then,

$$P_{Z(max)} = V_Z I_{Z(max)}$$

$$\therefore \quad I_{Z(max)} = \frac{P_{Z(max)}}{V_Z}$$

(*iii*) There is a minimum value of R_L to ensure that zener diode will remain in the regulating region *i.e.* breakdown region. If the value of R_L falls below this minimum value, the proper voltage will not be available across the zener to drive it into the breakdown region.

Example 17.8. *Fig. 17.11 shows the zener regulator. Calculate (i) current through the series resistance (ii) minimum and maximum load currents and (iii) minimum and maximum zener currents. Comment on the results.*

Solution.

(*i*)
$$I_S = \frac{V_{in} - V_{out}}{R_S} = \frac{24 - 12}{160} = \frac{12\text{ V}}{160\ \Omega} = \mathbf{75\ mA}$$

(*ii*) The minimum load current occurs when $R_L \to \infty$.

$$\therefore \quad I_{L(min)} = \mathbf{0\ A}$$

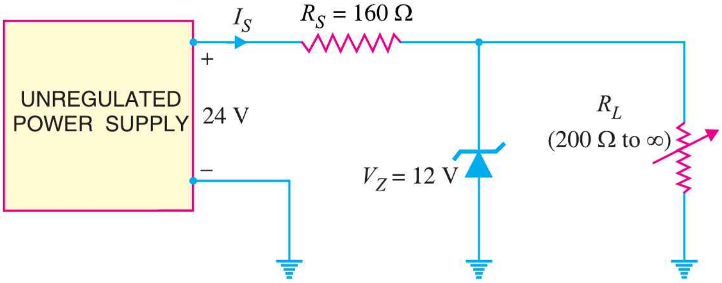


Fig. 17.11

The maximum load current occurs when $R_L = 200\ \Omega$.

$$\therefore \qquad I_{L\,(max)} = \frac{V_{out}}{R_{L(min)}} = \frac{12\text{ V}}{200\ \Omega} = \mathbf{60\ mA}$$

(*iii*)

$$I_{Z\,(min)} = I_S - I_{L\,(max)} = 75 - 60 = \mathbf{15\ mA}$$

$$I_{Z\,(max)} = I_S - I_{L\,(min)} = 75 - 0 = \mathbf{75\ mA}$$

Comments. The current I_S through the series resistance R_S is constant. When load current increases from 0 to 60 mA, the zener current decreases from 75 mA to 15 mA, maintaining I_S constant in value. This is the normal operation of zener regulator *i.e.* I_S and V_{out} remain constant inspite of changes in load current or source voltage.

Example 17.9. *A zener regulator has $V_Z = 15V$. The input voltage may vary from 22 V to 40 V and load current from 20 mA to 100 mA. To hold load voltage constant under all conditions, what should be the value of series resistance ?*

Solution. In order that zener regulator may hold output voltage constant under all operating conditions, it must operate in the breakdown region. In other words, there must be zener current for all input voltages and load currents. The worst case occurs when the input voltage is minimum and load current is maximum because then zener current drops to a minimum.

$$\therefore \qquad R_{S(max)} = \frac{V_{in\,(min)} - V_{out}}{I_{L(max)}}$$

$$= \frac{22 - 15}{0.1} = \frac{7\text{ V}}{0.1\text{ A}} = \mathbf{70\ \Omega}$$

Example 17.10. *Determine the minimum acceptable value of R_S for the zener voltage regulator circuit shown in Fig. 17.12. The zener specifications are :*

$V_Z = 3.3V$; $I_{Z\,(min)} = 3$ mA ; $I_{Z\,(max)} = 100$ mA

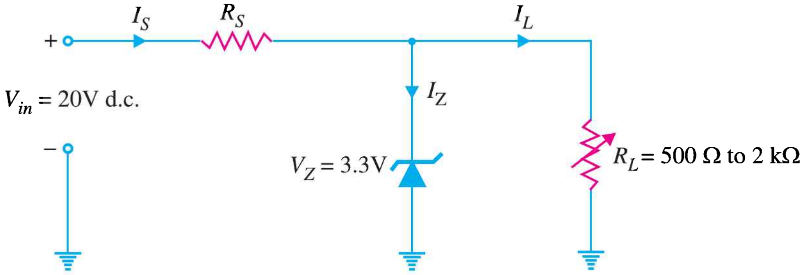


Fig. 17.12

Solution. When load R_L goes open (*i.e.* $R_L \rightarrow \infty$), the entire line current I_S will flow through the zener and the value of R_S should be such to prevent line current I_S from exceeding $I_{Z(max)}$ if the load opens.

$$\therefore \quad R_{S(min)} = \frac{V_{in} - V_Z}{I_{Z(max)}}$$

$$= \frac{20\text{V} - 3.3\text{V}}{100 \text{ mA}} = \mathbf{167\Omega}$$

Example 17.11. *Determine the maximum allowable value of R_S for the zener voltage regulator circuit shown in Fig. 17.12.*

Solution. The maximum value of R_S is limited by the total current requirements in the circuit. The value of R_S must be such so as to allow $I_{Z(min)}$ to flow through the zener diode when the load is drawing *maximum* current.

$$R_{S(max)} = \frac{V_{in} - V_Z}{I_{L(max)} + I_{Z(min)}}$$

$$\text{Now} \quad I_{L(max)} = \frac{V_Z}{R_{L(min)}} = \frac{3.3\text{V}}{500\Omega} = 6.6 \text{ mA}$$

$$\therefore \quad R_{S(max)} = \frac{20\text{V} - 3.3\text{V}}{6.6 \text{ mA} + 3 \text{ mA}} = \frac{16.7\text{V}}{9.6 \text{ mA}} = \mathbf{1739\Omega}$$

17.7. Transistor Series Voltage Regulator

Figure 17.13 shows a simple series voltage regulator using a transistor and zener diode. The circuit is called a series voltage regulator because the load current passes through the series transistor Q_1 as shown in Fig. 17.13. The unregulated d.c. supply is fed to the input terminals and the regulated output is obtained across the load. The zener diode provides the reference voltage.

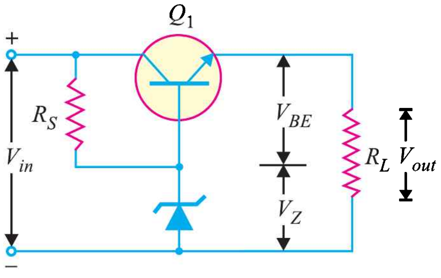


Fig. 17.13

Operation. The base voltage of transistor Q_1 is held to a relatively constant voltage across the zener diode. For example, if 8V zener (*i.e.*, $V_Z = 8\text{V}$) is used, the base voltage of Q_1 will remain approximately 8V. Referring to Fig. 17.13,

$$V_{out} = V_Z - V_{BE}$$

(*i*) If the output voltage decreases, the increased base-emitter voltage causes transistor Q_1 to conduct more, thereby raising the output voltage. As a result, the output voltage is maintained at a constant level.

(*ii*) If the output voltage increases, the decreased base-emitter voltage causes transistor Q_1 to conduct less, thereby reducing the output voltage. Consequently, the output voltage is maintained at a constant level.

The advantage of this circuit is that the changes in zener current are reduced by a factor β. Therefore, the effect of zener impedance is greatly reduced and much more stabilised output is obtained

Limitations

(*i*) Although the changes in zener current are much reduced, yet the output is not absolutely constant. It is because both V_{BE} and V_Z decrease with the increase in room temperature.

(*ii*) The output voltage cannot be changed easily as no such means is provided.

Example 17.12. *For the circuit shown in Fig. 17.13, if $V_Z = 10V$, $\beta = 100$ and $R_L = 1000\ \Omega$, find the load voltage and load current. Assume $V_{BE} = 0.5V$ and the zener operates in the breakdown region.*

Solution.

$$\text{Output voltage, } V_{out} = V_Z - V_{BE} = 10 - 0.5 = \mathbf{9.5\ V}$$

$$\text{Load current, } I_L = \frac{V_{out}}{R_L} = \frac{9.5\text{ V}}{1000\ \Omega} = \mathbf{9.5\ mA}$$

Example 17.13. *A series voltage regulator is required to supply a current of 1A at a constant voltage of 6V. If the supply voltage is 10 V and the zener operates in the breakdown region, design the circuit. Assume $\beta = 50$, $V_{BE} = 0.5V$ and minimum zener current = 10 mA.*

Solution. The design steps require the determination of zener breakdown voltage and current limiting resistance R_S. Fig. 17.14 shows the desired circuit of series voltage regulator.

(*i*) *Zener breakdown voltage.* The collector-emitter terminals are in series with the load. Therefore, the load current must pass through the transistor *i.e.*,

$$\text{Collector current, } I_C = 1\text{ A}$$

$$\text{Base current, } I_B = I_C/\beta = 1\text{A}/50 = 20\text{ mA}$$

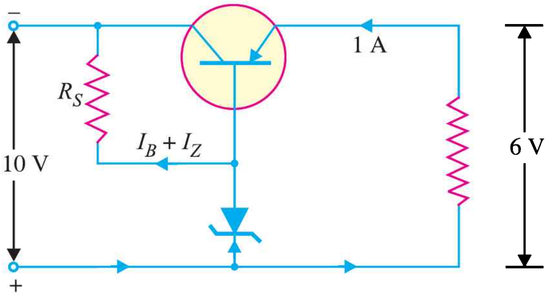


Fig. 17.14

$$\text{Output voltage, } V_{out} = V_Z - V_{BE}$$

or $$6 = V_Z - 0.5$$

$$\therefore \quad V_Z = 6 + 0.5 = \mathbf{6.5\ V}$$

Hence zener diode of breakdown voltage 6.5V is required.

(*ii*) *Value of R_S*

$$\text{Voltage across } R_S = V_{in} - V_Z = 10 - 6.5 = 3.5\text{ V}$$

$$\therefore \quad R_S = \frac{\text{Voltage across } R_S}{I_B + I_Z} = \frac{3.5\text{V}}{(20 + 10)\text{ mA}} = \mathbf{117\ \Omega}$$

Example 17.14. *For the series voltage regulator shown in Fig. 17.15, calculate (i) output voltage and (ii) zener current.*

Solution.

(*i*) $$V_{out} = V_Z - V_{BE} = 12 - 0.7 = \mathbf{11.3\ V}$$

(*ii*) $$\text{Voltage across } R_S = V_{in} - V_Z = 20 - 12 = 8\text{ V}$$

$$\text{Current through } R_S,\ I_R = \frac{8\text{ V}}{220\ \Omega} = 36.4\text{ mA}$$

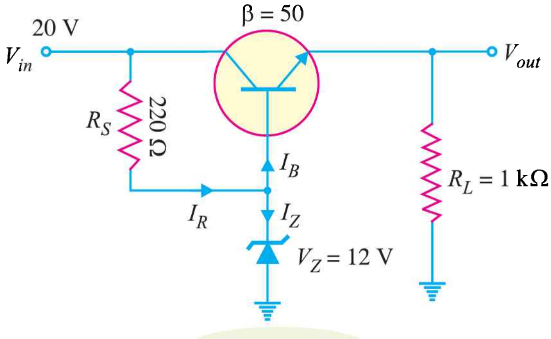


Fig. 17.15

$$\text{Load current, } I_L = \frac{V_{out}}{R_L} = \frac{11.3\text{ V}}{1\text{ k}\Omega} = 11.3\text{ mA}$$

$$\text{Base current, } I_B = \frac{I_C}{\beta} = \frac{11.3}{50} = 0.226\text{ mA}$$

$$\therefore \quad \text{Zener current, } I_Z = I_R - I_B = 36.4 - 0.226 \simeq \mathbf{36\ mA}$$

Example 17.15. *In a series transistor voltage regulator (See Fig. 17.16), the load current varies from 0 – 1A and the unregulated d.c. input varies from 12 – 18V. The 8.5V zener diode requires atleast 1 mA of current to stay in its regulating region (i.e. $I_{Z(min)}$ = 1 mA).*

(*i*) *Determine the value of R_S to ensure proper circuit operation.*

(*ii*) *Determine maximum power dissipation in R_S.*

(*iii*) *Determine maximum power dissipation in zener doide.*

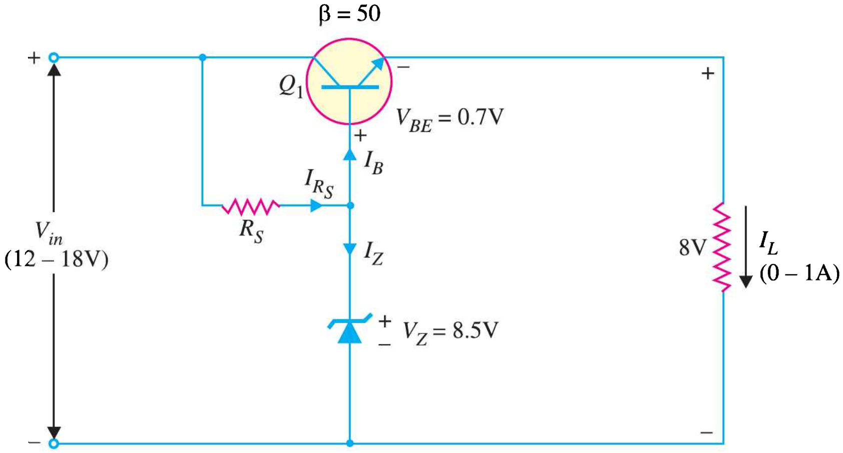


Fig. 17.16

Solution.

(*i*) The value of R_S should be such that it supplies current for the base of transistor Q_1 and for the zener diode to keep it in the regulating region. The worst condition occurs at the minimum input voltage and maximum load current. This means that under worst condition, the current through R_S must be atleast $I_{Z(min)}$ = 1 mA plus maximum base current.

$$I_{B(max)} = \frac{I_{L(max)}}{\beta} = \frac{1\text{A}}{50} = 20\text{ mA}$$

$$I_{R_S} = I_{Z\,(min)} + I_{B\,(max)}$$
$$= 1 + 20 = 21 \text{ mA}$$

Now 21 mA must be drawn by R_S under all conditions of input voltage variations—even when the input voltage falls to 12V which causes the minimum voltage across R_S and hence the lowest value of current it will be able to supply.

$$\therefore \quad R_S = \frac{V_{in\,(min)} - V_Z}{I_{R_S}}$$
$$= \frac{(12-8.5)\text{ V}}{21\text{ mA}} = \frac{3.5\text{V}}{21\text{ mA}} = \mathbf{166\ \Omega}$$

(*ii*) The maximum power dissipation in R_S occurs when the voltage across it is maximum.

$$\text{Max. voltage across } R_S,\ V_{R_{S\,(max)}} = V_{in\,(max)} - V_Z = 18 - 8.5 = 9.5\text{V}$$

$$\therefore \quad \text{Max. power dissipated in } R_S = \frac{(V_{R_{S\,(max)}})^2}{R_S} = \frac{(9.5)^2}{166} = \mathbf{0.542\ W}$$

(*iii*) Maximum power dissipation in zener occurs when current through it is maximum. The zener current will be maximum when V_{in} is maximum and load current is minimum (*i.e.* $I_L = 0$). Now $I_L = 0$ means $I_E = 0$ an hence $I_B = 0$. This, in turn, means that all the current passing through R_S will pass through the zener diode.

$$\therefore \quad I_{Z\,(max)} = I_{R_{S\,(max)}} = \frac{V_{in\,(max)} - V_Z}{R_S}$$
$$= \frac{18\text{V} - 8.5\text{V}}{166\Omega} = \mathbf{57.2\ mA}$$

∴ Max. power dissipated in zener diode is

$$P_{Z\,(max)} = V_Z I_{Z\,(max)}$$
$$= 8.5 \text{ V} \times 57.2 \text{ mA} = \mathbf{0.486\ W}$$

17.8 Series Feedback Voltage Regulator

Fig. 17.17 shows the circuit of series feedback voltage regulator. It employs principles of negative feedback to hold the output voltage almost constant despite changes in line voltage and load current. The transistor Q_2 is called a *pass transistor* because all the load current passes through it. The sample and adjust circuit is the voltage divider that consists of R_1 and R_2. The voltage divider samples the output voltage and delivers a negative feedback voltage to the base of Q_1. The feedback voltage V_F controls the collector current of Q_1.

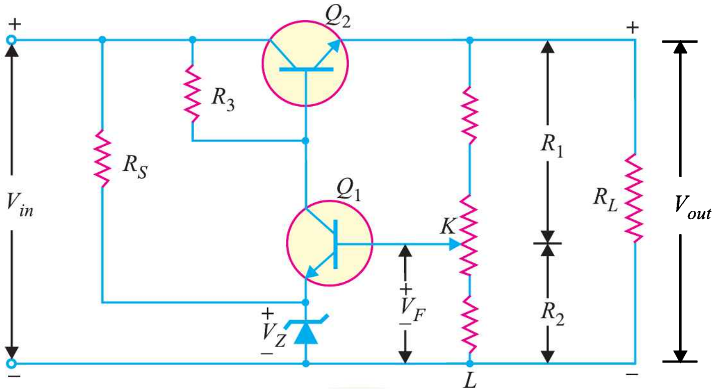


Fig. 17.17

Operation. The unregulated d.c. supply is fed to the voltage regulator. The circuit maintains constant output voltage irrespective of the variations in load or input voltage. Here is how the circuit operates.

(*i*) Suppose the output voltage increases due to any reason. This causes an increase in voltage across KL (*i.e.*, R_2) as it is a part of the output circuit. This in turn means that more V_F is fed back to the base of transistor Q_1; producing a large collector current of Q_1. Most of this collector current flows through R_3 and causes the base voltage of Q_2 to decrease. This results in less output voltage *i.e.*, increase in voltage is offset. Thus output voltage remains constant.

(*ii*) Similarly, if output voltage tries to decrease, the feedback voltage V_F also decreases. This reduces the current through Q_1 and R_3. This means more base voltage at Q_2 and more output voltage. Consequently, the output voltage remains at the original level.

Output Voltage. The voltage divider $R_1 - R_2$ provides the feedback voltage.

$$\text{Feedback fraction, } m = \frac{V_F}{V_{out}} = \frac{R_2}{R_1 + R_2}$$

$$\text{Closed loop voltage gain, } A_{CL} = \frac{1}{m} = \frac{R_1 + R_2}{R_2} = 1 + \frac{R_1}{R_2}$$

Now $$V_F = V_Z + V_{BE}$$

or $$m\,V_{out} = V_Z + V_{BE} \qquad (\because\ V_F = m\,V_{out})$$

or $$V_{out} = \frac{V_Z + V_{BE}}{m}$$

or $$V_{out} = A_{CL}\,(V_Z + V_{BE}) \qquad (\because\ 1/m = A_{CL})$$

Therefore, the regulated output voltage is equal to closed-loop voltage gain times the sum of zener voltage and base-emitter voltage.

17.9 Short-Circuit Protection

The main drawback of any series regulator is that the pass transistor can be destroyed by excessive load current if the load is accidentally shorted. To avoid such an eventuality, a current limiting circuit is added to a series regulator as shown in Fig. 17.18. A current limiting circuit consists of a transistor (Q_3) and a series resistor (R_4) that is connected between base and emitter terminals.

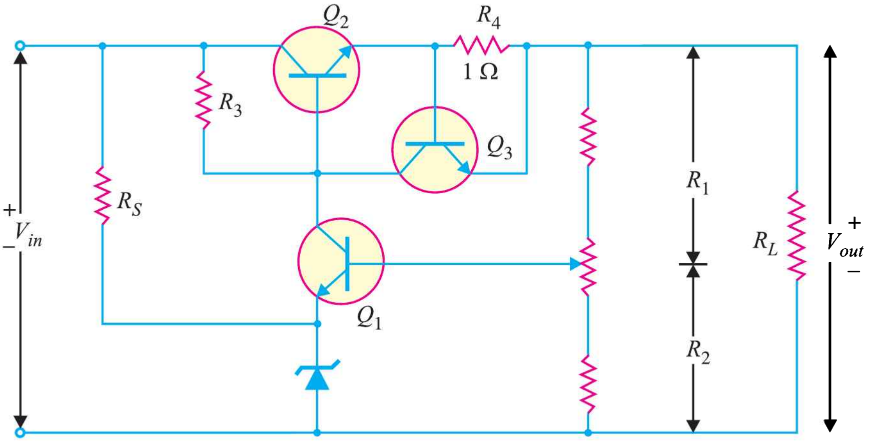


Fig. 17.18

(*i*) When the load current is normal, the voltage across R_4 (= voltage across base-emitter of Q_3) is small and Q_3 is *off. Under this condition, the circuit works as described earlier.

(*ii*) If load current becomes excessive, the voltage across R_4 becomes large enough to turn on Q_3. The collector current of Q_3 flows through R_3, thereby decreasing the base voltage of Q_2. The decrease in base voltage of Q_2 reduces the conduction of pass transistor (*i.e.*, Q_2), preventing any further increase in load current. Thus, the load current for the circuit is limited to about 700 mA.

Example 17.16. *In the series feedback voltage regulator shown in Fig. 17.18,* $R_1 = 2\ k\Omega$, $R_2 = 1\ k\Omega$, $V_Z = 6\ V$ *and* $V_{BE} = 0.7\ V$. *What is the regulated output voltage?*

Solution.

$$\text{Feedback fraction, } m = \frac{R_2}{R_1 + R_2} = \frac{1}{2+1} = \frac{1}{3}$$

$$\therefore \quad \text{Closed-loop voltage gain, } A_{CL} = \frac{1}{m} = 3$$

$$\therefore \quad \text{Regulated output voltage, } V_{out} = A_{CL}\,(V_Z + V_{BE})$$

$$= 3\,(6 + 0.7) = \mathbf{20.1\ V}$$

Example 17.17. *In the series feedback regulator circuit shown in Fig. 17.18,* $R_1 = 30\ k\Omega$ *and* $R_2 = 10\ k\Omega$. *What is the closed loop voltage gain?*

Solution.

$$\text{Feedback fraction, } m = \frac{R_2}{R_1 + R_2} = \frac{10}{30+10} = \frac{1}{4}$$

$$\therefore \quad \text{Closed-loop voltage gain, } A_{CL} = \frac{1}{m} = \mathbf{4}$$

17.10 Transistor Shunt Voltage Regulator

A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. Fig. 17.19 shows the circuit of shunt voltage regulator. The voltage drop across series resistance depends upon the current supplied to the load R_L. The output voltage is equal to the sum of zener voltage (V_Z) and transistor base-emitter voltage (V_{BE}) *i.e.*,

$$V_{out} = V_Z + V_{BE}$$

If the load resistance decreases, the current through base of transistor decreases. As a result, less collector current is shunted. Therefore, the load current becomes larger, thereby maintaining the regulated voltage across the load. Reverse happens should the load resistance increase.

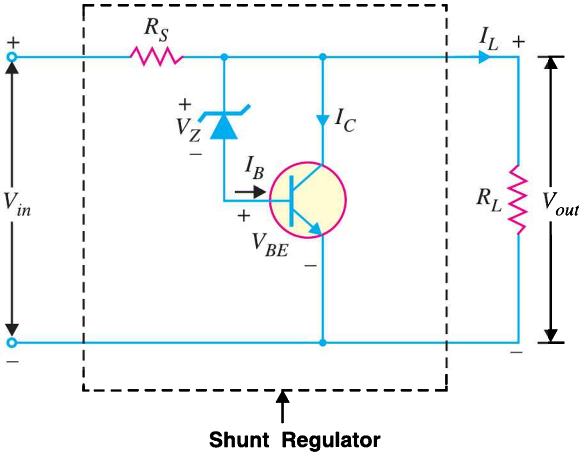


Fig. 17.19

Drawbacks. A shunt voltage regulator has the following drawbacks :

---

* In order that Q_3 is ON, voltage across R_4 must be about 0.7 V. This means that load current then is I_L = 0.7V/ 1 Ω = 700 mA. Therefore, if load current is less than 700 mA, Q_3 is off. If load current is more than 700 mA, Q_3 will be turned on.

(*i*) A large portion of the total current through R_S flows through transistor rather than to the load.

(*ii*) There is considerable power loss in R_S.

(*iii*) There are problems of overvoltage protection in this circuit.

For these reasons, a series voltage regulator is preferred over the shunt voltage regulator.

Example 17.18. *Determine the (i) regulated voltage and (ii) various currents for the shunt regulator shown in Fig. 17.20.*

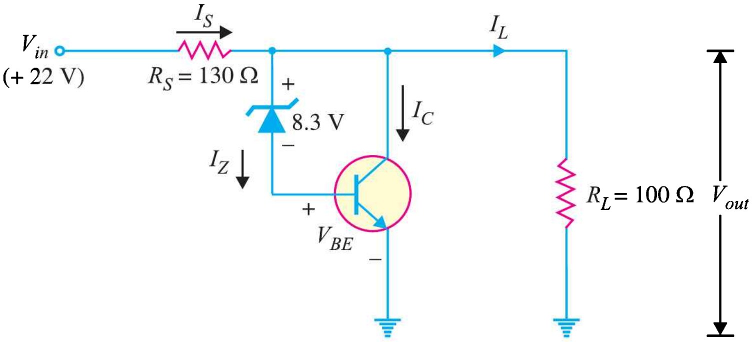


Fig. 17.20

Solution. (*i*) Output voltage, $V_{out} = V_Z + V_{BE} = 8.3 + 0.7 = \mathbf{9V}$

(*ii*) Load current, $I_L = \dfrac{V_{out}}{R_L} = \dfrac{9\text{ V}}{100\ \Omega} = \mathbf{90\ mA}$

Current through R_S, $I_S = \dfrac{V_{in} - V_{out}}{R_S} = \dfrac{22 - 9}{130} = \dfrac{13\text{ V}}{130\ \Omega} = \mathbf{100\ mA}$

∴ Collector current, $I_C = I_S - I_L = 100 - 90 = \mathbf{10\ mA}$

17.11 Shunt Feedback Voltage Regulator

This circuit is an improved form of the simple series voltage regulator discussed in Art. 17.8. As we shall see, this regulator is nearly identical to the series feedback regulator.

Circuit details. Fig. 17.21 shows the various parts of a shunt feedback voltage regulator. This circuit uses an error detector (Q_2) to control the conduction of a **shunt transistor* (Q_1). The error detector (Q_2) receives two inputs : a *reference voltage* and a *sample voltage.* The sample circuit is a simple voltage divider circuit ($R_2 - R_3 - R_4$) and derives the sample voltage from the regulated output voltage. The reference circuit is made up of zener D_1 and R_1 and derives the reference voltage from the unregulated d.c. input voltage. The outputs from the sample and reference circuits are applied to the error detector (Q_2). The output from Q_2 is used to control the conduction of the shunt transistor Q_1. Since Q_1 (shunt transistor) is in parallel with load R_L, the change in the current conduction through Q_1 can control the load voltage.

Circuit operation. In a shunt feedback voltage regulator, the outputs from the sample and reference circuits are applied to the *error detector/amplifier* Q_2. The output from Q_2 controls the conduction current through the shunt transistor Q_1 to maintain the constant load voltage V_L.

---

* Note that transistor Q_1 is in parallel with the load, it is called shunt transistor and hence the name of the regulator.

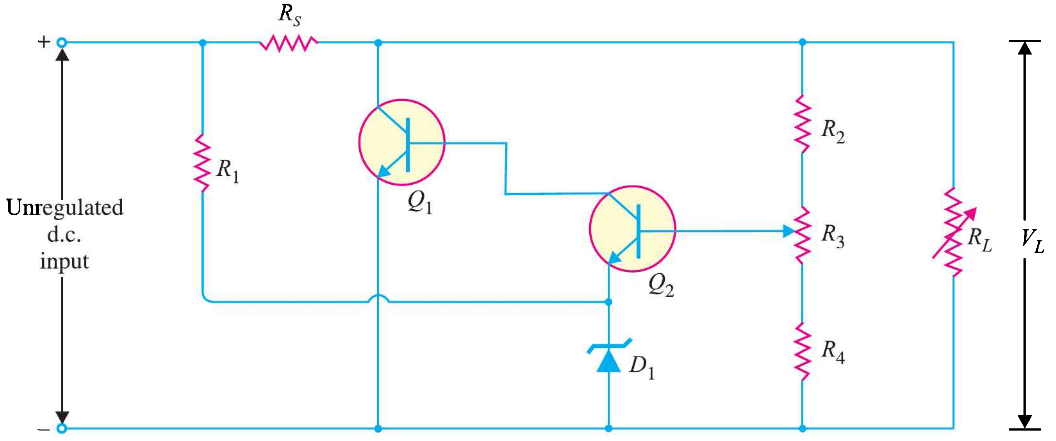


Fig. 17.21

(*i*) Suppose the load voltage V_L decreases due to any reason. This decrease causes the base voltage of Q_2 [$V_{B\,(Q2)}$] to decrease. Since emitter voltage of Q_2 [$V_{E\,(Q2)}$] is set to a fixed value (V_Z) by the zener diode, $V_{BE\,(Q2)}$ decreases when $V_{B\,(Q2)}$ decreases. This decreases base current $I_{B\,(Q1)}$ through the base of transistor Q_1. This in turn causes I_{C1} to decrease; thus increasing $V_{C\,(Q1)}$. Since $V_L = V_{C\,(Q1)}$, the increase in $V_{C\,(Q1)}$ offsets the initial decrease in V_L.

(*ii*) Suppose the load voltage increases due to any reason. This increases the conduction through Q_2, causing an increase in $I_{B\,(Q1)}$. The increase in $I_{B\,(Q1)}$ causes the shunt transistor's conduction to increase, decreasing $V_{C\,(Q1)}$. The decrease in $V_{C\,(Q1)}$ offsets the initial increase in V_L.

17.12 Glow-Tube Voltage Regulator

As discussed in chapter 3, when a glow tube (cold cathode gas diode) is operated in the *normal glow region*, the voltage across the tube remains constant over a wide range of tube current. This characteristic permits it to be used as a voltage regulator. Fig. 17.22 shows the circuit of a glow-tube voltage regulator. The unregulated d.c. input voltage must exceed the striking voltage of the tube. Once the gas in the tube ionises, the voltage across the tube and the load will drop to the ionising voltage. The tube will maintain constant voltage so long as the input d.c. voltage is greater than this value. The resistance R_S is used to limit the input current.

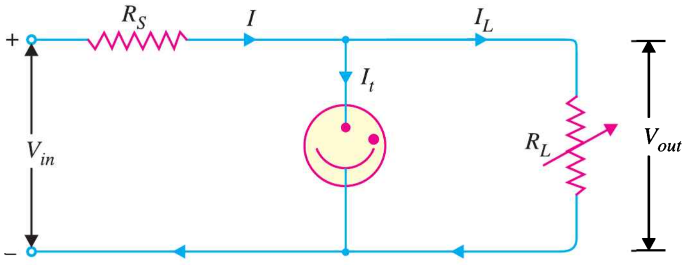


Fig. 17.22

Operation. The glow tube will maintain constant voltage across the load inspite of the changes in load current or input voltage. Now, should the load decrease, the output voltage would tend to increase. The glow tube will draw more current *without any increase in the output voltage. Meanwhile, the drop in load current is offset by the increase in tube current and the current through R_S remains constant. As output voltage = $V_{in} - IR_S$, therefore, output voltage remains unchanged. Similarly, the circuit will maintain constant output voltage if the input voltage changes. Suppose the input voltage decreases due to any reason. This would result in less current flow through the glow tube. Consequently, the voltage drop across R_S decreases, resulting in constant voltage across the load.

17.13 Series Triode Voltage Regulator

Fig. 17.23 shows the circuit of a series triode voltage regulator. It is similar to series transistor regulator except that here triode and glow tube are used instead of transistor and zener diode. The resistance R and glow tube (V.R.) help to maintain constant potential across the load. A potentiometer R_p is connected across the glow tube and its variable point is connected to the grid of the triode.

Operation. The d.c. input V_{in} from the unregulated power supply is fed to the voltage regulator. The circuit will maintain constant output voltage (V_{out}) inspite of changes in load current or input voltage. The output voltage is given by :

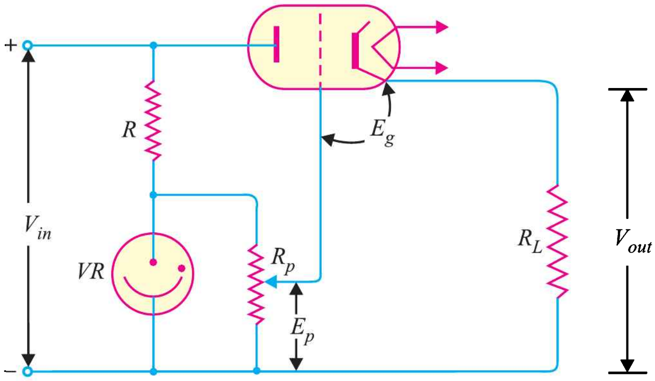


Fig. 17.23

$$V_{out} = E_p + E_g$$

Now, E_p is constant because the glow tube is operating in the normal glow region. Also grid voltage E_g is constant because it hardly depends upon plate current. Therefore, output will remain accurately fixed at one value. Any increase in the output voltage causes greater voltage drop across the limiting resistance R, tending to restore the output voltage to the original value.

17.14 Series Double Triode Voltage Regulator

Fig. 17.24 shows the circuit of a series double triode voltage regulator. Triodes T_1 and T_2 are used as direct coupled feedback amplifier in which output voltage variations are returned as feedback to oppose the input changes. The glow tube VR maintains the cathode of triode T_2 at constant potential w.r.t. ground. The triode T_2 functions as a control tube and obtains bias from the potentiometer R_3. The resistances R_3 and R_4 are range limiting resistors. The capacitor across VR tube helps to minimise the tendency of the circuit to generate audio frequency oscillations.

---

* More current will cause further ionisation, decreasing the tube resistance. Therefore, voltage across the tube remains unchanged.

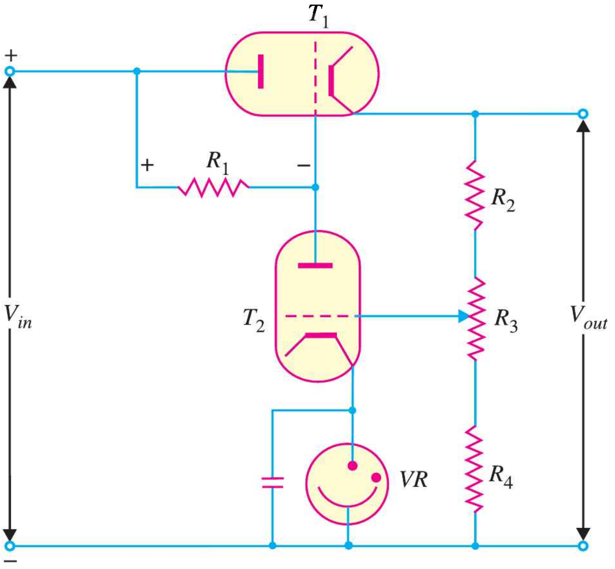


Fig. 17.24

Operation. The unregulated d.c. supply is fed to the voltage regulator. The circuit will produce an output voltage (V_{out}) which is independent of changes in input voltage and of changes in the load over a wide range. With a decrease in load or increase in the input voltage, there would be tendency for the voltage across the resistive network R_2, R_3 and R_4 to rise. The result is that voltage on the grid of triode T_2 becomes less negative. The triode T_2 then conducts more current and a greater current flows through R_1 which causes a greater voltage drop across this resistor. The increase in voltage across R_1 will raise the negative potential on the grid of triode T_1. This increases the resistance of T_1 and hence the voltage across it. The rise in voltage across T_1 tends to decrease the output voltage. The reverse would be true should the load increase or input voltage decrease.

17.15 IC Voltage Regulators

We can also use integrated circuits (*IC*) to produce voltage regulators. One advantage of *IC* voltage regulators is that properties like thermal compensation, short circuit protection and surge protection can be built into the device. Most of the commonly used *IC* voltage regulators are three-terminal devices. Fig. 17.25 shows the schematic symbol for a three-terminal *IC* voltage regulator.

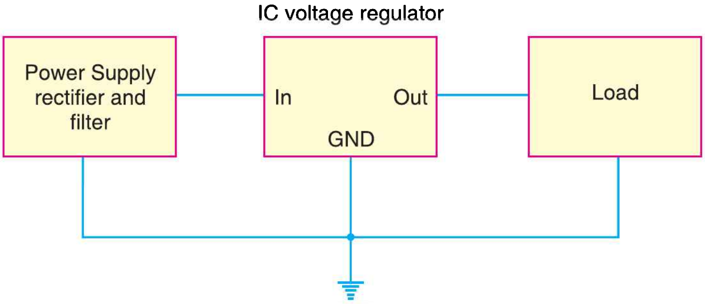


Fig. 17.25

There are basically four types of *IC* voltage regulators *viz.*

(*i*) Fixed positive voltage regulators

(*ii*) Fixed negative voltage regulators (*iii*) Adjustable voltage regulators

(*iv*) Dual-tracking voltage regulators

The *fixed positive* and *fixed negative IC voltage regulators* are designed to provide specific output voltages. For example, *LM* 309 (fixed positive) provides a + 5V d.c. output (as long as the regulator input voltages are within the specified ranges). The *adjustable voltage regulator* can be adjusted to provide any d.c. output voltage that is within its two specified limits. For example, the *LM* 317 output can be adjusted to any value between its limits of 1.2V and 32V d.c. Both positive and negative adjustable regulators are available. The *dual-tracking regulator* provides equal positive and negative output voltages. For example, the *RC* 4195 provides outputs of + 15V and – 15V d.c. Adjustable dual-tracking regulators are also available.

17.16 Fixed Positive Voltage Regulators

This *IC* regulator provides a fixed positive output voltage. Although many types of *IC* regulators are available, the 7800 series of *IC* regulators is the most popular. The last two digits in the part number indicate the d.c. output voltage. For example [See Table below], the 7812 is a + 12V regulator whereas the 7805 is a + 5V regulator. Note that this series (7800 series) provides fixed regulated voltages from + 5 V to + 24V.

Type number	Output voltage
7805	+5.0 V
7806	+6.0 V
7808	+8.0 V
7809	+9.0 V
7812	+12.0 V
7815	+15.0 V
7818	+18.0 V
7824	+24.0 V

The 7800 series

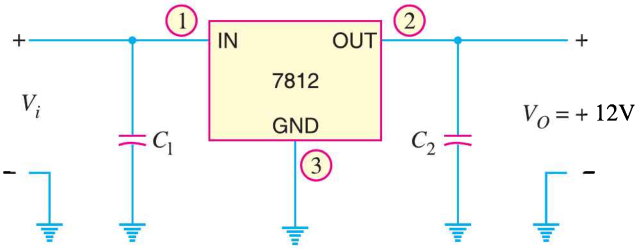


Fig. 17.26

Fig. 17.26 shows how the 7812 *IC* is connected to provide a fixed d.c. output of + 12V. The unregulated input voltage V_i is connected to the *IC*'*s IN* terminal and the *IC*'*s OUT* terminal provides + 12V. Capacitors, although not always necessary, are sometimes used on the input and output as shown in Fig. 17.26. The output capacitor (C_2) acts basically as a line filter to improve transient response. The input capacitor (C_1) is used to prevent unwanted oscillations.

Example 17.19. *Draw a voltage supply using a full-wave bridge rectifier, capacitor filter and IC regulator to provide an output of + 5V.*

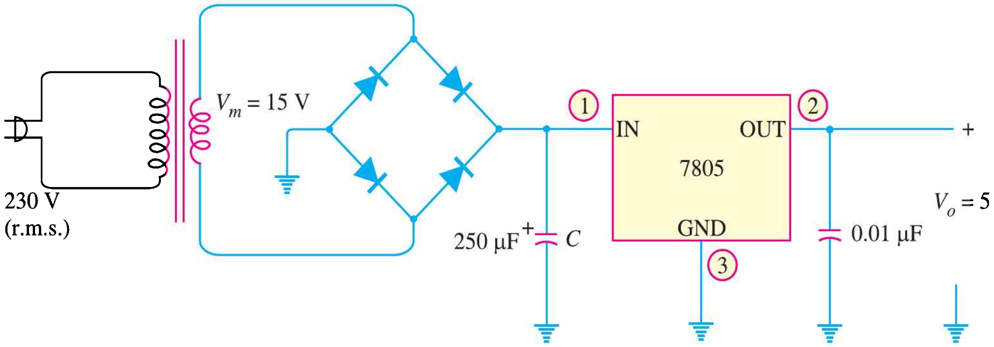


Fig. 17.27

Solution. The resulting circuit is shown in Fig. 17.27. Here we use 7805 *IC* with unregulated power supply.

17.17 Fixed Negative Voltage Regulators

This *IC* regulator provides a fixed negative ouput voltage. The 7900 series of *IC* regulators is commonly used for this purpose. This series (7900) is the negative-voltage counterpart of the7800 series [See Table below]. Note that 7900 series provides fixed regulated voltages from – 5V to – 24 V.

Type number	Output voltage
7905	−5.0 V
7905.2	−5.2 V
7906	−6.0 V
7908	−8.0 V
7912	−12.0 V
7915	−15.0 V
7918	−18.0 V
7924	−24.0 V

The 7900 series

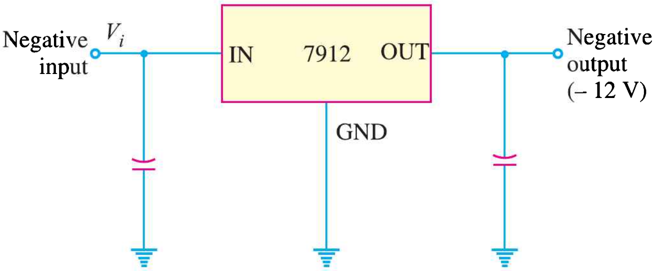


Fig. 17.28

Fig. 17.28 shows how 7912 *IC* is connected to provide a fixed d.c. output of – 12 V. The unregulated negative input voltage V_i is connected to *IC*'s *IN* terminal and the *IC*'s OUT terminal provides – 12 V. Capacitors used in the circuit perform the same function as in a fixed positive regulator.

17.18 Adjustable Voltage Regulators

The adjustable voltage regulator can be adjusted to provide any d.c. output voltage that is within its two specified limits. The most popular three-terminal *IC* adjustable voltage regulator is the *LM* 317. It has an input terminal, output terminal and an adjustment terminal. An external voltage divider is used to change the d.c. output voltage of the regulator. By changing R_2, a wide range of output voltages can be obtained.

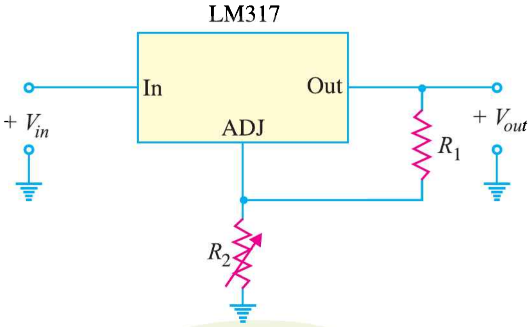


Fig. 17.29

The *LM* 317 is a three-terminal positive adjustable voltage regulator and can supply 1.5 A of load current over an adjustable output range of 1.25V to 37V. Fig. 17.29 shows an unregulated power supply driving an *LM* 317 circuit. The data sheet of an *LM* 317 gives the following formula for the output voltage :

$$V_{out} = 1.25\left(\frac{R_2}{R_1} + 1\right)$$

This formula is valid from 1.25 V to 37V.

Example 17.20. *In Fig. 17.30, R_2 is adjusted to 2.4 kΩ. Determine the regulated d.c. output voltage for the circuit.*

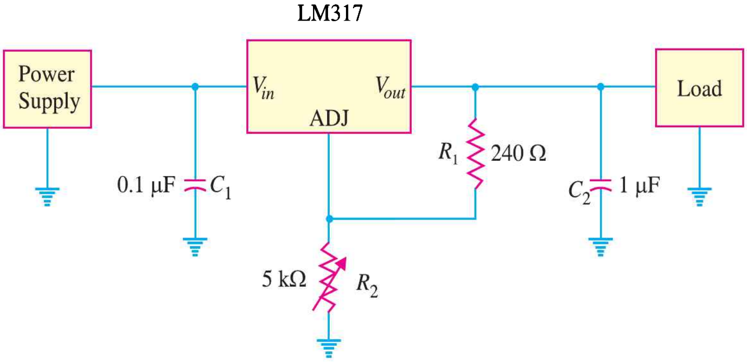


Fig. 17.30

Solution. The regulated d.c. output voltage for the circuit is given by ;

$$V_{out} = 1.25\left(\frac{R_2}{R_1}+1\right)$$

$$= 1.25\left(\frac{2.4\text{ k}\Omega}{240\ \Omega}+1\right) = (1.25)\ (11) = \mathbf{13.75V}$$

Example 17.21. *The LM 317 is adjusted to provide a + 8 V_{dc} regulated output voltage. Determine the maximum allowable input voltage to the device.*

Solution. The maximum allowable difference between V_{in} and V_{out} of an adjustable voltage regulator is called its input/output differential rating and is denoted by V_d. If this rating is exceeded, the device may be damaged. For the *LM* 317, V_d = 40V. Therefore, the maximum allowable value of input voltage is

$$V_{in\,(max)} = V_{out\,(adj)} + V_d$$

$$= +8\ V_{dc} + 40 = \mathbf{+\,48V}$$

17.19 Dual-Tracking Voltage Regulators

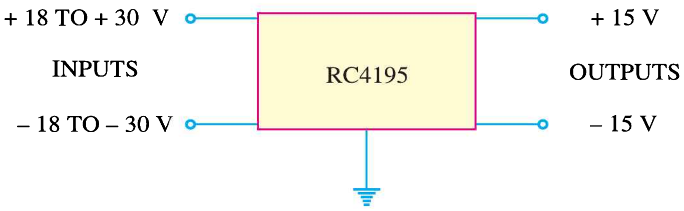


Fig. 17.31

The dual-tracking regulator provides equal positive and negative output voltages. This regulator is used when split-supply voltages are needed. The *RC* 4195 *IC* provides d.c. outputs of + 15V and – 15V. The device needs two unregulated input voltages. The positive input may be from + 18V to + 30V and the negative input from – 18V to –30V. As shown, the two outputs are ± 15V. The data sheet of an *RC* 4195 lists a maximum output current of 150 mA for each supply and a load regulation of 3mV. Adjustable dual-tracking regulators are also available. These regulators have outputs that can be varied between their two rated limits.

MULTIPLE-CHOICE QUESTIONS

1. In an unregulated power supply, if load current increases, the output voltage ....

(*i*) remains the same

(*ii*) decreases (*iii*) increases

(*iv*) none of the above

2. In an unregulated power supply, if input a.c. voltage increases, the output voltage ....

(*i*) increases (*ii*) decreases

(*iii*) remains the same

(*iv*) none of the above

3. A power supply which has a voltage regulation of .... is unregulated power supply.

(*i*) 0 % (*ii*) 0.5 %

(*iii*) 10 % (*iv*) 0.8 %

4. Commercial power supplies have voltage regulation ....

(*i*) of 10 % (*ii*) of 15 %

(*iii*) of 25 % (*iv*) within 1 %

5. An ideal regulated power supply is one which has voltage regulation of ....

(*i*) 0 % (*ii*) 5 %

(*iii*) 10 % (*iv*) 1 %

6. A zener diode utilises .... characteristic for voltage regulation.

(*i*) forward (*ii*) reverse

(*iii*) both forward and reverse

(*iv*) none of the above

7. Zener diode can be used as ....

(*i*) d.c. voltage regulator only

(*ii*) a.c. voltage regulator only

(*iii*) both d.c. and a.c. voltage regulator

(*iv*) none of the above

8. A zener diode is used as a .... voltage regulating device.

(*i*) shunt (*ii*) series

(*iii*) series-shunt (*iv*) none of the above

9. As the junction temperature increases, the voltage breakdown point for zener mechanism ....

(*i*) is increased (*ii*) is decreased

(*iii*) remains the same

(*iv*) none of the above

10. The rupture of co-valent bonds will occur when the electric field is ....

(*i*) 100 V/cm (*ii*) 0.6 V/cm

(*iii*) 1000 V/cm

(*iv*) more than 10^5 V/cm

11. In a 15 V zener diode, the breakdown mechanism will occur by ....

(*i*) avalanche mechanism

(*ii*) zener mechanism

(*iii*) both zener and avalanche mechanism

(*iv*) none of the above

12. A zener diode that has very narrow depletion layer will breakdown by .... mechanism.

(*i*) avalanche (*ii*) zener

(*iii*) both avalanche and zener

(*iv*) none of the above

13. As the junction temperature increases, the voltage breakdown point for avalanche mechanism ....

(*i*) remains the same

(*ii*) decreases (*iii*) increases

(*iv*) none of the above

14. Another name for zener diode is .... diode.

(*i*) breakdown (*ii*) voltage

(*iii*) power (*iv*) current

15. Zener diodes are generally made of ....

(*i*) germanium (*ii*) silicon

(*iii*) carbon (*iv*) none of the above

16. For increasing the voltage rating, zeners are connected in............

(*i*) parallel (*ii*) series-parallel

(*iii*) series (*iv*) none of the above

17. In a zener voltage regulator, the changes in load current produce changes in ....

(*i*) zener current (*ii*) zener voltage

(*iii*) zener voltage as well as zener current

(*iv*) none of the above

18. A zener voltage regulator is used for .... load currents.

(*i*) high (*ii*) very high
(*iii*) moderate (*iv*) small

19. A zener voltage regulator will cease to act as a voltage regulator if zener current becomes ....

(*i*) less than load current (*ii*) zero
(*iii*) more than load current
(*iv*) none of the above

20. If the doping level is increased, the breakdown voltage of the zener ....

(*i*) remains the same
(*ii*) is increased (*iii*) is decreased
(*iv*) none of the above

21. A 30 V zener will have depletion layer width .... that of 10 V zener.

(*i*) more than (*ii*) less than
(*iii*) equal to (*iv*) none of the above

22. The current in a zener diode is limited by ....

(*i*) external resistance
(*ii*) power dissipation
(*iii*) both (*i*) and (*ii*)
(*iv*) none of the above

23. A 5 mA change in zener current produces a 50 mV change in zener voltage. What is the zener impedance ?

(*i*) 1 Ω (*ii*) 0.1 Ω
(*iii*) 100 Ω (*iv*) 10 Ω

24. A certain regulator has a no-load voltage of 6 V and a full-load output of 5.82 V. What is the load regulation ?

(*i*) 3.09 % (*ii*) 2.87 %
(*iii*) 5.72 % (*iv*) none of the above

25. What is true about the breakdown voltage in a zener diode ?

(*i*) It decreases when load current increases.
(*ii*) It destroys the diode.
(*iii*) It equals current times the resistance.
(*iv*) It is approximately constant.

26. Which of these is the best description for a zener diode ?

(*i*) It is a diode.
(*ii*) It is a constant-current device.
(*iii*) It is a constant-voltage device.
(*iv*) It works in the forward region.

27. A zener diode ....

(*i*) is a battery
(*ii*) acts like a battery in the breakdown region
(*iii*) has a barrier potential of 1 V
(*iv*) is forward biased

28. The load voltage is approximately constant when a zener diode is ....

(*i*) forward biased
(*ii*) unbiased
(*iii*) reverse biased
(*iv*) operating in the breakdown region

29. In a loaded zener regulator, which is the largest zener current ?

(*i*) series current (*ii*) zener current
(*iii*) load current (*iv*) none of the above

30. If the load resistance decreases in a zener regulator, then zener current ....

(*i*) decreases (*ii*) stays the same
(*iii*) increases (*iv*) none of the above

31. If the input a.c. voltage to unregulated or ordinary power supply increases by 5 %, what will be the approximate change in d.c. output voltage ?

(*i*) 10 % (*ii*) 20 %
(*iii*) 15 % (*iv*) 5 %

32. If the load current drawn by unregulated power supply increases, the d.c. output voltage ....

(*i*) increases (*ii*) decreases
(*iii*) stays the same (*iv*) none of the above

33. If a power supply has no-load and full-load voltages of 30 V and 25 V respectively, then percentage voltage regulation is ....

(*i*) 10 % (*ii*) 20 %
(*iii*) 15 % (*iv*) none of the above

34. A power supply has a voltage regulation of 1 %. If the no-load voltage is 20 V, what is the full-load voltage ?

(*i*) 20.8 V (*ii*) 15.7 V
(*iii*) 18.6 V (*iv*) 17.2 V

35. Two similar 15 V zeners are connected in series. What is the regulated output voltage?

(*i*) 15 V (*ii*) 7.5 V
(*iii*) 30 V (*iv*) 45 V

36. A power supply can deliver a maximum rated current of 0.5 A at full-load output voltage of 20 V. What is the minimum load resistance that you can connect across the supply?

(*i*) 10 Ω (*ii*) 20 Ω
(*iii*) 15 Ω (*iv*) 40 Ω

37. In a regulated power supply, two similar 15 V zeners are connected in series. The input voltage is 45 V d.c. If each zener has a maximum current rating of 300 mA, what should be the value of series resistance ?

(*i*) 10 Ω (*ii*) 50 Ω
(*iii*) 25 Ω (*iv*) 40 Ω

38. A zener regulator .... in the power supply.

(*i*) increases the ripple
(*ii*) decreases the ripple
(*iii*) neither increases nor decreases ripple
(*iv*) data insufficient

39. When load current is zero, the zener current will be ....

(*i*) zero (*ii*) minimum
(*iii*) maximum (*iv*) none of the above

40. The zener current will be minimum when ....

(*i*) load current is maximum
(*ii*) load current is minimum
(*iii*) load current is zero
(*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*i*)	**3.** (*iii*)	**4.** (*iv*)	**5.** (*i*)
6. (*ii*)	**7.** (*iii*)	**8.** (*i*)	**9.** (*ii*)	**10.** (*iv*)
11. (*i*)	**12.** (*ii*)	**13.** (*iii*)	**14.** (*i*)	**15.** (*ii*)
16. (*iii*)	**17.** (*i*)	**18.** (*iv*)	**19.** (*ii*)	**20.** (*iii*)
21. (*i*)	**22.** (*iii*)	**23.** (*iv*)	**24.** (*i*)	**25.** (*iv*)
26. (*iii*)	**27.** (*ii*)	**28.** (*iv*)	**29.** (*i*)	**30.** (*i*)
31. (*iv*)	**32.** (*ii*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*iii*)
36. (*iv*)	**37.** (*ii*)	**38.** (*ii*)	**39.** (*iii*)	**40.** (*i*)

Chapter Review Topics

1. What do you understand by unregulated power supply ? Draw the circuit of such a supply.
2. What are the limitations of unregulated power supply ?
3. What do you understand by regulated power supply ? Draw the block diagram of such a supply.
4. Write a short note on the need for regulated power supply.
5. Explain the action of a zener voltage regulator with a neat diagram.
6. Write short notes on the following :
   (*i*) Transistor series voltage regulator
   (*ii*) Negative feedback voltage regulator
   (*iii*) Glow tube voltage regulator
7. What are the limitations of transistorised power supplies ?
8. Draw the circuit of the most practical valve operated power supply and explain its working.

Problems

1. A voltage regulator is rated at an output current of I_L = 0 to 40 mA. Under no-load conditions, the ouput voltage from the circuit is 8V. Under full-load conditions, the output voltage from the circuit is 7.996 V. Determine the value of load-regulation for the circuit. **[100 μV/mA]**
2. The zener diode in Fig. 17.32 has values of $I_{Z(min)}$ = 3 mA and $I_{Z(max)}$ = 100 mA. What is the minimum allowable value of R_L ? **[241 Ω]**

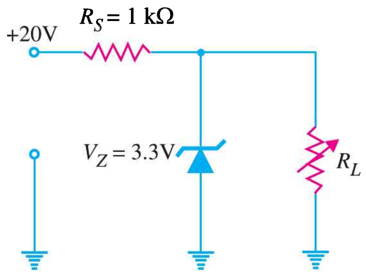

$R_S = 1\ k\Omega$
+20V
$V_Z = 3.3V$
R_L

Fig. 17.32

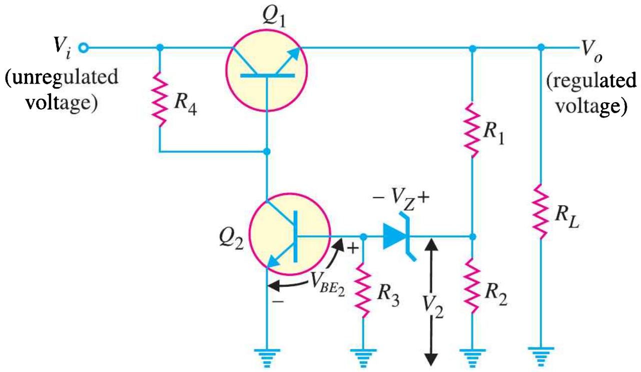

Q_1
V_i
(unregulated voltage)
R_4
V_o
(regulated voltage)
R_1
R_L
$- V_Z +$
Q_2
+
−
V_{BE_2}
R_3
V_2
R_2

Fig. 17.33

3. What regulated output voltage is provided by the circuit of Fig. 17.33 for circuit elements : $R_1 = 20$ kΩ, $R_2 = 30$ kΩ and $V_Z = 8.3$V? **[15 V]**

4. Calculate the output voltage and zener diode current in the regulator circuit of Fig. 17.34 **[7.6 V, 3.66 mA]**

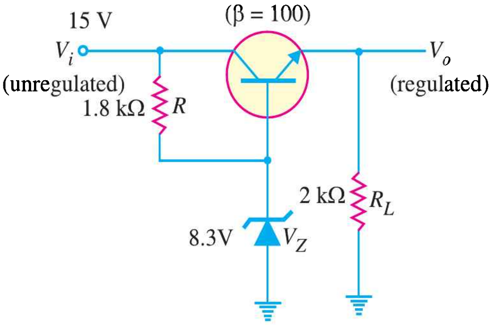

15 V
V_i
(unregulated)
(β = 100)
V_o
(regulated)
1.8 kΩ
R
2 kΩ
R_L
8.3V
V_Z

Fig. 17.34

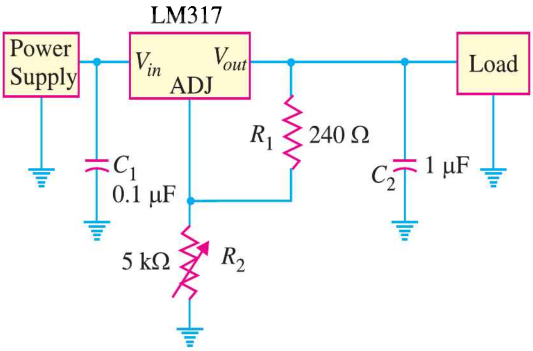

LM317
Power Supply
V_{in}
V_{out}
ADJ
Load
C_1
0.1 μF
R_1
240 Ω
C_2
1 μF
5 kΩ
R_2

Fig. 17.35

5. If R_2 in Fig. 17.35 is adjusted to 1.68 kΩ, determine the regulated d.c.output voltage for the LM 317. **[10 V]**

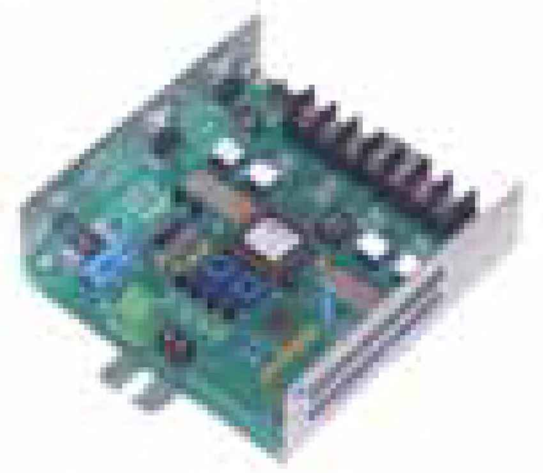
Discussion Questions

1. Why do you prefer d.c. power supply to batteries ?
2. How can you improve the regulation of an ordinary power supply ?
3. How does zener maintain constant voltage across load in the breakdown region?
4. Why is ionising potential of glow tube less than striking potential ?
5. What is the practical importance of voltage regulation in power supplies ?

18

Solid-State Switching Circuits

18.1 Switching Circuit
18.2 Switch
18.3 Mechanical Switch
18.4 Electro-mechanical Switch or Relay
18.5 Electronic Switches
18.6 Advantages of Electronic Switches
18.7 Important Terms
18.8 Switching Transistors
18.9 Switching Action of a Transistor
18.10 Multivibrators
18.11 Types of Multivibrators
18.12 Transistor Astable Multivibrator
18.13 Transistor Monostable Multivibrator
18.14 Transistor Bistable Multivibrator
18.15 Differentiating Circuit
18.16 Integrating Circuit
18.17 Important Applications of Diodes
18.18 Clipping Circuits
18.19 Applications of Clippers
18.20 Clamping Circuits
18.21 Basic Idea of a Clamper
18.22 Positive Clamper
18.23 Negative Clamper



INTRODUCTION

In practice, it is often required to make or break an electrical circuit in many operations. In some applications, it is desirable and necessary that this make and break should be very quick and without sparking. The mechanical switches cannot be used for the purpose for two main reasons. Firstly, a mechanical switch has high inertia which limits its speed of operation. Secondly, there is sparking at the contacts during breaking operation which results in the burning of the contacts.

The researches in the past years have revealed that tubes and transistors can serve as switching devices. They can turn ON or OFF power in an electrical circuit at a very high speed without any sparking. Such switches are known as electronic switches. The electronic switches are being extensively used to produce non-sinusoidal waves *e.g.*, square, rectangular, triangular or saw-tooth waves. Solid-state switching circuits are finding increasing applications. For example, solid-state switching circuits are the fundamental components of modern computer systems. In this chapter, we shall confine our attention to transistor as a switch. Once the reader gets acquainted with the switching action of a transistor, he can continue to study digital electronics on his/her own.

18.1 Switching Circuit

A circuit which can turn ON or OFF current in an electrical circuit is known as a **switching circuit.**

A switching circuit essentially consists of two parts *viz.* **(*i*)** a switch and **(*ii*)** associated circuitry. The switch is the most important part of the switching circuit. It actually makes or breaks the electrical circuit. The function of associated circuitry is to help the switch in turning ON or OFF current in the circuit. It may be worthwhile to mention here that associated circuitry is particularly used with electronic switches.

18.2 Switch

A switch is a device that can turn ON or OFF current in an electrical circuit. It is the most important part of a switching circuit. The switches can be broadly classified into the following three types :

(*i*) Mechanical switch

(*ii*) Electro-mechanical switch or Relay

(*iii*) Electronic switch

Although the basic purpose of this chapter is to discuss the switching action of a transistor, yet a brief description of mechanical and electromechanical switches is being presented. This will help the reader to understand the importance of transistor as a switch.

18.3 Mechanical Switch

A switch which is operated mechanically to turn ON or OFF current in an electrical circuit is known as a **mechanical switch.**

The familiar example of a mechanical switch is the tumbler switch used in homes to turn ON or OFF power supply to various appliances such as fans, heaters, bulbs etc. The action of a mechanical switch can be beautifully understood by referring to Fig. 18.1 where a load R_L is connected in series with a battery and a mechanical switch *S*. As long as the switch is open, there is no current in the circuit. When switch is closed, the current flow is established in the circuit. It is easy to see that the whole current flows through the load as well as the switch.

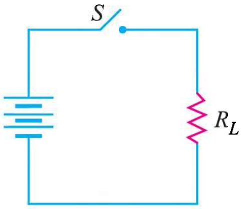


Fig. 18.1

Limitations. A mechanical switch suffers from the following drawbacks :

(*i*) In the closed position, the switch carries the whole of the load current. For a large load current, the switch contacts have to be made heavy to enable them to carry the necessary current without overheating. This increases the size of the switch.

(*ii*) If the load current carried by the circuit is large, there will be sparking at the contacts of the switch during breaking operation. This results in the wear and tear of the contacts.

(*iii*) Due to high inertia of a mechanical switch, the speed of operation is very small.

Mechanical Switches

Due to above limitations, the use of mechanical switches is restricted to situations where switching speed is small and the load current to be handled is not very heavy.

18.4 Electro-mechanical Switch or Relay

It is a mechanical switch which is operated electrically to turn ON or OFF current in an electrical circuit.

The electro-mechanical switch or relay is an improved form of simple mechanical switch. Fig. 18.2 shows the schematic diagram of a typical relay. It consists of lever *L* carrying armature *A* and a solenoid *C*. The spring pulls the lever upwards while the solenoid when energised pulls it downwards. The solenoid circuit is so designed that when switch *S* is closed, the downward pull of the solenoid exceeds the upward pull of the spring.

When the switch *S* is closed, the lever is pulled downward and the armature *A* closes the relay contacts 1 and 2. This turns ON current in the circuit. However, when switch *S* is opened, the solenoid is de-energised and the spring pulls the lever and hence the armature *A* upwards. Consequently, the relay contacts 1 and 2 are opened and current flow in the circuit is interrupted. In this way, a relay acts as a switch.

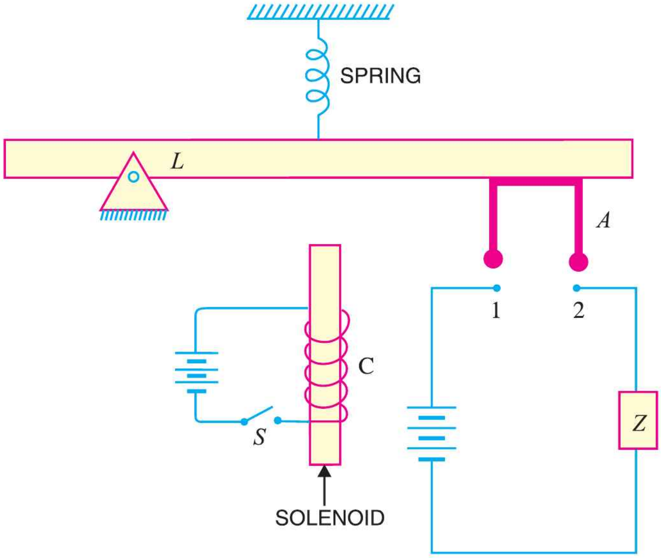


Fig. 18.2

Advantages. A relay possesses the following advantages over a simple mechanical switch :

(*i*) The relay or electro-mechanical switch requires a small power for its operation. This permits to control a large power in the load by a small power to the relay circuit. Thus a relay acts as a power amplifier *i.e.* it combines control with power amplification.

(*ii*) The switch in the relay coil carries a small current as compared to the load current. This permits the use of a smaller switch in the relay coil circuit.

(*iii*) The operator can turn ON or OFF power to a load even from a distance. This is a very important advantage when high voltages are to be handled.

(*iv*) There is no danger of sparking as the turning ON or OFF is carried by the relay coil switch which carries a small current.

However, a relay has two principal limitations. First, the speed of operation is very small; less than 5 operations per second. Secondly, a relay has moving parts and hence there is considerable wear and tear.

18.5 Electronic Switches

It is a device which can turn ON or OFF current in an electrical circuit with the help of electronic devices e.g., transistors or tubes.

Electronic switches have become very popular because of their high speed of operation and absence of sparking. A transistor can be used as a switch by driving it back and forth between *saturation* and *cut off*. This is illustrated in the discussion below :

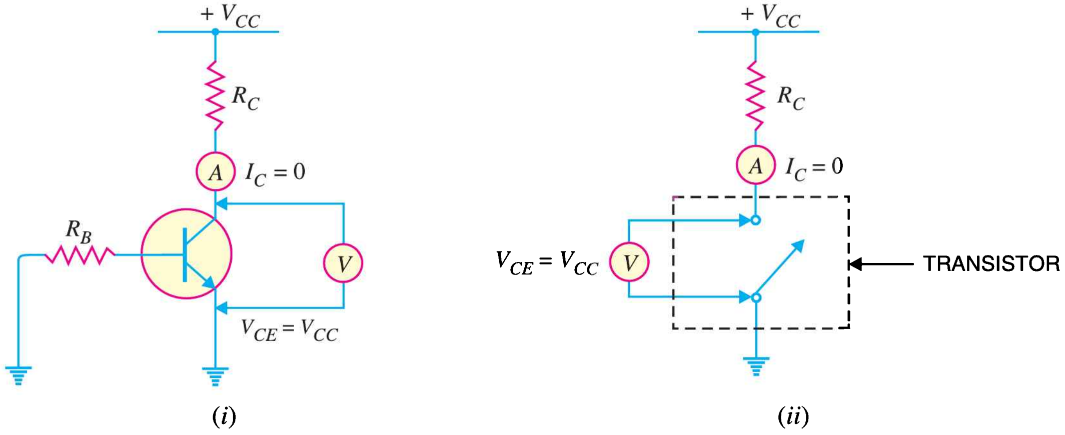

$+V_{CC}$
R_C
A
$I_C = 0$
R_B
V
$V_{CE} = V_{CC}$
(i)
$+V_{CC}$
R_C
A
$I_C = 0$
$V_{CE} = V_{CC}$
V
TRANSISTOR
(ii)

Fig. 18.3

(***i***) When the base input voltage is enough negative, the transistor is cut off and no current flows in collector load [See Fig. 18.3 (*i*)]. As a result, there is no voltage drop acorss R_C and the output voltage is *ideally V_{CC}. *i.e.*,

$$I_C = 0 \quad \text{and} \quad V_{CE} = V_{CC}$$

This condition is similar to that of an open switch (*i.e.*, OFF state) as shown in Fig. 18.3 (*ii*).

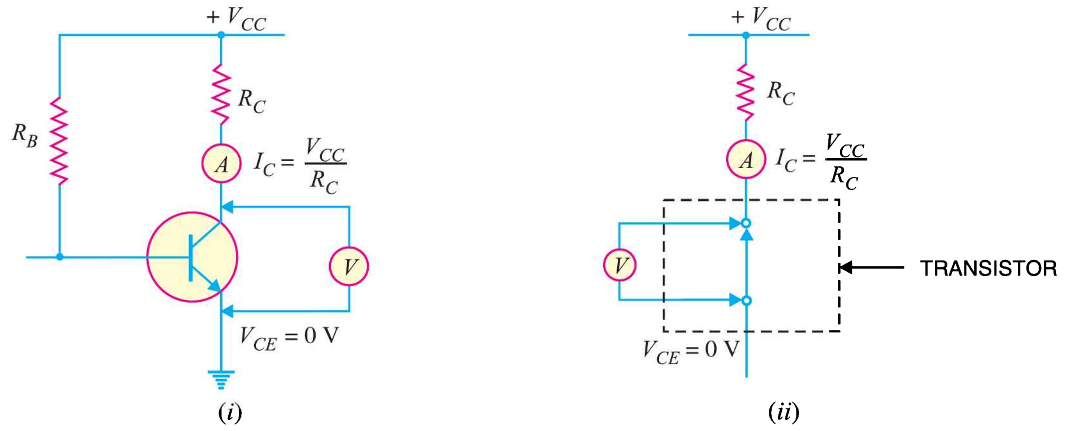

$+V_{CC}$
R_B
R_C
A
$I_C = \frac{V_{CC}}{R_C}$
V
$V_{CE} = 0$ V
(i)
$+V_{CC}$
R_C
A
$I_C = \frac{V_{CC}}{R_C}$
V
TRANSISTOR
$V_{CE} = 0$ V
(ii)

Fig. 18.4

(***ii***) When the input base voltage is positive enough that transistor saturates, then $I_{C(sat)}$ will flow through R_C. Under such conditions, the entire V_{CC} will drop across collector load R_C and output voltage is ideally zero *i.e.*,

---

* The collector current will not be zero since a little leakage current always flows even when the base input voltage is negative or zero.

∴ Output voltage $= V_{CC} - I_{leakage} R_C$. If $I_{leakage} = 0$, then output voltage $= V_{CC}$

$$I_C = I_{C(sat)} = \frac{V_{CC}}{R_C} \quad \text{and} \quad V_{CE} = 0$$

This condition is similar to that of a closed switch (*i.e.*, ON state) as shown in Fig. 18.4 (*ii*).

Conclusion. The above discussion leads to the conclusion that a transistor can behave as a switch under proper conditions. In other words, if the input base voltages are enough negative and positive, the transistor will be driven between *cut off* and *saturation*. These conditions can be easily fulfilled in a transistor circuit. Thus a transistor can act as a switch. Fig. 18.5 shows the switching action of a transistor in terms of dc load line. The point *A* of the load line represents the ON condition while point *B* represents the OFF condition.

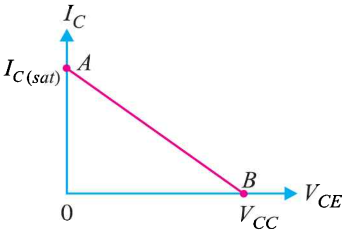


Fig. 18.5

Electronic Switches

Example 18.1. *Determine the minimum high input voltage (+V) required to saturate the transistor switch shown in Fig. 18.6.*

Solution. Assuming the transistor to be ideal,

$$I_{C(sat)} = V_{CC}/R_C = 10\text{ V}/1\text{ k}\Omega = 10\text{ mA}$$

$$\therefore \quad I_B = \frac{I_{C(sat)}}{\beta} = \frac{10\text{ mA}}{100} = 0.1\text{ mA}$$

Now

$$+V = I_B R_B + V_{BE}$$
$$= (0.1\text{ mA})(47\text{ k}\Omega) + 0.7$$
$$= 4.7 + 0.7 = \mathbf{5.4\text{ V}}$$

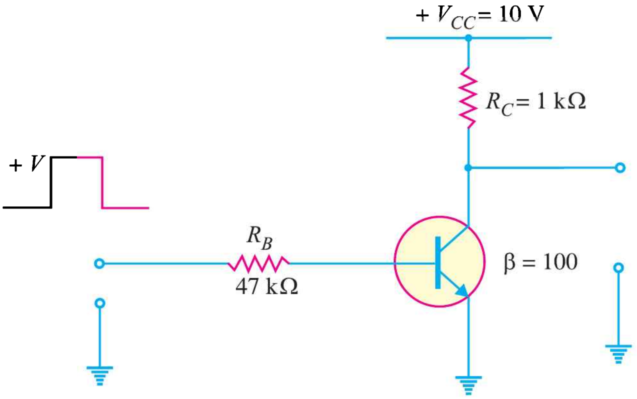


Fig. 18.6

Hence in order to saturate the transistor, we require + 5.4 V.

18.6 Advantages of Electronic Switches

The following are the advantages of transistor switch over other types of switches :

(*i*) It has no moving parts and hence there is little wear and tear. Therefore, it gives noiseless operation.

(*ii*) It has smaller size and weight.

(*iii*) It gives troublefree service because of solid state.

(*iv*) It is cheaper than other switches and requires little maintenance.

(*v*) It has a very fast speed of operation say upto 10^9 operations per second. On the other hand, the mechanical switches have a small speed of operation *e.g.* less than 5 operations in a second.

18.7. Important Terms

So far we have considered the transistor to be an ideal one. An ideal transistor has $V_{CE} = V_{CC}$ (or $I_C = 0$) in the OFF state and $V_{CE} = 0$ (or $I_C = I_{C(sat)}$) in the ON state. However, such ideal conditions are not realised in practice. In a practical transistor, the output voltage is neither V_{CC} in the OFF state nor it is zero in the ON state. While designing a transistor switching circuit, these points must be taken into consideration.

(*i*) **Collector leakage current.** When the input circuit is reverse biased or input voltage is zero, a small current (a few μA) flows in the collector. This is known as collector leakage current and is due to the minority carriers. The value of this leakage current is quite large in *Ge* transistors, but in modern silicon transistors, the value of leakage current is low enough to be ignored.

(*ii*) **Saturation collector current.** *It is the maximum collector current for a particular load in a transistor.*

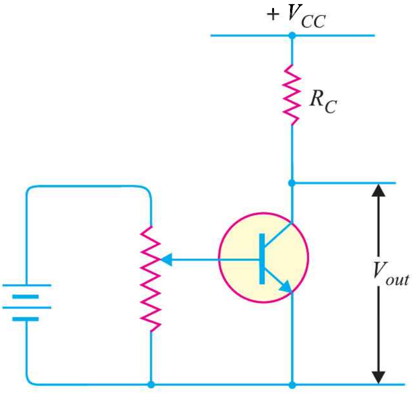


Fig. 18.7

Consider an *npn* transistor having a load R_C in its collector circuit as shown in Fig. 18.7. As the input forward bias is increased, the collector current I_C also increases because $I_C = \beta I_B$. However, with the increase in I_C, the voltage drop across R_C increases. This results in the *decrease of V_{CE}. When V_{CE} drops to knee voltage (V_{knee}), any further increase in collector current is not possible since β decreases sharply when V_{CE} falls below knee voltage. This maximum current is known as saturation collector current.

$$\therefore \quad \text{Saturation collector current, } I_{C\,(sat)} = \frac{V_{CC} - V_{knee}}{R_C}$$

18.8 Switching Transistors

A transistor which is used as a switch is known as a **switching transistor.**

In general, switching transistor is fabricated by the same process as an ordinary transistor except that it has special design features to reduce switch-off time and saturation voltage. It is so arranged in the circuit that either maximum current (called saturation collector current) flows through the load or minimum current (called collector leakage current) flows through the load. In other words, a switching transistor has two states *viz*. (*i*) ON state or when collector saturation current flows through the load (*ii*) OFF state or when collector leakage current flows through the load. In the discussion that follows transistor means the switching transistor.

---

* $V_{CE} = V_{CC} - I_C R_C$

18.9 Switching Action of a Transistor

The switching action of a transistor can also be explained with the help of output characteristics. Fig. 18.8 shows the output characteristics of a typical transistor for a *CE* configuration. The load line is drawn for load R_C and collector supply V_{CC}. The characteristics are arranged in three regions : OFF, ON or saturation and active regions.

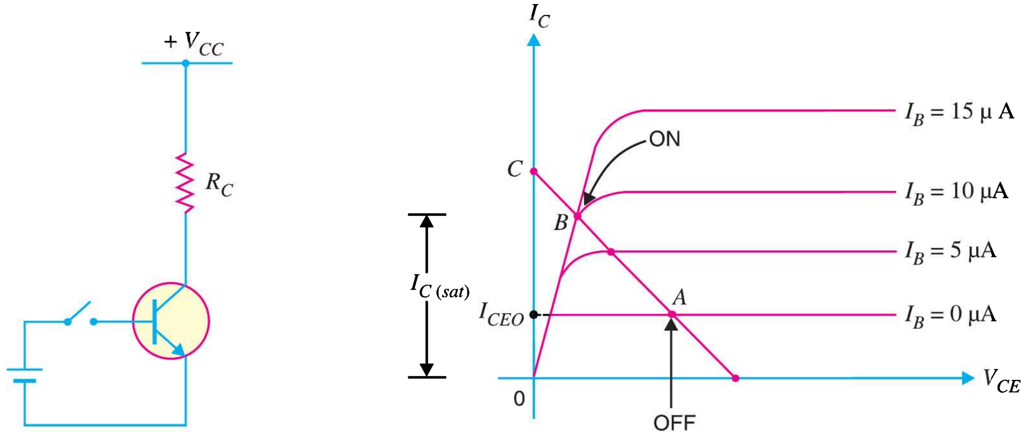


Fig. 18.8

(*i*) **OFF region.** When the input base voltage is zero or *negative, the transistor is said to be in the OFF condition. In this condition, $I_B = 0$ and the collector current is equal to the collector leakage current I_{CEO}. The value of I_{CEO} can be obtained from the characteristics if we know V_{CE}.

$$\text{Power loss} = \text{Output voltage} \times \text{Output current}$$

As already noted, in the OFF condition, the output voltage $= V_{CC}$ since voltage drop in the load due to I_{CEO} is negligible.

$$\therefore \quad \text{Power loss} = V_{CC} \times I_{CEO}$$

Since I_{CEO} is very small as compared to full-load current that flows in the ON condition, power loss in the transistor is quite small in the OFF condition. It means that the transistor has a high efficiency as a switch in the OFF condition.

(*ii*) **ON or saturation region.** When the input voltage is made so much positive that saturation collector current flows, the transistor is said to be in the ON condition. In this condition, the saturation collector current is given by :

$$I_{C(sat)} = \frac{V_{CC} - V_{knee}}{R_C}$$

$$\text{Power loss} = \text{Output voltage} \times \text{Output current}$$

---

* If a small negative voltage is given to the input, the base-emitter junction is reverse biased and load current becomes I_{CBO} instead of I_{CEO}.

The output voltage in the ON condition is equal to V_{knee} and output current is $I_{C(sat)}$.

$$\therefore \qquad \text{Power loss} = V_{knee} \times I_{C(sat)}$$

Again the efficiency of transistor as a switch in the ON condition is high. It is because the power loss in this condition is quite low due to small value of V_{knee}.

(*iii*) Active region. *It is the region that lies between OFF and ON conditions.*

The OFF and ON regions are the stable regions of operation. The active region is the unstable (or transient) region through which the operation of the transistor passes while changing from OFF state to the ON state. Thus referring to Fig. 18.8, the path *AB* is the active region. The collector current increases from I_{CEO} to $I_{C(sat)}$ along the path *AB* as the transistor is switched ON. However, when the transistor is switched OFF, the collector current decreases from $I_{C(sat)}$ to I_{CEO} along *BA*.

Conclusions

(*a*) In the **active region,** the transistor operates as a *linear amplifier* where small changes in input current (ΔI_B) cause relatively large changes in output current (ΔI_C).

(*b*) In the **saturation state,** the transistor behaves like a virtual short (collector – emitter shorted), where V_{CE} is approximately zero and I_C is maximum, limited only by the resistance R_C in the collector. In the cut off state, the transistor behaves like an open circuit (collector-emitter open), where I_C is practically zero and V_{CE} is equal to supply voltage V_{CC}. **Thus transistor in the saturation and cut off states behaves as a switch**—saturation state corresponds to the closure of switch and cut off state corresponding to opening of switch.

Note. Transistor switch is inferior to mechanical switch or relay in one respect. When the mechanical switch or relay is in the OFF condition, the load current is exactly zero. But when transistor switch is in the OFF condition, the collector current is not zero but is equal to small collector leakage current. However, for all practical purposes, this small collector leakage current may be neglected.

Example 18.2. *A transistor is used as a switch. If $V_{CC} = 10V$, $R_C = 1\ k\Omega$ and $I_{CBO} = 10\ \mu A$, determine the value of V_{CE} when the transistor is (i) cut off and (ii) saturated.*

Solution.

(*i*) *At cut off*

$$I_C = I_{CBO} = 10\ \mu\text{A}$$

$$\therefore \qquad V_{CE} = V_{CC} - I_{CBO} R_C$$

$$= 10\text{ V} - 10\ \mu\text{A} \times 1\text{ k}\Omega = 10\text{V} - 10\text{ mV} = \mathbf{9.99V}$$

(*ii*) *At saturation*

$$I_{C\,(sat)} = \frac{V_{CC} - V_{knee}}{R_C}$$

$$\therefore \qquad V_{CE} = V_{knee} = \mathbf{0.7V}$$

Example 18.3. *Fig. 18.9 shows the transistor switching circuit. Given that $R_B = 2.7\ k\Omega$, $V_{BB} = 2V$, $V_{BE} = 0.7V$ and $V_{knee} = 0.7V$.*

(*i*) *Calculate the minimum value of β for saturation.*

(*ii*) *If V_{BB} is changed to 1V and transistor has minimum β = 50, will the transistor be saturated.*

Solution.

(*i*)

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$= \frac{2\text{V} - 0.7\text{V}}{2.7\text{ k}\Omega} = \frac{1.3\text{ V}}{2.7\text{ k}\Omega} = 0.48\text{ mA}$$

Now

$$I_{C\,(sat)} = \frac{V_{CC} - V_{knee}}{R_C}$$

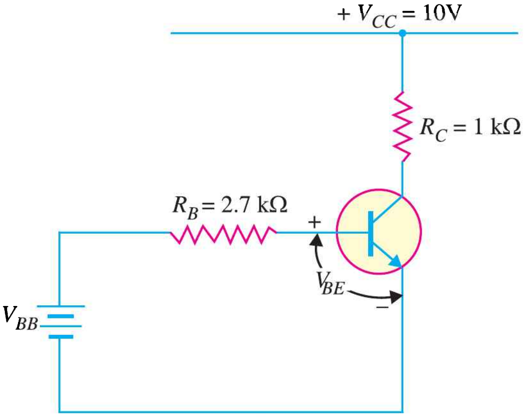

$+V_{CC} = 10\text{V}$
$R_C = 1\ \text{k}\Omega$
$R_B = 2.7\ \text{k}\Omega$
+
V_{BE}
−
V_{BB}

Fig. 18.9

$$= \frac{10\text{V} - 0.7\text{V}}{1\ \text{k}\Omega} = \frac{9.3\text{V}}{1\ \text{k}\Omega} = 9.3\ \text{mA}$$

$$\therefore \qquad \text{Minimum } \beta = \frac{I_{C(sat)}}{I_B} = \frac{9.3\ \text{mA}}{0.48\ \text{mA}} = \mathbf{19.4}$$

(*ii*)

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$= \frac{1\text{V} - 0.7\text{V}}{2.7\ \text{k}\Omega} = \frac{0.3\text{V}}{2.7\ \text{k}\Omega} = 0.111\ \text{mA}$$

$$\therefore \qquad I_C = \beta I_B = 50 \times 0.111 = 5.55\ \text{mA}$$

Since the collector current is less than saturation current (= 9.3 mA), **the transistor will not be saturated.**

18.10 Multivibrators

An electronic circuit that generates square waves (or other non-sinusoidals such as rectangular, saw-tooth waves) is known as a ***multivibrator.**

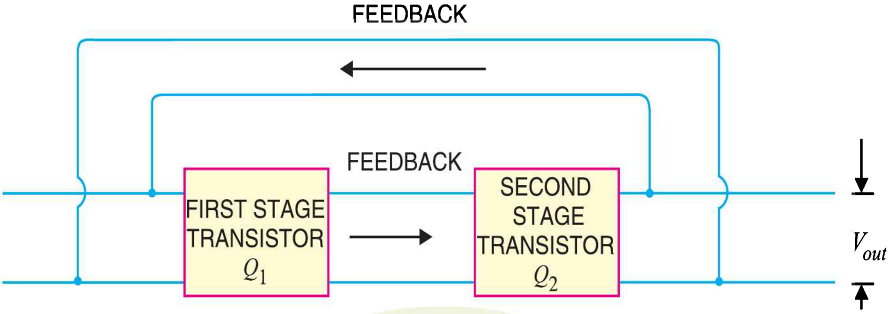

FEEDBACK
FEEDBACK
FIRST STAGE TRANSISTOR Q_1
SECOND STAGE TRANSISTOR Q_2
V_{out}

Fig. 18.10

A multivibrator is a switching circuit which depends for operation on positive feedback. It is basically a two-stage amplifier with output of one fedback to the input of the other as shown in Fig. 18.10.

---

* The name multivibrator is derived from the fact that a square wave actually consists of a large number of (fourier series analysis) sinusoidals of different frequencies.

The circuit operates in two states (*viz* ON and OFF) controlled by circuit conditions. Each amplifier stage supplies feedback to the other in such a manner that will drive the transistor of one stage to saturation (ON state) and the other to cut off (OFF state).

After a certain time controlled by circuit conditions, the action is reversed *i.e.* saturated stage is driven to cut off and the cut off stage is driven to saturation. The output can be taken across either stage and may be rectangular or square wave depending upon the circuit conditions.

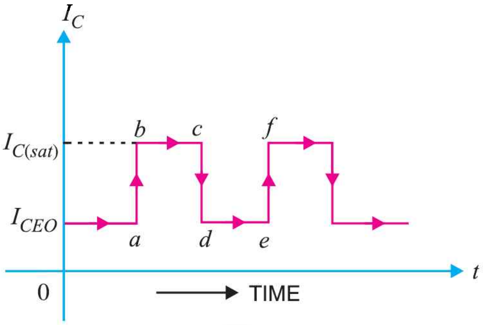


Fig. 18.11

Fig. 18.10 shows the block diagram of a multivibrator. It is a two-stage amplifier with 100% positive feedback. Suppose output is taken across the transistor Q_2. At any particular instant, one transistor is ON and conducts $I_{C(sat)}$ while the other is OFF. Suppose Q_2 is ON and Q_1 is OFF. The collector current in Q_2 will be $I_{C(sat)}$ as shown in Fig. 18.11. This condition will prevail for a time (*bc* in this case) determined by circuit conditions. After this time, transistor Q_2 is cut off and Q_1 is turned ON. The collector current in Q_2 is now I_{CEO} as shown. The circuit will stay in this condition for a time *de*. Again Q_2 is turned ON and Q_1 is driven to cut off. In this way, the output will be a square wave.

18.11 Types of Multivibrators

A multivibrator is basically a two-stage amplifier with output of one fedback to the input of the other. At any particular instant, one transistor is ON and the other is OFF. After a certain time depending upon the circuit components, the stages reverse their conditions – the conducting stage suddenly cuts off and the non-conducting stage suddenly starts to conduct. The two possible states of a multivibrator are :

	ON	**OFF**
First State	Q_1	Q_2
Second State	Q_2	Q_1

Depending upon the manner in which the two stages interchange their states, the multivibrators are classified as :

(*i*) Astable or free running multivibrator

(*ii*) Monostable or one-shot multivibrator

(*iii*) Bi-stable or flip-flop multivibrator

Fig. 18.12 shows the input/output relations for the three types of multivibrators.

(*i*) The astable or free running multivibrator alternates automatically between the two states and remains in each for a time dependent upon the circuit constants. Thus it is just an oscillator since it requires no external pulse for its operation. Of course, it does require a source of d.c. power. Because it continuously produces the square-wave output, it is often referred to as a *free running multivibrator*.

(*ii*) The monostable or one-shot multivibrator has one state stable and one quasi-stable (*i.e.* half-stable) state. The application of input pulse triggers the circuit into its quasi-stable state, in which it remains for a period determined by circuit constants. After this period of time, the circuit returns to its initial stable state, the process is repeated upon the application of each trigger pulse. Since the monostable multivibrator produces a single output pulse for each input trigger pulse, it is generally called *one-shot multivibrator*.

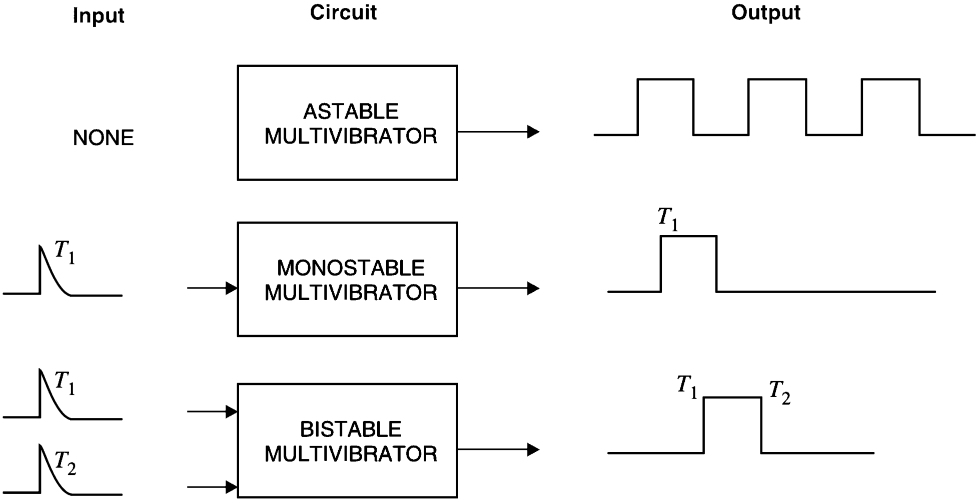


Fig. 18.12

(*iii*) The bistable multivibrator has both the two states stable. It requires the application of an external triggering pulse to change the operation from either one state to the other. Thus one pulse is used to generate half-cycle of square wave and another pulse to generate the next half-cycle of square wave. It is also known as a *flip-flop multivibrator* because of the two possible states it can assume.

18.12 Transistor Astable Multivibrator

A multivibrator which generates square waves of its own (i.e. without any external triggering pulse) is known as an **astable** *or* **free running multivibrator.**

The *astable multivibrator has no stable state. It switches back and forth from one state to the other, remaining in each state for a time determined by circuit constants. In other words, at first one transistor conducts (*i.e.* ON state) and the other stays in the OFF state for some time. After this period of time, the second transistor is automatically turned ON and the first transistor is turned OFF. Thus the multivibrator will generate a square wave output of its own. The width of the square wave and its frequency will depend upon the circuit constants.

Circuit details. Fig. 18.13 shows the circuit of a typical transistor astable multivibrator using two identical transistors Q_1 and Q_2. The circuit essentially consists of two symmetrical *CE* amplifier stages, each providing a feedback to the other. Thus collector loads of the two stages are equal *i.e.* $R_1 = R_4$ and the biasing resistors are also equal *i.e.* $R_2 = R_3$. The output of transistor Q_1 is coupled to the input of Q_2 through C_1 while the output of Q_2 is fed to the input of Q_1 through C_2. The square wave output can be taken from Q_1 or Q_2.

Operation. When V_{CC} is applied, collector currents start flowing in Q_1 and Q_2. In addition, the coupling capacitors C_1 and C_2 also start charging up. As the characteristics of no two transistors (*i.e.* β, V_{BE}) are *exactly* alike, therefore, one transistor, say Q_1, will conduct more rapidly than the other. The rising collector current in Q_1 drives its collector more and more positive. The increasing positive output at point A is applied to the base of transistor Q_2 through C_1. This establishes a reverse

---

* A means not. Hence astable means that it has no stable state.

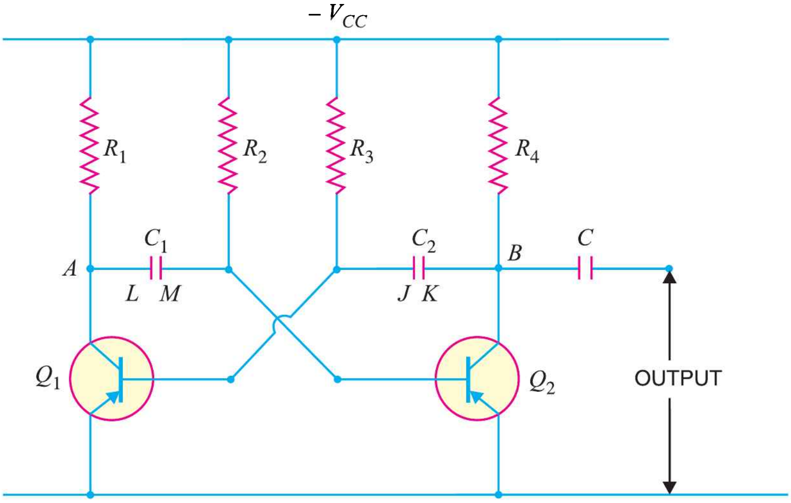


Fig. 18.13

bias on Q_2 and its collector current starts decreasing. As the collector of Q_2 is connected to the base of Q_1 through C_2, therefore, base of Q_1 becomes more negative *i.e.* Q_1 is more forward biased. This further increases the collector current in Q_1 and causes a further decrease of collector current in Q_2. This series of actions is repeated until the circuit drives Q_1 to saturation and Q_2 to cut off. These actions occur very rapidly and may be considered practically instantaneous. The output of Q_1 (ON state) is approximately zero and that of Q_2 (OFF state) is approximately V_{CC}. This is shown by *ab* in Fig. 18.14.

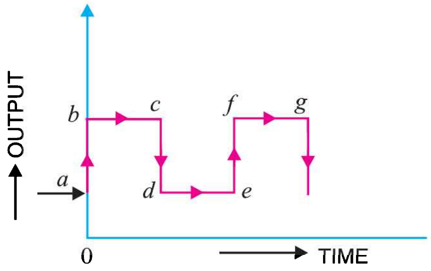


Fig. 18.14

When Q_1 is at saturation and Q_2 is cut off, the full voltage V_{CC} appears across R_1 and voltage across R_4 will be zero. The charges developed across C_1 and C_2 are sufficient to maintain the saturation and cut off conditions at Q_1 and Q_2 respectively. This condition is represented by time interval *bc* in Fig. 18.14. However, the capacitors will not retain the charges indefinitely but will discharge through their respective circuits. The discharge path for C_1, with plate L negative and Q_1 conducting, is $LAQ_1V_{CC}R_2M$ as shown in Fig. 18.15 (*i*).

The discharge path for C_2, with plate K negative and Q_2 cut off, is KBR_4R_3J as shown in Fig. 18.15 (*ii*). As the resistance of the discharge path for C_1 is lower than that of C_2, therefore, C_1 will discharge more rapidly.

As C_1 discharges, the base bias at Q_2 becomes less positive and at a time determined by R_2 and C_1, forward bias is re-established at Q_2. This causes the collector current to start in Q_2. The increasing positive potential at collector of Q_2 is applied to the base of Q_1 through the capacitor C_2. Hence the base of Q_1 will become more positive *i.e.* Q_1 is reverse biased. The decrease in collector current in Q_1 sends a negative voltage to the base of Q_2 through C_1, thereby causing further increase in the collector current of Q_2. With this set of actions taking place, Q_2 is quickly driven to saturation and Q_1 to cut off. This condition is represented by *cd* in Fig. 18.14. The period of time during which Q_2 remains at saturation and Q_1 at cut off is determined by C_2 and R_3.

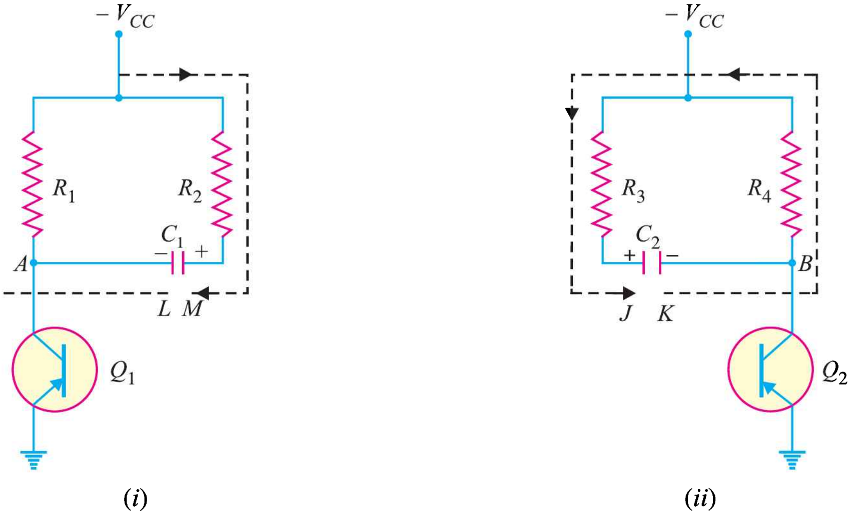


Fig. 18.15

ON or OFF time. The time for which either transistor remains ON or OFF is given by :

ON time for Q_1 (or OFF time for Q_2) is

$$T_1 = 0.694 R_2 C_1$$

OFF time for Q_1 (or ON time for Q_2) is

$$T_2 = 0.694 R_3 C_2$$

Total time period of the square wave is

$$T = T_1 + T_2 = 0.694\,(R_2 C_1 + R_3 C_2)$$

As $R_2 = R_3 = R$ and $C_1 = C_2 = C$,

$$\therefore \quad T = 0.694\,(RC + RC) \simeq 1.4\,RC \text{ seconds}$$

Frequency of the square wave is

$$f = \frac{1}{T} \simeq \frac{0.7}{RC} \text{Hz}$$

It may be noted that in these expressions, R is in ohms and C in farad.

Example 18.4. *In the astable multivibrator shown in Fig. 18.13, $R_2 = R_3 = 10\ k\Omega$ and $C_1 = C_2 = 0.01\ \mu F$. Determine the time period and frequency of the square wave.*

Solution.

Here $R = 10\text{ k}\Omega = 10^4\ \Omega;\ C = 0.01\ \mu\text{F} = 10^{-8}\text{ F}$

Time period of the square wave is

$$\begin{aligned} T &= 1.4\,RC = 1.4 \times 10^4 \times 10^{-8} \text{ second} \\ &= 1.4 \times 10^{-4} \text{ second} = 1.4 \times 10^{-4} \times 10^3 \text{ m sec} \\ &= \mathbf{0.14\ m\ sec} \end{aligned}$$

Frequency of the square wave is

$$\begin{aligned} f &= \frac{1}{T \text{ in second}} \text{Hz} = \frac{1}{1.4 \times 10^{-4}} \text{Hz} \\ &= 7 \times 10^3 \text{ Hz} = \mathbf{7\ kHz} \end{aligned}$$

18.13 Transistor Monostable Multivibrator

A multivibrator in which one transistor is always conducting (i.e. in the ON state) and the other is non-conducting (i.e. in the OFF state) is called a **monostable multivibrator.**

A *monostable multivibrator has only one state stable. In other words, if one transistor is conducting and the other is non-conducting, the circuit will remain in this position. It is only with the application of external pulse that the circuit will interchange the states. However, after a certain time, the circuit will automatically switch back to the original stable state and remains there until another pulse is applied. Thus a monostable multivibrator cannot generate square waves of its own like an astable multivibrator. Only external pulse will cause it to generate the square wave.

Circuit details. Fig. 18.16 shows the circuit of a transistor monostable multivibrator. It consists of two similar transistors Q_1 and Q_2 with equal collector loads *i.e.* $R_1 = R_4$. The values of V_{BB} and R_5 are such as to reverse bias Q_1 and keep it at cut off. The collector supply V_{CC} and R_2 forward bias Q_2 and keep it at saturation. The input pulse is given through C_2 to obtain the square wave. Again output can be taken from Q_1 or Q_2.

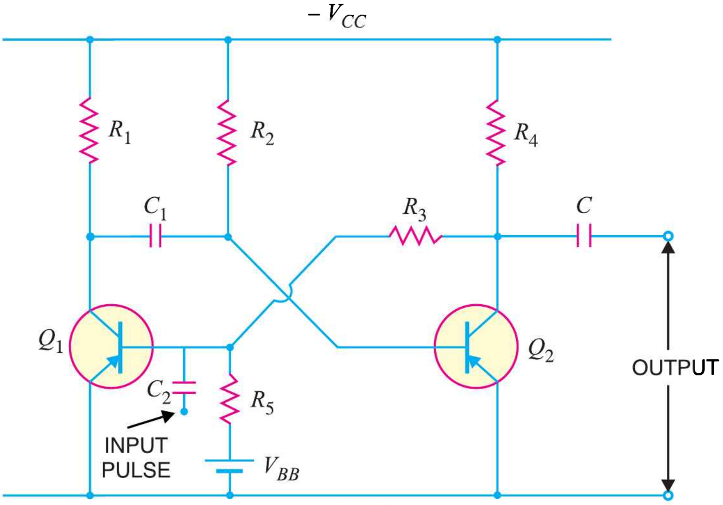
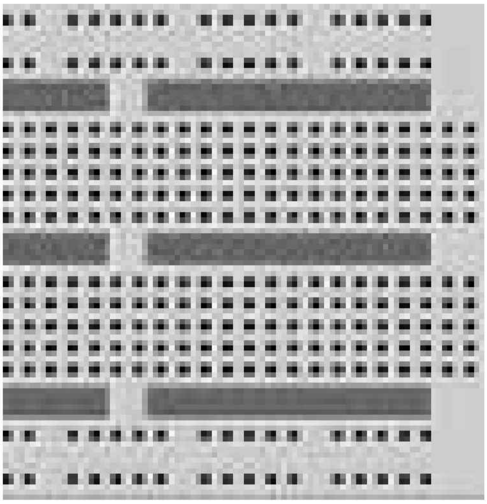


Fig. 18.16

Operation. With the circuit arrangement shown, Q_1 is at cut off and Q_2 is at saturation. This is the stable state for the circuit and it will continue to stay in this state until a triggering pulse is applied at C_2. When a negative pulse of short duration and sufficient magnitude is applied to the base of Q_1 through C_2, the transistor Q_1 starts conducting and positive potential is established at its collector. The positive potential at the collector of Q_1 is coupled to the base of Q_2 through capacitor C_1. This decreases the forward bias on Q_2 and its collector current decreases. The increasing negative potential on the collector of Q_2 is applied to the base of Q_1 through R_3. This further increases the forward bias on Q_1 and hence its collector current. With this set of actions taking place, Q_1 is quickly driven to saturation and Q_2 to cut off.



Monostable Multivibrator

---

* Mono means single.

With Q_1 at saturation and Q_2 at cut off, the circuit will come back to the original stage (*i.e.* Q_2 at saturation and Q_1 at cut off) after some time as explained in the following discussion. The capacitor C_1 (charged to approximately V_{CC}) discharges through the path $R_2 V_{CC} Q_1$. As C_1 discharges, it sends a voltage to the base of Q_2 to make it less positive. This goes on until a point is reached when forward bias is re-established on Q_2 and collector current starts to flow in Q_2. The step by step events already explained occur and Q_2 is quickly driven to saturation and Q_1 to cut off. This is the stable state for the circuit and it remains in this condition until another pulse causes the circuit to switch over the states.

18.14 Transistor Bistable Multivibrator

A multivibrator which has both the states stable is called a **bistable multivibrator.**

The bistable multivibrator has both the states stable. It will remain in whichever state it happens to be until a trigger pulse causes it to switch to the other state. For instance, suppose at any particular instant, transistor Q_1 is conducting and transistor Q_2 is at cut off. If left to itself, the bistable multivibrator will stay in this position forever. However, if an external pulse is applied to the circuit in such a way that Q_1 is cut off and Q_2 is turned on, the circuit will stay in the new position. Another trigger pulse is then required to switch the circuit back to its original state.

Circuit details. Fig. 18.17 shows the circuit of a typical transistor bistable multivibrator. It consists of two identical *CE* amplifier stages with output of one fed to the input of the other. The feedback is coupled through resistors (R_2, R_3) shunted by capacitors C_1 and C_2. The main purpose of capacitors C_1 and C_2 is to improve the switching characteristics of the circuit by passing the high frequency components of the square wave. This allows fast rise and fall times and hence distortionless square wave output. The output can be taken across either transistor.

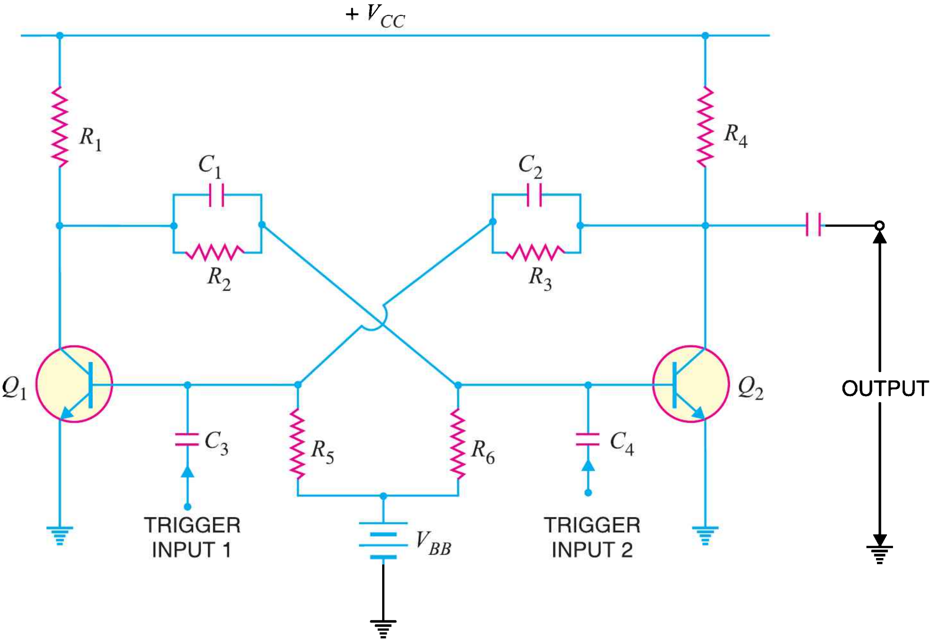


Fig. 18.17

Operation. When V_{CC} is applied, one transistor will start conducting slightly ahead of the other due to some differences in the characteristics of the transistors. This will drive one transistor to saturation and the other to cut off in a manner described for the astable multivibrator. Assume that Q_1 is turned ON and Q_2 is cut OFF. If left to itself, the circuit will stay in this condition. In order to switch the multivibrator to its other state, a trigger pulse must be applied. A negative pulse applied to the base of Q_1 through C_3 will cut it off or a positive pulse applied to the base of Q_2 through C_4 will cause it to conduct.

Suppose a negative pulse of sufficient magnitude is applied to the base of Q_1 through C_3. This will reduce the forward bias on Q_1 and cause a decrease in its collector current and an increase in collector voltage. The rising collector voltage is coupled to the base of Q_2 where it forward biases the base-emitter junction of Q_2. This will cause an increase in its collector current and decrease in collector voltage. The decreasing collector voltage is applied to the base of Q_1 where it further reverse biases the base-emitter junction of Q_1 to decrease its collector current. With this set of actions taking place, Q_2 is quickly driven to saturation and Q_1 to cut off. The circuit will now remain stable in this state until a negative trigger pulse at Q_2 (or a positive trigger pulse at Q_1) changes this state.

18.15 Differentiating Circuit

A circuit in which output voltage is directly proportional to the derivative of the input is known as a **differentiating circuit.**

$$\text{Output} \propto \frac{d}{dt}(\text{Input})$$

A differentiating circuit is a simple RC series circuit with output taken across the resistor R. The circuit is suitably designed so that output is proportional to the derivative of the input. Thus if a d.c. or constant input is applied to such a circuit, the output will be zero. It is because the derivative of a constant is zero.

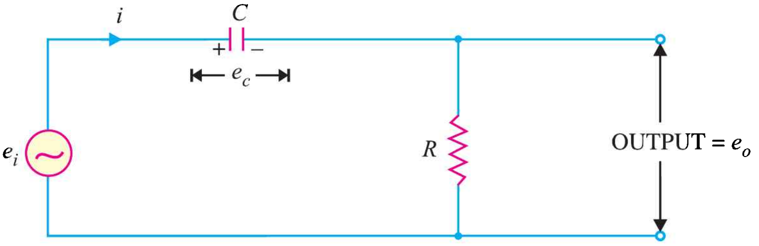


Fig. 18.18

Fig. 18.18 shows a typical differentiating circuit. The output across R will be the derivative of the input. It is important to note that merely using voltage across R does not make the circuit a differentiator; it is also necessary to set the proper circuit values. In order to achieve good differentiation, the following two conditions should be satisfied :

(*i*) The time constant RC of the circuit should be much smaller than the time period of the input wave.

(*ii*) The value of X_C should be 10 or more times larger than R at the operating frequency.

Fulfilled these conditions, the output across R in Fig. 18.18 will be the derivative of the input.

Let e_i be the input alternating voltage and let i be the resulting alternating current. The charge q on the capacitor at any instant is

$$q = C\,e_c$$

Now
$$i = \frac{dq}{dt} = \frac{d}{dt}(q) = \frac{d}{dt}(C\,e_c)$$

or $$i = C\frac{d}{dt}(e_c)$$

Since the capacitive reactance is very much larger than R, the input voltage can be considered equal to the capacitor voltage with negligible error *i.e.* $e_c = e_i$.

$$\therefore \quad i = C\frac{d}{dt}(e_i)$$

$$\text{Output voltage, } e_o = iR$$

$$= RC\frac{d}{dt}(e_i)$$

$$\propto \frac{d}{dt}(e_i) \qquad (\because RC \text{ is constant})$$

$$\therefore \quad \text{Output voltage} \propto \frac{d}{dt}(\text{Input})$$

Output waveforms. The output waveform from a differentiating circuit depends upon the time constant and shape of the input wave. Three important cases will be considered.

(*i*) **When input is a square wave.** When the input fed to a differentiating circuit is a square wave, output will consist of sharp narrow pulses as shown in Fig. 18.19. During the *OC* part of input wave, its amplitude changes abruptly and hence the differentiated wave will be a sharp narrow pulse as shown in Fig. 18.19. However, during the constant part *CB* of the input, the output will be zero because the derivative of a constant is zero.

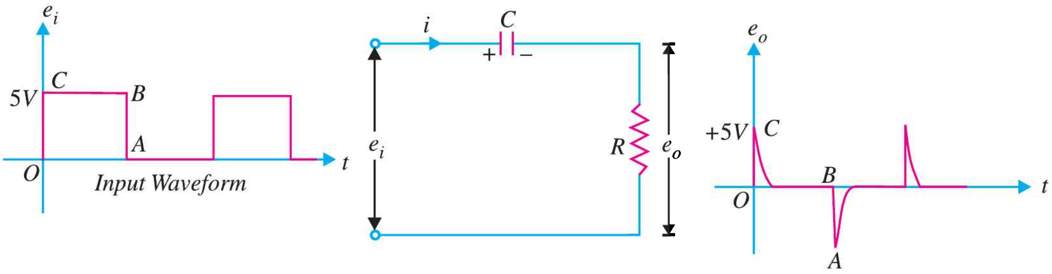


Fig. 18.19

Let us look at the physical explanation of this behaviour of the circuit. Since time constant *RC* of the circuit is very small *w.r.t.* time period of input wave and $X_C >> R$, the capacitor will become fully charged during the early part of each half-cycle of the input wave. During the remainder part of the half-cycle, the output of the circuit will be zero because the capacitor voltage (e_c) neutralises the input voltage and there can be no current flow through *R*. Thus we shall get sharp pulse at the output during the start of each half-cycle of input wave while for the remainder part of the half-cycle of input wave, the output will be zero. In this way, a symmetrical output wave with sharp positive and negative peaks is produced. Such pulses are used in many ways in electronic circuits *e.g.* in television transmitters and receivers, in multivibrators to initiate action etc.

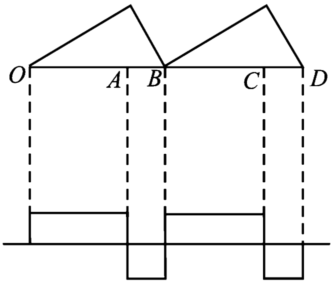


Fig. 18.20

(*ii*) **When input is a triangular wave.** When the input fed to a differentiating circuit is a triangular wave, the output will be a rectangular wave as shown in Fig. 18.20. During the period *OA* of the input wave, its amplitude changes at a constant rate and, therefore, the differentiated wave has a constant value for each constant rate of change. During the period *AB* of the input wave, the change is less abrupt so that the output will be a very narrow pulse of rectangular form. Thus when a triangular wave is fed to a differentiating circuit, the output consists of a succession of rectangular waves of equal or unequal duration depending upon the shape of the input wave.

(*iii*) When input is a sine wave. A sine wave input becomes a cosine wave and a cosine wave input becomes an inverted sine wave at the output.

Example 18.5. (*i*) *What is the effect of time constant of an RC circuit on the differentiated wave?*

(*ii*) *Sketch the output waveform from the differentiating circuit when input is square wave for* $T = 100\,RC$, $T = 10\,RC$, $T = RC$.

Solution.

(*i*) In an *RC* differentiating circuit, the output voltage is taken across *R* and the waveform of the output depends upon the time constant of the circuit. The circuit will function as a differentiator if the product *RC* is many times smaller than the time period of the input wave.

(*ii*) Square wave input. Fig. 18.21 shows the input square wave fed to a differentiating circuit. Fig. 18.22 shows the output waveforms for different values of time period of the input wave.

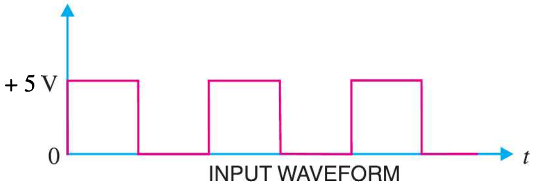


Fig. 18.21

It may be noted that *RC* coupling circuit is the same as a differentiating circuit except that it has a long time constant—in excess of 5 *RC*. Therefore, a coupling circuit does not noticeably differentiate the input wave.

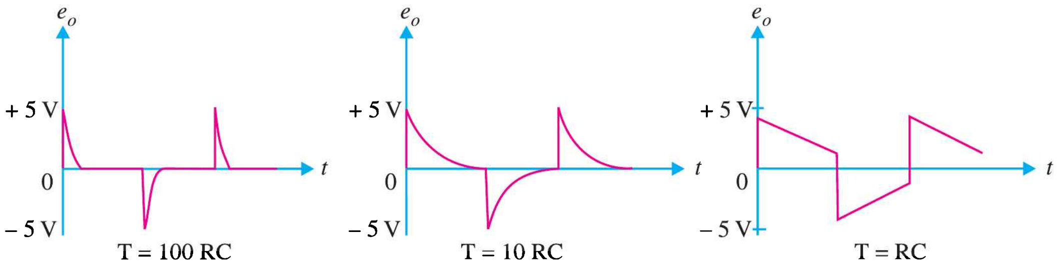


Fig. 18.22

Example 18.6. *In a differentiating circuit, R = 10 kΩ and C = 2.2 μF. If the input voltage goes from 0 V to 10 V at a constant rate in 0.4 s, determine the output voltage.*

Solution.

$$e_o = RC\frac{d}{dt}(e_i) = RC\frac{de_i}{dt} \quad \text{... See Art. 18.15}$$

Here $R = 10\text{ k}\Omega\ ;\ C = 2.2\ \mu\text{F}\ ;\ \dfrac{de_i}{dt} = \dfrac{10-0}{0.4} = 25\text{ V/s}$

$\therefore \quad e_o = (10 \times 10^3) \times (2.2 \times 10^{-6}) \times 25 = \mathbf{0.55\ V}$

18.16 Integrating Circuit

A circuit in which output voltage is directly proportional to the integral of the input is known as an **integrating circuit** *i.e.*

$$\text{Output} \propto \int \text{Input}$$

An integrating circuit is a simple *RC* series circuit with output taken across the capacitor *C* as shown in Fig. 18.23. It may be seen that *R* and *C* of the differentiating circuit have changed places. In order that the circuit renders good integration, the following conditions should be fulfilled :

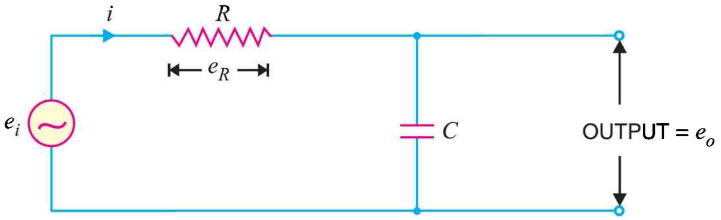


Fig. 18.23

(*i*) The time constant *RC* of the circuit should be very large as compared to the time period of the input wave.

(*ii*) The value of *R* should be 10 or more times larger than X_C.

Let e_i be the input alternating voltage and let *i* be the resulting alternating current. Since *R* is very large as compared to capacitive reactance X_C of the capacitor, it is reasonable to assume that voltage across *R* (*i.e.* e_R) is equal to the input voltage *i.e.*

$$e_i = e_R$$

Now $$i = \frac{e_R}{R} = \frac{e_i}{R}$$

The charge *q* on the capacitor at any instant is

$$q = \int i\,dt$$

$$\text{Output voltage, } e_o = \frac{q}{C} = \frac{\int i\,dt}{C}$$

$$= \frac{\int \frac{e_i}{R}\,dt}{C} \qquad \left(\because i = \frac{e_i}{R}\right)$$

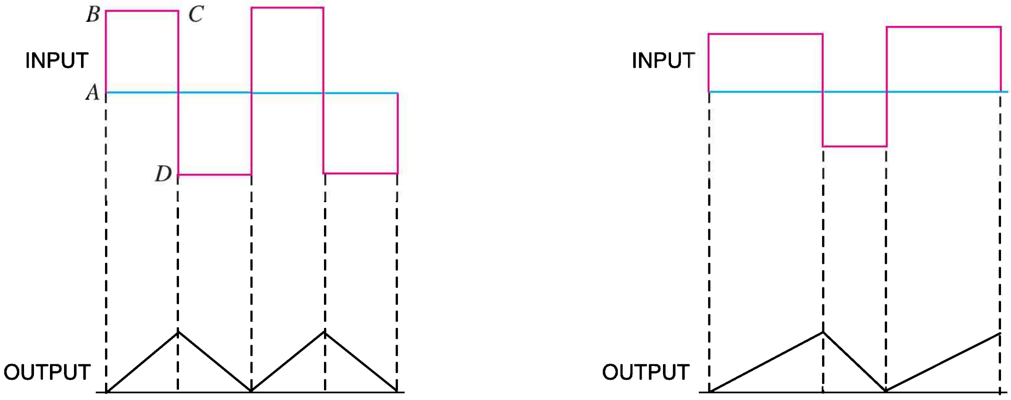
$$= \frac{1}{RC}\int e_i\,dt$$

$$\propto \int e_i\,dt \qquad (\because RC \text{ is constant})$$

$$\therefore \quad \text{Output voltage} \propto \int \text{Input}$$

Output waveforms. The output waveform from an integrating circuit depends upon time constant and shape of the input wave. Two important cases will be discussed :

(*i*) **When input is a square wave.** When the input fed to an integrating circuit is a square wave, the output will be a triangular wave as shown in Fig. 18.24 (*i*). As integration means summation, therefore, output from an integrating circuit will be the sum of all the input waves at any instant. This sum is zero at *A* and goes on increasing till it becomes maximum at *C*. After this, the summation goes on decreasing to the onset of negative movement *CD* of the input.



(*i*) (*ii*)

Fig. 18.24

(*ii*) **When input is rectangular wave.** When the input fed to an integrating circuit is a rectangular wave, the output will be a triangular wave as shown in Fig. 18.24 (*ii*).

18.17 Important Applications of Diodes

We have seen that diodes can be used as rectifiers. Apart from this, diodes have many other applications. However, we shall confine ourselves to the following two applications of diodes :

(*i*) as a clipper (*ii*) as a clamper

A clipper (or limiter) is used to clip off or remove a portion of an a.c. signal. The half-wave rectifier is basically a clipper that eliminates one of the alternations of an a.c. signal.

A clamper (or *dc* restorer) is used to restore or change the *dc* reference of an *ac* signal. For example, you may have a 10 V_{pp} *ac* signal that varies equally above and below 2 V *dc*.

18.18 Clipping Circuits

The circuit with which the waveform is shaped by removing (or clipping) a portion of the applied wave is known as a **clipping circuit.**

Clippers find extensive use in radar, digital and other electronic systems. Although several clipping circuits have been developed to change the wave shape, we shall confine our attention to diode clippers. These clippers can remove signal voltages above or below a specified level. The important diode clippers are (*i*) positive clipper (*ii*) biased clipper (*iii*) combination clipper.

(*i*) **Positive clipper.** A positive clipper is that which removes the positive half-cycles of the input voltage. Fig. 18.25 shows the typical circuit of a positive clipper using a diode. As shown, the output voltage has all the positive half-cycles removed or clipped off.

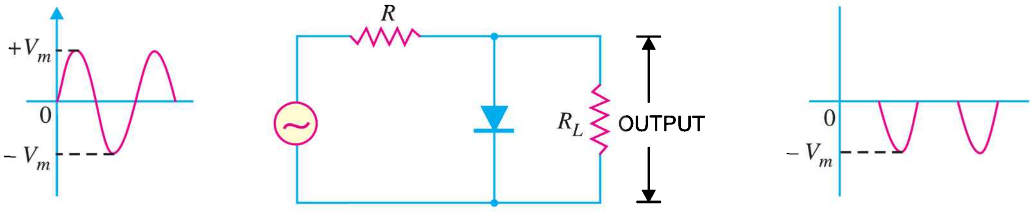


Fig. 18.25

The circuit action is as follows. During the positive half-cycle of the input voltage, the diode is forward biased and conducts heavily. Therefore, the voltage across the diode (which behaves as a short) and hence across the load R_L is zero. Hence *output voltage during positive half-cycles is zero.

During the negative half-cycle of the input voltage, the diode is reverse biased and behaves as an open. In this condition, the circuit behaves as a voltage divider with an output given by :

$$\text{Output voltage} = -\frac{R_L}{R + R_L} V_m$$

Generally, R_L is much greater than R.

$$\therefore \qquad \text{Output voltage} = -V_m$$

It may be noted that if it is desired to remove the negative half-cycle of the input, the only thing to be done is to reverse the polarities of the diode in the circuit shown in Fig. 18.25. Such a clipper is then called a *negative clipper*.

(*ii*) **Biased clipper.** Sometimes it is desired to remove a small portion of positive or negative half-cycle of the signal voltage. For this purpose, biased clipper is used. Fig. 18.26 shows the circuit of a biased clipper using a diode with a battery of V volts. With the polarities of battery shown, a portion of each positive half-cycle will be clipped. However, the negative half-cycles will appear as such across the load. Such a clipper is called *biased positive clipper*.

The circuit action is as follows. The diode will conduct heavily so long as input voltage is greater than $+V$. When input voltage is greater than $+V$, the diode behaves as a short and the output equals $+V$. The output will stay at $+V$ so long as the input voltage is greater than $+V$. During the period the input voltage is less than $+V$, the diode is reverse biased and behaves as an open. Therefore, most of the input voltage appears across the output. In this way, the biased positive clipper removes input voltage above $+V$.

During the negative half-cycle of the input voltage, the diode remains reverse biased. Therefore, almost entire negative half-cycle appears across the load.

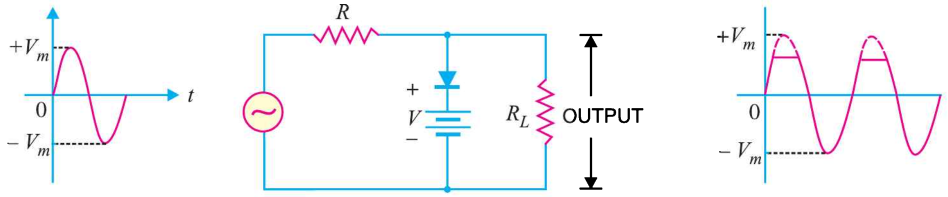


Fig. 18.26

If it is desired to clip a portion of negative half-cycles of input voltage, the only thing to be done is to reverse the polarities of diode or battery. Such a circuit is then called a *biased negative clipper*.

(*iii*) **Combination clipper.** It is a combination of biased positive and negative clippers. With a combination clipper, a portion of both positive and negative half-cycles of input voltage can be removed or clipped as shown in Fig. 18.27.

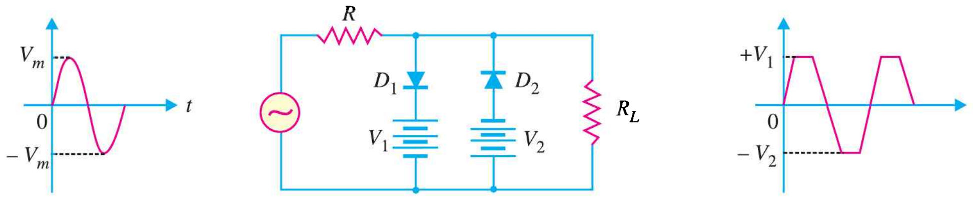


Fig. 18.27

---

* It may be noted that all the input voltage during this half-cycle is dropped across R.

The circuit action is as follows. When positive input voltage is greater than $+V_1$, diode D_1 conducts heavily while diode D_2 remains reverse biased. Therefore, a voltage $+V_1$ appears across the load. This output stays at $+V_1$ so long as the input voltage exceeds $+V_1$. On the other hand, during the negative half-cycle, the diode D_2 will conduct heavily and the output stays at $-V_2$ so long as the input voltage is greater than $-V_2$. Note that $+V_1$ and $-V_2$ are less than $+V_m$ and $-V_m$ respectively.

Between $+V_1$ and $-V_2$ neither diode is on. Therefore, in this condition, most of the input voltage appears across the load. It is interesting to note that this clipping circuit can give square wave output if V_m is much greater than the clipping levels.

Example 18.7. *For the negative series clipper shown in Fig.18.28, what is the peak output voltage from the circuit ?*

Solution. When the diode is connected in series with the load, it is called a series clipper. Since it is a negative clipper, it will remove negative portion of input a.c. signal.

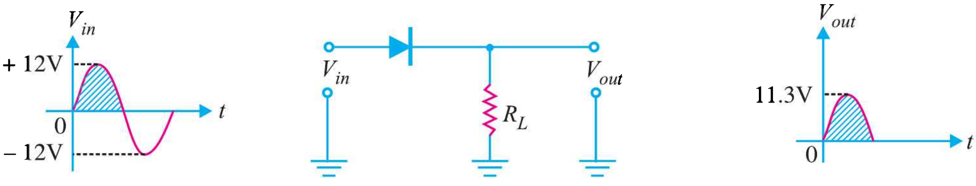


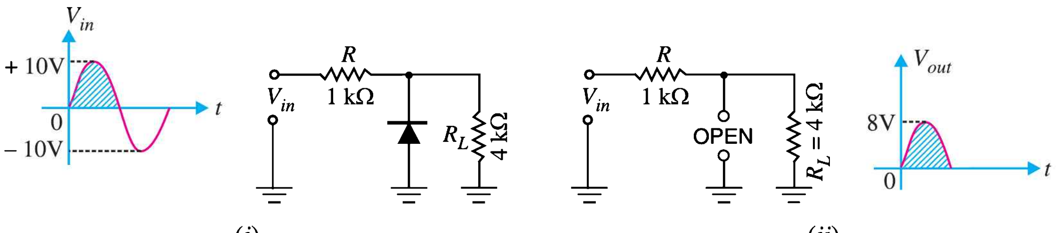
Fig. 18.28

During the positive half-cycle of input signal, the dioide is forward biased. As a result, the diode will conduct. The output voltage is

$$V_{out\,(peak)} = V_{in\,(peak)} - 0.7 = 12 - 0.7 = \mathbf{11.3\ V}$$

During the negative half-cycle of input signal, the diode is reverse biased and consequently it will not conduct. Therefore, $V_{out} = 0$. Note that under this condition, the entire input voltage will appear across the diode.

Example 18.8. *The negative shunt clipper shown in Fig. 18.29 (i) has a peak input voltage of + 10 V. What is the peak output voltage from this circuit ?*



(*i*) (*ii*)

Fig. 18.29

Solution. When the diode is connected in parallel with the load, it is called a shunt clipper. During the positive half-cycle of input ac signal, the diode is reverse biased and it will behave as an open. This is shown in Fig. 18.29 (*ii*). With diode as an open,

$$V_{out\,(peak)} = \text{Peak voltage across } R_L$$

$$= \frac{R_L}{R + R_L} V_{in\,(peak)} = \frac{4}{1+4} \times 10 = \mathbf{8V}$$

Note that peak output voltage is somewhat less than the peak input voltage.

Example 18.9. *In example 18.8, what will be the output voltage and voltage across R when the input voltage is −10 V ?*

Solution. During the negative half-cycle of input signal, the diode is forward biased. Therefore, diode can be replaced by its simplified equivalent circuit as shown in Fig. 18.30. Since load is connected in parallel with the diode,

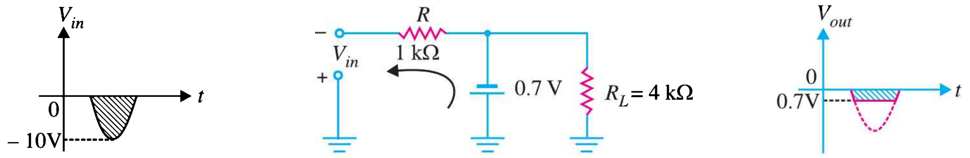

V_{in}
t
0
− 10V
R
−
V_{in}
+
1 kΩ
0.7 V
R_L = 4 kΩ
V_{out}
0
0.7V
t

Fig. 18.30

$$\therefore \qquad V_{out} = \mathbf{-0.7\ V}$$

$$\text{Voltage across } R,\ V_R = (-10) - (-0.7) = -10 + 0.7 = \mathbf{-9.3\ V}$$

Example 18.10. *The positive shunt clipper shown in Fig. 18.31 has the input waveform as indicated. Determine the value of V_{out} for each of the input alternations.*

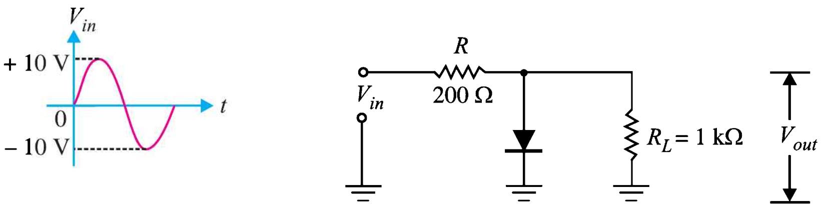

V_{in}
+ 10 V
0
− 10 V
t
R
200 Ω
V_{in}
R_L = 1 kΩ
V_{out}

Fig. 18.31

Solution.

Positive half-cycle. During the positive half-cycle of the input ac signal, the diode is forward biased. Therefore, diode can be replaced by its simplified equivalent circuit as shown in Fig. 18.32. Since the load is connected in parallel with the diode,

$$\therefore \qquad V_{out} = \mathbf{0.7\ V}$$

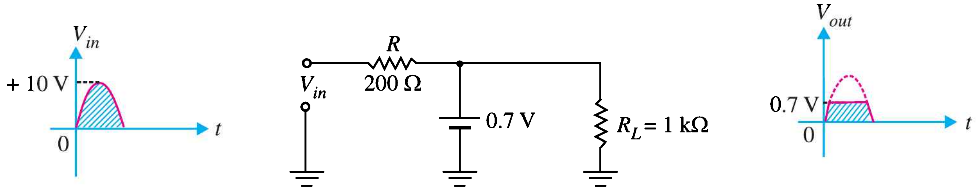

V_{in}
+ 10 V
0
t
R
200 Ω
V_{in}
0.7 V
R_L = 1 kΩ
V_{out}
0.7 V
0
t

Fig. 18.32

Negative half-cycle. During the negative half-cycle of the input a.c. signal, the diode is reverse biased and it conducts no current. Therefore, the diode will behave as an open as shown in Fig. 18.33.

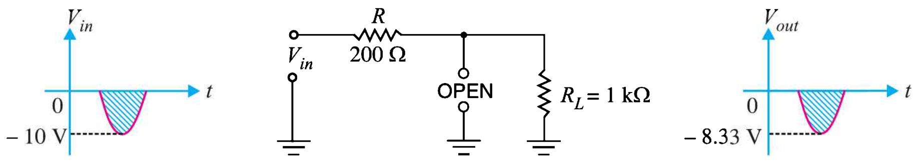

V_{in}
0
− 10 V
t
R
200 Ω
V_{in}
OPEN
R_L = 1 kΩ
V_{out}
0
− 8.33 V
t

Fig. 18.33

$$\therefore \qquad V_{out(peak)} = \frac{R_L}{R + R_L} V_{in(peak)}$$

$$= \left(\frac{1000}{200 + 1000}\right)(-10\text{ V}) = \mathbf{-8.33\text{ V}}$$

Again the peak output voltage is somewhat less than the peak input voltage.

Example 18.11. *In Fig. 18.31, what is the purpose of using the series resistance R ?*

Solution. The purpose of series resistance R is to protect the diode from damage. Let us explain this point. Suppose the series resistance R is not in the circuit. The circuit then becomes as shown in Fig. 18.34.

During the positive half-cycle of the input signal, the diode is forward biased. Since series resistance R is not present, it is easy to see that the diode will short the signal source to the ground. As a result, excessive current will flow through the diode as well as through the signal source. This large current may damage/destroy either the diode or the signal source.

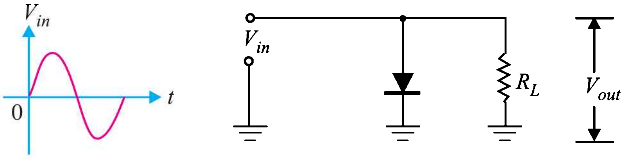


Fig. 18.34

Note. The series resistance R protects the diode and signal source when diode is forward biased. However, the presence of this resistance affects the output voltage to a little extent. It is because in a practical clipper circuit, the value of R is much lower than R_L. Consequently, output voltage will be approximately equal to V_{in} when the diode is reverse biased.

Example 18.12. *For the input wave to the clipping circuit shown in Fig. 18.35, find the output waveform.*

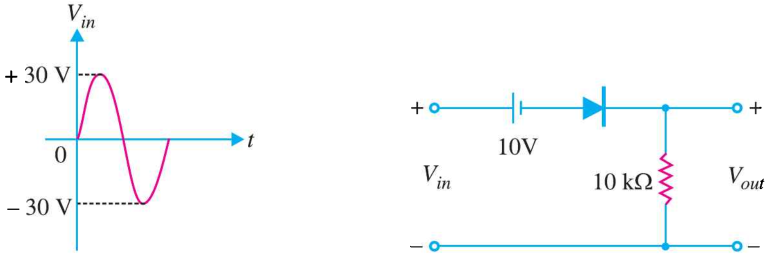
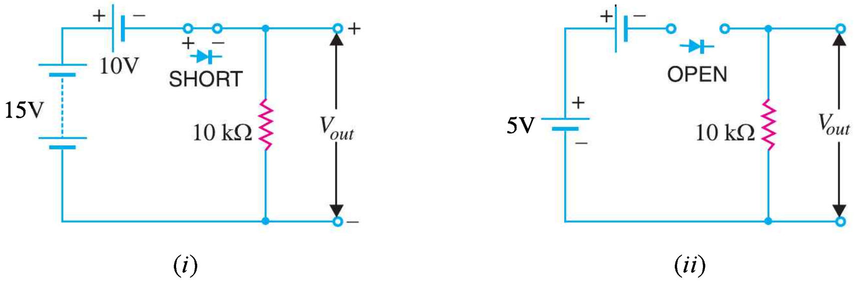


Fig. 18.35

Solution. For any value of $V_{in} > 10\text{V}$, the ideal diode is forward biased and $V_{out} = V_{in} - 10$. For example, at $V_{in} = 15\text{V}$ [See Fig. 18.36 (*i*)], $V_{out} = 15 - 10 = 5\text{V}$.



(*i*) (*ii*)

Fig. 18.36

For any value of $V_{in} < 10$V, the ideal diode is reverse biased. Therefore, circuit current is zero and hence $V_{out} = 0$. For example, with $V_{in} = 5$V [See Fig. 18.36 (*ii*)], $V_{out} = 0$ and V_d (drop across diode) = 5V

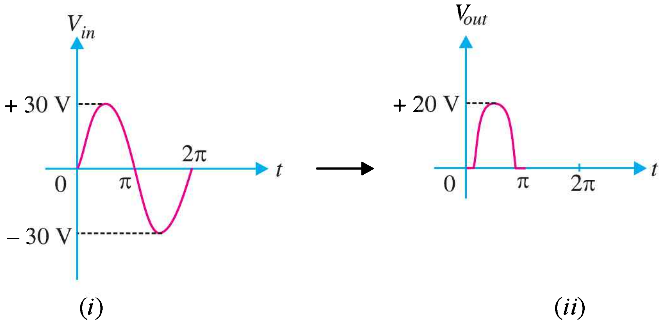


Fig. 18.37

The output waveform will be as shown in Fig. 18.37 (*ii*).

Example 18.13. *For the input wave to the clipping circuit in Fig. 18.38, find the output waveform.*

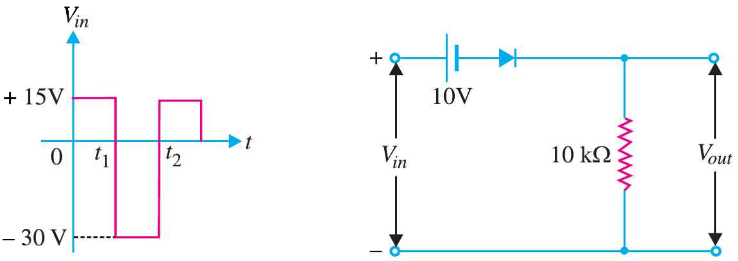


Fig. 18.38

Solution. For any value of $V_{in} > 10$V, the ideal diode is forward biased and $V_{out} = V_{in} - 10$. For any value of $V_{in} < 10$V, the ideal diode is reverse biased and $V_{out} = 0$.

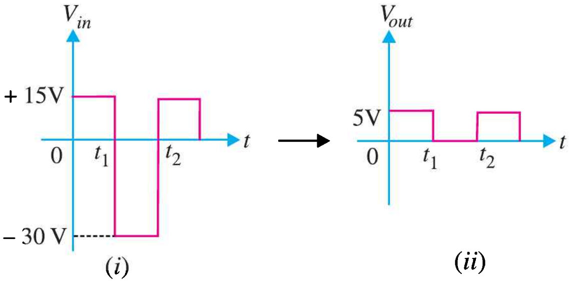


Fig. 18.39

The output waveform will be as shown in Fig. 18.39 (*ii*).

Example 18.14. *For the input waveform to the clipping circuit in Fig. 18.40, find the output voltage waveform.*

Solution. The battery of 5V reverse biases the diode. The point *A must go positive to 5V before the diode turns on. For all voltages at point A equal to or greater than 5V, the diode conducts and the output voltage stays at 5V. For all negative voltages at A and positive voltages less than 5V, the diode is reverse biased. When reverse biased, the diode acts like an open circuit and $V_{out} = V_{in}$. Thus circuit in Fig. 18.40 is an adjustable positive peak clipper that clips all positive peaks greater than battery voltage (*i.e.* 5V).

---

* Assuming the diode to be ideal. Actually point A must go positive to 5.6V before the diode turns on. Here 0.6V accounts for potential barrier.

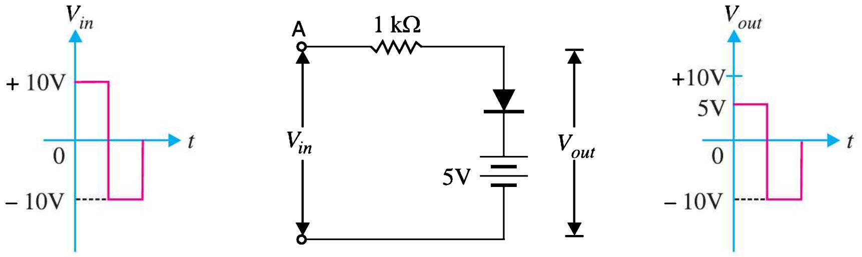


Fig. 18.40

Example 18.15. *For the input wave to the symmetrical clipper shown in Fig. 18.41, find the output voltage waveform. Assume that the barrier voltage of each diode is 0.6V.*

Solution. Fig. 18.41 shows the symmetrical clipper.

(*i*) Diode D_1 is reverse biased for all positive inputs and negative inputs less than 0.6V. Diode D_2 is reverse biased for all negative inputs and positive inputs less than 0.6V.

(*ii*) For all positive inputs greater than 0.6V, D_2 is forward biased and output voltage stays at 0.6V. For all negative inputs greater than –0.6V, D_1 is forward biased and output stays at – 0.6V.

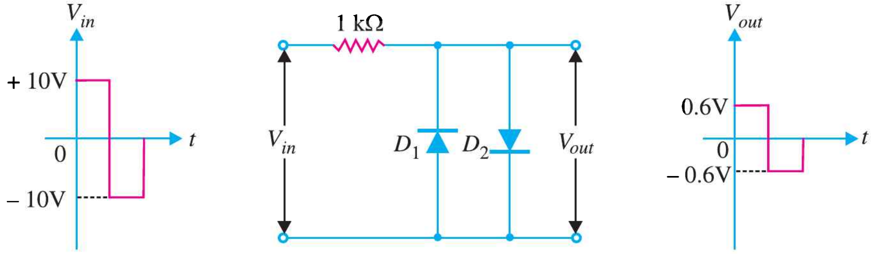


Fig. 18.41

Thus for the input voltage waveform, the output voltage varies between – 0.6V and 0.6V. This circuit is sometimes used to convert a sine-wave input to a reasonably square-wave output signal.

Example 18.16. *Fig. 18.42 shows a zener shunt clipper with sine wave input. Determine the output waveform.*

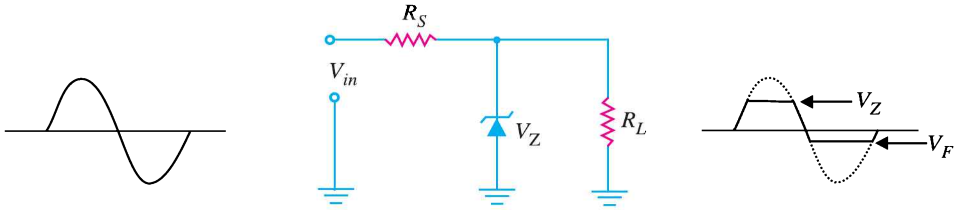


Fig. 18.42

Solution. The *zener shunt clipper* uses a zener diode in place of the ordinary diode. The zener shunt clipper uses both the forward and reverse characteristics of the zener diode. Thus when the zener diode is forward biased, this clipper acts just like the standard shunt clipper.

When the input signal in Fig. 18.42 goes positive, the zener is reverse biased. Therefore, the zener diode will remain OFF until the value of V_{in} reaches the value of V_Z. At that time, the zener diode will turn ON, clipping the input signal. As long as V_{in} is greater than V_Z, the zener will remain ON and the output voltage is

$$V_{out} = V_Z$$

When the input signal goes negative, the zener is forward biased. Therefore, the zener is clipped off at 0.7 V.

Example 18.17. *Fig. 18.43 shows a symmetrical zener shunt clipper with sine wave input. Determine the output waveform.*

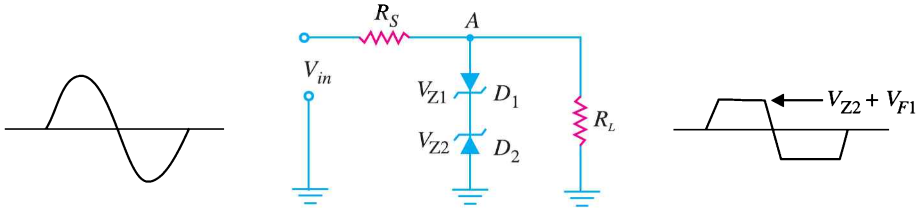


Fig. 18.43

Solution. The *symmetrical zener clipper* uses two zener diodes that are connected as shown in Fig. 18.43. When the input is positive, D_1 is forward biased and D_2 is reverse biased (assuming that the value of V_{in} is high enough to turn both diodes ON). When both diodes are conducting, the voltage from point A to ground will be equal to the sum of V_{Z2} and the forward voltage drop of D_1 *i.e.*, $V_{F1} = 0.7\text{V}$.

$$\therefore \quad V_{out} = V_{Z2} + V_{F1} = V_{Z2} + 0.7\text{V}$$

When the input is negative, D_1 is reverse biased and D_2 is forward biased. The output voltage in this case is

$$V_{out} = -V_{Z1} - V_{F2} = -(V_{Z1} + 0.7\text{V})$$

In practice, the two zeners have the same voltage rating *i.e.* $V_{Z1} = V_{Z2} = V_Z$.

$$\therefore \quad V_{out} = \pm(V_Z + 0.7\text{V})$$

18.19 Applications of Clippers

There are numerous clipper applications and it is not possible to discuss all of them. However, in general, clippers are used to perform one of the following two functions :

(*i*) Changing the shape of a waveform

(*ii*) Circuit transient protection

(*i*) **Changing the shape of waveform.** Clippers can alter the shape of a waveform. For example, a clipper can be used to convert a sine wave into a rectangular wave, square wave etc. They can limit either the negative or positive alternation or both alternations of an a.c. voltage.

(*ii*) **Circuit Transient protection.** *Transients can cause considerable damage to many types of circuits *e.g.*, a digital circuit. In that case, a clipper diode can be used to prevent the transient form reaching that circuit.

---

* A transient is a sudden current or voltage rise that has an extremely short duration.

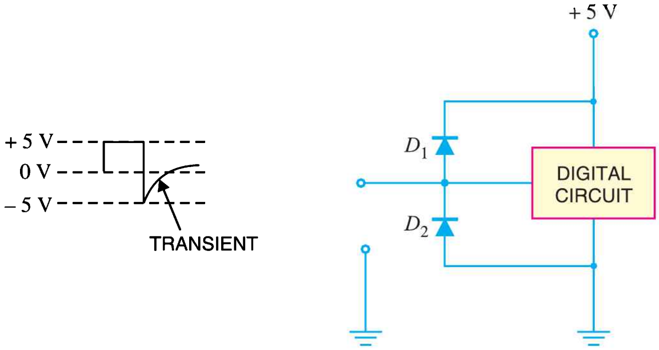


Fig. 18.44

Fig. 18.44 shows the protection of a typical digital circuit against transients by the diode clipper. When the transient shown in Fig. 18.44 occurs on the input line, it causes diode D_2 to be forward biased. The diode D_2 will conduct; thus shorting the transient to the ground. Consequently, the input of the circuit is protected from the transient.

18.20 Clamping Circuits

A circuit that places either the positive or negative peak of a signal at a desired d.c. level is known as a **clamping circuit.**

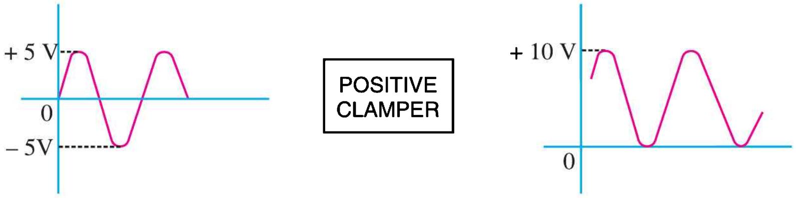


Fig. 18.45

A clamping circuit (or a clamper) essentially adds a *d.c.* component to the signal. Fig. 18.45 shows the key idea behind clamping. The input signal is a sine wave having a peak-to-peak value of 10 V. The clamper adds the *d.c.* component and pushes the signal upwards so that the negative peaks fall on the zero level. As you can see, the waveform now has peak values of +10 V and 0 V.

It may be seen that the shape of the original signal has not changed; only there is vertical shift in the signal. Such a clamper is called a *positive clamper*. The *negative clamper* does the reverse *i.e.* it pushes the signal downwards so that the positive peaks fall on the zero level.

The following points may be noted carefully :

(*i*) The clamping circuit does not change the peak-to-peak or r.m.s. value of the waveform. Thus referring to Fig. 18.45 above, the input waveform and clamped output have the same peak-to-peak value *i.e.*, 10 V in this case. If you measure the input voltage and clamped output with an a.c. voltmeter, the readings will be the same.

(*ii*) A clamping circuit changes the peak and average values of a waveform. This point needs explanation. Thus in the above circuit, it is easy to see that input waveform has a peak value of 5 V and average value over a cycle is zero. The clamped output varies between 10 V and 0 V. Therefore, the peak value of clamped output is 10 V and *average value is 5 V. Hence we arrive at a very important conclusion that *a clamper changes the peak value as well as the average value of a waveform.*

---

* Average value (or *dc* value) $= \dfrac{10 + 0}{2} = 5$ V

18.21 Basic Idea of a Clamper

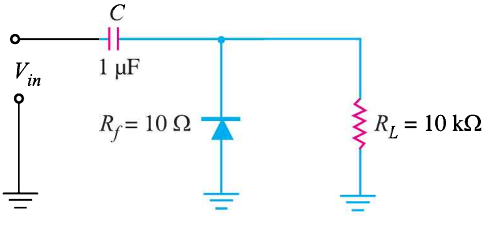


Fig. 18.46

A clamping circuit should not change peak-to-peak value of the signal; it should only change the *dc* level. To do so, a clamping circuit uses a capacitor, together with a diode and a load resistor R_L. Fig. 18.46 shows the circuit of a positive clamper. *The operation of a clamper is based on the principle that charging time of a capacitor is made very small as compared to its discharging time.* Thus referring to Fig. 18.46,

$$\text{*Charging time constant, } \tau = R_f C = (10\ \Omega) \times (10^{-6}\ \text{F}) = 10\ \mu\text{s}$$

$$\text{Total charging time, } \tau_C = \text{**}5R_f C = 5 \times 10 = 50\ \mu\text{s}$$

$$\text{***Discharging time constant, } \tau = R_L\, C = (10 \times 10^3) \times (1 \times 10^{-6}) = 10\ \text{ms}$$

$$\text{Total discharging time, } \tau_D = 5\, R_L\, C = 5 \times 10 = 50\ \text{ms}$$

It may be noted that charging time (*i.e.*, 50 μs) is very small as compared to the discharging time (*i.e.*, 50 ms). This is the basis of clamper circuit operation. In a practical clamping circuit, the values of C and R_L are so chosen that discharging time is very large.

18.22 Positive Clamper

Fig. 18.47 shows the circuit of a †positive clamper. The input signal is assumed to be a square wave with time period T. The clamped output is obtained across R_L. The circuit design incorporates two main features. Firstly, the values of C and R_L are so selected that time constant $\tau = CR_L$ is very large. This means that voltage across the capacitor will not discharge significantly during the interval the diode is non-conducting. Secondly, $R_L C$ time constant is deliberately made much greater than the time period T of the incoming signal.

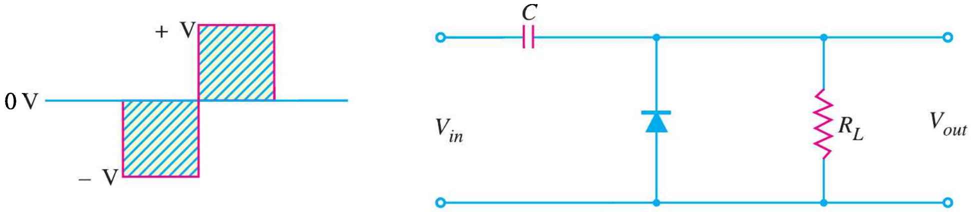


Fig. 18.47

Operation

(*i*) During the negative half-cycle of the input signal, the diode is forward biased. Therefore, the diode behaves as a short as shown in Fig. 18.48. The charging time constant (= CR_f, where R_f= forward resistance of the diode) is very small so that the capacitor will charge to V volts very quickly. It is easy to see that during this interval, the output voltage is directly across the short circuit. Therefore, $V_{out} = 0$.

---

* When diode is forward biased.

** From the knowledge of electrical engineering, we know that charging time of a capacitor is ≃ 5 *RC*.

*** When diode is reverse biased.

† If you want to determine what type of clamper you are dealing with, here is an easy memory trick. If the diode is pointing up (away from ground), the circuit is a positive clamper. On the other hand, if diode is pointing down (towards ground), the circuit is a negative clamper.

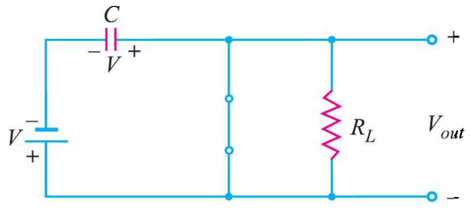


Fig. 18.48

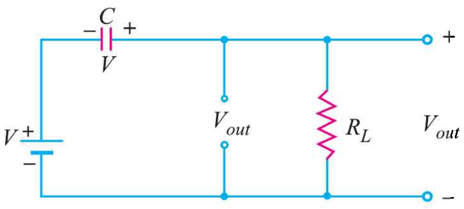


Fig. 18.49

(*ii*) When the input switches to $+V$ state (*i.e.*, positive half-cycle), the diode is reverse biased and behaves as an open as shown in Fig. 18.49. Since the discharging time constant (= CR_L) is much greater than the time period of the input signal, the capacitor remains almost fully charged to V volts during the off time of the diode. Referring to Fig. 18.49 and applying Kirchhoff 's voltage law to the input loop, we have,

$$V + V - V_{out} = 0$$

or

$$V_{out} = 2V$$

The resulting waveform is shown in Fig. 18.50. It is clear that it is a positively clamped output. That is to say the input signal has been pushed upward by V volts so that negative peaks fall on the zero level.

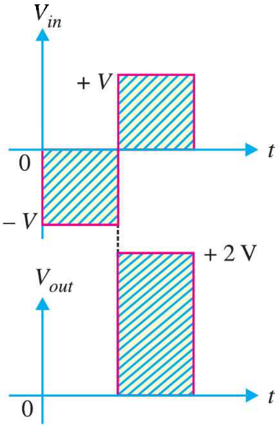


Fig. 18.50

18.23 Negative Clamper

Fig. 18.51 shows the circuit of a negative clamper. The clamped output is taken across R_L. Note that only change from the positive clamper is that the connections of diode are reversed.

(*i*) During the positive half-cycle of the input signal, the diode is forward biased. Therefore, the diode behaves as a short as shown in Fig. 18.52. The charging time constant (= CR_f) is very small so that the capacitor will charge to V volts very quickly. It is easy to see that during this interval, the output voltage is directly across the short circuit. Therefore, $V_{out} = 0$.

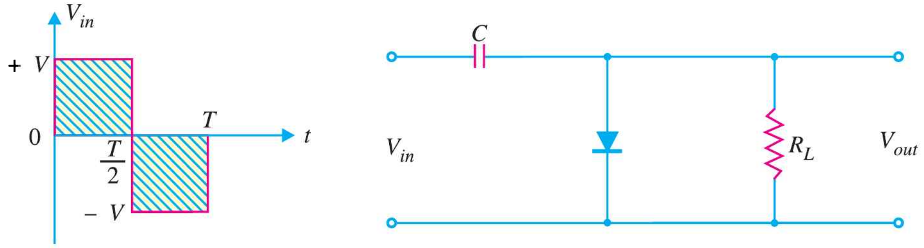


Fig. 18.51

(*ii*) When the input switches to $-V$ state (*i.e.*, negative half-cycle), the diode is reverse biased

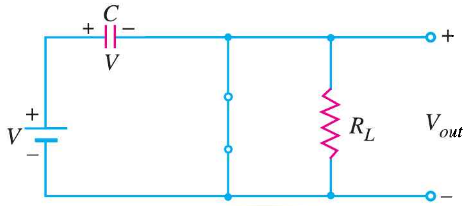


Fig. 18.52

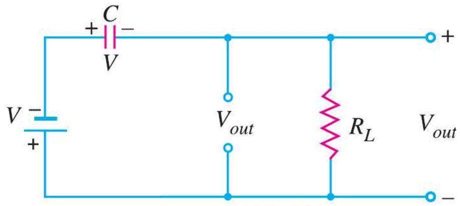


Fig. 18.53

and behaves as an open as shown in Fig. 18.53. Since the discharging time constant (= CR_L) is much greater than the time period of the input signal, the capacitor almost remains fully charged to V volts during the off time of the diode. Referring to Fig. 18.53 and applying Kirchhoff 's voltage law to the input loop, we have,

$$-V - V - V_{out} = 0$$

or $$V_{out} = -2\text{ V}$$

The resulting waveform is shown in Fig. 18.54. Note that total swing of the output signal is equal to the total swing of the input signal.

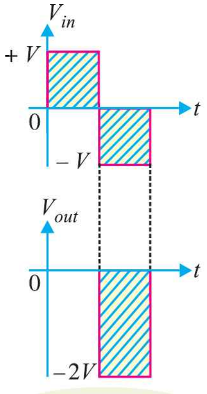


Fig. 18.54

Example 18.18. *Sketch the output waveform for the circuit shown in Fig. 18.55. It is given that discharging time constant (CR_L) is much greater than the time period of input wave.*

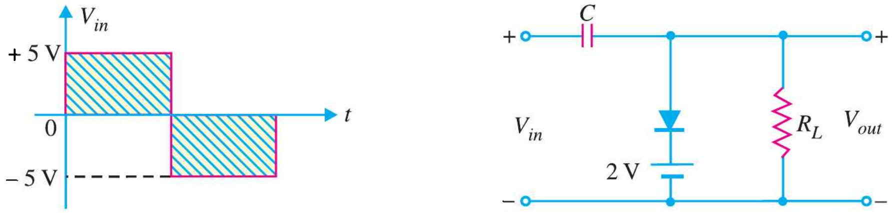


Fig. 18.55

Solution.

During positive half-cycle of the input signal, the diode is forward biased. The network will appear as shown in Fig. 18.56. It is clear that V_{out} = + 2 V. Further, applying Kirchhoff's voltage law to the input loop in Fig. 18.56, we have,

$$5\text{ V} - V_C - 2\text{ V} = 0$$

$$\therefore \quad V_C = 3\text{ V}$$

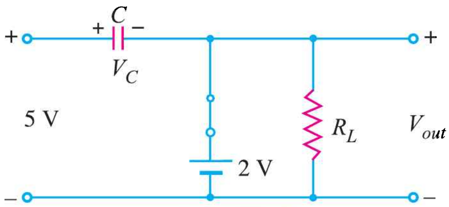


Fig. 18.56

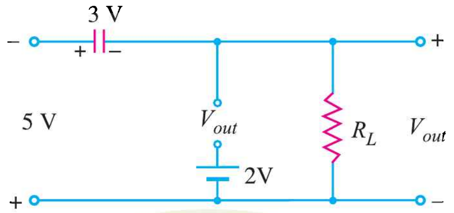


Fig. 18.57

Therefore, the capacitor will charge up to 3 V.

During the negative half-cycle of the input signal, the diode is reverse biased and will behave as an open [See Fig. 18.57]. Now battery of 2 V has no effect on V_{out}. Applying Kirchhoff's voltage law to the outside loop of Fig. 18.57, we have,

$$-5 - 3 - V_{out} = 0$$

or $$V_{out} = -8 \text{ V}$$

The negative sign results from the fact that the polarity of 8 V is opposite to the polarity defined for V_{out}. The clamped output is shown in Fig. 18.58. Note that the output swing of 10 V matches with the input swing.

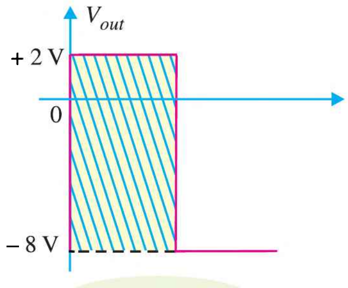


Fig. 18.58

Note. It is a biased clamper circuit. It allows a waveform to be shifted above or below (depending upon the polairty of 2 V battery) a *dc* reference other than 0 V.

Example 18.19. *Sketch the output waveform for the circuit shown in Fig. 18.59. It is given that discharging time constant (= CR_L) is much greater than the time period of input wave.*

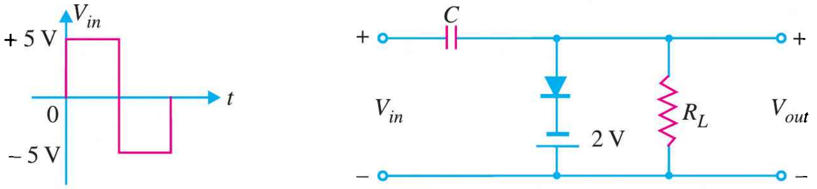


Fig. 18.59

Solution.

During the positive half-cycle of input signal, the diode is forward biased. Therefore, the diode behaves as a short [See Fig. 18.60]. It is easy to see that V_{out} = –2 V. Further, applying Kirchhoff's voltage law to the input loop [See Fig. 18.60], we have,

$$5 \text{ V} - V_C + 2 \text{ V} = 0$$

or $$V_C = 7 \text{ V}$$

Therefore, the capacitor will charge upto 7 V.

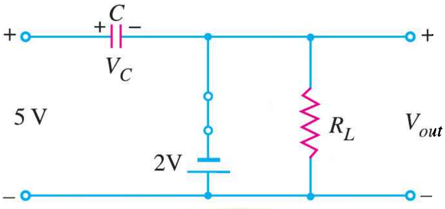


Fig. 18.60

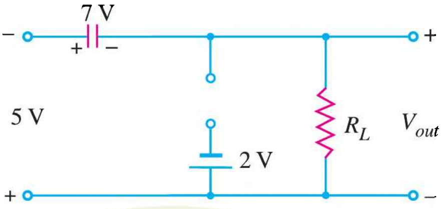


Fig. 18.61

During the negative half-cycle of the input signal, the diode is reverse biased and behaves as an open as shown in Fig. 18.61. Now battery of 2 V has no effect on V_{out}. Applying Kirchhoff's voltage law to the outside loop of Fig. 18.61, we have,

$$-5 \text{ V} - 7 \text{ V} - V_{out} = 0$$

or $$V_{out} = -12 \text{ V}$$

The negative sign results from the fact that the polarity of 12 V is opposite to the polarity defined for V_{out}. The clamped output is shown in Fig. 18.62. Note that output and input swings are the same.

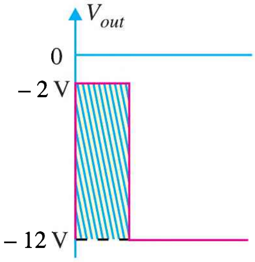
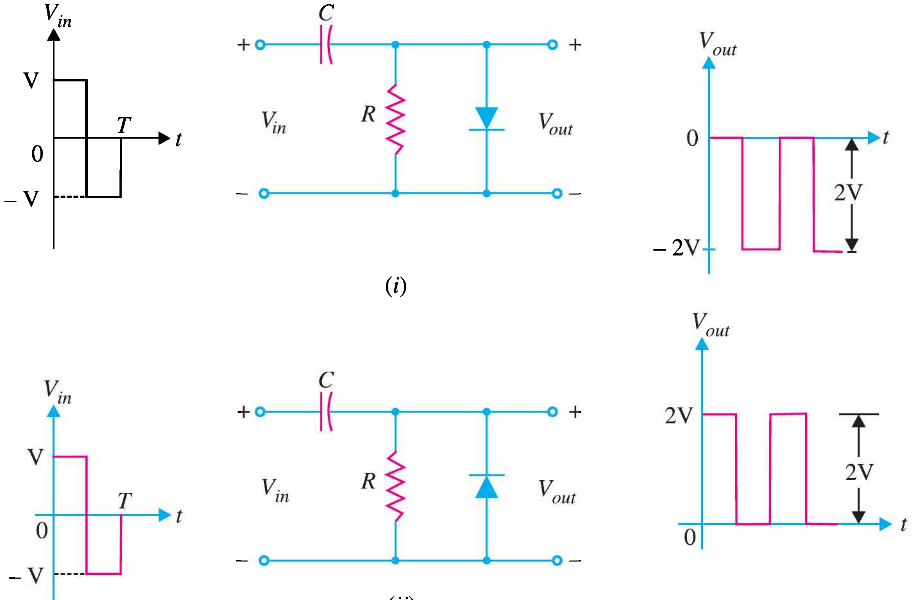


Fig. 18.62

Examle 18.20. *Draw the output voltage waveform for the input shown in Fig. 18.63.*


V_{in}
V
0
T
t
– V
C
+
–
V_{in}
R
V_{out}
V_{out}
0
– 2V
2V
2V
0

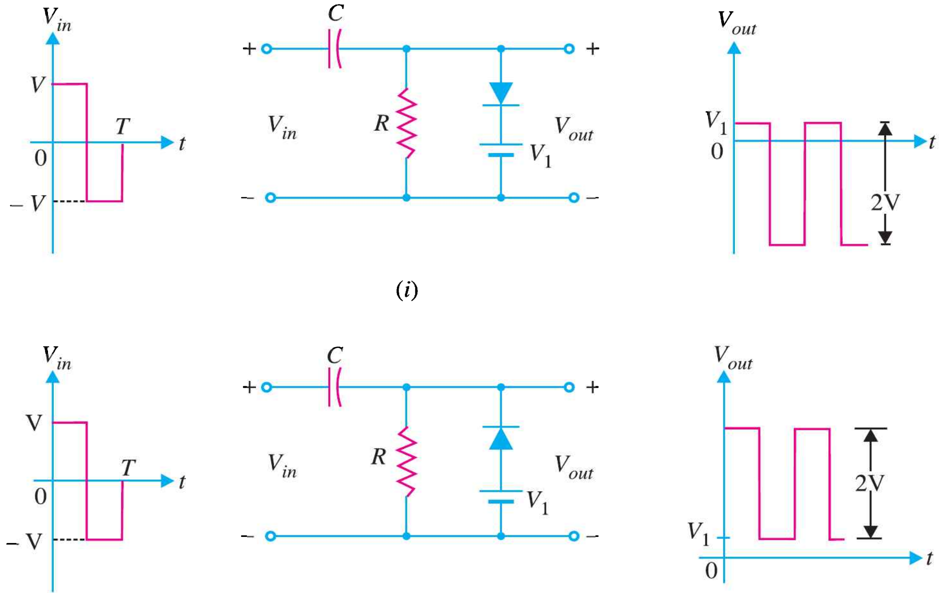
(*i*)

(*ii*)

Fig. 18.63

Solution. Fig. 18.63 (*i*) shows the output voltage waveform for the input wave to the clamping circuit. Note that it is a negative clamper and pushes the input wave downwards so that positive peaks fall on the zero level. Fig. 18.63 (*ii*) shows the output voltage waveform for the input wave to a positive clamper. The clamper pushes the input wave upwards so that the negative peaks fall on the zero level.

Example 18.21. *Draw the output voltage waveform for the input wave shown in Fig. 18.64.*


V_{in}
V
0
T
t
– V
C
+
–
V_{in}
R
V_{out}
V_1
V_{out}
V_1
0
2V

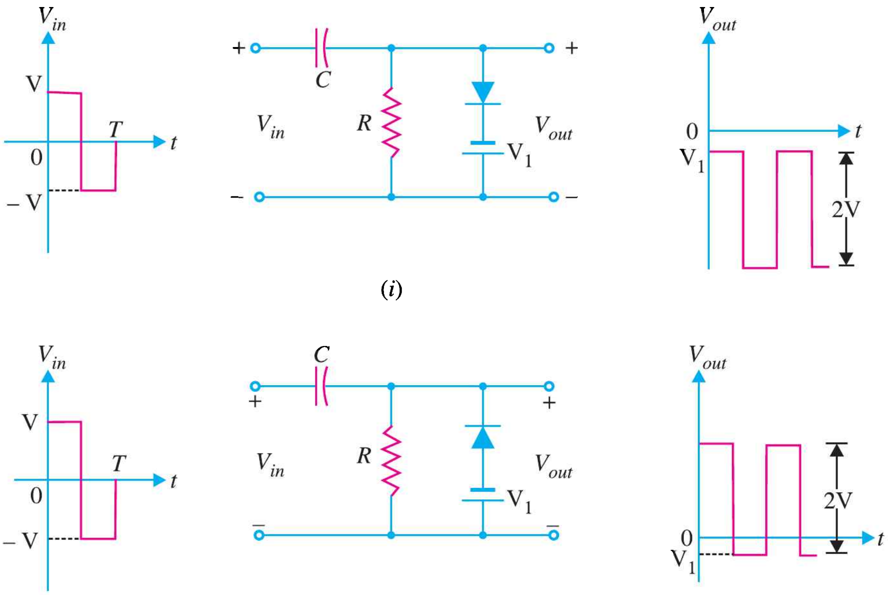
(*i*)

(*ii*)

Fig. 18.64

Solution. Fig. 18.64 (*i*) shows the output voltage waveform for the input wave to the clamping circuit. This is a negative clamper and pushes the input wave downward so that positive peak voltage is now V_1. Fig. 18.64 (*ii*) shows the output voltage waveform from a positive clamper. Note that the input wave is pushed upwards so that negative peaks are V'_1 volts above the zero level.

Example 18.22. *Draw the output voltage waveform for the input wave shown in Fig. 18.65.*



(*i*)

(*ii*)

Fig. 18.65

Solution. Fig. 18.65 (*i*) shows the output voltage waveform for the input wave to the clamping circuit. This is a negative clamper and pushes the input wave downward so that positive peaks lie V_1 volts below the zero level. Fig. 18.65 (*ii*) shows the output voltage waveform from a positive clamper. Note that the input waveform is pushed upwards so that negative peaks lie V_1 volts below zero level.

MULTIPLE-CHOICE QUESTIONS

1. A switch has ....
(*i*) one state (*ii*) two states
(*iii*) three states (*iv*) none of the above

2. A relay is .... switch.
(*i*) a mechanical (*ii*) an electronic
(*iii*) an electromechanical
(*iv*) none of the above

3. The switch that has the fastest speed of operation is .... switch.
(*i*) electronic
(*ii*) mechanical
(*iii*) electromechanical
(*iv*) none of the above

4. The most inexpensive switch is .... switch.
(*i*) electronic
(*ii*) mechanical
(*iii*) electromechanical
(*iv*) none of the above

5. The main disadvantage of a mechanical switch is that it ....
(*i*) is operated mechanically
(*ii*) is costly
(*iii*) has high inertia
(*iv*) none of the above

6. When a transistor is driven to saturation, ideally the output is ....

(*i*) V_{CC} (*ii*) 0
(*iii*) $V_{CC}/2$ (*iv*) $2V_{CC}$

7. The maximum speed of electronic switch can be .... operations per second.

(*i*) 10^4 (*ii*) 10
(*iii*) 1000 (*iv*) 10^9

8. A relay is superior to a mechanical switch because it ....

(*i*) is relatively inexpensive
(*ii*) does not require moving contacts
(*iii*) combines control with power amplification
(*iv*) none of the above

9. When a transistor is driven to cut off, ideally the output is ....

(*i*) V_{CC} (*ii*) 0
(*iii*) $V_{CC}/2$ (*iv*) $V_{CC}/3$

10. .... multivibrator is a square wave oscillator.

(*i*) monostable (*ii*) astable
(*iii*) bistable (*iv*) none of the above

11. An astable multivibrator has ....

(*i*) one stable state (*ii*) two stable states
(*iii*) no stable state (*iv*) none of the above

12. If d.c. supply of 10 V is fed to a differentiating circuit, then output will be ....

(*i*) 20 V (*ii*) 10 V
(*iii*) 0 V (*iv*) none of the above

13. If the input to a differentiating circuit is a saw-tooth wave, then output will be .... wave.

(*i*) square (*ii*) triangular
(*iii*) sine (*iv*) rectangular

14. A bistable multivibrator has ....

(*i*) two stable states
(*ii*) one stable state
(*iii*) no stable state
(*iv*) none of the above

15. If a square wave is fed to a differentiating circuit, the output will be ....

(*i*) sine wave
(*ii*) sharp narrow pulses
(*iii*) rectangular wave
(*iv*) triangular wave

16. An integrating circuit is a simple *RC* series circuit with output taken across ....

(*i*) both *R* and *C* (*ii*) *R*
(*iii*) *C* (*iv*) none of the above

17. For an integrating circuit to be effective, the *RC* product should be .... the time period of the input wave.

(*i*) 5 times greater than
(*ii*) 5 times smaller than
(*iii*) equal to
(*iv*) atleast 10 times greater than

18. A differentiating circuit is a simple RC circuit with output taken across ....

(*i*) R (*ii*) C
(*iii*) both R and C (*iv*) none of the above

19. A monostable multivibrator has ....

(*i*) no stable state
(*ii*) one stable state
(*iii*) two stable states
(*iv*) none of the above

20. The multivibrator which generates square wave of its own is the .... multivibrator.

(*i*) monostable (*ii*) bistable
(*iii*) astable (*iv*) none of the above

21. For a differentiating circuit to be effective, the RC product should be .... the time period of the input wave.

(*i*) equal to
(*ii*) 5 times greater than
(*iii*) 5 times smaller than
(*iv*) atleast 10 times greater than

22. When a rectangular voltage waveform is applied to a capacitor, then the current waveform is ....

(*i*) rectangular (*ii*) sinusoidal
(*iii*) sawtooth (*iv*) square

23. The positive clipper is that which removes the .... half-cycles of the input voltage.

(*i*) negative
(*ii*) positive
(*iii*) both positive and negative
(*iv*) none of the above

24. A clamping circuit adds .... component to the signal.

(*i*) d.c.
(*ii*) a.c.
(*iii*) both d.c. and a.c.
(*iv*) none of the above

25. One would find a clamping circuit in ....
(*i*) receiving antenna
(*ii*) radio transmitter
(*iii*) radio receiver (*iv*) television receiver

26. When transistor is used as an amplifier, it is operated in the .... region.
(*i*) off (*ii*) saturation
(*iii*) active (*iv*) none of the above

27. When the transistor (CE arrangement) is in the cut off region, the collector current is ....
(*i*) I_{CBO} (*ii*) I_{CEO}
(*iii*) $(\beta + 1)\, I_{CEO}$ (*iv*) $I_{C\,(sat)}$

28. A negative clipper removes the .... half-cycles of the input voltage.
(*i*) negative
(*ii*) positive
(*iii*) both positive and negative
(*iv*) none of the above

29. If the input to an integrating circuit is a succession of alternating positive and negative pulses of very short duration, the output will be .... wave.
(*i*) rectangular (*ii*) triangular
(*iii*) sine (*iv*) square

30. In a multivibrator, we have .... feedback.
(*i*) negative
(*ii*) 100 % positive
(*iii*) both positive and negative
(*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iii*)	**3.** (*i*)	**4.** (*i*)	**5.** (*iii*)
6. (*ii*)	**7.** (*iv*)	**8.** (*iii*)	**9.** (*i*)	**10.** (*ii*)
11. (*iii*)	**12.** (*iii*)	**13.** (*iv*)	**14.** (*i*)	**15.** (*ii*)
16. (*iii*)	**17.** (*iv*)	**18.** (*i*)	**19.** (*ii*)	**20.** (*iii*)
21. (*iv*)	**22.** (*i*)	**23.** (*ii*)	**24.** (*i*)	**25.** (*iv*)
26. (*iii*)	**27.** (*ii*)	**28.** (*i*)	**29.** (*iv*)	**30.** (*ii*)

Chapter Review Topics

1. What is a switching circuit ?

2. Discuss the advantages of an electronic switch over a mechanical or electro-mechanical switch.

3. Explain the terms collector leakage current and saturation collector current.

4. Explain the switching action of a transistor with the help of output characteristics.

5. What is a multivibrator ? Explain the principle on which it works.

6. With a neat sketch, explain the working of (*i*) astable multivibrator (*ii*) monostable multivibrator (*iii*) bistable multivibrator.

7. What is the basic difference among the three types of multivibrators ?

8. Show that the output from a differentiating circuit is derivative of the input. What assumptions are made in the derivation ?

9. Sketch the output waveforms from a differentiating circuit when input is (*i*) a square wave (*ii*) saw-tooth wave.

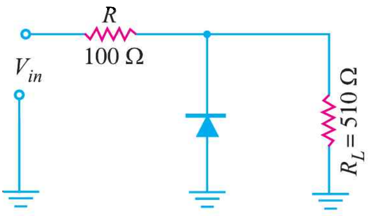
10. Show that the output from an integrating circuit is the integral of the input.

11. What is a clipper ? Describe (*i*) positive clipper (*ii*) biased clipper and (*iii*) combination clipper.

12. What do you understand by a clamping circuit ? With neat diagrams explain the action of a (*i*) positive clamper (*ii*) negative clamper.

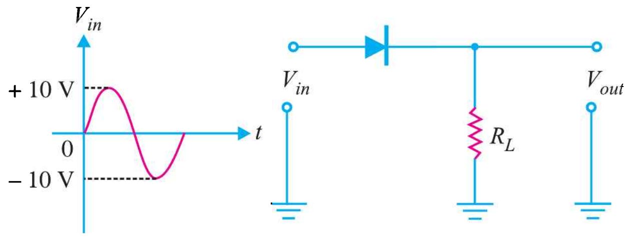
Problems

1. The negative shunt clipper shown in Fig. 18.66 has peak input voltage of +15 V. What is the output peak voltage ? **[12.54 V]**



R
100 Ω
V_{in}
$R_L = 510\ \Omega$

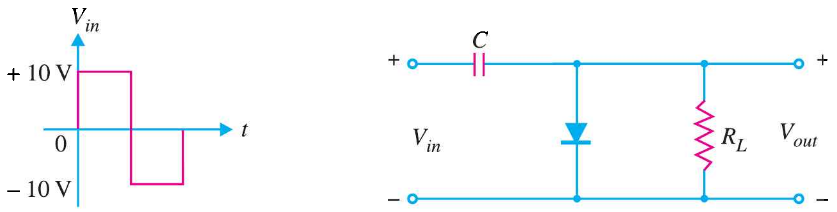
Fig. 18.66



V_{in}
+ 10 V
0
– 10 V
t
V_{in}
R_L
V_{out}

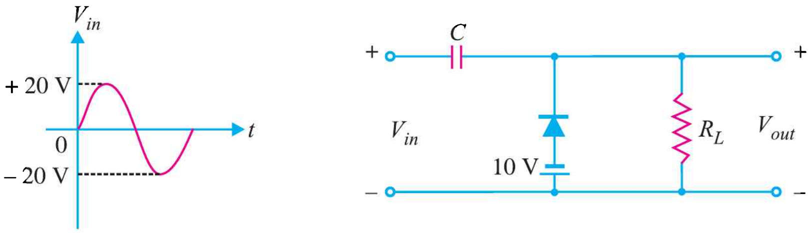
Fig. 18.67

2. In the negative series clipper shown in Fig. 18.67, what is the peak output voltage ? **[9.3 V]**
3. In the circuit shown in Fig. 18.68, what are the minimum and peak values of the clamped output ? **[0 V ; –20 V]**



V_{in}
+ 10 V
0
– 10 V
t
C
+
–
V_{in}
R_L
V_{out}
+
–

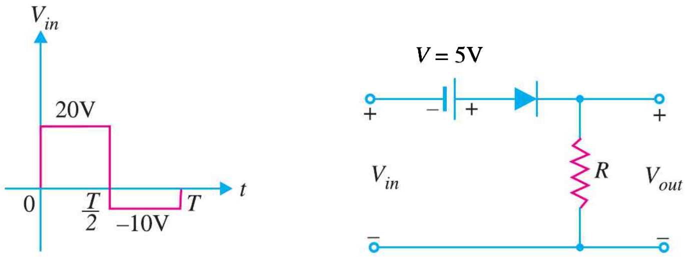
Fig. 18.68



V_{in}
+ 20 V
0
– 20 V
t
C
+
–
V_{in}
10 V
R_L
V_{out}
+
–

Fig. 18.69

4. Sketch the wave shape of clamped output in Fig. 18.69.
5. Determine the output waveform for the clipper network shown in Fig. 18.70.



V_{in}
20V
0
$\frac{T}{2}$
–10V
T
t
V = 5V
–
+
+
–
V_{in}
R
V_{out}
+
–

Fig. 18.70

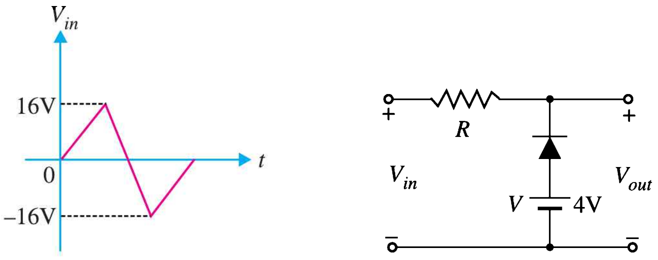


Fig. 18.71

6. Determine the output waveform for the clipper network shown in Fig. 18.71.

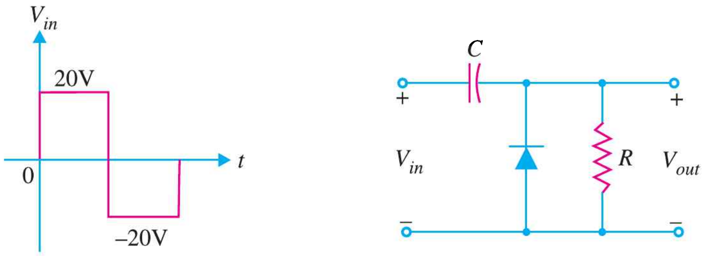


Fig. 18.72

7. Determine the output waveform for the clamper network shown in Fig. 18.72.

Discussion Questions

1. What is the effect of *RC* product on the output waveform in a differentiating circuit ?
2. A differentiating circuit is essentially an *RC* circuit. Why the output from *RC* coupling is not a differentiated wave ?
3. What is the difference between a switching transistor and an ordinary transistor ?
4. What effect does a clamper have on the average value of a given input wave ?
5. What effect does a clamper have on the r.m.s. voltage of a sine-wave input ?
6. What determines the d.c. reference voltage of a clamper ?
7. Discuss the differences between shunt and series clippers.

19

Field Effect Transistors

19.1 Types of Field Effect Transistors
19.3 Principle and Working of JFET
19.5 Importance of JFET
19.7 JFET as an Amplifier
19.9 Salient Features of JFET
19.11 Expression for Drain Current (I_D)
19.13 Parameters of JFET
19.15 Variation of Transconductance (g_m or g_{fs}) of JFET
19.17 JFET Biasing by Bias Battery
19.19 JFET with Voltage-Divider Bias
19.21 Practical JFET Amplifier
19.23 D.C. Load Line Analysis
19.25 Voltage Gain of JFET Amplifier (With Source Resistance R_s)
19.27 Metal Oxide Semiconductor FET (MOSFET)
19.29 Symbols for D-MOSFET
19.31 D-MOSFET Transfer Characteristic
19.33 D-MOSFET Biasing
19.35 D-MOSFETs Versus JFETs
19.37 E-MOSFET Biasing Circuits

INTRODUCTION

In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a bipolar transistor. The ordinary or bipolar transistor has two principal disadvantages. First, it has a low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms. The field effect transistor (*FET*) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms. The *FET* is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding *FET* market has led many semiconductor marketing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications. In this chapter, we shall focus our attention on the construction, working and circuit applications of field effect transistors.

19.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

(*i*) Junction field effect transistor (*JFET*)

(*ii*) Metal oxide semiconductor field effect transistor (*MOSFET*)

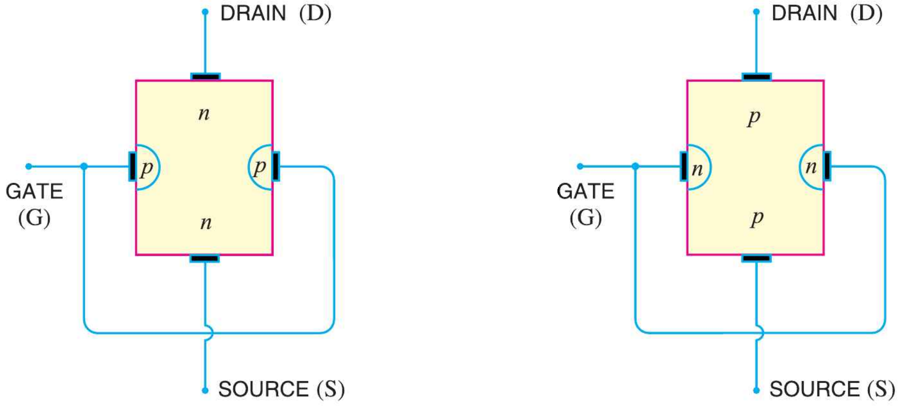
To begin with, we shall study about *JFET* and then improved form of *JFET*, namely; *MOSFET.*

19.2 Junction Field Effect Transistor (JFET)

A **junction field effect transistor** *is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.*

The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details. A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig.19.1. The bar forms the conducting channel for the charge carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. 19.1 (*i*) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. 19.1 (*ii*). The two *pn* junctions forming diodes are connected *internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz.*, *gate* (*G*), *source* (*S*) and *drain* (*D*).



n-Channel JFET (*i*)   *p-Channel JFET* (*ii*)

Fig. 19.1

---

* It would seem from Fig. 19.1 that there are three doped material regions. However, this is not the case. The gate material *surrounds* the channel in the same manner as a belt surrounding your waist.

JFET polarities. Fig. 19.2 (*i*) shows *n*-channel *JFET* polarities whereas Fig. 19.2 (*ii*) shows the *p*-channel *JFET* polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of *JFET* connection. The drain and source terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain.

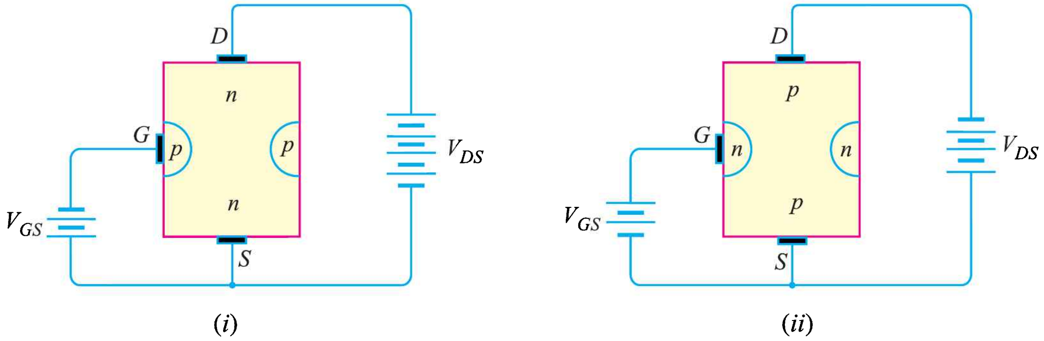


Fig. 19.2

The following points may be noted :

(*i*) The input circuit (*i.e.* gate to source) of a *JFET* is reverse biased. This means that the device has high input impedance.

(*ii*) The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.

(*iii*) In all *JFETs*, source current I_S is equal to the drain current *i.e.* $I_S = I_D$.

19.3 Principle and Working of JFET

Fig. 19.3 shows the circuit of *n*-channel *JFET* with normal polarities. Note that the gate is reverse biased.

Principle. The two *pn* junctions at the sides form two depletion layers. The current conduction by charge carriers (*i.e.* free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence *resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease. *Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage* V_{GS}. In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

Working. The working of *JFET* is as under :

(*i*) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [See Fig. 19.3 (*i*)], the two *pn* junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

(*ii*) When a reverse voltage V_{GS} is applied between the gate and source [See Fig. 19.3 (*ii*)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of *n*-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.

---

* The resistance of the channel depends upon its area of X-section. The greater the X-sectional area of this channel, the lower will be its resistance and the greater will be the current flow through it.

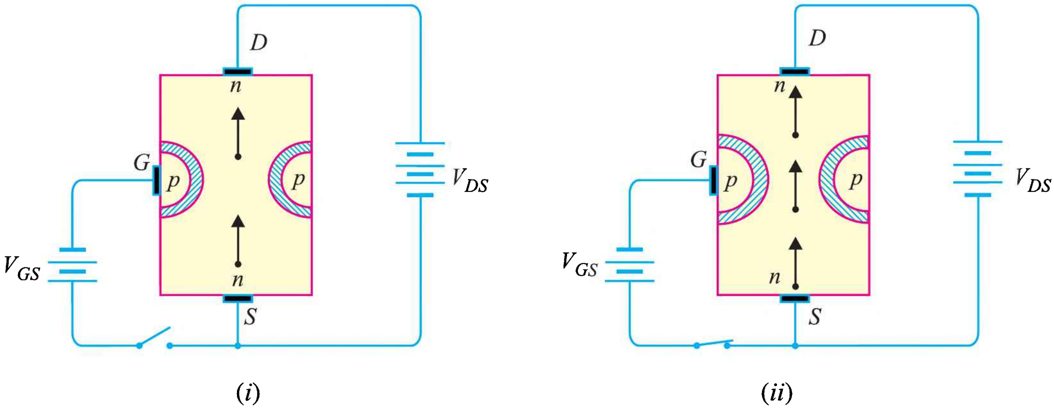
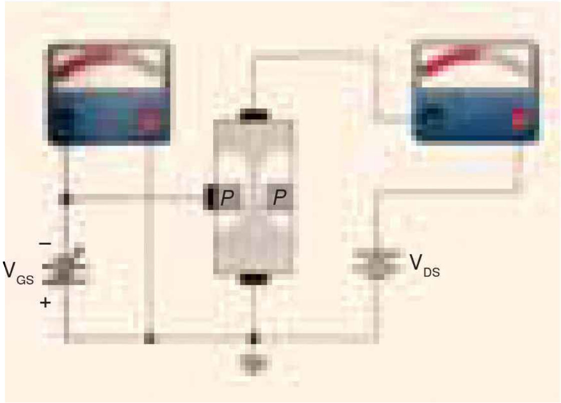


Fig. 19.3

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (*i.e.* electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a *p*-channel *JFET* operates in the same manner as an *n* -channel *JFET* except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

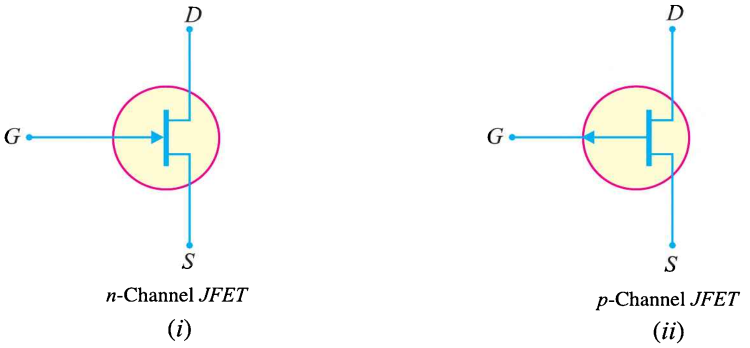
Note. If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other and the channel is cut off. Under such conditions, the channel becomes a non-conductor.



JFET biased for Conduction

19.4 Schematic Symbol of JFET

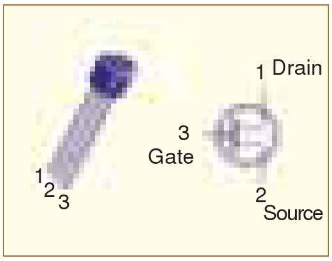
Fig. 19.4 shows the schematic symbol of *JFET*. The vertical line in the symbol may be thought



n-Channel *JFET*
(*i*)

p-Channel *JFET*
(*ii*)

Fig. 19.4



as channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. 19.4 (*i*). However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig. 19.4 (*ii*)].

19.5 Importance of JFET

A *JFET* acts like a voltage controlled device *i.e.* input voltage (V_{GS}) controls the output current. This is different from ordinary transistor (or bipolar transistor) where input current controls the output current. Thus *JFET* is a semiconductor device acting *like a vacuum tube. The need for *JFET* arose because as modern electronic equipment became increasingly transistorised, it became apparent that there were many functions in which bipolar transistors were unable to replace vacuum tubes. Owing to their extremely high input impedance, *JFET* devices are more like vacuum tubes than are the bipolar transistors and hence are able to take over many vacuum-tube functions. Thus, because of *JFET*, electronic equipment is closer today to being completely solid state.

The *JFET* devices have not only taken over the functions of vacuum tubes but they now also threaten to depose the bipolar transistors as the most widely used semiconductor devices. As an amplifier, the *JFET* has higher input impedance than that of a conventional transistor, generates less noise and has greater resistance to nuclear radiations.

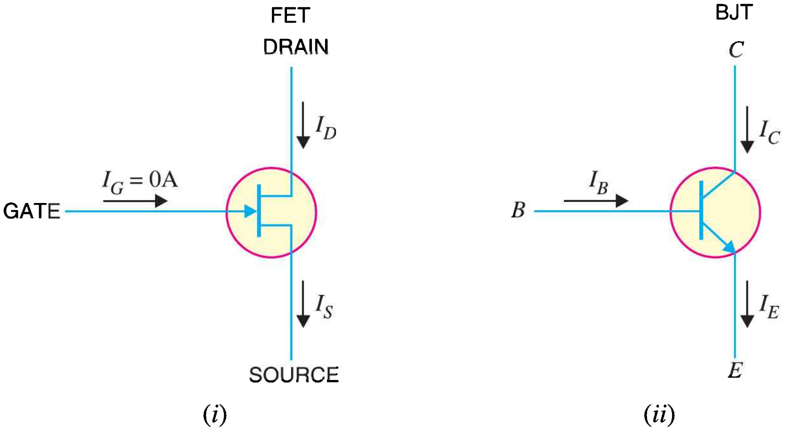
19.6 Difference Between JFET and Bipolar Transistor

The *JFET* differs from an ordinary or bipolar transistor in the following ways :

(*i*) In a *JFET*, there is only one type of carrier, holes in *p*-type channel and electrons in *n*-type channel. For this reason, it is also called a *unipolar transistor*. However, in an ordinary transistor, both holes and electrons play part in conduction. Therefore, an ordinary transistor is sometimes called a *bipolar transistor*.

(*ii*) As the input circuit (*i.e.*, gate to source) of a *JFET* is reverse biased, therefore, the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(*iii*) The primary functional difference between the *JFET* and the *BJT* is that no current (actually, a very, very small current) enters the gate of *JFET* (*i.e.* $I_G = 0$A). However, typical *BJT* base current might be a few μA while *JFET* gate current a thousand times smaller [See Fig. 19.5].



(*i*) (*ii*)

Fig. 19.5

---

* The gate, source and drain of a *JFET* correspond to grid, cathode and anode of a vacuum tube.

(*iv*) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(*v*) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*- type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

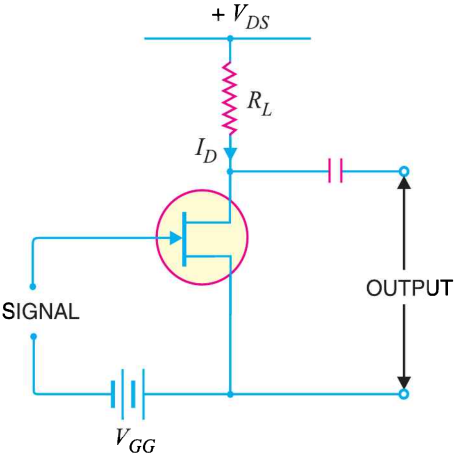


Fig. 19.6

19.7 JFET as an Amplifier

Fig. 19.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative w.r.t. source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is that a small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L. In this way, *JFET* acts as an amplifier.

19.8 Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *output characteristics of JFET*. Fig. 19.7 shows the circuit for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drian-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristic of *JFET* at V_{GS} = 1V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 19.8 shows a family of output characteristics.

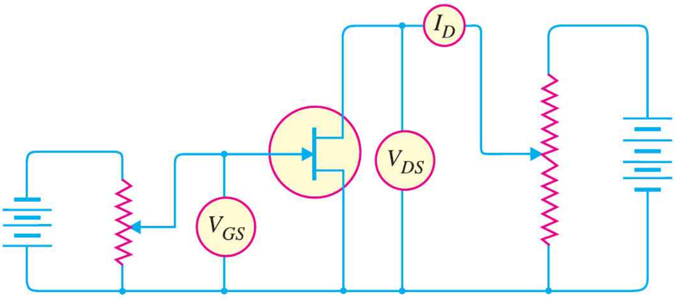


Fig. 19.7

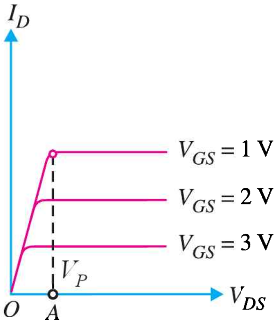


Fig. 19.8

The following points may be noted from the characteristics :

(*i*) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. 19.8, *OA* is the *pinch off voltage* V_P.

(*ii*) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

(*iii*) The characteristics resemble that of a pentode valve.

19.9 Salient Features of JFET

The following are some salient features of *JFET* :

(*i*) A *JFET* is a three-terminal *voltage-controlled* semiconductor device *i.e.* input voltage controls the output characteristics of *JFET*.

(*ii*) The *JFET* is *always* operated with gate-source *pn* junction *reverse biased.

(*iii*) In a *JFET*, the gate current is zero *i.e.* $I_G = 0$A.

(*iv*) Since there is no gate current, $I_D = I_S$.

(*v*) The *JFET* must be operated between $V_{GS} = 0$V and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero. [See Fig. 19.12].

(*vi*) Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.

(*vii*) The *JFET* is not subjected to thermal runaway when the temperature of the device increases.

(*viii*) The drain current I_D is controlled by changing the channel width.

(*ix*) Since *JFET* has no gate current, there is no β rating of the device. We can find drain current I_D by using the eq. mentioned in Art. 19.11.

19.10 Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current.*

Fig 19.9 shows the *JFET* circuit with $V_{GS} = 0$ *i.e.*, source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 19.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and **holds drain current constant at I_{DSS}.

---

* Forward biasing gate-source *pn* junction may destroy the device.

** When drain voltage equals V_P, the channel becomes narrow and the depletion layers almost touch each other. The channel now acts as a current limiter and holds drain current at a constant value of I_{DSS}.

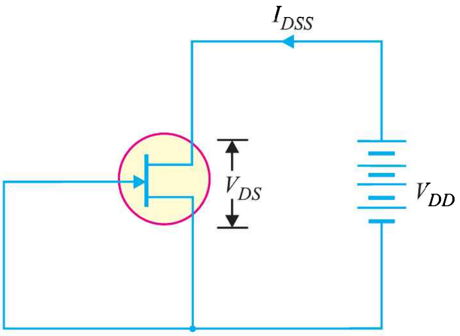


Fig. 19.9

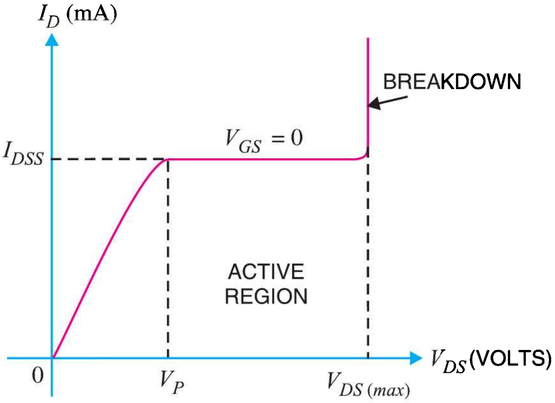


Fig. 19.10

The following points may be noted carefully :

(*i*) Since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation of *JFET*.

(*ii*) There is a maximum drain voltage [$V_{DS\,(max)}$] that can be applied to a *JFET*. If the drain voltage exceeds $V_{DS\,(max)}$, *JFET* would breakdown as shown in Fig. 19.10.

(*iii*) The region between V_P and $V_{DS\,(max)}$ (breakdown voltage) is called *constant-current region* or *active region*. As long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS}. In other words, in the active region, *JFET* behaves as a constant–current device. For proper working of *JFET*, it must be operated in the active region.

2. Pinch off Voltage (V_P). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

Figure 19.11 shows the drain curves of a *JFET*. Note that pinch off voltage is V_P. The highest curve is for V_{GS} = 0V, the shorted-gate condition. For values of V_{DS} greater than V_P, the drain current is almost constant. It is because when V_{DS} equals V_P, the channel is effectively closed and does not allow further increase in drain current. It may be noted that for proper function of *JFET*, it is always operated for $V_{DS} > V_P$. However, V_{DS} should not exceed $V_{DS\,(max)}$ otherwise *JFET* may breakdown.

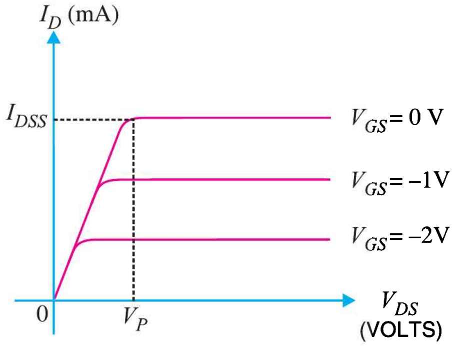


Fig . 19.11

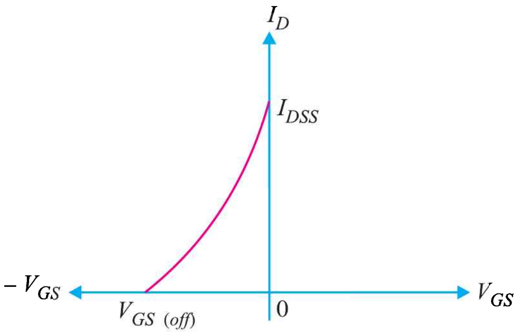


Fig . 19.12

3. Gate-source cut off voltage $V_{GS\,(off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

The idea of gate-source cut off voltage can be easily understood if we refer to the transfer characteristic of a *JFET* shown in Fig. 19.12. As the reverse gate-source voltage is increased, the cross-sectional area of the channel decreases. This in turn decreases the drain current. At some reverse gate-source voltage, the depletion layers extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero. The gate voltage at which the channel is cut off (*i.e.* channel becomes non-conducting) is called gate-source cut off voltage $V_{GS\,(off)}$.

Notes. (*i*) It is interesting to note that $V_{GS\,(off)}$ will always have the same magnitude value as V_P. For example if $V_P = 6$ V, then $V_{GS\,(off)} = -6$ V. Since these two values are always equal and opposite, only one is listed on the specification sheet for a given *JFET*.

(*ii*) There is a distinct difference between V_P and $V_{GS\,(off)}$. Note that V_P is the value of V_{DS} that causes the *JEFT* to become a constant current device. It is measured at $V_{GS} = 0$ V and will have a constant drain current $= I_{DSS}$. However, $V_{GS\,(off)}$ is the value of V_{GS} that causes I_D to drop to nearly zero.

19.11 Expression for Drain Current (I_D)

The relation between I_{DSS} and V_P is shown in Fig. 19.13. We note that gate-source cut off voltage [*i.e.* $V_{GS\,(off)}$] on the transfer characteristic is equal to pinch off voltage V_P on the drain characteristic *i.e.*

$$V_P = |V_{GS\,(off)}|$$

For example, if a *JFET* has $V_{GS\,(off)} = -4$V, then $V_P = 4$V.

The transfer characteristic of *JFET* shown in Fig. 19.13 is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

where I_D = drain current at given V_{GS}

I_{DSS} = shorted – gate drain current

V_{GS} = gate–source voltage

$V_{GS\,(off)}$ = gate–source cut off voltage

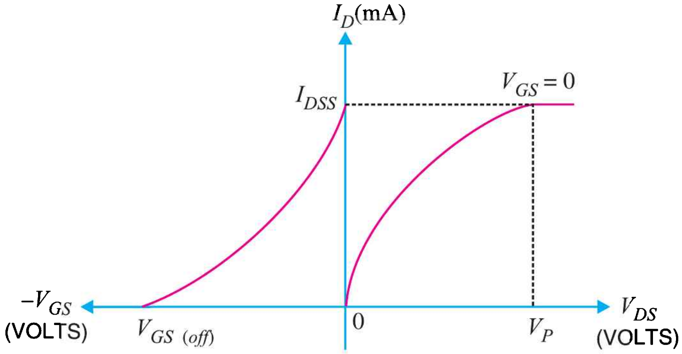


Fig. 19.13

Example 19.1. *Fig. 19.14 shows the transfer characteristic curve of a JFET. Write the equation for drain current.*

Solution. Referring to the transfer characteristic curve in Fig. 19.14, we have,

$$I_{DSS} = 12 \text{ mA}$$

$$V_{GS\,(off)} = -5 \text{ V}$$

$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or

$$I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA } \textbf{Ans.}$$

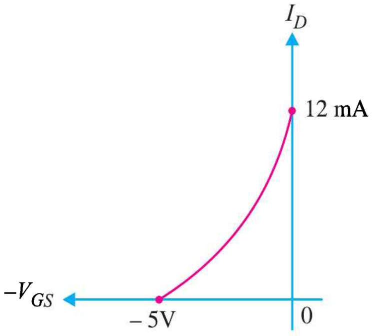


Fig. 19.14

Example 19.2. *A JFET has the following parameters: I_{DSS} = 32 mA ; $V_{GS\,(off)}$ = – 8V; V_{GS} = – 4.5 V. Find the value of drain current.*

Solution.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 \text{ mA}$$

$$= \mathbf{6.12\ mA}$$

Example 19.3. *A JFET has a drain current of 5 mA. If I_{DSS} = 10 mA and $V_{GS\,(off)}$ = – 6 V, find the value of (i) V_{GS} and (ii) V_P.*

Solution.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or

$$5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$

or

$$1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

(*i*) ∴ $V_{GS} = \mathbf{-1.76\ V}$

(*ii*) and $V_P = -V_{GS\,(off)} = \mathbf{6\ V}$

Example 19.4. *For the JFET in Fig. 19.15, $V_{GS\,(off)}$ = – 4V and I_{DSS} = 12 mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation.*

Solution. Since $V_{GS\,(off)}$ = – 4V, V_P = 4V. The minimum value of V_{DS} for the *JFET* to be in constant-current region is

$$V_{DS} = V_P = 4\text{V}$$

In the constant current region with V_{GS} = 0V,

$$I_D = I_{DSS} = 12 \text{ mA}$$

Applying Kirchhoff's voltage law around the drain circuit, we have,

$$V_{DD} = V_{DS} + V_{R_D} = V_{DS} + I_D R_D$$

$$= 4\text{V} + (12 \text{ mA})\,(560\Omega) = 4\text{V} + 6.72\text{V} = \mathbf{10.72V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

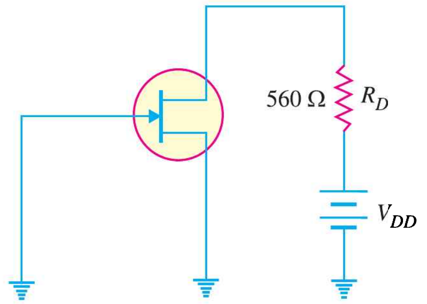


Fig. 19.15

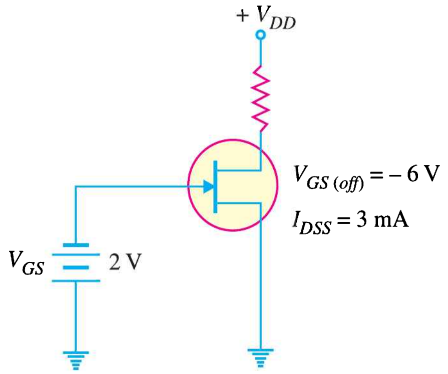


Fig. 19.16

Example 19.5. *Determine the value of drain current for the circuit shown in Fig. 19.16.*

Solution. It is clear from Fig. 19.16 that $V_{GS} = -2$V. The drain current for the circuit is given by;

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 3\text{ mA}\left(1 - \frac{-2\text{V}}{-6\text{V}}\right)^2$$

$$= (3\text{ mA})\,(0.444) = \mathbf{1.33\ mA}$$

Example 19.6. *A particular p-channel JFET has a $V_{GS\,(off)} = +4V$. What is I_D when $V_{GS} = +6V$?*

Solution. The *p*-channel *JFET* requires a positive gate-to-source voltage to pass drain current I_D. The more the positive voltage, the less the drain current. When $V_{GS} = 4$V, $I_D = 0$ and *JFET* is cut off. Any further increase in V_{GS} keeps the *JFET* cut off. Therefore, at $V_{GS} = +6$V, $I_D =$ **0A.**

19.12 Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

(*i*) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(*ii*) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(*iii*) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(*iv*) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(*v*) A *JFET* has a smaller size, longer life and high efficiency.

19.13 Parameters of JFET

Like vacuum tubes, a *JFET* has certain parameters which determine its performance in a circuit. The main parameters of a *JFET* are (*i*) a.c. drain resistance (*ii*) transconductance (*iii*) amplification factor.

(*i*) **a.c. drain resistance (r_d).** Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a *JFET*. It may be defined as follows :

It is the ratio of change in drain-source voltage (ΔV_{DS}) *to the change in drain current* (ΔI_D) *at constant gate-source voltage i.e.*

$$\text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA, then,

$$\text{a.c. drain resistance, } r_d = \frac{2\text{ V}}{0.02\text{ mA}} = 100\text{ k}\Omega$$

Referring to the output characteristics of a *JFET* in Fig. 19.8, it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat. Therefore, drain resistance of a *JFET* has a large value, ranging from 10 kΩ to 1 MΩ.

(*ii*) **Transconductance (g_{fs}).** The control that the gate voltage has over the drain current is measured by transconductance g_{fs} and is similar to the transconductance g_m of the tube. It may be defined as follows :

It is the ratio of change in drain current (ΔI_D) *to the change in gate-source voltage* (ΔV_{GS}) *at constant drain-source voltage i.e.*

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a *JFET* is usually expressed either in mA/volt or micromho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then,

$$\text{Transconductance, } g_{fs} = \frac{0.3\text{ mA}}{0.1\text{ V}} = 3\text{ mA/V} = 3 \times 10^{-3}\text{ A/V or mho or } S \text{ (siemens)}$$

$$= 3 \times 10^{-3} \times 10^{6}\ \mu\text{ mho} = 3000\ \mu\text{ mho (or } \mu\text{S)}$$

(*iii*) **Amplification factor (μ).** *It is the ratio of change in drain-source voltage* (ΔV_{DS}) *to the change in gate-source voltage* (ΔV_{GS}) *at constant drain current i.e.*

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor of a *JFET* indicates how much more control the gate voltage has over drain current than has the drain voltage. For instance, if the amplification factor of a *JFET* is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

19.14 Relation Among JFET Parameters

The relationship among *JFET* parameters can be established as under :

$$\text{We know} \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \mu = r_d \times g_{fs}$$

i.e. amplification factor = a.c. drain resistance × transconductance

Example 19.7. *When a reverse gate voltage of 15 V is applied to a JFET, the gate current is* 10^{-3} *μA. Find the resistance between gate and source.*

Solution. $V_{GS} = 15\text{ V}$; $I_G = 10^{-3}\ \mu\text{A} = 10^{-9}\text{ A}$

$$\therefore \quad \text{Gate to source resistance} = \frac{V_{GS}}{I_G} = \frac{15\text{ V}}{10^{-9}\text{ A}} = 15 \times 10^9\ \Omega = \mathbf{15{,}000\ M\Omega}$$

This example shows the major difference between a *JFET* and a bipolar transistor. Whereas the input impedance of a *JFET* is several hundred MΩ, the input impedance of a bipolar transistor is only hundreds or thousands of ohms. The large input impedance of a *JFET* permits high degree of isolation between the input and output.

Example 19.8. *When V_{GS} of a JFET changes from –3.1 V to –3 V, the drain current changes from 1 mA to 1.3 mA. What is the value of transconductance ?*

Solution. $\Delta V_{GS} = 3.1 - 3 = 0.1\text{ V}$ ... magnitude

$$\Delta I_D = 1.3 - 1 = 0.3\text{ mA}$$

$$\therefore \quad \text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3\text{ mA}}{0.1\text{ V}} = 3\text{ mA/V} = \mathbf{3000\ \mu\ mho}$$

Example 19.9. *The following readings were obtained experimentally from a JFET :*

V_{GS}	0 V	0 V	– 0.2 V
V_{DS}	7 V	15 V	15 V
I_D	10 mA	10.25 mA	9.65 mA

Determine (i) a. c. drain resistance (ii) transconductance and (iii) amplification factor.

Solution. (*i*) With V_{GS} constant at 0V, the increase in V_{DS} from 7 V to 15 V increases the drain current from 10 mA to 10.25 mA *i.e.*

Change in drain-source voltage, $\Delta V_{DS} = 15 - 7 = 8\text{ V}$

Change in drain current, $\Delta I_D = 10.25 - 10 = 0.25\text{ mA}$

$$\therefore \quad \text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{8\text{ V}}{0.25\text{ mA}} = \mathbf{32\ k\Omega}$$

(*ii*) With V_{DS} constant at 15 V, drain current changes from 10.25 mA to 9.65 mA as V_{GS} is changed from 0 V to – 0.2 V.

$$\Delta V_{GS} = 0.2 - 0 = 0.2\text{ V}$$

$$\Delta I_D = 10.25 - 9.65 = 0.6\text{ mA}$$

$$\therefore \quad \text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.6\text{ mA}}{0.2\text{ V}} = 3\text{ mA/V} = \mathbf{3000\ \mu\ mho}$$

(*iii*) Amplification factor, $\mu = r_d \times g_{fs} = (32 \times 10^3) \times (3000 \times 10^{-6}) = \mathbf{96}$

19.15 Variation of Transconductance (g_m or g_{fs}) of JFET

We have seen that transconductance g_m of a *JFET* is the ratio of a change in drain current (ΔI_D) to a change in gate-source voltage (ΔV_{GS}) at constant V_{DS} *i.e.*

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

The transconductance g_m of a *JFET* is an important parameter because it is a major factor in determining the voltage gain of *JFET* amplifiers. However, the transfer characteristic curve for a *JFET* is nonlinear so that the value of g_m depends upon the location on the curve. Thus the value of g_m at point *A* in Fig. 19.17 will be different from that at point *B*. Luckily, there is following equation to determine the value of g_m at a specified value of V_{GS}:

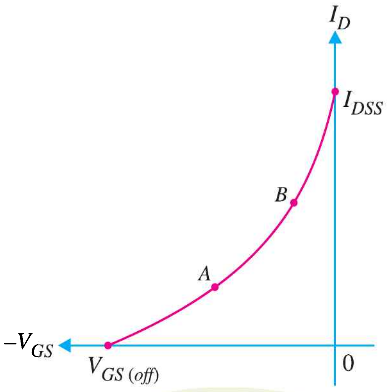


Fig. 19.17

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)$$

where g_m = value of transconductance at any point on the transfer characteristic curve

g_{mo} = value of transconductance(maximum) at $V_{GS} = 0$

Normally, the data sheet provides the value of g_{mo}. When the value of g_{mo} is not available, you can approximately calculate g_{mo} using the following relation :

$$g_{mo} = \frac{2I_{DSS}}{|V_{GS\,(off)}|}$$

Example 19.10. *A JFET has a value of* $g_{mo} = 4000\ \mu S$. *Determine the value of* g_m *at* $V_{GS} = -3V$. *Given that* $V_{GS\,(off)} = -8V$.

Solution.

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)$$

$$= 4000\ \mu\text{S}\left(1 - \frac{-3\text{V}}{-8\text{V}}\right)$$

$$= 4000\ \mu\text{S}\ (0.625) = \mathbf{2500\ \mu S}$$

Example 19.11. *The data sheet of a JFET gives the following information :* $I_{DSS} = 3\ mA$, $V_{GS\,(off)} = -6V$ *and* $g_{m\,(max)} = 5000\ \mu S$. *Determine the transconductance for* $V_{GS} = -4V$ *and find drain current* I_D *at this point.*

Solution. At $V_{GS} = 0$, the value of g_m is maximum *i.e.* g_{mo}.

$\therefore$ $g_{mo} = 5000\ \mu\text{S}$

Now $$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)$$

$$= 5000\ \mu\text{S}\left(1 - \frac{-4\text{V}}{-6\text{V}}\right)$$

$$= 5000\ \mu\text{S}\ (1/3) = \mathbf{1667\ \mu S}$$

Also $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 3\ \text{mA}\left(1 - \frac{-4}{-6}\right)^2 = \mathbf{333\ \mu A}$$

19.16 JFET Biasing

For the proper operation of *n*-channel *JFET*, gate must be negative *w.r.t.* source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit. The latter method is preferred because batteries are costly and require frequent replacement.

1. Bias battery. In this method, *JFET* is biased by a bias battery V_{GG}. This battery ensures that gate is always negative *w.r.t.* source during all parts of the signal.

2. Biasing circuit. The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. Two most commonly used methods are (*i*) self-bias (*ii*) potential divider method. We shall discuss each method in turn.

19.17 JFET Biasing by Bias Battery

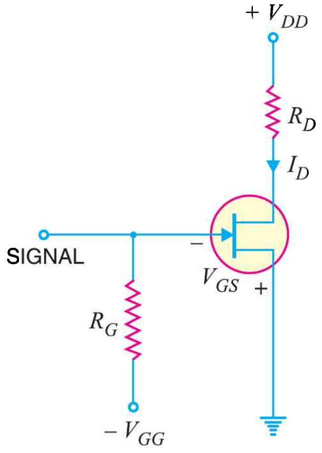


Fig. 19.18

Fig. 19.18 shows the biasing of a *n*-channel *JFET* by a bias battery – V_{GG}. This method is also called *gate bias*. The battery voltage – V_{GG} ensures that gate – source junction remains reverse biased.

Since there is no gate current, there will be no voltage drop across R_G.

$$\therefore \qquad V_{GS} = V_{GG}$$

We can find the value of drain current I_D from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

The value of V_{DS} is given by ;

$$V_{DS} = V_{DD} - I_D R_D$$

Thus the d.c. values of I_D and V_{DS} stand determined. The operating point for the circuit is V_{DS}, I_D.

Example 19.12. *A JFET in Fig. 19.19 has values of* $V_{GS\,(off)} = -8V$ *and* $I_{DSS} = 16$ *mA. Determine the values of* V_{GS}, I_D *and* V_{DS} *for the circuit.*

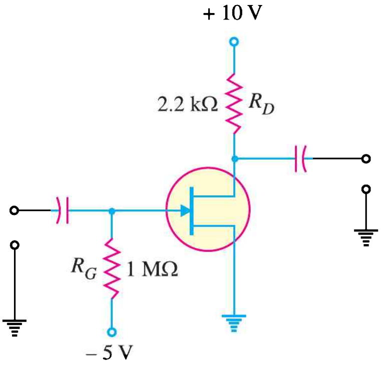


Fig. 19.19

Solution. Since there is no gate current, there will be no voltage drop across R_G.

$$\therefore \qquad V_{GS} = V_{GG} = \mathbf{-5V}$$

$$\text{Now} \qquad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 16 \text{ mA}\left(1 - \frac{-5}{-8}\right)^2$$

$$= 16 \text{ mA } (0.1406) = \mathbf{2.25\ mA}$$

$$\text{Also} \qquad V_{DS} = V_{DD} - I_D R_D$$

$$= 10 \text{ V} - 2.25 \text{ mA} \times 2.2 \text{ k}\Omega = \mathbf{5.05\ V}$$

Note that operating point for the circuit is 5.05V, 2.25 mA.

19.18 Self-Bias for JFET

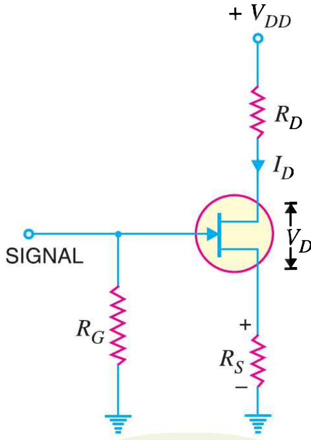


Fig. 19.20

Fig. 19.20 shows the self-bias method for *n*-channel *JFET*. The resistor R_S is the bias resistor. The d.c. component of drain current flowing through R_S produces the desired bias voltage.

$$\text{Voltage across } R_S,\ V_S = I_D R_S$$

Since gate current is negligibly small, the gate terminal is at d.c. ground *i.e.*, $V_G = 0$.

$$\therefore \qquad V_{GS} = V_G - V_S = 0 - I_D R_S$$

$$\text{or} \qquad V_{GS} = -{}^{*}I_D R_S$$

Thus bias voltage V_{GS} keeps gate negative *w.r.t.* source.

---

* $V_{GS} = V_G - V_S$ = Negative. This means that V_G is negative w.r.t. V_S. Thus if V_G = 2V and V_S = 4V, then V_{GS} = 2 – 4 = – 2V *i.e.* gate is less positive than the source. Again if V_G = 0V and V_S = 2V, then V_{GS} = 0 – 2 = – 2V. Note that V_G is less positive than V_S.

Operating point. The operating point (*i.e.*, zero signal I_D and V_{DS}) can be easily determined. Since the parameters of the *JFET* are usually known, zero signal I_D can be calculated from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

Also $$V_{DS} = V_{DD} - I_D\,(R_D + R_S)$$

Thus d.c. conditions of *JFET* amplifier are fully specified *i.e.* operating point for the circuit is V_{DS}, I_D.

Also, $$R_S = \frac{|V_{GS}|}{|I_D|}$$

Note that gate resistor *R_G does not affect bias because voltage across it is zero.

Midpoint Bias. It is often desirable to bias a *JFET* near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. When signal is applied, the midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0. It can be proved that when $V_{GS} = V_{GS\,(off)}/3.4$, midpoint bias conditions are obtained for I_D.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS\,(off)}/3.4}{V_{GS\,(off)}}\right)^2 = 0.5\,I_{DSS}$$

To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop.

Example 19.13. *Find V_{DS} and V_{GS} in Fig. 19.21, given that I_D = 5 mA.*

Solution.

$$V_S = I_D R_S = (5\text{ mA})\,(470\ \Omega) = 2.35\text{ V}$$

and $$V_D = V_{DD} - I_D R_D$$
$$= 15\text{V} - (5\text{ mA}) \times (1\text{ k}\Omega) = 10\text{V}$$

$$\therefore \quad V_{DS} = V_D - V_S = 10\text{V} - 2.35\text{ V} = \mathbf{7.65V}$$

Since there is no gate current, there will be no voltage drop across R_G and $V_G = 0$.

Now $$V_{GS} = V_G - V_S = 0 - 2.35\text{V} = \mathbf{-\,2.35\ V}$$

Example 19.14. *The transfer characteristic of a JFET reveals that when $V_{GS} = -5V$, I_D = 6.25 mA. Determine the value of R_S required.*

Solution.

$$R_S = \frac{|V_{GS}|}{|I_D|} = \frac{5\text{V}}{6.25\text{ mA}} = \mathbf{800\ \Omega}$$

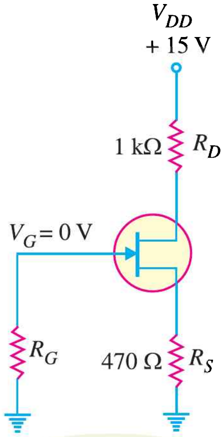


Fig. 19.21

Example 19.15. *Determine the value of R_S required to self-bias a p-channel JFET with I_{DSS} = 25 mA, $V_{GS\,(off)}$ = 15 V and V_{GS} = 5V.*

Solution.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2 = 25\text{ mA}\left(1 - \frac{5\text{ V}}{15\text{ V}}\right)^2 = 25\text{mA}\ (1 - 0.333)^2 = 11.1\text{ mA}$$

$$\therefore \quad R_S = \frac{|V_{GS}|}{|I_D|} = \frac{5\text{V}}{11.1\text{ mA}} = \mathbf{450\ \Omega}$$

---

* R_G is necessary only to isolate an a.c. signal from ground in amplifier applications.

Example 19.16. *Select resistor values in Fig. 19.22 to set up an approximate midpoint bias. The JFET parameters are : I_{DSS} = 15 mA and $V_{GS\,(off)}$ = – 8V. The voltage V_D should be 6V (one-half of V_{DD}).*

Solution. For midpoint bias, we have,

$$I_D \simeq \frac{I_{DSS}}{2} = \frac{15\text{ mA}}{2} = 7.5\text{ mA}$$

and
$$V_{GS} = \frac{V_{GS\,(off)}}{3.4} = \frac{-8}{3.4} = -2.35\text{ V}$$

∴
$$R_S = \frac{|V_{GS}|}{|I_D|} = \frac{2.35\text{V}}{7.5\text{ mA}} = \mathbf{313\Omega}$$

Now
$$V_D = V_{DD} - I_D R_D$$

∴
$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12\text{V} - 6\text{V}}{7.5\text{ mA}} = \mathbf{800\Omega}$$

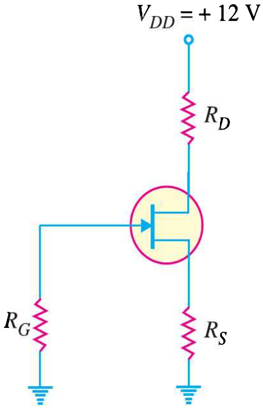


Fig. 19.22

Example 19.17. *In a self-bias n-channel JFET, the operating point is to be set at I_D = 1.5 mA and V_{DS} =10 V. The JFET parameters are I_{DSS} = 5 mA and $V_{GS\,(off)}$ = – 2 V. Find the values of R_S and R_D. Given that V_{DD} = 20 V.*

Solution. Fig. 19.23 shows the circuit arrangement.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

or
$$1.5 = 5\left(1 + \frac{V_{GS}}{2}\right)^2$$

or
$$1 + \frac{V_{GS}}{2} = \sqrt{1.5/5} = 0.55$$

or
$$V_{GS} = -0.9\text{ V}$$

Now
$$V_{GS} = V_G - V_S$$

or
$$V_S = V_G - V_{GS}$$
$$= 0 - (-0.9) = 0.9\text{ V}$$

∴
$$R_S = \frac{V_S}{I_D} = \frac{0.9\text{ V}}{1.5\text{ mA}} = \mathbf{0.6\ k\,\Omega}$$

Applying Kirchhoff's voltage law to the drain circuit, we have,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

or
$$20 = 1.5\text{ mA} \times R_D + 10 + 0.9$$

∴
$$R_D = \frac{(20 - 10 - 0.9)\text{ V}}{1.5\text{ mA}} = \mathbf{6\ k\,\Omega}$$

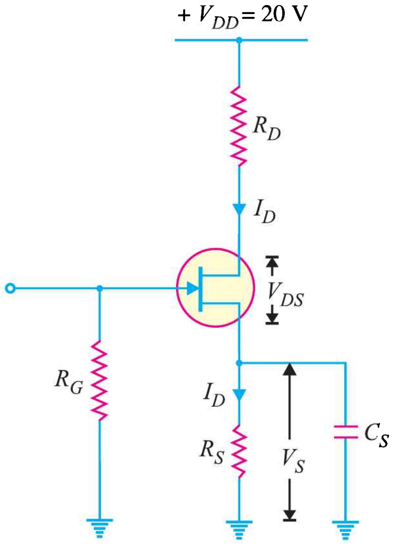


Fig. 19.23

Example 19.18. *In the JFET circuit shown in Fig. 19.24, find (i) V_{DS} and (ii) V_{GS}.*

Solution.

(i) $V_{DS} = V_{DD} - I_D(R_D + R_S) = 30 - 2.5\text{ mA}\,(5 + 0.2) = 30 - 13 = \mathbf{17\ V}$

(ii) $V_{GS} = -I_D R_S = -(2.5 \times 10^{-3}) \times 200 = \mathbf{-0.5\ V}$

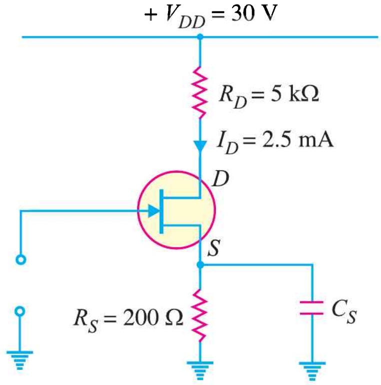

+ V_{DD} = 30 V
R_D = 5 kΩ
I_D = 2.5 mA
D
S
R_S = 200 Ω
C_S

Fig. 19.24

Example 19.19. *Figure 19.25 shows two stages of JFET amplifier. The first stage has* I_D = *2.15mA and the second stage has* I_D = *9.15mA. Find the d.c. voltage of drain and source of each stage w.r.t. ground.*

Solution. Voltage drop in 8.2 kΩ = 2.15 mA × 8.2 kΩ = 17.63 V

D.C. potential of drain of first stage *w.r.t.* ground is

$$V_D = V_{DD} - 17.63 = 30 - 17.63 = \mathbf{12.37\ V}$$

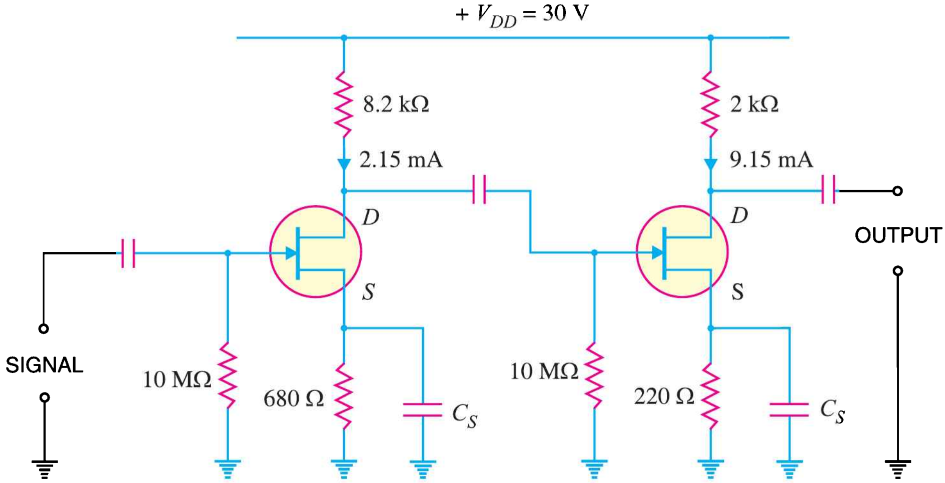

+ V_{DD} = 30 V
8.2 kΩ
2.15 mA
2 kΩ
9.15 mA
D
D
OUTPUT
S
S
SIGNAL
10 MΩ
680 Ω
C_S
10 MΩ
220 Ω
C_S

Fig. 19.25

D.C. potential of source of first stage to ground is

$$V_S = I_D R_S = 2.15\text{ mA} \times 0.68\text{ k}\Omega = \mathbf{1.46\ V}$$

$$\text{Voltage drop in 2 k}\Omega = 9.15\text{ mA} \times 2\text{ k}\Omega = 18.3\text{ V}$$

D.C. potential of drain of second stage to ground is

$$V_D = V_{DD} - 18.3 = 30 - 18.3 = \mathbf{11.7\ V}$$

D.C. potential of source of second stage to ground is

$$V_S = I_D R_S = 9.15\text{ mA} \times 0.22\text{ k}\Omega = \mathbf{2.01\ V}$$

19.19 JFET with Voltage-Divider Bias

Fig. 19.26 shows potential divider method of biasing a *JFET*. This circuit is identical to that used for a transistor. The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 (= V_G)across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $\quad V_2 = V_{GS} + I_D R_S$

or $\quad V_{GS} = V_2 - I_D R_S$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under :

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

and $\quad V_{DS} = V_{DD} - I_D (R_D + R_S)$

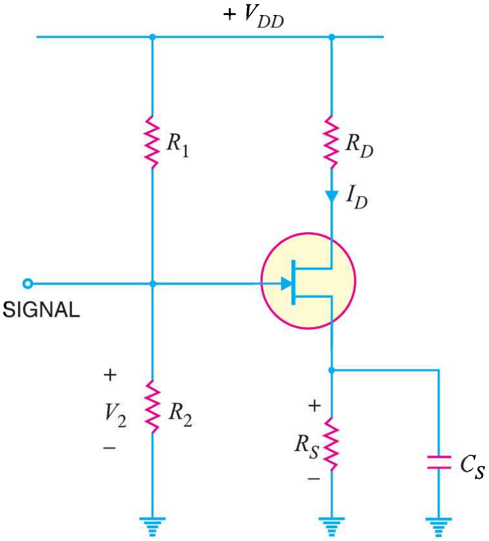


Fig. 19.26

Although the circuit of voltage-divider bias is a bit complex, yet the advantage of this method of biasing is that it provides good stability of the operating point. The input impedance Z_i of this circuit is given by ;

$$Z_i = R_1 \parallel R_2$$

Example 19.20. *Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig. 19.27, given that V_D = 7V.*

Solution.

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{V} - 7\text{V}}{3.3\text{ k}\Omega}$$

$$= \frac{5\text{V}}{3.3\text{ k}\Omega} = \mathbf{1.52\ mA}$$

$$V_S = I_D R_S = (1.52\text{ mA})\ (1.8\text{ k}\Omega) = 2.74\text{V}$$

$$V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2 = \frac{12\text{V}}{7.8\text{ M}\Omega} \times 1\text{ M}\Omega = 1.54\text{V}$$

$$\therefore \quad V_{GS} = V_G - V_S = 1.54\text{ V} - 2.74\text{ V} = \mathbf{-\ 1.2V}$$

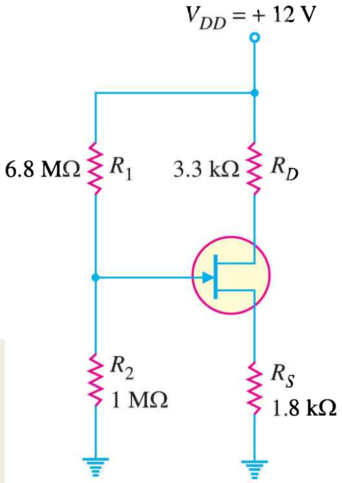


Fig. 19.27

Example 19.21. *In an n-channel JFET biased by potential divider method, it is desired to set the operating point at I_D = 2.5 mA and V_{DS} = 8V. If V_{DD} = 30 V, R_1 = 1 MΩ and R_2 = 500 kΩ, find the value of R_S. The parameters of JFET are I_{DSS} = 10 mA and $V_{GS\ (off)}$ = – 5 V.*

Solution. Fig. 19.28 shows the conditions of the problem.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

or $$2.5 = 10\left(1 + \frac{V_{GS}}{5}\right)^2$$

or $$1 + \frac{V_{GS}}{5} = \sqrt{2.5/10} = 0.5$$

or $$V_{GS} = -2.5 \text{ V}$$

Now, $$V_2 = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{30}{1000 + 500} \times 500$$

$$= 10 \text{ V}$$

Now $$V_2 = V_{GS} + I_D R_S$$

or $$10 \text{ V} = -2.5 \text{ V} + 2.5 \text{ mA} \times R_S$$

$$\therefore \quad R_S = \frac{10 \text{ V} + 2.5 \text{ V}}{2.5 \text{ mA}} = \frac{12.5 \text{ V}}{2.5 \text{ mA}}$$

$$= \mathbf{5\ k\Omega}$$

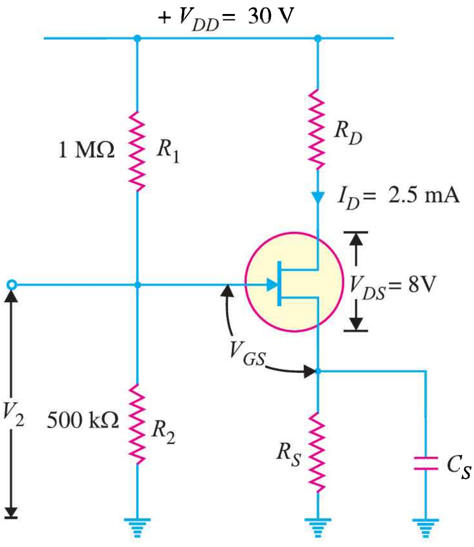


Fig. 19.28

19.20 JFET Connections

There are three leads in a *JFET viz.*, source, gate and drain terminals. However, when *JFET* is to be connected in a circuit, we require four terminals ; two for the input and two for the output. This difficulty is overcome by making one terminal of the *JFET* common to both input and output terminals. Accordingly, a *JFET* can be connected in a circuit in the following three ways :

(*i*) Common source connection **(*ii*)** Common gate connection

(*iii*) Common drain connection

The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and a moderate output impedance. However, the circuit produces a phase reversal *i.e.*, output signal is 180° out of phase with the input signal. Fig. 19.29 shows a common source *n*-channel *JFET* amplifier. Note that source terminal is common to both input and output.

Note. A common source *JFET* amplifier is the *JFET* equivalent of common emitter amplifier. Both amplifiers have a 180° phase shift from input to output. Although the two amplifiers serve the same basic purpose, the means by which they operate are quite different.

19.21 Practical JFET Amplifier

It is important to note that a *JFET* can accomplish faithful amplification only if proper associated circuitry is used. Fig. 19.29 shows the practical circuit of a *JFET*. The gate resistor R_G serves two purposes. It keeps the gate at approximately 0 V dc ($\because$ gate current is nearly zero) and its large value (usually several megaohms) prevents loading of the a.c. signal source. The bias voltage is created by the drop across R_S. The bypass capacitor C_S bypasses the a.c. signal and thus keeps the source of the *JFET* effectively at a.c. ground. The coupling capacitor C_{in} couples the signal to the input of *JFET* amplifier.

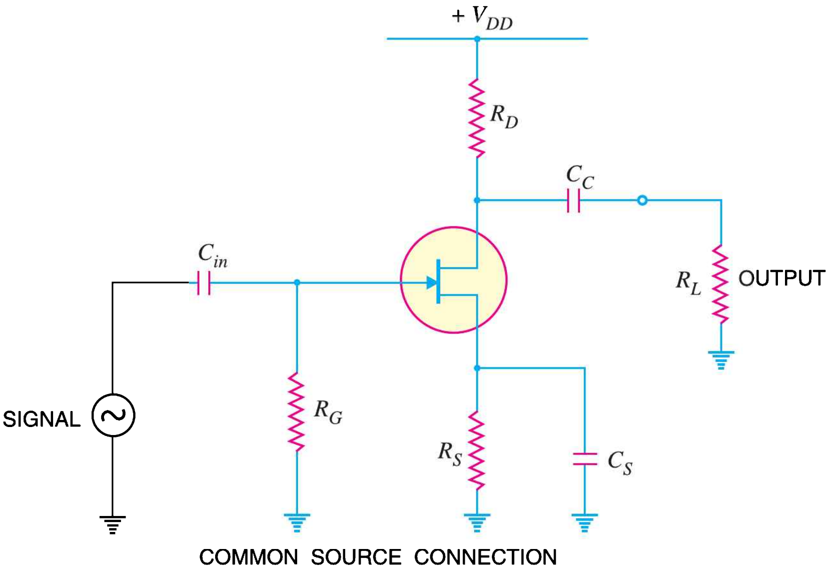


Fig. 19.29

19.22 D.C. and A.C. Equivalent Circuits of JFET

Like in a transistor amplifier, both d.c. and a.c. conditions prevail in a *JFET* amplifier. The d.c. sources set up d.c. currents and voltages whereas the a.c. source (*i.e.* signal) produces fluctuations in the *JFET* currents and voltages. Therefore, a simple way to analyse the action of a *JFET* amplifier is to split the circuit into two parts *viz. d.c. equivalent circuit* and *a.c. equivalent circuit.* The d.c. equivalent circuit will determine the operating point (d.c. bias levels) for the circuit while a.c. equivalent circuit determines the output voltage and hence voltage gain of the circuit.

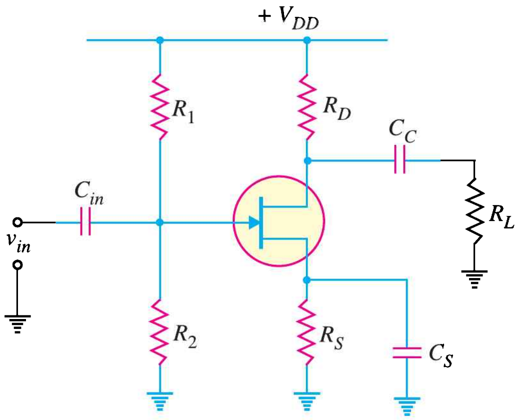


Fig. 19.30

We shall split the *JFET* amplifier shown in Fig. 19.30 into d.c. and a.c. equivalent circuits. Note that biasing is provided by voltage-divider circuit.

1. **D. C. equivalent circuit.** In the d.c. equivalent circuit of a *JFET* amplifier, only d.c. conditions are considered *i.e.* it is presumed that no signal is applied. As direct current cannot

flow through a capacitor, *all the capacitors look like open circuits in the d.c. equivalent circuit.* It follows, therefore, that in order to draw the d.c. equivalent circuit, the following two steps are applied to the *JFET* amplifier circuit :

(*i*) Reduce all a.c. sources to zero.

(*ii*) Open all the capacitors.

Applying these two steps to the *JFET* amplifier circuit shown in Fig. 19.30, we get the d.c. equivalent circuit shown in Fig. 19.31. We can easily calculate the d.c. currents and voltages from this circuit.

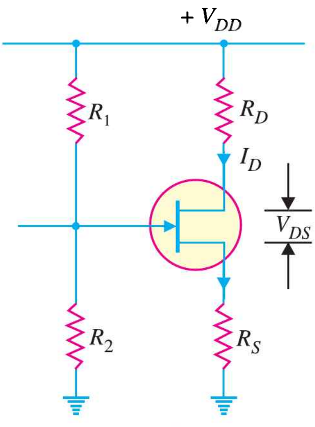


Fig. 19.31

2. A. C. equivalent circuit. In the a.c. equivalent circuit of a *JFET* amplifier, only a.c. conditions are to be considered. Obviously, the d.c. voltage is not important for such a circuit and may be considered zero. The capacitors are generally used to couple or bypass the a.c. signal. The designer intentionally selects capacitors that are large enough to appear as *short circuits* to the a.c. signal. It follows, therefore, that in order to draw the a.c. equivalent circuit, the following two steps are applied to the *JFET* amplifier circuit :

(*i*) Reduce all d.c. sources to zero (*i.e.* $V_{DD} = 0$).

(*ii*) Short all the capacitors.

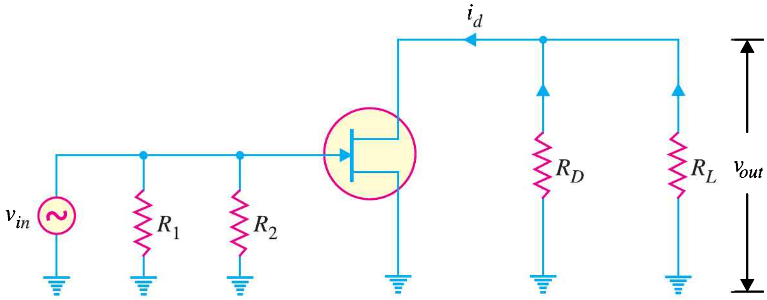


Fig. 19.32

Applying these two steps to the circuit shown in Fig. 19.30, we get the a.c. *equivalent circuit shown in Fig. 19.32. We can easily calculate the a.c. currents and voltages from this circuit.

19.23 D.C. Load Line Analysis

The operating point of a *JFET* amplifier can be determined graphically by drawing d.c. load line on the drain characteristics ($V_{DS} - I_D$ curves). This method is identical to that used for transistors.

The d.c. equivalent circuit of a *JFET* amplifier using voltage-divider bias is shown in Fig. 19.33 (*i*). It is clear that :

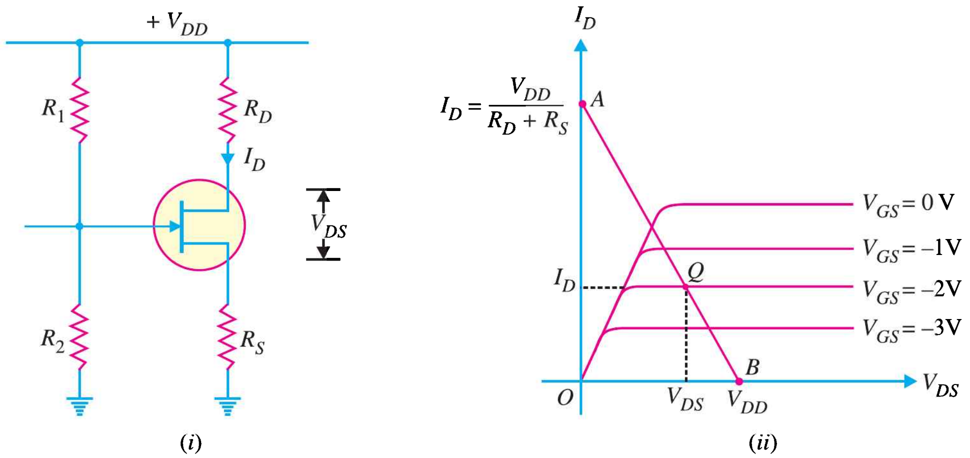
$$V_{DD} = V_{DS} + I_D (R_D + R_S)$$

or

$$V_{DS} = V_{DD} - I_D (R_D + R_S) \qquad \text{... } (i)$$

---

* Note that one end of R_1 and R_2 is connected to one point (See Fig. 19.30) and the other end of R_1 and R_2 is connected to ground. Therefore, $R_1 \parallel R_2$. Similar is the case with R_D and R_L so that $R_D \parallel R_L$.



+ V_{DD}
R_1
R_D
I_D
V_{DS}
R_2
R_S
(i)
I_D
$I_D = \frac{V_{DD}}{R_D + R_S}$
A
V_{GS} = 0 V
V_{GS} = –1V
V_{GS} = –2V
V_{GS} = –3V
Q
I_D
B
O
V_{DS}
V_{DD}
V_{DS}
(ii)

Fig. 19.33

As for a given circuit, V_{DD} and $(R_D + R_S)$ are constant, therefore, exp. (*i*) is a first degree equation and can be represented by a straight line on the drain characteristics. This is known as d.c. load line for *JFET* and determines the locus of I_D and V_{DS} (*i.e.* operating point) in the absence of the signal. The d.c. load line can be readily plotted by locating the *two end points* of the straight line.

(*i*) The value of V_{DS} will be maximum when $I_D = 0$. Therefore, by putting $I_D = 0$ in exp. (*i*) above, we get,

$$\text{Max. } V_{DS} = V_{DD}$$

This locates the first point B ($OB = V_{DD}$) of the d.c. load line on drain-source voltage axis.

(*ii*) The value of I_D will be maximum when $V_{DS} = 0$.

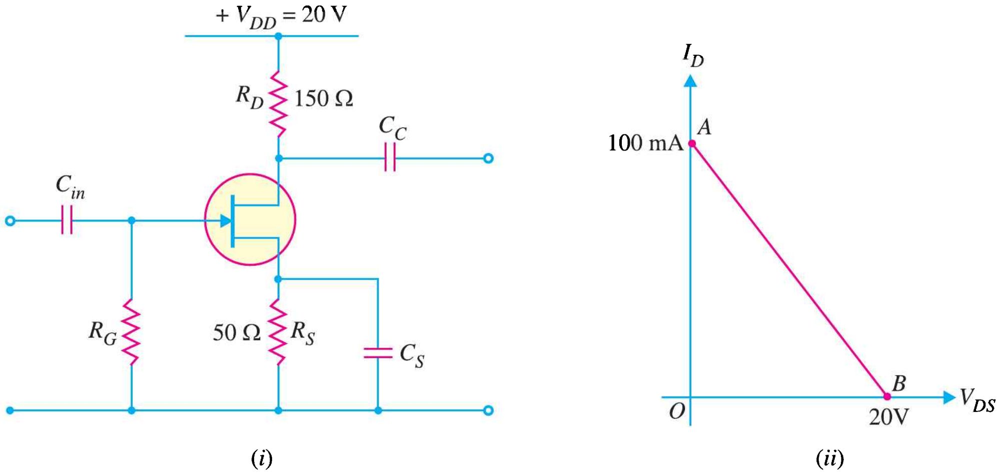
$$\therefore \quad \text{Max. } I_D = \frac{V_{DD}}{R_D + R_S}$$

This locates the second point A ($OA = V_{DD} / R_D + R_S$) of the d.c. load line on drain current axis.

By joining points A and B, d.c. load line AB is constructed [See Fig. 19.33 (*ii*)].

The operating point Q is located at the intersection of the d.c. load line and the drain curve which corresponds to V_{GS} provided by biasing. If we assume in Fig. 19.33 (*i*) that $V_{GS} = -2$V, then point Q is located at the intersection of the d.c. load line and the $V_{GS} = -2$V curve as shown in Fig. 19.33 (*ii*). The I_D and V_{DS} of Q point are marked on the graph.

Example 19.22. *Draw the d.c. load line for the JFET amplifier shown in Fig. 19.34 (i).*



+ V_{DD} = 20 V
R_D
150 Ω
C_C
C_{in}
R_G
50 Ω
R_S
C_S
(i)
I_D
100 mA
A
B
O
20V
V_{DS}
(ii)

Fig. 19.34

Solution. To draw d.c. load line, we require two end points *viz.*, max V_{DS} and max. I_D points.

$$\text{Max. } V_{DS} = V_{DD} = 20\text{V}$$

This locates point *B* (*OB* = 20V) of the d.c. load line.

$$\text{Max. } I_D = \frac{V_{DD}}{R_D + R_S} = \frac{20\text{V}}{(150+50)\ \Omega}$$

$$= \frac{20\text{V}}{200\Omega} = 100 \text{ mA}$$

This locates point *A* (*OA* = 100 mA) of the d.c. load line. Joining *A* and *B*, d.c. load line *AB* is constructed as shown in Fig. 19.34 (*ii*).

Example 19.23. *Draw the d.c. load line for the JFET amplifier shown in Fig. 19.35 (i).*

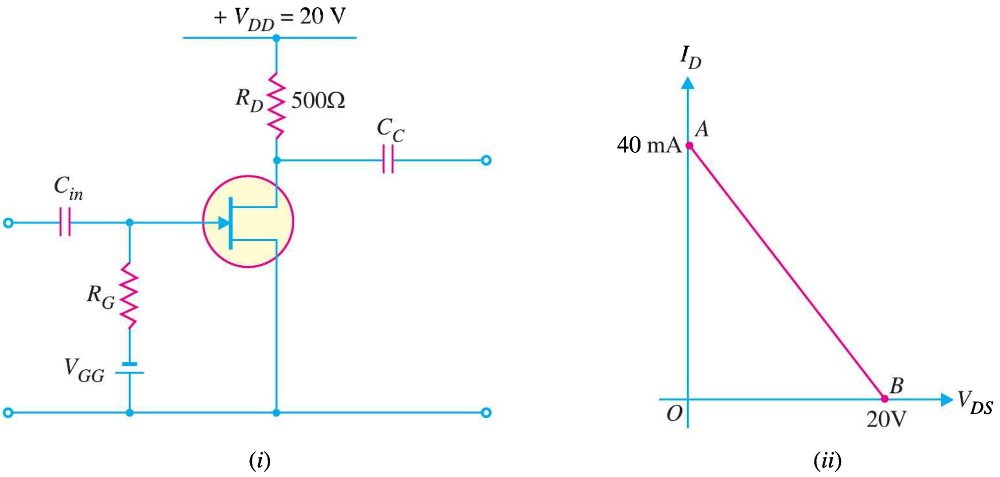


Fig. 19.35

Solution.

$$\text{Max. } V_{DS} = V_{DD} = 20\text{V}$$

This locates the point *B* (*OB* = 20V) of the d.c. load line.

$$\text{Max. } I_D = \frac{V_{DD}}{R_D} = \frac{20\text{V}}{500\Omega} = 40 \text{ mA}$$

This locates the point *A* (*OA* = 40 mA) of the d.c. load line.

Fig. 19.35 (*ii*) shows the d.c. load line *AB*.

19.24 Voltage Gain of JFET Amplifier

The a.c. equivalent circuit of *JFET* amplifier was developed in Art. 19.22 and is redrawn as Fig. 19.36 (*i*) for facility of reference. Note that $R_1 \parallel R_2$ and can be replaced by a single resistance R_T. Similarly, $R_D \parallel R_L$ and can be replaced by a single resistance R_{AC} (= total a.c. drain resistance). The a.c. equivalent circuit shown in Fig. 19.36 (*i*) then reduces to the one shown in Fig. 19.36 (*ii*).

We now find the expression for voltage gain of this amplifier. Referring to Fig. 19.36 (*ii*), output voltage (v_{out}) is given by ;

$$v_{out} = i_d R_{AC} \qquad \ldots (i)$$

Remember that we define g_m as :

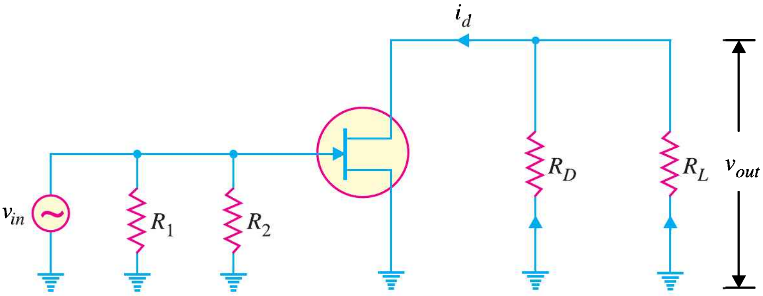

i_d
v_{in}
R_1
R_2
R_D
R_L
v_{out}

Fig. 19.36 (*i*)

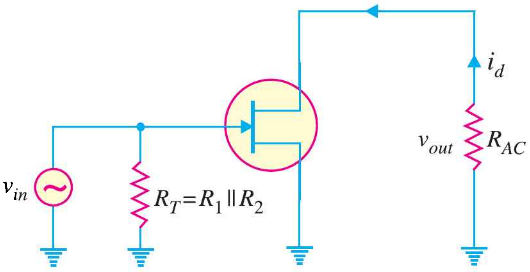

i_d
v_{out}
R_{AC}
v_{in}
$R_T = R_1 \| R_2$

Fig. 19.36 (*ii*)

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

or $$g_m = \frac{i_d}{v_{gs}}$$

or $$i_d = g_m v_{gs}$$

Putting the value of i_d (= $g_m v_{gs}$) in eq. (*i*), we have,

$$v_{out} = g_m v_{gs} R_{AC}$$

Now $v_{in} = v_{gs}$ so that a.c. output voltage is

$$v_{out} = g_m v_{in} R_{AC}$$

or $$v_{out}/v_{in} = g_m R_{AC}$$

But v_{out}/v_{in} is the voltage gain (A_v) of the amplifier.

$\therefore$ Voltage gain, $A_v = g_m R_{AC}$ ... for loaded amplifier

$= g_m R_D$ ... for unloaded amplifier

Example 19.24. *The JFET in the amplifier of Fig. 19.37 has a transconductance g_m = 1 mA/V. If the source resistance R_S is very small as compared to R_G, find the voltage gain of the amplifier.*

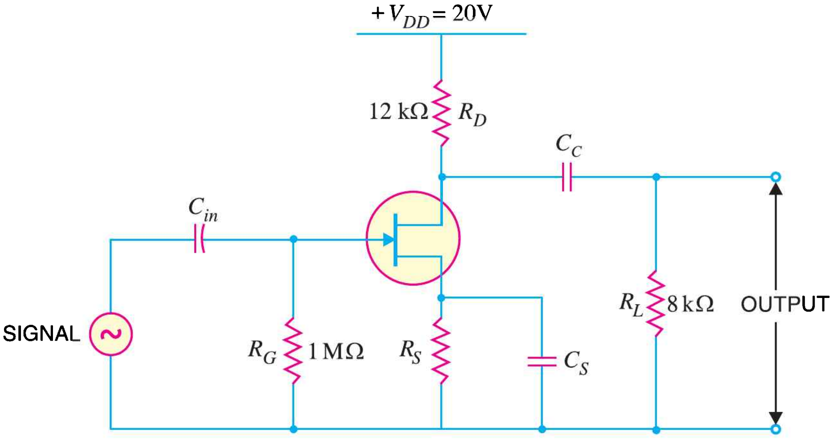

$+V_{DD} = 20V$
12 kΩ
R_D
C_C
C_{in}
SIGNAL
R_G
1 MΩ
R_S
C_S
R_L
8 kΩ
OUTPUT

Fig. 19.37

Solution.

Transconductance of *JFET*, g_m = 1 mA/V

$$= 1000\ \mu\text{ mho} = 1000 \times 10^{-6}\text{ mho}$$

The total *ac* load (*i.e.* R_{AC}) in the drain circuit consists of the parallel combination of R_D and R_L *i.e.*

$$\text{Total a.c. load, } R_{AC} = R_D \parallel R_L$$

$$= 12\text{ k}\Omega \parallel 8\text{ k}\Omega = \frac{12 \times 8}{12 + 8} = 4.8\text{ k}\Omega$$

$$\therefore \quad \text{Voltage gain, } A_v = g_m \times R_{AC}$$

$$= (1000 \times 10^{-6}) \times (4.8 \times 10^3) = \mathbf{4.8}$$

Example 19.25. *The transconductance of a JFET used as a voltage amplifier is 3000 μmho and drain resistance is 10 kΩ. Calculate the voltage gain of the amplifier.*

Solution.

$$\text{Transconductance of } JFET,\ g_m = 3000\ \mu\text{mho} = 3000 \times 10^{-6}\text{ mho}$$

$$\text{Drain resistance, } R_D = 10\text{ k}\Omega = 10 \times 10^3\Omega$$

$$\therefore \quad \text{Voltage gain, } A_v = g_m R_D = (3000 \times 10^{-6})(10 \times 10^3) = \mathbf{30}$$

Example 19.26. *What is the r.m.s. output voltage of the unloaded amplifier in Fig. 19.38? The* $I_{DSS} = 8$ *mA,* $V_{GS\,(off)} = -10V$ *and* $I_D = 1.9$ *mA.*

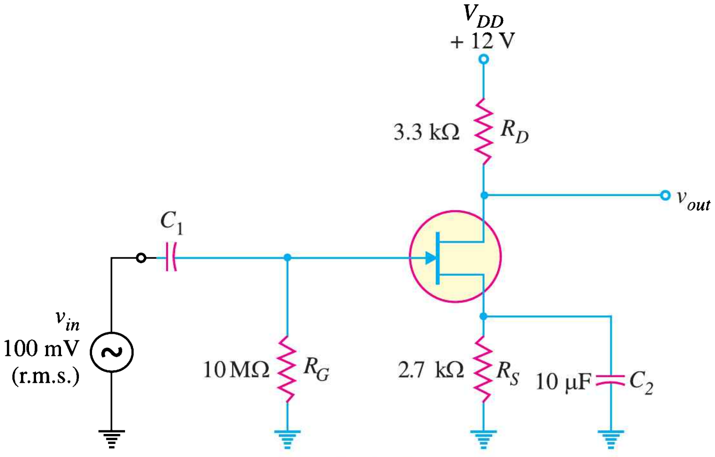


Fig. 19.38

Solution.

$$V_{GS} = -I_D R_S = -1.9\text{ mA} \times 2.7 \times 10^3\Omega = -5.13\text{V}$$

$$g_{mo} = \frac{2\,I_{DSS}}{|V_{GS\,(off)}|} = \frac{2 \times 8\text{ mA}}{10\text{ V}} = 1.6 \times 10^{-3}\text{S}$$

$$\therefore \quad g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right) = 1.6 \times 10^{-3}\left(1 - \frac{-5.13\text{V}}{-10\text{V}}\right) = 779 \times 10^{-6}\text{ S}$$

$$\text{Voltage gain, } A_v = g_m R_D = (779 \times 10^{-6})(3.3 \times 10^3) = 2.57$$

$$\therefore \quad \text{Output voltage, } v_{out} = A_v v_{in} = 2.57 \times 100\text{ mV} = \mathbf{257\ mV\ (r.m.s.)}$$

Example 19.27. *If a 4.7 kΩ load resistor is a.c. coupled to the output of the amplifier in Fig. 19.38 above, what is the resulting r.m.s. output voltage?*

Solution. The value of g_m remains the same. However, the value of total a.c. drain resistance R_{AC} changes due to the connection of load R_L (= 4.7 kΩ).

$$\text{Total a.c. drain resistance, } R_{AC} = R_D \parallel R_L$$

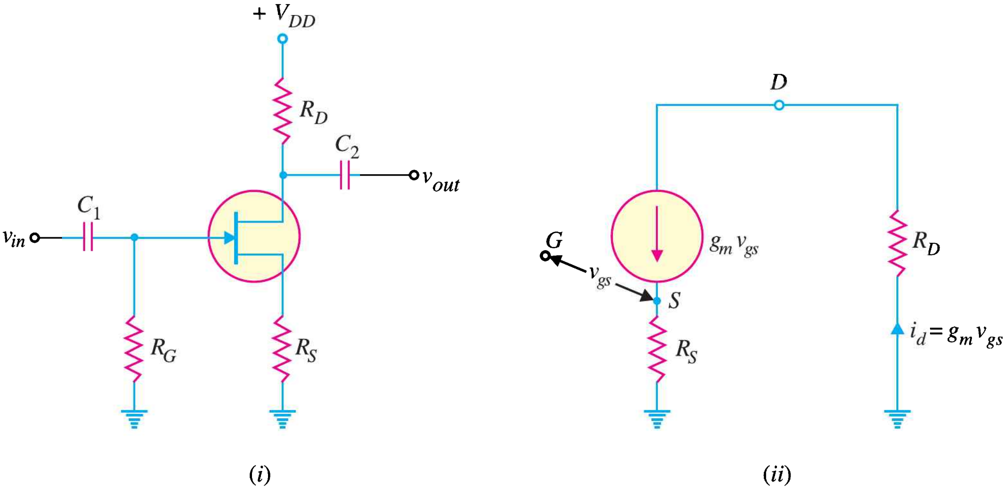
$$= \frac{R_D R_L}{R_D + R_L} = \frac{(3.3\,\text{k}\Omega)\,(4.7\,\text{k}\Omega)}{3.3\,\text{k}\Omega + 4.7\,\text{k}\Omega} = 1.94\,\text{k}\Omega$$

$$\therefore \quad \text{Voltage gain, } A_v = g_m R_{AC} = (779 \times 10^{-6})\,(1.94 \times 10^3) = 1.51$$

$$\text{Output voltage, } v_{out} = A_v v_{in} = 1.51 \times 100\,\text{mV} = \mathbf{151\,mV\ (r.m.s.)}$$

19.25 Voltage Gain of JFET Amplifier (*With Source Resistance R_S*)

Fig. 19.39 (*i*) shows the *JFET* amplifier with source resistor R_S unbypassed. This means that a.c. signal will not be bypassed by the capacitor C_S.



(*i*) (*ii*)

Fig. 19.39

Fig. 19.39 (*ii*) shows the simplified a.c. equivalent circuit of the *JFET* amplifier. Since $g_m = i_d / v_{gs}$, a current source $i_d = g_m v_{gs}$ appears between drain and source. Referring to Fig. 19.39 (*ii*),

$$v_{in} = v_{gs} + i_d R_S$$

$$v_{out} = i_d R_D$$

$$\therefore \quad \text{Voltage gain, } A_v = \frac{v_{out}}{v_{in}} = \frac{i_d R_D}{v_{gs} + i_d R_S}$$

$$= \frac{g_m v_{gs} R_D}{v_{gs} + g_m v_{gs} R_S} = \frac{g_m v_{gs} R_D}{v_{gs}(1 + g_m R_S)} \qquad (\because i_d = g_m v_{gs})$$

$$\therefore \quad A_v = \frac{g_m R_D}{1 + g_m R_S} \quad \text{... for unloaded amplifier}$$

$$= \frac{g_m R_{AC}}{1 + g_m R_S} \quad \text{... for loaded amplifier}$$

Note that R_{AC} (= $R_D \,||\, R_L$) is the total a.c. drain resistance.

Example 19.28. *In a JFET amplifier, the source resistance R_S is unbypassed. Find the voltage gain of the amplifier. Given g_m = 4 mS; R_D = 1.5 kΩ and R_S = 560Ω.*

Solution.

$$\text{Voltage gain, } A_v = \frac{g_m R_D}{1 + g_m R_S}$$

Here $g_m = 4\text{mS} = 4 \times 10^{-3} S$; $R_D = 1.5\,\text{k}\Omega = 1.5 \times 10^3 \Omega$; $R_S = 560\Omega$

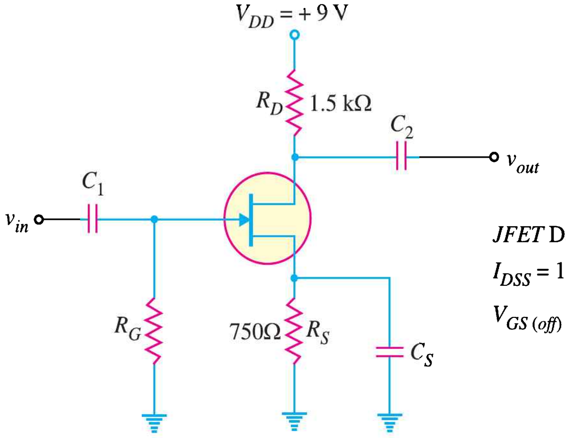
$$\therefore \quad A_v = \frac{(4\times10^{-3})(1.5\times10^{3})}{1+(4\times10^{-3})\,(560)} = \frac{6}{1+2.24} = \mathbf{1.85}$$

If R_S is bypassed by a capacitor, then,

$$A_v = g_m R_D = (4 \times 10^{-3})\,(1.5 \times 10^{3}) = 6$$

Thus with unbypassed R_S, the gain = 1.85 whereas with R_S bypassed by a capacitor, the gain is 6. Therefore, voltage gain is reduced when R_S is unbypassed.

Example 19.29. *For the JFET amplifier circuit shown in Fig. 19.40, calculate the voltage gain with (i) R_S bypassed by a capacitor (ii) R_S unbypassed.*



JFET Data
I_{DSS} = 10 mA
$V_{GS\,(off)}$ = – 3.5V

Fig. 19.40

Solution. From the d.c. bias analysis, we get, *I_D = 2.3 mA and V_{GS} = – 1.8V.

The value of g_m is given by;

$$g_m = \frac{2\,I_{DSS}}{|V_{GS\,(off)}|}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

$$= \frac{2\times10}{3.5}\left(1-\frac{-1.8}{-3.5}\right) = (5.7 \text{ mS})\ (0.486) = 2.77 \text{ mS}$$

(*i*) The voltage gain with R_S bypassed is

$$A_v = g_m R_D = (2.77 \text{ mS})\ (1.5 \text{ k}\Omega) = \mathbf{4.155}$$

(*ii*) The voltage gain with R_S unbypassed is

$$A_v = \frac{g_m R_D}{1+g_m R_S} = \frac{4.155}{1+(2.77 \text{ mS})\ (0.75 \text{ k}\Omega)} = \mathbf{1.35}$$

19.26 JFET Applications

The high input impedance and low output impedance and low noise level make *JFET* far superior to the bipolar transistor. Some of the circuit applications of *JFET* are :

---

* $$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS\,(off)}}\right]^2 \text{ and } V_{GS} = -I_D R_S$$

The unknown quantities V_{GS} and I_D can be found from these two equations.

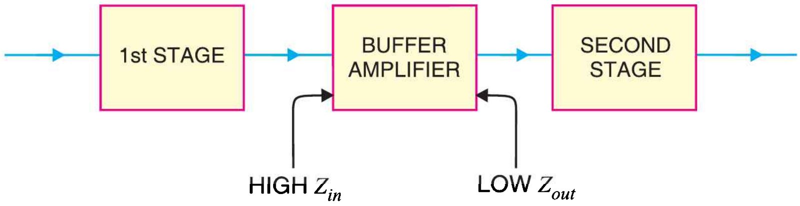


Fig. 19.41

(*i*) **As a buffer amplifier.** A buffer amplifier is a stage of amplification that isolates the preceding stage from the following stage. Because of the high input impedance and low output impedance, a *JFET* can act as an excellent buffer amplifier (See Fig. 19.41). The high input impedance of *JFET* means light loading of the preceding stage. This permits almost the entire output from first stage to appear at the buffer input. The low output impedance of *JFET* can drive heavy loads (or small load resistances). This ensures that all the output from the buffer reaches the input of the second stage.

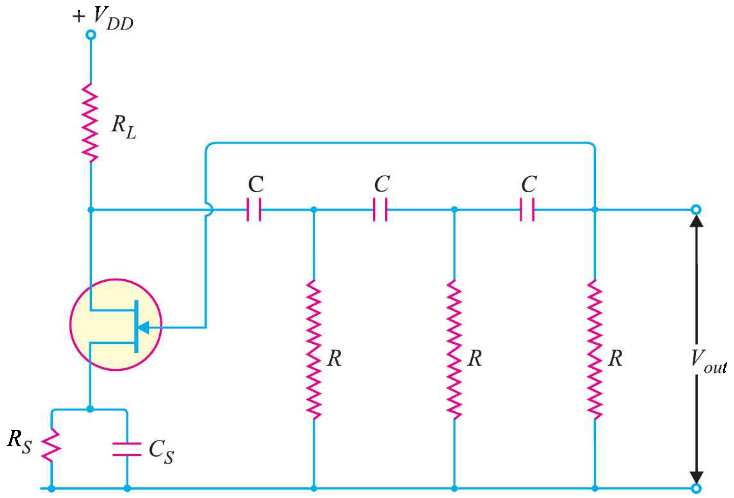


Fig. 19.42

(*ii*) **Phase-shift oscillators.** The oscillators discussed in chapter 14 will also work with *JFETs*. However, the high input impedance of *JFET* is especially valuable in phase-shift oscillators to minimise the loading effect. Fig. 19.42 shows the phase-shift oscillator using *n*-channel *JFET*.

(*iii*) **As RF amplifier.** In communication electronics, we have to use *JFET RF* amplifier in a receiver instead of *BJT* amplifier for the following reasons :

(*a*) The noise level of *JFET* is very low. The *JFET* will not generate significant amount of noise and is thus useful as an *RF* amplifier.

(*b*) The antenna of the receiver receives a very weak signal that has an extremely low amount of current. Since *JFET* is a voltage controlled device, it will well respond to low current signal provided by the antenna.

19.27 Metal Oxide Semiconductor FET (MOSFET)

The main drawback of *JFET* is that its gate *must* be reverse biased for proper operation of the device *i.e.* it can only have negative gate operation for *n*-channel and positive gate operation for *p*-channel. This means that we can *only* decrease the width of the channel (*i.e.* decrease the *conductivity of the channel) from its zero-bias size. This type of operation is referred to as ***depletion-mode* operation. Therefore, a *JFET* can only be operated in the depletion-mode. However, there is a field effect transistor (*FET*) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) *i.e.* it can have *enhancement-mode* operation. Such a *FET* is called *MOSFET*.

A field effect transistor (FET) that can be operated in the enhancement-mode is called a ***MOSFET****.*

A *MOSFET* is an important semiconductor device and can be used in any of the circuits covered for *JFET*. However, a *MOSFET* has several advantages over *JFET* including high input impedance and low cost of production.

19.28 Types of MOSFETs

There are two basic types of *MOSFETs viz.*

1. Depletion-type *MOSFET* or ***D-MOSFET.*** The *D-MOSFET* can be operated in both the depletion-mode and the enhancement-mode. For this reason, a *D-MOSFET* is sometimes called depletion/enhancement *MOSFET*.
2. Enhancement-type *MOSFET* or ***E-MOSFET.*** The *E-MOSFET* can be operated *only* in enhancement-mode.

The manner in which a *MOSFET* is constructed determines whether it is *D-MOSFET* or *E-MOSFET*.

1. D-MOSFET. Fig. 19.43 shows the constructional details of *n*-channel *D-MOSFET*. It is similar to *n*-channel *JFET* except with the following modifications/remarks :

(i) The *n*-channel *D-MOSFET* is a piece of *n*-type material with a *p*-type region (called *substrate*) on the right and an *insulated gate* on the left as shown in Fig. 19.43. The free electrons (∵ it is *n*-channel) flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region (*i.e.* substrate).

(ii) Note carefully the gate construction of *D-MOSFET*. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric. Recall that we have a gate diode in a *JFET*.

(iii) It is a usual practice to connect the substrate to the source (*S*) internally so that a *MOSFET* has three terminals *viz source* (*S*), *gate* (*G*) and *drain* (*D*).

(iv) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, *D-MOSFET* can be operated in both depletion-mode and enhancement-mode. However, *JFET* can be operated only in depletion-mode.

---

* With the decrease in channel width, the X-sectional area of the channel decreases and hence its resistance increases. This means that conductivity of the channel will decrease. Reverse happens if channel width increases.

** With gate reverse biased, the channel is depleted (*i.e.* emptied) of charge carriers (free electrons for *n*-channel and holes for *p*-channel) and hence the name depletion-mode. Note that depletion means decrease. In this mode of operation, conductivity decreases from the zero-bias level.

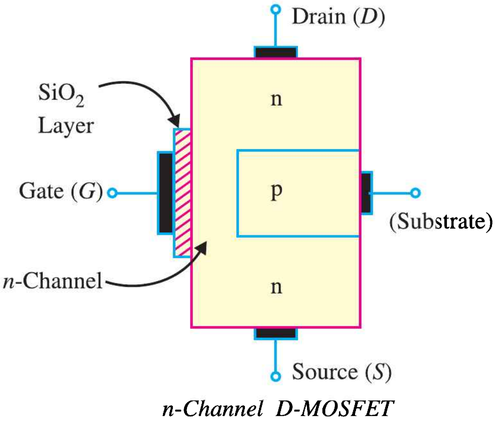

Drain (D)
SiO₂ Layer
n
Gate (G)
p
(Substrate)
n-Channel
n
Source (S)
n-Channel D-MOSFET

Fig. 19.43

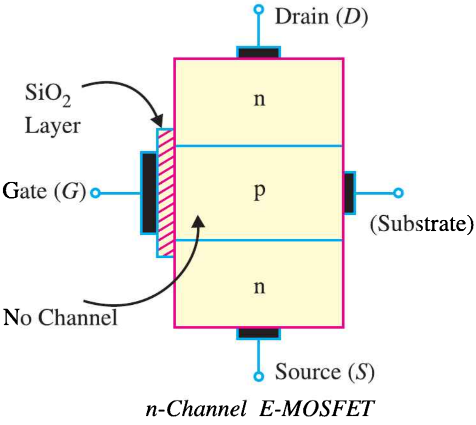

Drain (D)
SiO₂ Layer
n
Gate (G)
p
(Substrate)
n
No Channel
Source (S)
n-Channel E-MOSFET

Fig. 19.44

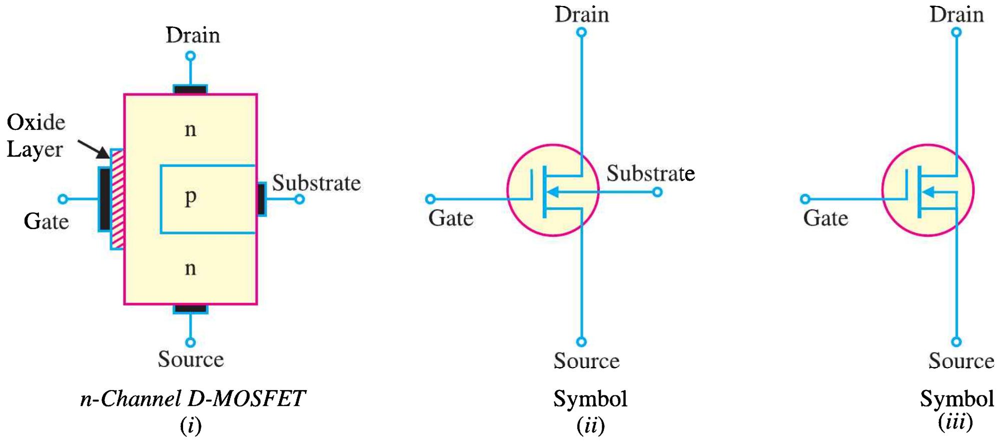
2. E-MOSFET. Fig. 19.44 shows the constructional details of *n*-channel *E-MOSFET*. Its gate construction is similar to that of *D-MOSFET*. The *E-MOSFET* has no channel between source and drain unlike the *D-MOSFET*. Note that the substrate extends completely to the SiO_2 layer so that no channel exists. The *E-MOSFET* requires a proper gate voltage to *form* a channel (called induced channel). It is reminded that *E-MOSFET* can be operated *only* in enhancement mode. In short, the construction of *E-MOSFET* is quite similar to that of the *D-MOSFET* except for the absence of a channel between the drain and source terminals.

Why the name MOSFET ? The reader may wonder why is the device called *MOSFET?* The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor. Thus, going from gate to substrate, you have a ***metal oxide semiconductor*** and hence the name *MOSFET*. Since the gate is insulated from the channel, the *MOSFET* is sometimes called *insulated-gate FET (IGFET)*. However, this term is rarely used in place of the term *MOSFET*.

19.29 Symbols for D-MOSFET

There are two types of *D-MOSFETs viz* (*i*) *n*-channel *D-MOSFET* and (*ii*) *p*-channel *D-MOSFET*.

(*i*) n-channel D-MOSFET. Fig. 19.45 (*i*) shows the various parts of *n*-channel *D-MOSFET*. The *p*-type substrate constricts the channel between the source and drain so that only a small passage


Drain
Oxide Layer
n
p
Substrate
Gate
n
Source
Drain
Substrate
Gate
Source
Drain
Gate
Source

n-Channel D-MOSFET
(*i*)

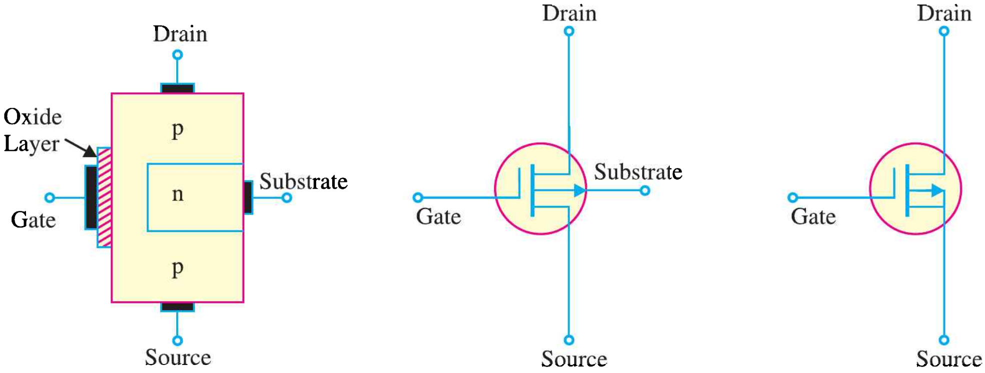
Symbol
(*ii*)

Symbol
(*iii*)

Fig. 19.45

remains at the left side. Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel. The symbol for *n*-channel *D-MOSFET* is shown in Fig. 19.45 (*ii*). The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel. The drain lead comes out of the top of the channel and the source lead connects to the bottom. The arrow is on the substrate and points to the *n*-material, therefore we have *n*-channel *D-MOSFET*. It is a usual practice to connect the substrate to source internally as shown in Fig. 19.45 (*iii*). This gives rise to a three-terminal device.

(*ii*) *p*-channel D-MOSFET. Fig. 19.46 (*i*) shows the various parts of *p*-channel *D-MOSFET*. The *n*-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side. The conduction takes place by the flow of holes from source to drain through this narrow channel. The symbol for *p*-channel *D-MOSFET* is shown in Fig. 19.46 (*ii*). It is a usual practice to connect the substrate to source internally. This results in a three-terminal device whose schematic symbol is shown in Fig. 19.46 (*iii*).



p-Channel D-MOSFET
(*i*)

Symbol
(*ii*)

Symbol
(*iii*)

Fig. 19.46

19.30 Circuit Operation of D-MOSFET

Fig. 19.47 (*i*) shows the circuit of *n*-channel *D-MOSFET*. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric. When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel. Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. The negative-gate operation is called *depletion mode* whereas positive-gate operation is known as *enhancement mode*.

(*i*) Depletion mode. Fig. 19.47 (*i*) shows depletion-mode operation of *n*-channel *D-MOSFET*. Since gate is negative, it means electrons are on the gate as shown is Fig. 19.47 (*ii*). These electrons *repel the free electrons in the *n*-channel, leaving a layer of positive ions in a part of the channel as shown in Fig. 19.47 (*ii*). In other words, we have depleted (*i.e.* emptied) the *n*-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the *n*-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.

Thus by changing the negative voltage on the gate, we can vary the resistance of the *n*-channel and hence the current from source to drain. Note that with negative voltage to the gate, the action of *D-MOSFET* is similar to *JFET*. Because the action with negative gate depends upon depleting (*i.e.* emptying) the channel of free electrons, the negative-gate operation is called *depletion mode*.

---

* If one plate of the capacitor is negatively charged, it induces positive charge on the other plate.

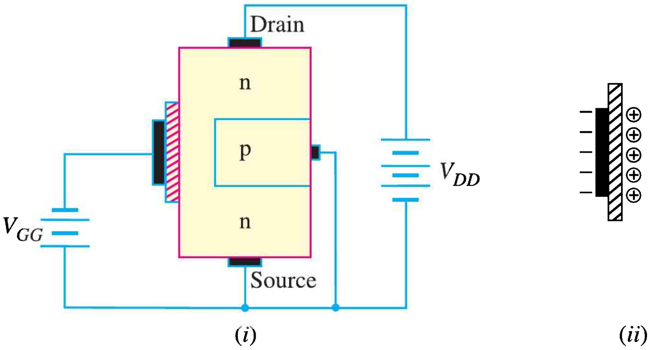


Fig. 19.47

***(ii)* Enhancement mode.** Fig. 19.48 (*i*) shows enhancement-mode operation of *n*-channel *D-MOSFET*. Again, the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the *n*-channel as shown in Fig. 19.48 (*ii*). These negative charges are the free electrons drawn into the channel. Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased. Thus a positive gate voltage *enhances* or *increases* the conductivity of the channel. The greater the positive voltage on the gate, greater the conduction from source to drain.

Thus by changing the positive voltage on the gate, we can change the conductivity of the channel. The main difference between *D-MOSFET* and *JFET* is that we can apply positive gate voltage to *D-MOSFET* and still have essentially *zero current. Because the action with a positive gate depends upon *enhancing* the conductivity of the channel, the positive gate operation is called *enhancement mode*.

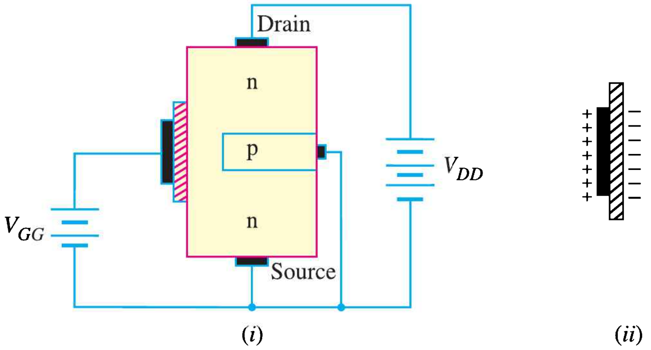


Fig. 19.48

The following points may be noted about *D-MOSFET* operation :

(i) In a *D-MOSFET*, the source to drain current is controlled by the electric field of capacitor formed at the gate.

(ii) The gate of *JFET* behaves as a reverse-biased diode whereas the gate of a *D-MOSFET* acts like a capacitor. For this reason, it is possible to operate *D-MOSFET* with positive or negative gate voltage.

(iii) As the gate of *D-MOSFET* forms a capacitor, therefore, negligible gate current flows whether positive or negative voltage is applied to the gate. For this reason, the input impedance of *D-MOSFET* is very high, ranging from 10,000 MΩ to 10,000,00 MΩ.

---

* Note that gate of *JFET* is always reverse biased for proper operation. However, in a *MOSFET*, because of the insulating layer, a negligible gate current flows whether we apply negative or positive voltage to gate.

(iv) The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the *D-MOSFET* has, therefore, a very low input capacitance. This characteristic makes the *D-MOSFET* useful in high-frequency applications.

19.31 D-MOSFET Transfer Characteristic

Fig. 19.49 shows the transfer characteristic curve (or transconductance curve) for *n*-channel *D-MOSFET*. The behaviour of this device can be beautifully explained with the help of this curve as under :

(i) The point on the curve where $V_{GS} = 0$, $I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted *i.e.* $V_{GS} = 0$.

(ii) As V_{GS} goes *negative*, I_D decreases below the value of I_{DSS} till I_D reaches zero when $V_{GS} = V_{GS\,(off)}$ just as with *JFET*.

(iii) When V_{GS} is *positive*, I_D increases above the value of I_{DSS}. The maximum allowable value of I_D is given on the data sheet of *D-MOSFET*.

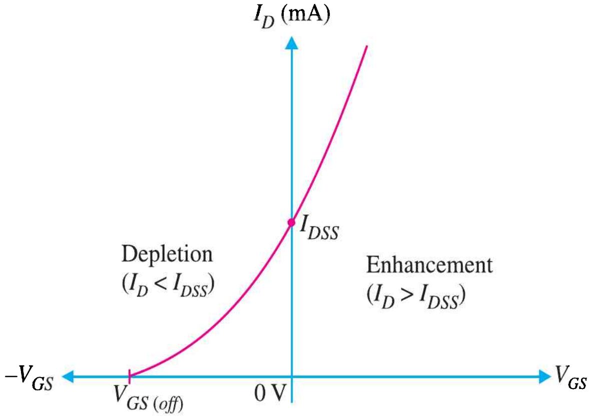


Fig. 19.49

Note that the transconductance curve for the *D-MOSFET* is very similar to the curve for a *JFET*. Because of this similarity, the *JFET* and the *D-MOSFET* have the same transconductance equation *viz.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

Example 19.30. *For a certain D-MOSFET, I_{DSS} = 10 mA and $V_{GS\,(off)} = -8V$.*

(i) Is this an n-channel or a p-channel ?

(ii) Calculate I_D at $V_{GS} = -3V$.

(iii) Calculate I_D at $V_{GS} = +3V$.

Solution.

(i) The device has a negative $V_{GS\,(off)}$. Therefore, it is ***n*-channel *D-MOSFET***.

(ii)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 10\text{ mA}\left(1 - \frac{-3}{-8}\right)^2 = \mathbf{3.91\ mA}$$

(*iii*)
$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 10\,\text{mA}\left(1-\frac{+3V}{-8V}\right)^2 = \mathbf{18.9\ mA}$$

Example 19.31. *A D-MOSFET has parameters of $V_{GS\,(off)} = -6V$ and $I_{DSS} = 1$ mA. How will you plot the transconductance curve for the device ?*

Solution. When $V_{GS} = 0$ V, $I_D = I_{DSS} = 1$ mA and when $V_{GS} = V_{GS\,(off)}$, $I_D = 0$A. This locates two points *viz* I_{DSS} and $V_{GS\,(off)}$ on the transconductance curve. We can locate more points of the curve by *changing V_{GS} values.

When $V_{GS} = -3\text{V}$; $I_D = 1\,\text{mA}\left(1-\frac{-3\text{V}}{-6\text{V}}\right)^2 = 0.25\,\text{mA}$

When $V_{GS} = -1\text{V}$; $I_D = 1\,\text{mA}\left(1-\frac{-1\text{V}}{-6\text{V}}\right)^2 = 0.694\,\text{mA}$

When $V_{GS} = +1\text{V}$; $I_D = 1\,\text{mA}\left(1-\frac{+1\text{V}}{-6\text{V}}\right)^2 = 1.36\,\text{mA}$

When $V_{GS} = +3\text{V}$; $I_D = 1\,\text{mA}\left(1-\frac{+3\text{V}}{-6\text{V}}\right)^2 = 2.25\,\text{mA}$

Thus we have a number of $V_{GS} - I_D$ readings so that transconductance curve for the device can be readily plotted.

19.32 Transconductance and Input Impedance of D-MOSFET

These are important parameters of a *D-MOSFET* and a brief discussion on them is desirable.

(*i*) **D-MOSFET Transconductance (g_m).** The value of g_m is found for a *D-MOSFET* in the same way that it is for the *JFET i.e.*

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

(*ii*) **D-MOSFET Input Impedance.** The gate impedance of a *D-MOSFET* is extremely high. For example, a typical *D-MOSFET* may have a maximum gate current of 10 pA when $V_{GS} = 35$V.

$$\therefore \quad \text{Input impedance} = \frac{35\,\text{V}}{10\,\text{pA}} = \frac{35\text{V}}{10\times10^{-12}\,\text{A}} = 3.5\times10^{12}\,\Omega$$

With an input impedance in this range, *D-MOSFET* would present virtually no load to a source circuit.

19.33 D-MOSFET Biasing

The following methods may be used for *D-MOSFET* biasing :

(*i*) Gate bias
(*ii*) Self-bias
(*iii*) Voltage-divider bias
(*iv*) Zero bias

The first three methods are exactly the same as those used for *JFETs* and are not discussed here. However, the last method of zero-bias is widely used in *D-MOSFET* circuits.

Zero bias. Since a *D-MOSFET* can be operated with either positive or negative values of V_{GS}, we can set its Q-point at $V_{GS} = 0$V as shown in Fig. 19.50. Then an input a.c. signal to the gate can produce variations above and below the Q-point.

---

* We can only change V_{GS} because the values of I_{DSS} and $V_{GS\,(off)}$ are constant for a given *D-MOSFET*.

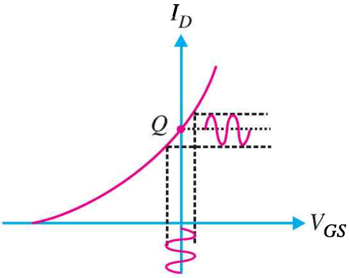


Fig. 19.50

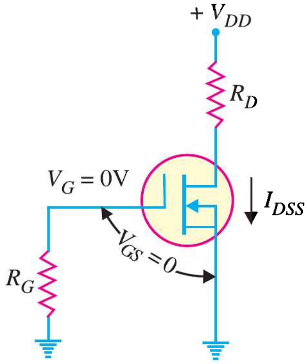


Fig. 19.51

We can use the simple circuit of Fig. 19.51 to provide zero bias. This circuit has $V_{GS} = 0V$ and $I_D = I_{DSS}$. We can find V_{DS} as under :

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

Note that for the *D-MOSFET* zero bias circuit, the source resistor (R_S) is not necessary. With no source resistor, the value of V_S is 0V. This gives us a value of $V_{GS} = 0V$. This biases the circuit at $I_D = I_{DSS}$ and $V_{GS} = 0V$. For mid-point biasing, the value of R_D is so selected that $V_{DS} = V_{DD}/2$.

Example 19.32. *Determine the drain-to-source voltage (V_{DS}) in the circuit shown in Fig. 19.51 above if $V_{DD} = +18V$ and $R_D = 620\Omega$. The MOSFET data sheet gives $V_{GS(off)} = -8V$ and $I_{DSS} = 12$ mA.*

Solution. Since $I_D = I_{DSS} = 12$ mA, the V_{DS} is given by;

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

$$= 18V - (12 \text{ mA})(0.62 \text{ k}\Omega) = \mathbf{10.6V}$$

19.34 Common-Source D-MOSFET Amplifier

Fig. 19.52 shows a common-source amplifier using *n*-channel *D-MOSFET*. Since the source terminal is common to the input and output terminals, the circuit is called *common-source amplifier. The circuit is zero biased with an a.c. source coupled to the gate through the coupling capacitor C_1. The gate is at approximately 0V d.c. and the source terminal is grounded, thus making $V_{GS} = 0V$.

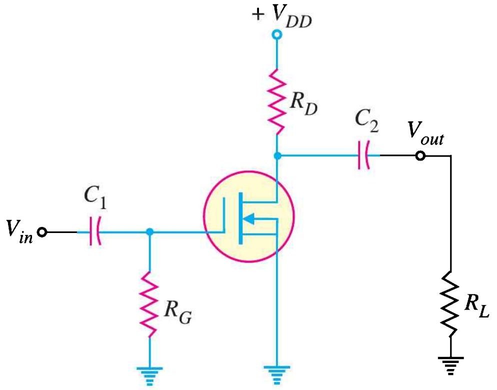


Fig. 19.52

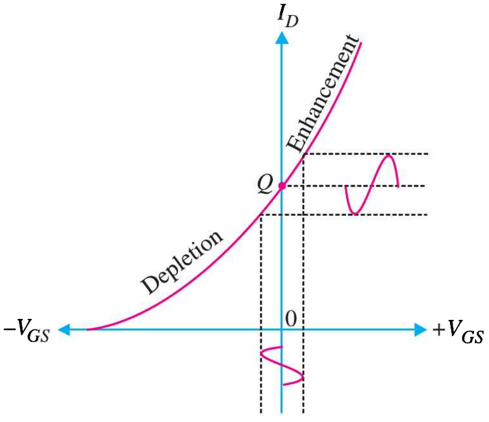


Fig. 19.53

---

* It is comparable to common-emitter transistor amplifier.

Operation. The input signal (V_{in}) is capacitively coupled to the gate terminal. In the absence of the signal, d.c. value of V_{GS} = 0V. When signal (V_{in}) is applied, V_{gs} swings above and below its zero value ($\because$ d.c. value of V_{GS} = 0V), producing a swing in drain current I_d.

(*i*) A small change in gate voltage produces a large change in drain current as in a *JFET*. This fact makes *MOSFET* capable of raising the strength of a weak signal; thus acting as an amplifier.

(*ii*) During the positive half-cycle of the signal, the positive voltage on the gate increases and produces the enhancement-mode. This increases the channel conductivity and hence the drain current.

(*iii*) During the negative half-cycle of the signal, the positive voltage on the gate decreases and produces depletion-mode. This decreases the conductivity and hence the drain current.

The result of above action is that a small change in gate voltage produces a large change in the drain current. This large variation in drain current produces a large a.c. output voltage across drain resistance R_D. In this way, *D-MOSFET* acts as an amplifier. Fig. 19.53 shows the amplifying action of *D-MOSFET* on transconductance curve.

Voltage gain. The a.c. analysis of *D-MOSFET* is similar to that of the *JFET*. Therefore, voltage gain expressions derived for *JFET* are also applicable to *D-MOSFET*.

Voltage gain, $A_v = g_m R_D$ ... for unloaded *D-MOSFET* amplifier

$= g_m R_{AC}$ ... for loaded *D-MOSFET* amplifier

Note the total a.c. drain resistance $R_{AC} = R_D \parallel R_L$.

Example 19.33. *The D-MOSFET used in the amplifier of Fig. 19.54 has an* I_{DSS} *= 12 mA and* g_m *= 3.2 mS. Determine (i) d.c. drain-to-source voltage* V_{DS} *and (ii) a.c. output voltage. Given* v_{in} *= 500 mV.*

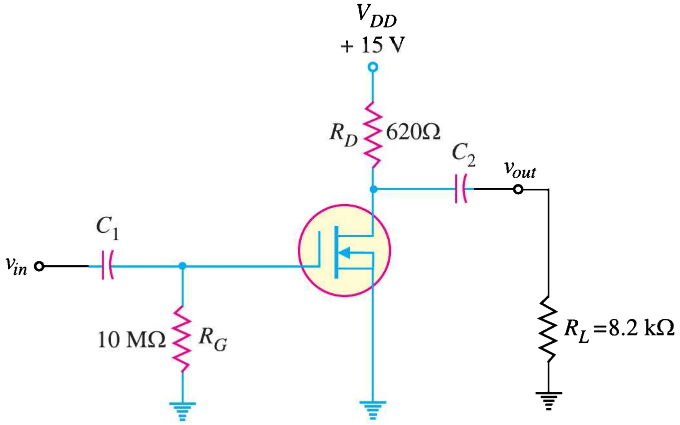


Fig. 19.54

Solution.

(*i*) Since the amplifier is zero biased, $I_D = I_{DSS}$ = 12 mA.

$$\therefore \quad V_{DS} = V_{DD} - I_{DSS} R_D$$

$$= 15\text{V} - (12\text{ mA})(0.62\text{ k}\Omega) = \mathbf{7.56V}$$

(*ii*) Total a.c. drain resistance R_{AC} of the circuit is

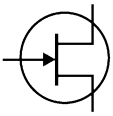
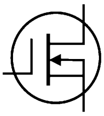
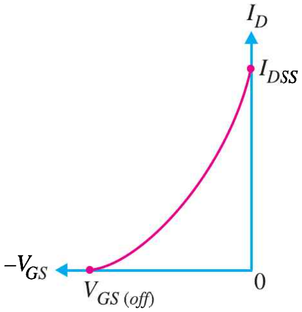
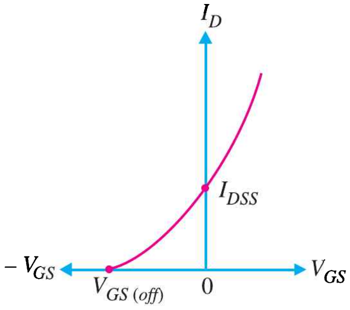
$$R_{AC} = R_D \parallel R_L = 620\Omega \parallel 8.2\text{ k}\Omega = 576\Omega$$

$$\therefore \quad v_{out} = A_v \times v_{in} = (g_m R_{AC})(v_{in})$$

$$= (3.2 \times 10^{-3} S \times 576\ \Omega)(500\text{ mV}) = \mathbf{922\ mV}$$

19.35 D-MOSFETs Versus JFETs

Table below summarises many of the characteristics of *JFET*s and *D-MOSFET*s.

Devices:	*JFETs*	*D-MOSFETs*
Schematic symbol:		
Transconductance curve:		
Modes of operation:	Depletion only	Depletion and enhancement
Commonly used bias circuits:	Gate bias Self bias Voltage-divider bias	Gate bias Self bias Voltage-divider bias Zero bias
Advantages:	Extremely high input impedance.	Higher input impedance than a comparable *JFET*. Can operate in both modes (depletion and enhancement).
Disadvantages:	Bias instability. Can operate only in the depletion mode.	Bias instability. More sensitive to changes in temperature than the *JFET*.

19.36 E-MOSFET

Two things are worth noting about *E-MOSFET*. First, *E-MOSFET* operates *only* in the enhancement mode and has no depletion mode. Secondly, the *E-MOSFET* has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer [See Fig. 19.55 (*i*)]. It is only by the application of V_{GS} (gate-to-source voltage) of proper magnitude and polarity that the device starts conducting. The minimum value of V_{GS} of proper polarity that turns on the *E-MOSFET* is called *Threshold voltage* [$V_{GS\,(th)}$]. The *n*-channel device requires positive V_{GS} ($\geqslant V_{GS\,(th)}$) and the *p*-channel device requires negative V_{GS} ($\geqslant V_{GS\,(th)}$).

Operation. Fig. 19.55 (*i*) shows the circuit of *n*-channel *E-MOSFET*. The circuit action is as under :

(*i*) When $V_{GS} = 0$V [See Fig. 19.55(*i*)], there is no channel connecting the source and drain. The *p* substrate has only a few thermally produced free electrons (minority carriers) so that drain current is essentially zero. For this reason, *E-MOSFET* is normally *OFF* when $V_{GS} = 0$ V. Note that this behaviour of *E-MOSFET* is quite different from *JFET* or *D-MOSFET*.

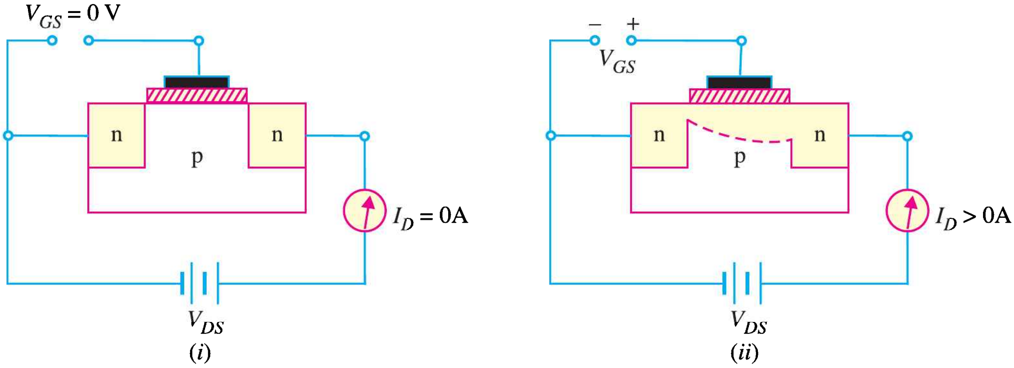


Fig. 19.55

(ii) When gate is made positive (*i.e.* V_{GS} is positive) as shown in Fig. 19.55 (*ii*), it attracts free electrons into th *p* region. The free electrons combine with the holes next to the SiO_2 layer. If V_{GS} is positive enough, all the holes touching the SiO_2 layer are filled and free electrons begin to flow from the source to drain. The effect is the same as creating a thin layer of *n*-type material (*i.e.* inducing a thin *n*-channel) adjacent to the SiO_2 layer. Thus the *E-MOSFET* is turned *ON* and drain current I_D starts flowing form the source to the drain.

***The minimum value of V_{GS} that turns the E-MOSFET ON is called threshold voltage** [$V_{GS\,(th)}$].*

(iii) When V_{GS} is less than $V_{GS\,(th)}$, there is no induced channel and the drain current I_D is zero. When V_{GS} is equal to $V_{GS\,(th)}$, the *E-MOSFET* is turned *ON* and the induced channel conducts drain current from the source to the drain. Beyond $V_{GS\,(th)}$, if the value of V_{GS} is *increased*, the newly formed channel becomes wider, causing I_D to increase. If the value of V_{GS} decreases [not less than $V_{GS\,(th)}$], the channel becomes narrower and I_D will decrease. This fact is revealed by the transconductance curve of *n*-channel *E-MOSFET* shown in Fig. 19.56. As you can see, $I_D = 0$ when $V_{GS} = 0$. Therefore, the value of I_{DSS} for the *E-MOSFET* is zero. Note also that there is no drain current until V_{GS} reaches $V_{GS\,(th)}$.

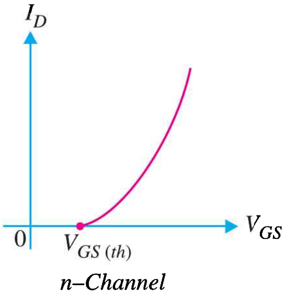


Fig. 19.56

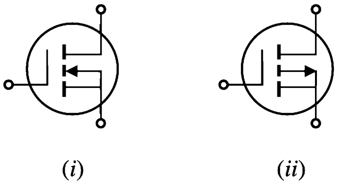


Fig. 19.57

Schematic Symbols. Fig. 19.57 (*i*) shows the schematic symbols for *n*-channel *E-MOSFET* whereas Fig. 19.57 (*ii*) shows the schematic symbol for *p*-channel *E-MOSFET*. When $V_{GS} = 0$, the *E-MOSFET* is *OFF* because there is no conducting channel between source and drain. The broken channel line in the symbols indicates the normally *OFF* condition.

Equation for Transconductance Curve. Fig. 19.58 shows the transconductance curve for *n*-channel *E-MOSFET*. Note that this curve is different from the transconductance curve for *n*-channel *JFET* or *n*-channel *D-MOSFET*. It is because it starts at $V_{GS\,(th)}$ rather than $V_{GS\,(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the *E-MOSFET* transconductance curve (for $V_{GS} > V_{GS\,(th)}$) is

$$I_D = K\,(V_{GS} - V_{GS\,(th)})^2$$

The constant *K* depends on the particular *E-MOSFET* and its value is determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

Any data sheet for an *E-MOSFET* will include the current $I_{D(on)}$ and the voltage $V_{GS\,(on)}$ for one point well above the threshold voltage as shown in Fig. 19.58.

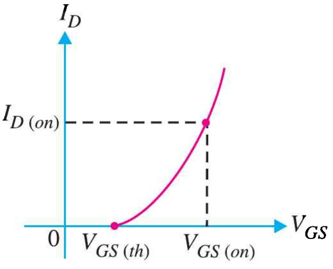


Fig. 19.58

Example 19.34. *The data sheet for an E-MOSFET gives* $I_{D(on)}$ *= 500 mA at* V_{GS} *= 10V and* $V_{GS\,(th)}$ *= 1V. Determine the drain current for* V_{GS} *= 5V.*

Solution. Here $V_{GS\,(on)}$ = 10 V.

$$I_D = K\,(V_{GS} - V_{GS\,(th)})^2 \qquad \text{... }(i)$$

Here

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2} = \frac{500 \text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17 \text{ mA/V}^2$$

Putting the various values in eq. (*i*), we have,

$$I_D = 6.17\,(5\text{V} - 1\text{V})^2 = \mathbf{98.7\ mA}$$

Example 19.35. *The data sheet for an E-MOSFET gives* $I_{D\,(on)}$ *= 3 mA at* V_{GS} *= 10V and* $V_{GS\,(th)}$ *= 3V. Determine the resulting value of K for the device. How will you plot the transconductance curve for this MOSFET ?*

Solution. The value of *K* can be determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

Here $I_{D\,(on)}$ = 3 mA ; $V_{GS\,(on)}$ = 10V ; $V_{GS\,(th)}$ = 3V

$$\therefore \quad K = \frac{3 \text{ mA}}{(10\text{V} - 3\text{V})^2} = \frac{3 \text{ mA}}{(7\text{V})^2} = \mathbf{0.061 \times 10^{-3}\ A/V^2}$$

Now

$$I_D = K\,(V_{GS} - V_{GS\,(th)})^2$$

In order to plot the transconductance curve for the device, we shall determine a few points for the curve by changing the value of V_{GS} and noting the corresponding values of I_D.

For V_{GS} = 5V ; $I_D = 0.061 \times 10^{-3}\,(5\text{V} - 3\text{V})^2 = 0.244$ mA

For V_{GS} = 8V ; $I_D = 0.061 \times 10^{-3}\,(8\text{V} - 3\text{V})^2 = 1.525$ mA

For V_{GS} = 10V ; $I_D = 0.061 \times 10^{-3}\,(10\text{V} - 3\text{V})^2 = 3$ mA

For V_{GS} = 12V ; $I_D = 0.061 \times 10^{-3}\,(12\text{V} - 3\text{V})^2 = 4.94$ mA

Thus we can plot the transconductance curve for the *E-MOSFET* from these V_{GS}/I_D points.

19.37 E-MOSFET Biasing Circuits

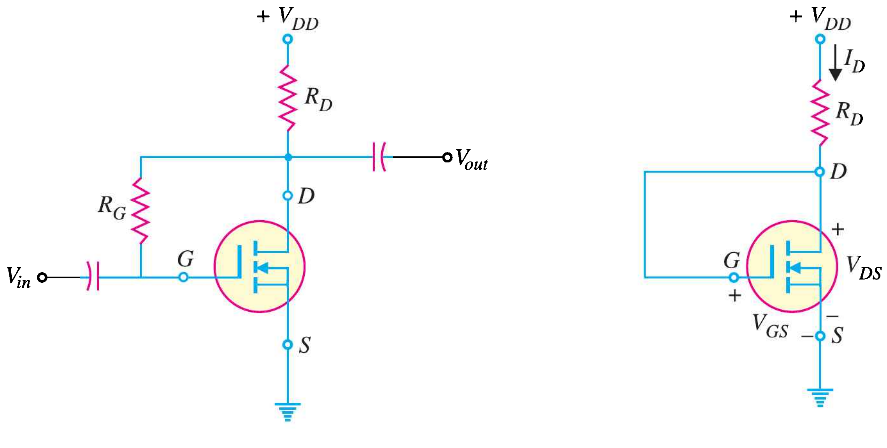
One of the problems with *E-MOSFET* is the fact that many of the biasing circuits used for *JFETs* and *D-MOSFETs* cannot be used with this device. For example, *E-MOSFETs* must have V_{GS} greater than the threshold value ($V_{GS\,(th)}$) so that zero bias cannot be used. However, there are two popular methods for *E-MOSFET* biasing *viz.*

(*i*) Drain-feedback bias

(*ii*) Voltage-divider bias

(*i*) **Drain-feedback bias.** This method of *E-MOSFET* bias is equivalent to collector-feedback bias in transistors. Fig. 19.59 (*i*) shows the drain-feedback bias circuit for *n*-channel *E-MOSFET*. A high resistance R_G is connected between the drain and the gate. Since the gate resistance is superhigh, no current will flow in the gate circuit (*i.e.* $I_G = 0$). Therefore, there will be no voltage drop across R_G. Since there is no voltage drop across R_G, the gate will be at the same potential as the drain. This fact is illustrated in the d.c. equivalent circuit of drain-feedback bias as in Fig. 19.59 (*ii*).

$$\therefore \qquad V_D = V_G \quad \text{and} \quad V_{DS} = V_{GS}$$



(*i*) (*ii*)

Fig. 19.59

The value of drain-source voltage V_{DS} for the drain-feedback circuit is

$$V_{DS} = V_{DD} - I_D R_D$$

$$\text{Since} \quad V_{DS} = V_{GS},\ V_{GS} = V_{DD} - I_D R_D$$

$$\text{Since in this circuit} \quad V_{DS} = V_{GS}\ ;\ I_D = I_{D\,(on)}.$$

Therefore, the Q-point of the circuit stands determined.

***(ii)* Voltage-divider Bias.** Fig. 19.60 shows voltage divider biasing arrangement for *n*-channel *E-MOSFET*. Since $I_G = 0$, the analysis of the method is as follows :

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$\text{and} \qquad V_{DS} = V_{DD} - I_D R_D$$

$$\text{where} \qquad I_D = K\,(V_{GS} - V_{GS\,(th)})^2$$

Once I_D and V_{DS} are known, all the remaining quantities of the circuit such as V_D etc. can be determined.

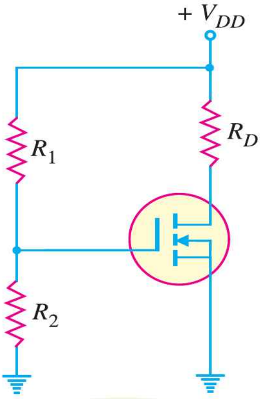


Fig. 19.60

Example 19.36. *Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Fig. 19.61. The data sheet for this particular MOSFET gives $I_{D\,(on)}$ = 500 mA at V_{GS} = 10V and $V_{GS\,(th)}$ = 1V.*

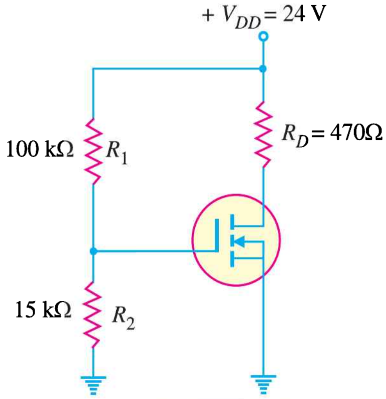


Fig. 19.61

Solution. Referring to the circuit shown in Fig. 19.61, we have,

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{24\text{V}}{(100 + 15)\ \text{k}\Omega} \times 15\ \text{k}\Omega = \mathbf{3.13V}$$

The value of K can be determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

$$= \frac{500\text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17\text{ mA/V}^2 \quad [\because V_{GS\,(on)} = 10\text{V}]$$

$$\therefore \quad I_D = K\,(V_{GS} - V_{GS\,(th)})^2 = 6.17\text{ mA/V}^2\,(3.13\text{V} - 1\text{ V})^2 = 28\text{ mA}$$

$$\therefore \quad V_{DS} = V_{DD} - I_D R_D = 24\text{V} - (28\text{ mA})\,(470\Omega) = \mathbf{10.8V}$$

Example 19.37. *Determine the values of* I_D *and* V_{DS} *for the circuit shown in Fig. 19.62. The data sheet for this particular MOSFET gives* $I_{D\,(on)} = 10$ *mA when* $V_{GS} = V_{DS}$.

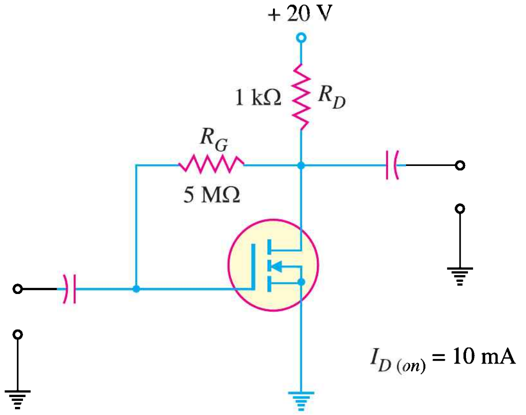


Fig. 19.62

Solution. Since in the drain-feedback circuit $V_{GS} = V_{DS}$,

$$\therefore \quad I_D = I_{D\,(on)} = \mathbf{10\text{ mA}}$$

The value of V_{DS} (and thus V_{GS}) is given by ;

$$V_{DS} = V_{DD} - I_D R_D$$

$$= 20\text{V} - (10\text{ mA})\,(1\text{ k}\Omega) = 20\text{V} - 10\text{V} = \mathbf{10V}$$

Example 19.38. *Determine the value of* I_D *for the circuit shown in Fig. 19.63. The data sheet for this particular MOSFET gives* $I_{D\,(on)} = 10$ *mA at* $V_{GS} = 10$ *V and* $V_{GS\,(th)} = 1.5$ *V.*

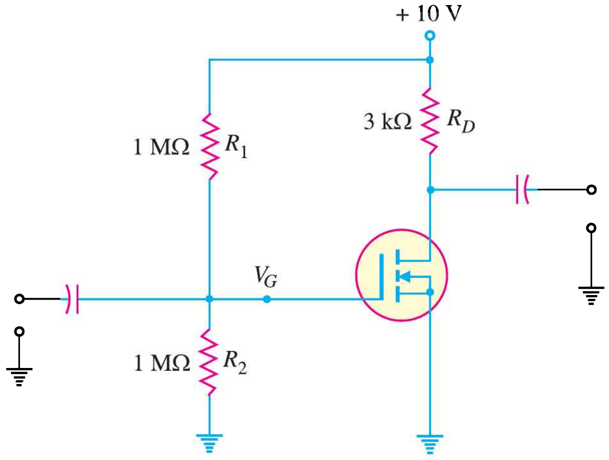


Fig. 19.63

Solution. The value of K can be determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

$$= \frac{10\text{ mA}}{(10\text{ V} - 1.5\text{V})^2} = 1.38 \times 10^{-1}\text{ mA/V}^2 \qquad [\because V_{GS\,(on)} = 10\text{V}]$$

From the circuit, the source voltage is seen to be 0V. Therefore, $V_{GS} = V_G - V_S = V_G - 0 = V_G$. The value of V_G (= V_{GS}) is given by ;

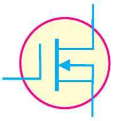
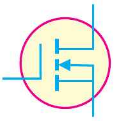
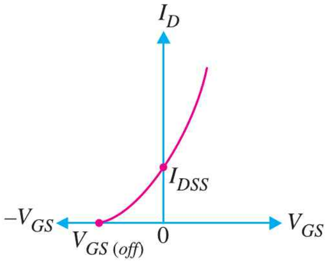
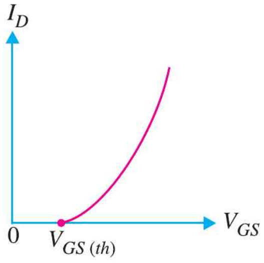
$$V_G \text{ (or } V_{GS}) = \frac{V_{DD}}{R_1 + R_2} \times R_2 = \frac{10\text{V}}{(1+1)\text{ M}\Omega} \times 1\text{M}\Omega = 5\text{V}$$

$$\therefore \quad I_D = K\,(V_{GS} - V_{GS\,(th)})^2$$

$$= (1.38 \times 10^{-1}\text{ mA/V}^2)\,(5\text{V} - 1.5\text{V})^2 = \mathbf{1.69\ mA}$$

19.38 D-MOSFETs Versus E-MOSFETs

Table below summarises many of the characteristics of *D-MOSFETs* and *E-MOSFETs*

Devices:	*D-MOSFETs*	*E-MOSFETs*
Schematic symbol:		
Transconductance curve:		
Modes of operation:	Depletion and enhancement.	Enhancement only.
Commonly used bias circuits:	Gate bias Self bias Voltage-divider bias Zero bias	Gate bias Voltage-divider bias Drain-feedback bias

MULTIPLE-CHOICE QUESTIONS

1. A *JFET* has three terminals, namely ....
(*i*) cathode, anode, grid
(*ii*) emitter, base, collector
(*iii*) source, gate, drain
(*iv*) none of the above

2. A *JFET* is similar in operation to .... valve.
(*i*) diode (*ii*) pentode
(*iii*) triode (*iv*) tetrode

3. A *JFET* is also called .... transistor.
(*i*) unipolar (*ii*) bipolar
(*iii*) unijunction (*iv*) none of the above

4. A *JFET* is a .... driven device.

(*i*) current
(*ii*) voltage
(*iii*) both current and voltage
(*iv*) none of the above

5. The gate of a *JFET* is .... biased.
(*i*) reverse
(*ii*) forward
(*iii*) reverse as well as forward
(*iv*) none of the above

6. The input impedance of a *JFET* is .... that of an ordinary transistor.
(*i*) equal to (*ii*) less than
(*iii*) more than (*iv*) none of the above

7. In a *p*-channel *JFET*, the charge carriers are ....
(*i*) electrons
(*ii*) holes
(*iii*) both electrons and holes
(*iv*) none of the above

8. When drain voltage equals the pinch-off voltage, then drain current .... with the increase in drain voltage.
(*i*) decreases
(*ii*) increases
(*iii*) remains constant
(*iv*) none of the above

9. If the reverse bias on the gate of a *JFET* is increased, then width of the conducting channel ....
(*i*) is decreased
(*ii*) is increased
(*iii*) remains the same
(*iv*) none of the above

10. A *MOSFET* has .... terminals.
(*i*) two (*ii*) five
(*iii*) four (*iv*) three

11. A *MOSFET* can be operated with ....
(*i*) negative gate voltage only
(*ii*) positive gate voltage only
(*iii*) positive as well as negative gate voltage
(*iv*) none of the above

12. A *JFET* has .... power gain.
(*i*) small (*ii*) very high
(*iii*) very small (*iv*) none of the above

13. The input control parameter of a *JFET* is ....
(*i*) gate voltage (*ii*) source voltage
(*iii*) drain voltage (*iv*) gate current

14. A common base configuration of a ***pnp*** transistor is analogous to .... of a *JFET*.
(*i*) common source configuration
(*ii*) common drain configuration
(*iii*) common gate configuration
(*iv*) none of the above

15. A *JFET* has high input impedance because ....
(*i*) it is made of semiconductor material
(*ii*) input is reverse biased
(*iii*) of impurity atoms
(*iv*) none of the above

16. In a *JFET*, when drain voltage is equal to pinch-off voltage, the depletion layers ....
(*i*) almost touch each other
(*ii*) have large gap
(*iii*) have moderate gap
(*iv*) none of the above

17. In a *JFET*, I_{DSS} is known as ....
(*i*) drain to source current
(*ii*) drain to source current with gate shorted
(*iii*) drain to source current with gate open
(*iv*) none of the above

18. The two important advantages of a *JFET* are ....
(*i*) high input impedance and square-law property
(*ii*) inexpensive and high output impedance
(*iii*) low input impedance and high output impedance
(*iv*) none of the above

19. .... has the lowest noise-level.
(*i*) triode (*ii*) ordinary transistor
(*iii*) tetrode (*iv*) *JFET*

20. A *MOSFET* is sometimes called .... *JFET*.
(*i*) many gate (*ii*) open gate
(*iii*) insulated gate (*iv*) shorted gate

21. Which of the following devices has the highest input impedance ?
(*i*) *JFET*

(*ii*) *MOSFET*
(*iii*) crystal diode
(*iv*) ordinary transistor

22. A *MOSFET* uses the electric field of a .... to control the channel current.
(*i*) capacitor (*ii*) battery
(*iii*) generator (*iv*) none of the above

23. The pinch-off voltage in a *JFET* is analogous to .... voltage in a vacuum tube.
(*i*) anode
(*ii*) cathode
(*iii*) grid cut off
(*iv*) none of the above

24. The formula for a.c. drain resistance of a *JFET* is ....
(*i*) $\frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}
(*ii*) $\frac{\Delta V_{GS}}{\Delta I_D}$ at constant V_{DS}
(*iii*) $\frac{\Delta I_D}{\Delta V_{GS}}$ at constant V_{DS}
(*iv*) $\frac{\Delta I_D}{\Delta V_{DS}}$ at constant V_{GS}

25. In class *A* operation, the input circuit of a *JFET* is .... biased.
(*i*) forward (*ii*) reverse
(*iii*) not (*iv*) none of the above

26. If the gate of a *JFET* is made less negative, the width of the conducting channel ....
(*i*) remains the same
(*ii*) is decreased
(*iii*) is increased
(*iv*) none of the above

27. The pinch-off voltage of a *JFET* is about ....
(*i*) 5 V (*ii*) 0.6 V
(*iii*) 15 V (*iv*) 25 V

28. The input impedance of a *MOSFET* is of the order of ....
(*i*) Ω (*ii*) a few hundred Ω
(*iii*) k Ω (*iv*) several M Ω

29. The gate voltage in a *JFET* at which drain current becomes zero is called .... voltage.
(*i*) saturation (*ii*) pinch-off
(*iii*) active (*iv*) cut-off

30. The drain current I_D in a *JFET* is given by ....
(*i*) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
(*ii*) $I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$
(*iii*) $I_D = I_{DSS}\left(1 - \frac{V_P}{V_{GS}}\right)^2$
(*iv*) $I_D = I_{DSS}\left(1 + \frac{V_P}{V_{GS}}\right)^{1/2}$

31. In a *FET*, there are .... *pn* junctions at the sides.
(*i*) three (*ii*) four
(*iii*) five (*iv*) two

32. The transconductance of a *JFET* ranges from ....
(*i*) 100 to 500 mA/V
(*ii*) 500 to 1000 mA/V
(*iii*) 0.5 to 30 mA/V
(*iv*) above 1000 mA/V

33. The source terminal of a *JFET* corresponds to .... of a vacuum tube.
(*i*) plate (*ii*) cathode
(*iii*) grid (*iv*) none of the above

34. The output characteristics of a *JFET* closely resemble the output characteristics of a .... valve.
(*i*) pentode (*ii*) tetrode
(*iii*) triode (*iv*) diode

35. If the cross-sectional area of the channel in *n*-channel *JFET* increases, the drain current ....
(*i*) is increased
(*ii*) is decreased
(*iii*) remains the same
(*iv*) none of the above

36. The channel of a *JFET* is between the ....
(*i*) gate and drain
(*ii*) drain and source
(*iii*) gate and source
(*iv*) input and output

37. For V_{GS}= 0 V, the drain current becomes constant when V_{DS} exceeds ....

(*i*) cut off (*ii*) V_{DD}

(*iii*) V_P (*iv*) 0 V

38. A certain *JFET* data sheet gives $V_{GS(off)}$ = – 4 V. The pinch-off voltage V_P is ....

(*i*) + 4 V (*ii*) – 4 V

(*iii*) dependent on V_{GS}

(*iv*) data insufficient

39. The constant-current region of a *JFET* lies between ....

(*i*) cut off and saturation

(*ii*) cut off and pinch-off

(*iii*) 0 and I_{DSS}

(*iv*) pinch-off and breakdown

40. At cut-off, the *JFET* channel is ....

(*i*) at its widest point

(*ii*) completely closed by the depletion region

(*iii*) extremely narrow

(*iv*) reverse biased

41. A *MOSFET* differs from a *JFET* mainly because ....

(*i*) of power rating

(*ii*) the *MOSFET* has two gates

(*iii*) the *JFET* has a ***pn*** junction

(*iv*) none of above

42. A certain *D-MOSFET* is biased at V_{GS} = 0V. Its data sheet specifies I_{DSS} = 20 mA and $V_{GS\,(off)}$ = – 5V. The value of the drain current is ....

(*i*) 20 mA (*ii*) 0 mA

(*iii*) 40 mA (*iv*) 10 mA

43. An *n*-channel *D-MOSFET* with a positive V_{GS} is operating in ....

(*i*) the depletion-mode

(*ii*) the enhancement-mode

(*iii*) cut off (*iv*) saturation

44. A certain *p*-channel E-MOSFET has a $V_{GS\,(th)}$ = – 2V. If V_{GS} = 0V, the drain current is ....

(*i*) 0 mA (*ii*) $I_{D\,(on)}$

(*iii*) maximum (*iv*) I_{DSS}

45. In a common-source *JFET* amplifier, the output voltage is ....

(*i*) 180° out of phase with the input

(*ii*) in phase with the input

(*iii*) 90° out of phase with the input

(*iv*) taken at the source

46. In a certain common-source *D-MOSFET* amplifier, V_{ds} = 3.2 V r.m.s. and V_{gs} = 280 mV r.m.s. The voltage gain is ....

(*i*) 1 (*ii*) 11.4

(*iii*) 8.75 (*iv*) 3.2

47. In a certain *CS JFET* amplifier, R_D = 1 kΩ, R_S = 560Ω, V_{DD} = 10 V and g_m = 4500 μS. If the source resistor is completely bypassed, the voltage gain is ....

(*i*) 450 (*ii*) 45

(*iii*) 2.52 (*iv*) 4.5

48. A certain common-source *JFET* has a voltage gain of 10. If the source bypass capacitor is removed, ...

(*i*) the voltage gain will increase

(*ii*) the transconductance will increase

(*iii*) the voltage gain will decrease

(*iv*) the Q-point will shift

49. A *CS JFET* amplifier has a load resistance of 10 kΩ and R_D = 820Ω. If g_m = 5 mS and V_{in} = 500 mV, the output signal voltage is ...

(*i*) 2.05 V (*ii*) 25 V

(*iii*) 0.5 V (*iv*) 1.89 V

50. If load resistance in Q. 49 is removed, the output voltage will ....

(*i*) increase (*ii*) decrease

(*iii*) stay the same (*iv*) be zero

Answers to Multiple-Choice Questions

1. (*iii*)	**2.** (*ii*)	**3.** (*i*)	**4.** (*ii*)	**5.** (*i*)
6. (*iii*)	**7.** (*ii*)	**8.** (*iii*)	**9.** (*i*)	**10.** (*iv*)
11. (*iii*)	**12.** (*ii*)	**13.** (*i*)	**14.** (*iii*)	**15.** (*ii*)
16. (*i*)	**17.** (*ii*)	**18.** (*i*)	**19.** (*iv*)	**20.** (*iii*)
21. (*ii*)	**22.** (*i*)	**23.** (*iii*)	**24.** (*i*)	**25.** (*ii*)
26. (*iii*)	**27.** (*i*)	**28.** (*iv*)	**29.** (*ii*)	**30.** (*i*)
31. (*iv*)	**32.** (*iii*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*i*)
36. (*ii*)	**37.** (*iii*)	**38.** (*i*)	**39.** (*iv*)	**40.** (*ii*)
41. (*iii*)	**42.** (*i*)	**43.** (*ii*)	**44.** (*i*)	**45.** (*i*)
46. (*ii*)	**47.** (*iv*)	**48.** (*iii*)	**49.** (*iv*)	**50.** (*i*)

Chapter Review Topics

1. Explain the construction and working of a *JFET*.
2. What is the difference between a *JFET* and a bipolar transistor ?
3. How will you determine the drain characteristics of *JFET* ? What do they indicate?
4. Define the *JFET* parameters and establish the relationship between them.
5. Briefly describe some practical applications of *JFET*.
6. Explain the construction and working of *MOSFET*.
7. Write short notes on the following :
   (*i*) Advantages of *JFET* (*ii*) Difference between *MOSFET* and *JFET*

Problems

1. A *JFET* has a drain current of 5 mA. If I_{DSS} = 10 mA and $V_{GS(off)}$ is – 6 V, find the value of (*i*) V_{GS} and (*ii*) V_P. **[(*i*) – 1.5 V (*ii*) 6 V]**
2. A *JFET* has an I_{DSS} of 9 mA and a $V_{GS\,(off)}$ of – 3V. Find the value of drain current when V_{GS} = –1.5V. **[2.25mA]**
3. In the *JFET* circuit shown in Fig. 19.64 if I_D = 1.9 mA, find V_{GS} and V_{DS}. **[– 1.56V; 13.5V]**

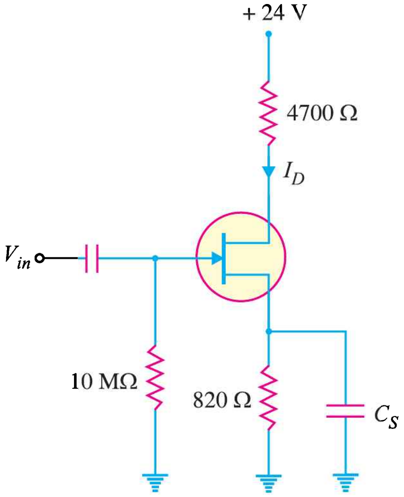


Fig. 19.64

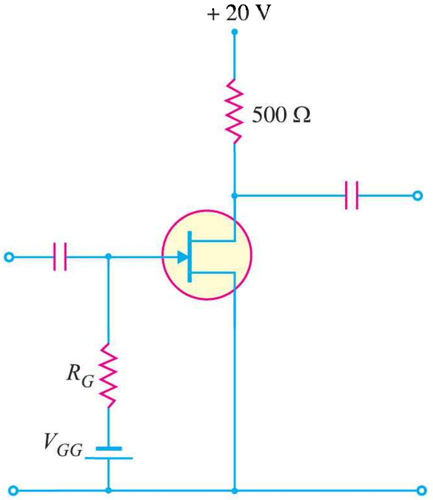
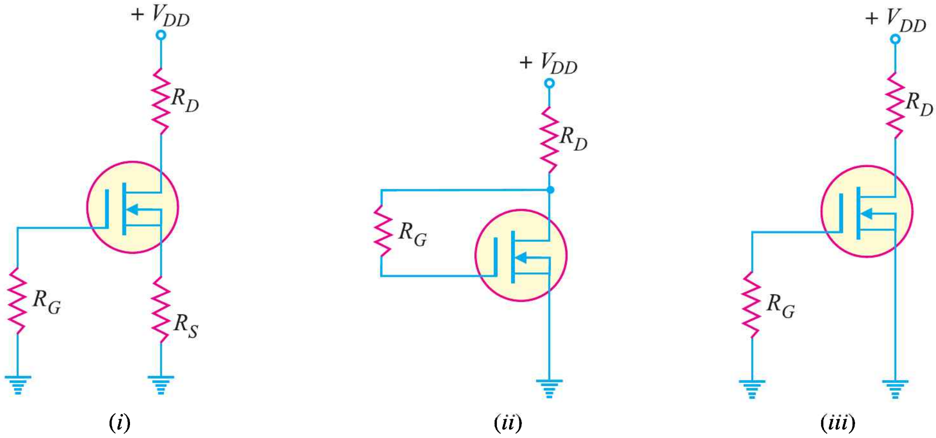


Fig. 19.65

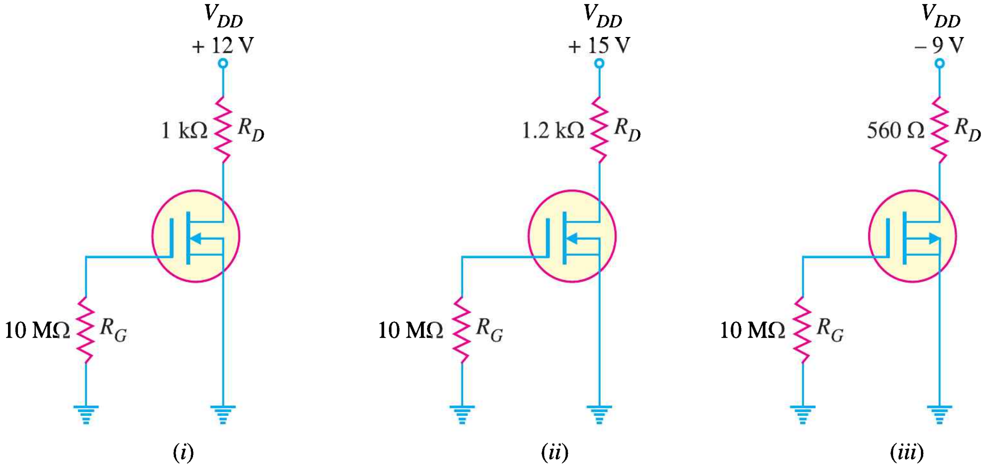
4. For the *JFET* amplifier shown in Fig. 19.65, draw the d.c. load line.



(*i*) (*ii*) (*iii*)

Fig. 19.66

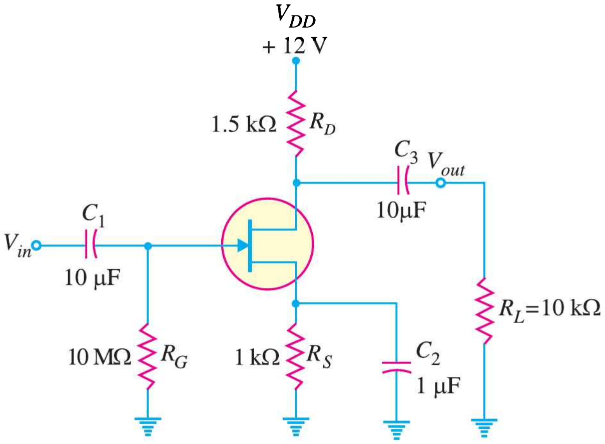
5. For a *JFET*, $I_{DSS} = 9$ mA and $V_{GS} = -3.5$ V. Determine I_D when (*i*) $V_{GS} = 0$ V (*ii*) $V_{GS} = -2$V. **[(*i*) 9mA (*ii*) 1.65 mA]**
6. Sketch the transfer curve for a *p*-channel *JFET* with $I_{DSS} = 4$ mA and $V_P = 3$ V.
7. In a *D-MOSFET*, determine I_{DSS}, given $I_D = 3$ mA, $V_{GS} = -2$V and $V_{GS\,(off)} = -10$V. **[4.69 mA]**
8. Determine in which mode each *D-MOSFET* in Fig. 19.66 is biased. **[(*i*) Depletion (*ii*) Enhancement (*iii*) Zero bias]**
9. Determine V_{DS} for each circuit in Fig. 19.67. Given $I_{DSS} = 8$ mA. **[(*i*) 4V (*ii*) 5.4V (*iii*) – 4.52V]**



V_{DD}
+ 12 V
1 kΩ
R_D
10 MΩ
R_G
(*i*)
V_{DD}
+ 15 V
1.2 kΩ
R_D
10 MΩ
R_G
(*ii*)
V_{DD}
– 9 V
560 Ω
R_D
10 MΩ
R_G
(*iii*)

Fig. 19.67

10. If a 50 mV r.m.s. input signal is applied to the amplifier in Fig. 19.68, what is the peak-to-peak output voltage? Given that $g_m = 5000$ μS. **[920 mV]**



V_{DD}
+ 12 V
1.5 kΩ
R_D
C_3
V_{out}
10μF
C_1
V_{in}
10 μF
R_L=10 kΩ
10 MΩ
R_G
1 kΩ
R_S
C_2
1 μF

Fig. 19.68

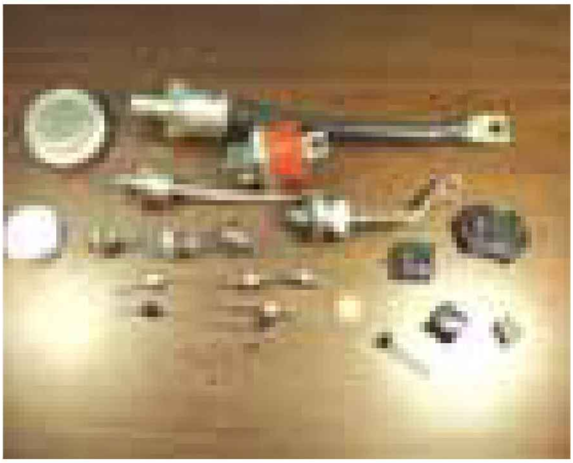
Discussion Questions

1. Why is the input impedance of *JFET* more than that of the transistor ?
2. What is the importance of *JFET* ?
3. Why is *JFET* called unipolar transistor ?
4. What is the basic difference between *D-MOSFET* and *E-MOSFET* ?
5. What was the need to develop *MOSFET* ?

20

Silicon Controlled Rectifiers

20.1 Silicon Controlled Rectifier (SCR)
20.2 Working of SCR
20.3 Equivalent Circuit of SCR
20.4 Important Terms
20.5 V-I Characteristics of SCR
20.6 SCR in Normal Operation
20.7 SCR as a Switch
20.8 SCR Switching
20.9 SCR Half-Wave Rectifier
20.10 SCR Full-Wave Rectifier
20.11 Single-Phase SCR Inverter Circuit
20.12 Applications of SCR
20.13 Light-Activated SCR



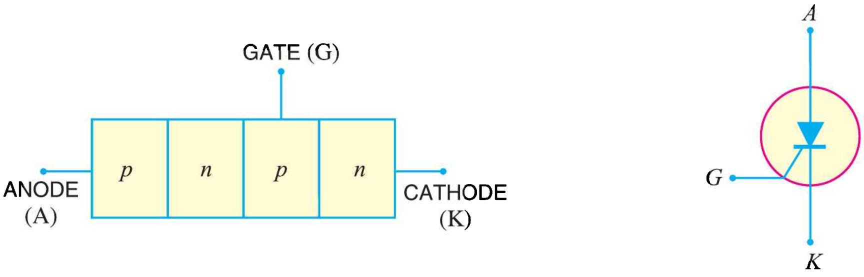
INTRODUCTION

The silicon controlled rectifier (abbreviated as *SCR*) is a three-terminal semiconductor switching device which is probably the most important circuit element after the diode and the transistor. Invented in 1957, an *SCR* can be used as a controlled switch to perform various functions such as rectification, inversion and regulation of power flow. The *SCR* has assumed paramount importance in electronics because it can be produced in versions to handle currents upto several thousand amperes and voltages upto more than 1 kV.

The *SCR* has appeared in the market under different names such as thyristor, thyrode transistor. It is a unidirectional power switch and is being extensively used in switching d.c. and a.c., rectifying a.c. to give controlled d.c. output, converting d.c. into a.c. etc. In this chapter, we shall examine the various characteristics of silicon controlled rectifiers and their increasing applications in power electronics.

20.1 Silicon Controlled Rectifier (SCR)

A silicon *controlled rectifier is a semiconductor **device that acts as a true electronic switch. It can change alternating current into direct current and at the same time can control the amount of power fed to the load. Thus *SCR* combines the features of a rectifier and a transistor.

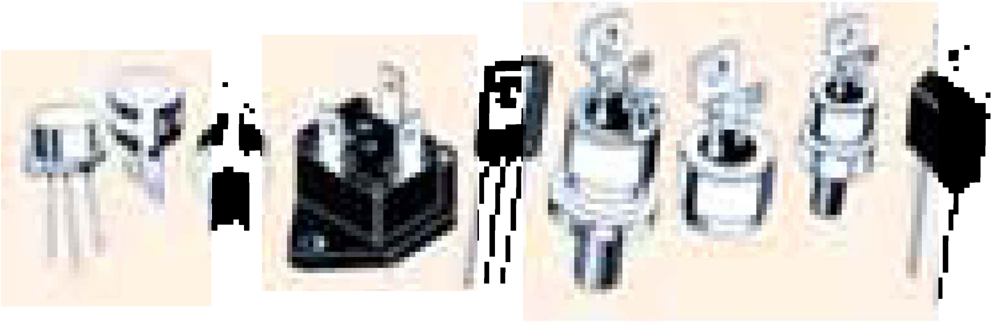


(*i*) (*ii*)

Fig. 20.1

Constructional details. When a *pn* junction is added to a junction transistor, the resulting three *pn* junction device is called a silicon controlled rectifier. Fig. 20.1 (*i*) shows its construction. It is clear that it is essentially an ordinary rectifier (*pn*) and a junction transistor (*npn*) combined in one unit to form *pnpn device*. Three terminals are taken; one from the outer *p-type* material called *anode A*, second from the outer *n*-type material called *cathode K* and the third from the base of transistor section and is called *gate G*. In the normal operating conditions of *SCR*, anode is held at high positive potential *w.r.t.* cathode and gate at small positive potential *w.r.t.* cathode. Fig. 20.1 (*ii*) shows the symbol of *SCR*.

The silicon controlled rectifier is a solid state equivalent of thyratron. The gate, anode and cathode of *SCR* correspond to the grid, plate and cathode of thyratron. For this reason, *SCR* is sometimes called *thyristor*.



Typical SCR Packages

20.2 Working of SCR

In a silicon controlled rectifier, load is connected in series with anode. The anode is always kept at positive potential *w.r.t.* cathode. The working of *SCR* can be studied under the following two heads:

---

* **Why not germanium controlled rectifier ?** The device is made of silicon because leakage current in silicon is very small as compared to germanium. Since the device is used as a switch, it will carry leakage current in the off condition which should be as small as possible.

** It got this name because it is a silicon device and is used as a rectifier and that rectification can be controlled.

(*i*) **When gate is open.** Fig. 20.2 shows the *SCR* circuit with gate open *i.e.* no voltage applied to the gate. Under this condition, junction J_2 is reverse biased while junctions J_1 and J_3 are forward biased. Hence, the situation in the junctions J_1 and J_3 is just as in a *npn* transistor with base open. Consequently, no current flows through the load R_L and the *SCR* is *cut off*. However, if the applied voltage is gradually increased, a stage is reached when * reverse biased junction J_2 breaks down. The *SCR* now conducts ** heavily and is said to be in the *ON* state. The applied voltage at which *SCR* conducts heavily without gate voltage is called *Breakover voltage*.

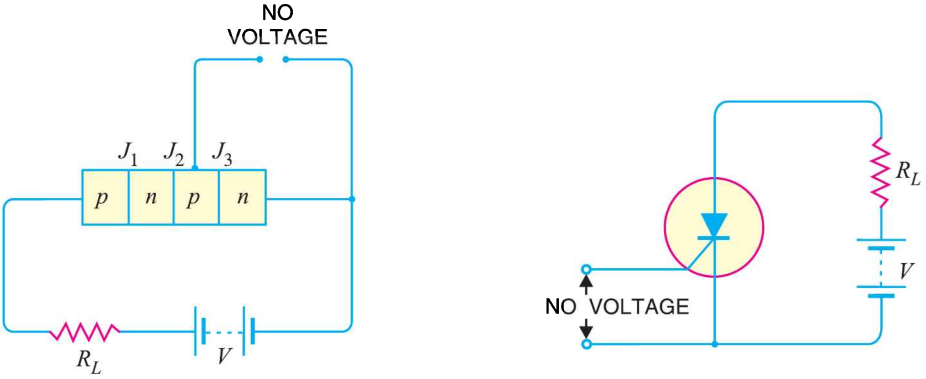


Fig. 20.2

(*ii*) **When gate is positive w.r.t. cathode.** The *SCR* can be made to conduct heavily at smaller applied voltage by applying a small positive potential to the gate as shown in Fig. 20.3. Now junction J_3 is forward biased and junction J_2 is reverse biased. The electrons from *n*-type material start moving across junction J_3 towards left whereas holes from *p*-type towards the right. Consequently, the electrons from junction J_3 are attracted across junction J_2 and gate current starts flowing. As soon as the gate current flows, anode current increases. The increased anode current in turn makes more electrons available at junction J_2. This process continues and in an extremely small time, junction J_2 breaks down and the *SCR* starts conducting heavily. *Once SCR starts conducting, the gate* (the reason for this name is obvious) *loses all control*. Even if gate voltage is removed, the anode current does not decrease at all. The only way to stop conduction (*i.e.* bring *SCR* in off condition) is to reduce the applied voltage to zero.

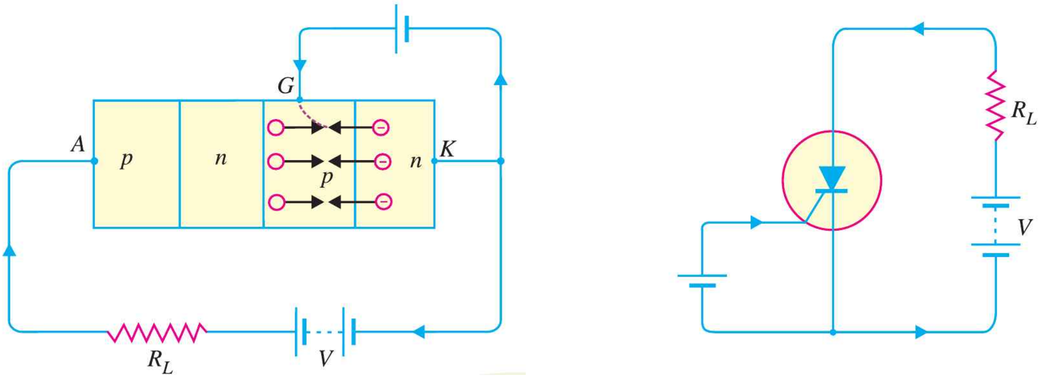


Fig. 20.3

---

* The whole applied voltage *V* appears as reverse bias across junction J_2 as junctions J_1 and J_3 are forward biased.

** Because J_1 and J_3 are forward biased and J_2 has broken down.

Conclusion. The following conclusions are drawn from the working of *SCR* :

(*i*) An *SCR* has two states *i.e.* either it does not conduct or it conducts heavily. There is no state inbetween. Therefore, *SCR* behaves like a switch.

(*ii*) There are two ways to turn on the *SCR*. The first method is to keep the gate open and make the supply voltage equal to the breakover voltage. The second method is to operate *SCR* with supply voltage less than breakover voltage and then turn it on by means of a small voltage (typically 1.5 V, 30 mA) applied to the gate.

(*iii*) Applying small positive voltage to the gate is the normal way to close an *SCR* because the breakover voltage is usually much greater than supply voltage.

(*iv*) To open the *SCR* (*i.e.* to make it non-conducting), reduce the supply voltage to zero.

20.3 Equivalent Circuit of SCR

The *SCR* shown in Fig. 20.4 (*i*) can be visualised as separated into two transistors as shown in Fig. 20.4 (*ii*). Thus, the equivalent circuit of *SCR* is composed of *pnp* transistor and *npn* transistor connected as shown in Fig. 20.4. (*iii*). It is clear that collector of each transistor is coupled to the base of the other, thereby making a positive feedback loop.

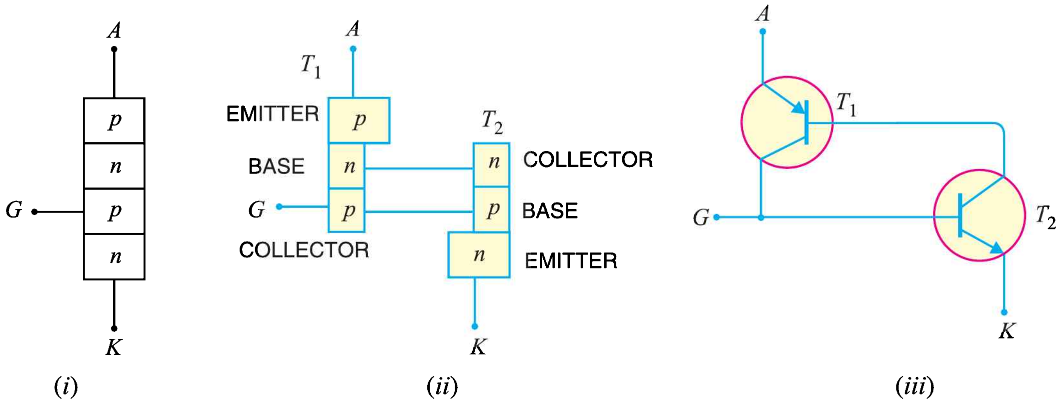


Fig. 20.4

The working of *SCR* can be easily explained from its equivalent circuit. Fig. 20.5. shows the equivalent circuit of *SCR* with supply voltage *V* and load resistance R_L. Assume the supply voltage *V* is less than breakover voltage as is usually the case. With gate open (*i.e.* switch *S* open), there is no base current in transistor T_2. Therefore, no current flows in the collector of T_2 and hence that of T_1. Under such conditions, the *SCR* is open. However, if switch *S* is closed, a small gate current will flow through the base of T_2 which means its collector current will increase. The collector current of T_2 is the base current of T_1. Therefore, collector current of T_1 increases. But collector current of T_1 is the base current of T_2. This action is accumulative since an increase of current in one transistor causes an increase of current in the other transistor. As a result of this action, both

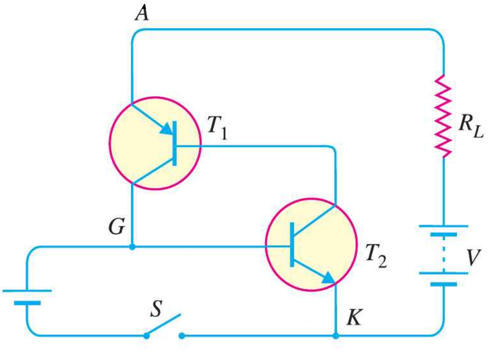


Fig. 20.5

transistors are driven to saturation, and heavy current flows through the load R_L. Under such conditions, the *SCR* closes.

20.4 Important Terms

The following terms are much used in the study of *SCR* :

(*i*) Breakover voltage

(*ii*) Peak reverse voltage

(*iii*) Holding current

(*iv*) Forward current rating

(*v*) Circuit fusing rating

(*i*) **Breakover voltage.** *It is the minimum forward voltage, gate being open, at which SCR starts conducting heavily i.e. turned on.*

Thus, if the breakover voltage of an *SCR* is 200 V, it means that it can block a forward voltage (*i.e. SCR* remains open) as long as the supply voltage is less than 200 V. If the supply voltage is more than this value, then *SCR* will be turned on. In practice, the *SCR* is operated with supply voltage less than breakover voltage and it is then turned on by means of a small voltage applied to the gate. Commercially available *SCRs* have breakover voltages from about 50 V to 500 V.

(*ii*) **Peak reverse voltage (*PRV*).** *It is the maximum reverse voltage (cathode positive w.r.t. anode) that can be applied to an SCR without conducting in the reverse direction.*

Peak reverse voltage (*PRV*) is an important consideration while connecting an *SCR* in an a.c. circuit. During the negative half of a.c. supply, reverse voltage is applied across *SCR*. If *PRV* is exceeded, there may be avalanche breakdown and the *SCR* will be damaged if the external circuit does not limit the current. Commercially available *SCRs* have *PRV* ratings upto 2.5 kV.

(*iii*) **Holding current.** *It is the maximum anode current, gate being open, at which SCR is turned off from ON conditions.*

As discussed earlier, when *SCR* is in the conducting state, it cannot be turned *OFF* even if gate voltage is removed. The only way to turn off or open the *SCR* is to reduce the supply voltage to almost zero at which point the internal transistor comes out of saturation and opens the *SCR*. The anode current under this condition is very small (a few mA) and is called *holding current*. Thus, if an *SCR* has a holding current of 5mA, it means that if anode current is made less than 5mA, then *SCR* will be turned off.

(*iv*) **Forward current rating.** *It is the maximum anode current that an SCR is capable of passing without destruction.*

Every *SCR* has a safe value of forward current which it can conduct. If the value of current exceeds this value, the *SCR* may be destroyed due to intensive heating at the junctions. For example, if an *SCR* has a forward current rating of 40A, it means that the *SCR* can safely carry only 40 A. Any attempt to exceed this value will result in the destruction of the *SCR*. Commercially available *SCRs* have forward current ratings from about 30A to 100A.

(*v*) **Circuit fusing (I^2t) rating.** *It is the product of square of forward surge current and the time of duration of the surge i.e.,*

$$\text{Circuit fusing rating} = I^2t$$

The circuit fusing rating indicates the maximum forward surge current capability of *SCR*. For example, consider an *SCR* having circuit fusing rating of 90 A^2s. If this rating is exceeded in the *SCR* circuit, the device will be destroyed by excessive power dissipation.

Example 20.1. *An SCR has a breakover voltage of 400 V, a trigger current of 10 mA and holding current of 10 mA. What do you infer from it ? What will happen if gate current is made 15 mA ?*

Solution. (*i*) *Breakover voltage of 400 V.* It means that if gate is open and the supply voltage is

400 V, then *SCR* will start conducting heavily. However, as long as the supply voltage is less than 400 V, the *SCR* stays open *i.e.* it does not conduct.

(*ii*) *Trigger current of 10 mA.* It means that if the supply voltage is less than breakover voltage (*i.e.* 400 V) and a minimum gate current of 10 mA is passed, the *SCR* will close *i.e.* starts conducting heavily. The *SCR* will not conduct if the gate current is less than 10 mA. It may be emphasised that triggering is the normal way to close an *SCR* as the supply voltage is normally much less than the breakover voltage.

(*iii*) *Holding current of 10 mA.* When the *SCR* is conducting, it will not open (*i.e.* stop conducting) even if triggering current is removed. However, if supply voltage is reduced, the anode current also decreases. When the anode current drops to 10 mA, the holding current, the *SCR* is turned off.

(*iv*) If gate current is increased to 15 mA, the *SCR* will be turned on lower supply voltage.

Example 20.2. *An SCR in a circuit is subjected to a 50 A surge that lasts for 12 ms. Determine whether or not this surge will destroy the device. Given that circuit fusing rating is 90* A^2s.

Solution. Circuit fusing rating $= I^2t = (50)^2 \times (12 \times 10^{-3}) = \mathbf{30\ A^2s}$

Since this value is well below the maximum rating of 90 A^2s, the device will not be destroyed.

Example 20.3. *An SCR has a circuit fusing rating of 50* A^2s. *The device is being used in a circuit where it could be subjected to a 100 A surge. Determine the maximum allowable duration of such a surge.*

Solution.
$$t_{max} = \frac{I^2t\ \text{(rating)}}{I_s^2} \quad \text{where } I_s = \text{known value of surge current}$$

$$\therefore \quad t_{max} = \frac{50}{(100)^2} = 5 \times 10^{-3} s = \mathbf{5\ ms}$$

Example 20.4. *A 220Ω resistor is connected in series with the gate of an SCR as shown in Fig. 20.6. The gate current required to fire the SCR is 7mA. What is the input voltage* (V_{in}) *required to fire the SCR ?*

Solution. The input voltage must overcome the junction voltage between the gate and cathode (0.7V) and also cause 7mA to flow through the 220Ω resistor. According to Kirchhoff's voltage law, V_{in} is given by;

$$V_{in} = V_{GK} + I_G R$$
$$= 0.7\text{V} + (7\text{mA})\,(220\Omega) = \mathbf{2.24V}$$

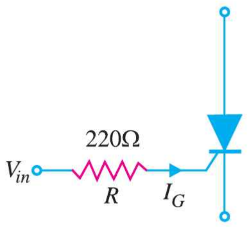


Fig. 20.6

20.5 V-I Characteristics of SCR

It is the curve between anode-cathode voltage (*V*) and anode current (*I*) of an *SCR* at constant gate current. Fig. 20.7 shows the *V-I* characteristics of a typical *SCR*.

(*i*) Forward characteristics. When anode is positive *w.r.t.* cathode, the curve between *V* and *I* is called the forward characteristic. In Fig. 20.7, *OABC* is the forward characteristic of *SCR* at $I_G = 0$. If the supply voltage is increased from zero, a point is reached (point *A*) when the *SCR* starts conducting. Under this condition, the voltage across *SCR* suddenly drops as shown by dotted curve *AB* and most of supply voltage appears across the load resistance R_L. If proper gate current is made to flow, *SCR* can close at much smaller supply voltage.

(*ii*) Reverse characteristics. When anode is negative *w.r.t.* cathode, the curve between *V* and *I* is known as *reverse characteristic*. The reverse voltage does come across *SCR* when it is operated with a.c. supply. If the reverse voltage is gradually increased, at first the anode current remains small (*i.e.* leakage current) and at some reverse voltage, avalanche breakdown occurs and the *SCR* starts conducting heavily in the reverse direction as shown by the curve *DE*. This maximum reverse voltage at which *SCR* starts conducting heavily is known as *reverse breakdown voltage*.

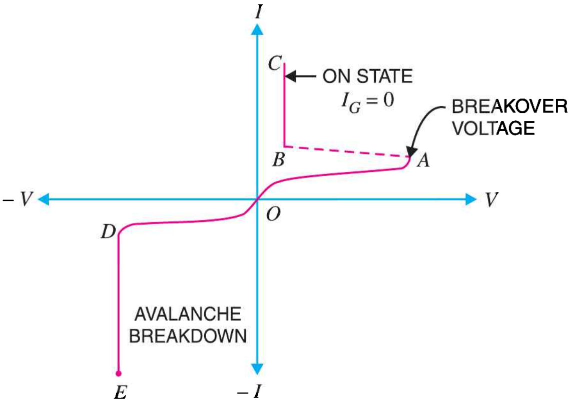


Fig. 20.7

20.6 SCR in Normal Operation

In order to operate the *SCR* in normal operation, the following points are kept in view :

(*i*) The supply voltage is generally much less than breakover voltage.

(*ii*) The *SCR* is turned on by passing an appropriate amount of gate current (a few mA) and not by breakover voltage.

(*iii*) When *SCR* is operated from a.c. supply, the peak reverse voltage which comes during negative half-cycle should not exceed the reverse breakdown voltage.

(*iv*) When *SCR* is to be turned *OFF* from the *ON* state, anode current should be reduced to holding current.

(*v*) If gate current is increased above the required value, the *SCR* will close at much reduced supply voltage.

20.7 SCR as a Switch

The *SCR* has only two states, namely; *ON* state and *OFF* state and no state inbetween. When appropriate gate current is passed, the *SCR* starts conducting heavily and remains in this position indefinitely even if gate voltage is removed. This corresponds to the *ON* condition. However, when the anode current is reduced to the holding current, the *SCR* is turned *OFF*. It is clear that behaviour of *SCR* is similar to a mechanical switch. As *SCR* is an electronic device, therefore, it is more appropriate to call it an *electronic switch*.

Advantages of SCR as a switch. An *SCR* has the following advantages over a mechanical or electromechanical switch (relay) :

(*i*) It has no moving parts. Consequently, it gives noiseless operation at high efficiency.

(*ii*) The switching speed is very high upto 10^9 operations per second.

(*iii*) It permits control over large current (30–100 A) in the load by means of a small gate current (a few mA).

(*iv*) It has small size and gives trouble free service.

20.8 SCR Switching

We have seen that *SCR* behaves as a switch *i.e.* it has only two states *viz.* *ON* state and *OFF* state. It is profitable to discuss the methods employed to turn-on or turn-off an *SCR*.

1. SCR turn-on methods. In order to turn on the *SCR*, the gate voltage V_G is increased upto a minimum value to initiate triggering. This minimum value of gate voltage at which *SCR* is turned *ON* is called *gate triggering voltage* V_{GT}. The resulting gate current is called gate *triggering current* I_{GT}. Thus to turn on an *SCR* all that we have to do is to apply positive gate voltage equal to V_{GT} or pass a gate current equal to I_{GT}. For most of the *SCRs*, V_{GT} = 2 to 10 V and I_{GT} = 100 μA to 1500 mA. We shall discuss two methods to turn on an *SCR*.

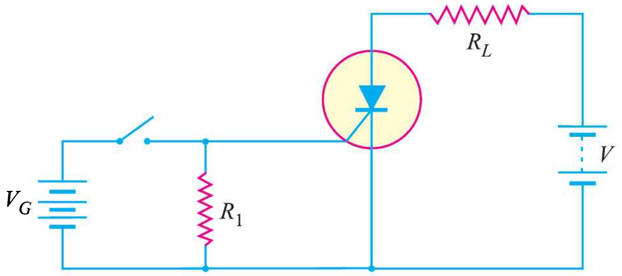
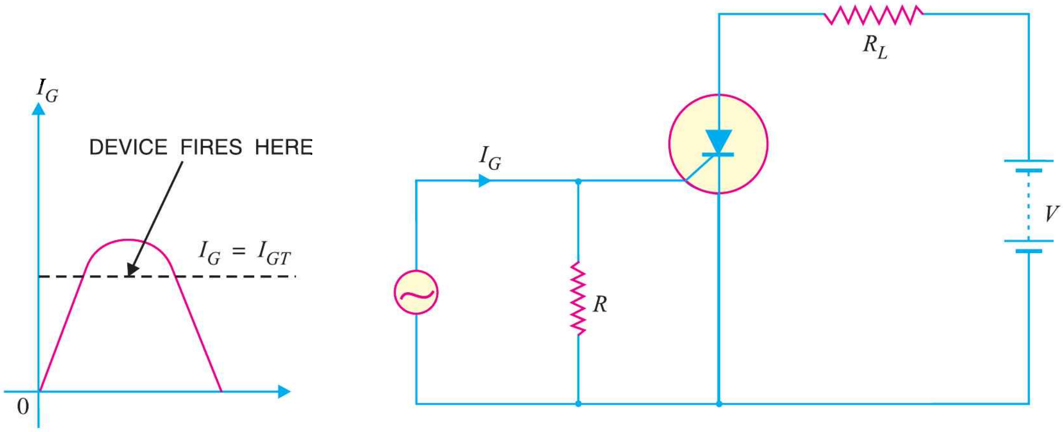


Fig. 20.8

(*i*) *D.C. gate trigger circuit.* Fig. 20.8 shows a typical circuit used for triggering an *SCR* with a d.c. gate bias. When the switch is closed, the gate receives sufficient positive voltage (= V_{GT}) to turn the *SCR* on. The resistance R_1 connected in the circuit provides noise suppression and improves the turn-on time. The turn-on time primarily depends upon the magnitude of the gate current. The higher the gate-triggered current, the shorter the turn-on time.



(*i*) (*ii*)

Fig. 20.9

(*ii*) *A.C. trigger circuit.* An *SCR* can also be turned on with positive cycle of a.c. gate current. Fig. 20.9 (*ii*) shows such a circuit. During the positive half-cycle of the gate current, at some point $I_G = I_{GT}$, the device is turned on as shown in Fig. 20.9 (*i*).

2. SCR turn-off methods. The *SCR* turn-off poses more problems than *SCR* turn-on. It is because once the device is *ON*, the gate loses all control. There are many methods of *SCR* turn-off but only two will be discussed.

(*i*) *Anode current interruption.* When the anode current is reduced below a minimum value called holding current, the *SCR* turns off. The simple way to turn off the *SCR* is to open the line switch *S* as shown in Fig. 20.10.

(*ii*) *Forced commutation.* The method of discharging a capacitor in parallel with an *SCR* to turn off the *SCR* is called forced commutation. Fig. 20.11 shows the forced commutation of *SCR* where capacitor *C* performs the commutation. Assuming the *SCRs* are switches with *SCR*1 *ON* and *SCR*2 *OFF*, current flows through the load and *C* as shown in Fig. 20.11. When *SCR*2 is triggered on, *C* is effectively paralleled across *SCR*1. The charge on *C* is then opposite to *SCR*1's forward voltage, *SCR*1 is thus turned off and the current is transferred to *R*–*SCR*2 path.

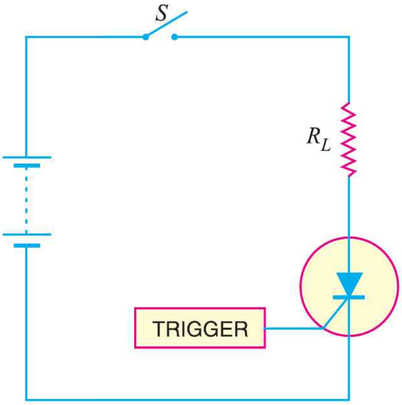


Fig. 20.10

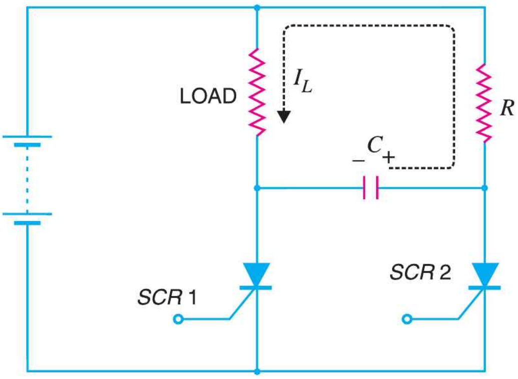
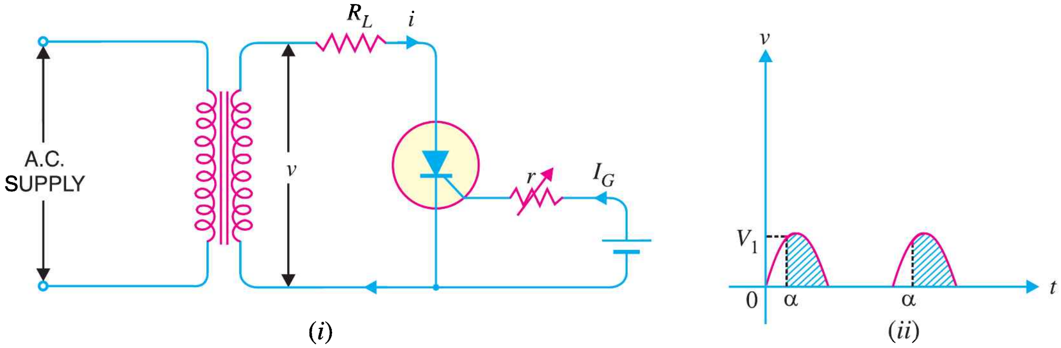


Fig. 20.11

20.9 SCR Half-Wave Rectifier

One important application of an *SCR* is the controlled half-wave rectification. Fig. 20.12 (*i*) shows the circuit of an *SCR* half-wave rectifier. The a.c. supply to be rectified is supplied through the transformer. The load resistance R_L is connected in series with the anode. A variable resistance *r* is inserted in the gate circuit to control the gate current.



(*i*) (*ii*)

Fig. 20.12

Operation. The a.c. supply to be converted into d.c. supply is applied to the primary of the transformer. Suppose the peak reverse voltage appearing across secondary is less than the reverse breakdown voltage of the *SCR*. This condition ensures that *SCR* will not break down during negative half-cycles of a.c. supply. The circuit action is as follows :

(*i*) During the negative half-cycles of a.c. voltage appearing across secondary, the *SCR* does not conduct regardless of the gate voltage. It is because in this condition, anode is negative *w.r.t.* cathode and also *PRV* is less than the reverse breakdown voltage.

(*ii*) The *SCR* will conduct during the positive half-cycles provided proper gate current is made to flow. The greater the gate current, the lesser the supply voltage at which *SCR* is turned *ON*. The gate current can be changed by the variable resistance r as shown in Fig. 20.12 (*i*).

(*iii*) Suppose that gate current is adjusted to such a value that *SCR* closes at a positive voltage V_1 which is less than the peak voltage V_m. Referring to Fig. 20.12 (*ii*), it is clear that *SCR* will start conducting when secondary a.c. voltage becomes V_1 in the positive half-cycle. Beyond this, the *SCR* will continue to conduct till voltage becomes zero at which point it is turned *OFF*. Again at the start of the next positive half-cycle, *SCR* will start conducting when secondary voltage becomes V_1.

(*iv*) Referring to Fig. 20.12 (*ii*), it is clear that firing angle is α *i.e.* at this angle in the positive half-cycle, *SCR* starts conduction. The conduction angle is ϕ (= 180° – α).

It is worthwhile to distinguish between an ordinary half-wave rectifier and *SCR* half-wave rectifier. Whereas an ordinary half-wave rectifier will conduct full positive half-cycle, an *SCR* half-wave rectifier can be made to conduct full or part of a positive half-cycle by proper adjustment of gate current. Therefore, an *SCR* can control power fed to the load and hence the name *controlled rectifier*.

Mathematical treatment. Referring to Fig. 20.12 (*i*), let $v = V_m \sin\theta$ be the alternating voltage that appears across the secondary. Let α be the firing angle. It means that rectifier will conduct from α to 180° during the positive half-cycles.

$$\therefore \quad \text{Average output,} \quad V_{av} = \frac{1}{2\pi}\int_{\alpha}^{180^\circ} V_m \sin\theta\, d\theta = \frac{V_m}{2\pi}\int_{\alpha}^{180^\circ} \sin\theta\, d\theta$$

$$= \frac{V_m}{2\pi}\left[-\cos\theta\right]_{\alpha}^{180^\circ}$$

$$= \frac{V_m}{2\pi}(\cos\alpha - \cos 180^\circ)$$

$$\therefore \quad V_{av} = \frac{V_m}{2\pi}(1 + \cos\alpha)$$

$$\text{Average current,} \quad I_{av} = \frac{V_{av}}{R_L} = \frac{V_m}{2\pi R_L}(1 + \cos\alpha)$$

The following points may be noted :

(*i*) If the firing angle $\alpha = 0°$, then full positive half-cycle will appear across the load R_L and the output current becomes :

$$I_{av} = \frac{V_m}{2\pi R_L}(1 + \cos 0^\circ) = \frac{V_m}{\pi R_L}$$

This is the value of average current for ordinary half-wave rectifier. This is expected since the full positive half-cycle is being conducted.

(*ii*) If $\alpha = 90°$, then average current is given by :

$$I_{av} = \frac{V_m}{2\pi R_L}(1 + \cos 90^\circ) = \frac{V_m}{2\pi R_L}$$

This shows that greater the firing angle α, the smaller is the average current and *vice-versa*.

Example 20.5. *A half-wave rectifier circuit employing an SCR is adjusted to have a gate current of 1mA. The forward breakdown voltage of SCR is 100 V for I_g = 1mA. If a sinusoidal voltage of 200 V peak is applied, find :*

(i) firing angle (ii) conduction angle (iii) average current.

Assume load resistance = 100Ω and the holding current to be zero.

Solution. $v = V_m \sin\theta$

Here, $v = 100\text{ V},\quad V_m = 200\text{ V}$

(*i*) ∴ $100 = 200 \sin\theta$

or $\sin\theta = \dfrac{100}{200} = 0.5$

∴ $\theta = \sin^{-1}(0.5) = 30°$ *i.e.* Firing angle, $\alpha = \theta = \mathbf{30°}$

(*ii*) Conduction angle, $\phi = 180° - \alpha = 180° - 30° = \mathbf{150°}$

(*iii*) $$\text{Average voltage} = \frac{V_m}{2\pi}(1+\cos\alpha) = \frac{200}{2\pi}(1+\cos 30°) = 59.25\text{ V}$$

∴ $$\text{Average current} = \frac{\text{Average voltage}}{R_L} = \frac{59.25}{100} = \mathbf{0.5925\ A}$$

Example 20.6. *An SCR half-wave rectifier has a forward breakdown voltage of 150 V when a gate current of 1 mA flows in the gate circuit. If a sinusoidal voltage of 400 V peak is applied, find:*

(i) firing angle (ii) average output voltage

(iii) average current for a load resistance of 200Ω (iv) power output

Assume that the gate current is 1mA throughout and the forward breakdown voltage is more than 400 V when I_g = 1 mA.

Solution. $V_m = 400\text{ V},\quad v = 150\text{ V},\quad R_L = 200\ \Omega$

(*i*) Now $v = V_m \sin\theta$

or $\sin\theta = \dfrac{v}{V_m} = \dfrac{150}{400} = 0.375$

i.e. firing angle, $\alpha\,(=\theta) = \sin^{-1} 0.375 = \mathbf{22°}$

(*ii*) Average output voltage is

$$V_{av} = \frac{V_m}{2\pi}(1+\cos 22°) = \frac{400}{2\pi}(1+\cos 22°) = \mathbf{122.6\ V}$$

(*iii*) Average current, $$I_{av} = \frac{\text{average output voltage}}{R_L} = \frac{122.6}{200} = \mathbf{0.613\ A}$$

(*iv*) Output power $= V_{av} \times I_{av} = 122.6 \times 0.613 = \mathbf{75.15\ W}$

Example 20.7. *An a.c. voltage v = 240 sin314 t is applied to an SCR half-wave rectifier. If the SCR has a forward breakdown voltage of 180 V, find the time during which SCR remains off.*

Solution. The *SCR* will remain off till the voltage across it reaches 180 V. This is shown in Fig. 20.13. Clearly, *SCR* will remain off for *t* second.

Now $v = V_m \sin 314\, t$

Here $v = 180\text{ V};\quad V_m = 240\text{ V}$

∴ $180 = 240 \sin(314\, t)$

$$\text{or} \quad \sin 314\,t = \frac{180}{240} = 0.75$$

$$\text{or} \quad 314\,t = \sin^{-1}(0.75)$$

$$= 48.6° = 0.848 \text{ radian}$$

$$\therefore \quad t = \frac{0.848}{314} = 0.0027 \text{ sec}$$

$$= \mathbf{2.7\ millisecond}$$

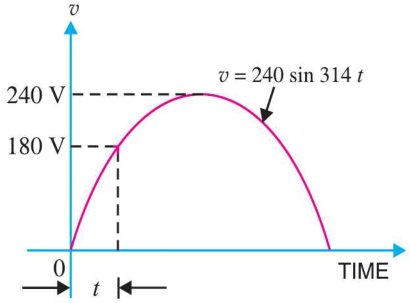


Fig. 20.13

Example 20.8. *In an SCR half-wave rectifier circuit, what peak-load current will occur if we measure an average (d.c.) load current of 1A at a firing angle of 30° ?*

Solution. Let I_m be the peak load current.

$$\text{Now,} \quad I_{av} = \frac{V_m}{2\pi R_L}(1+\cos\alpha)$$

$$= \frac{I_m}{2\pi}(1+\cos\alpha) \qquad \left(\because I_m = \frac{V_m}{R_L}\right)$$

$$\therefore \quad I_m = \frac{2\pi\, I_{av}}{1+\cos\alpha}$$

$$\text{Here} \quad I_{av} = I_{dc} = 1\text{A} \;;\; \alpha = 30°$$

$$\therefore \quad I_m = \frac{2\pi \times 1}{1+\cos 30°} = \mathbf{3.36A}$$

Example 20.9. *Power (brightness) of a 100W, 110 V tungsten lamp is to be varied by controlling the firing angle of an SCR in a half-wave rectifier circuit supplied with 110 V a.c. What r.m.s. voltage and current are developed in the lamp at firing angle α = 60°?*

Solution. The a.c. voltage is given by;

$$v = V_m \sin\theta$$

Let α be the firing angle as shown in Fig. 20.14. This means that the *SCR* will fire (*i.e.* start conducting) at θ = α. Clearly, *SCR* will conduct from α to 180°.

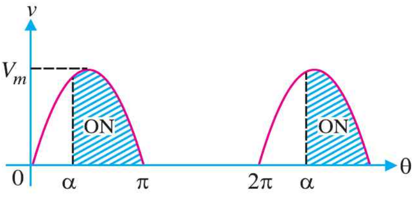


Fig. 20.14

$$E^2_{r.m.s.} = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2\theta\, d\theta$$

$$= V_m^2\,\frac{2(\pi-\alpha)+\sin 2\alpha}{8\pi}$$

$$\therefore \quad E_{r.m.s.} = V_m\sqrt{\frac{2(\pi-\alpha)+\sin 2\alpha}{8\pi}}$$

$$\text{Here,} \quad V_m = \sqrt{2}\times 110 = 156\text{V};\ \alpha = 60° = \pi/3$$

$$\therefore \quad E_{r.m.s.} = 156\sqrt{\frac{2(\pi-\pi/3)+\sin 120°}{8\pi}} = \mathbf{70\ V}$$

$$\text{Lamp resistance,} \quad R_L = \frac{V^2}{P} = \frac{(110)^2}{100} = 121\Omega$$

$$\therefore \quad I_{r.m.s.} = \frac{E_{r.m.s.}}{R_L} = \frac{70}{121} = \mathbf{0.58\ A}$$

---

* On carrying out the integration.

Comments. The load current can be decreased by increasing the firing angle. The larger the value of α, the smaller is the load current and vice-versa. This method of controlling power is very efficient because other methods, such as added series resistance, waste much power in the added control element.

20.10 SCR Full-Wave Rectifier

Fig. 20.15 (*i*) shows the circuit of *SCR* full-wave rectifier. It is exactly like an ordinary centre-tap circuit except that the two diodes have been replaced by two *SCRs*. The gates of both *SCR*s get their supply from two gate controls. One *SCR* conducts during the positive half-cycle and the other during the negative half-cycle. Consequently, full-wave rectified output is obtained across the load.

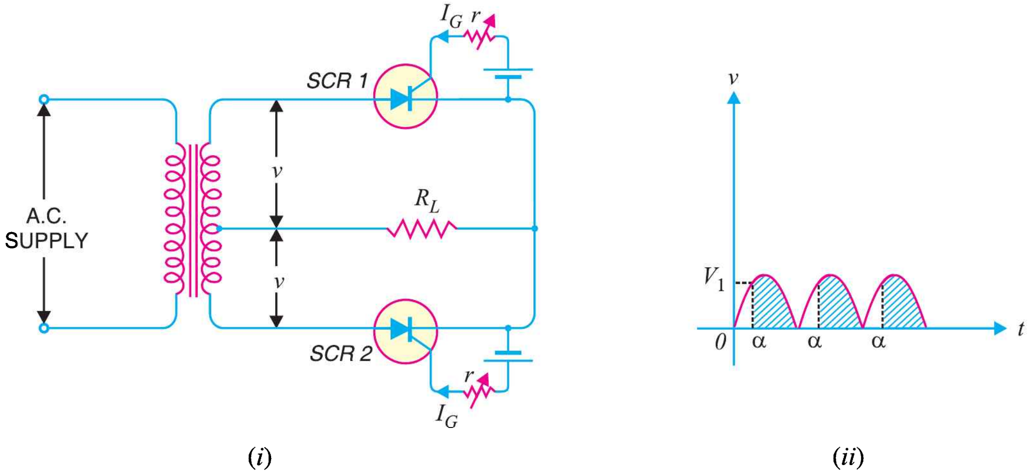


Fig. 20.15

Operation. The angle of conduction can be changed by adjusting the gate currents. Suppose the gate currents are so adjusted that *SCRs* conduct as the secondary voltage (across half winding) becomes V_1. During the positive half-cycle of a.c. across secondary, the upper end of secondary is positive and the lower end negative. This will cause *SCR*1 to conduct. However, the conduction will start only when the voltage across the upper half of secondary becomes V_1 as shown in Fig. 20.15 (*ii*). In this way, only shaded portion of positive half-cycle will pass through the load.

During the negative half-cycle of a.c. input, the upper end of secondary becomes negative and the lower end positive. This will cause *SCR*2 to conduct when the voltage across the lower half of secondary becomes V_1. It may be seen that current through the load is in the same direction (d.c.) on both half-cycles of input a.c. The obvious advantage of this circuit over ordinary full-wave rectifier circuit is that by adjusting the gate currents, we can change the conduction angle and hence the output voltage.

Mathematical treatment. Referring to Fig. 20.15 (*i*), let $v = V_m \sin \theta$ be the alternating voltage that appears between centre tap and either end of secondary. Let α be the firing angle.

$$\text{Average output, } V_{av} = \frac{1}{\pi}\int_{\alpha}^{180^\circ} V_m \sin \theta \, d\theta = \frac{V_m}{\pi}\int_{\alpha}^{180^\circ} \sin \theta \, d\theta$$

$$= \frac{V_m}{\pi}[-\cos \theta]_{\alpha}^{180^\circ} = \frac{V_m}{\pi}(\cos \alpha - \cos 180^\circ)$$

$$\therefore \qquad V_{av} = \frac{V_m}{\pi}(1 + \cos\alpha)$$

This value is double that of a half-wave rectifier. It is expected since now negative half-cycle is also rectified.

$$\text{Average current, } I_{av} = \frac{V_{av}}{R_L} = \frac{V_m}{\pi R_L}(1 + \cos\alpha)$$

Example 20.10. *An SCR full-wave rectifier supplies to a load of 100 Ω. If the peak a.c. voltage between centre tap and one end of secondary is 200V, find (i) d.c. output voltage and (ii) load current for a firing angle of 60°.*

Solution. $V_m = 200\text{ V}; \quad \alpha = 60°; \quad R_L = 100\ \Omega$

(*i*) D.C. output voltage, $V_{av} = \frac{V_m}{\pi}(1 + \cos\alpha) = \frac{200}{\pi}(1 + \cos 60°) = \mathbf{95.5\ V}$

(*ii*) Load current, $I_{av} = \frac{V_{av}}{R_L} = \frac{95.5}{100} = \mathbf{0.955\ A}$

Example 20.11. *Power (brightness) of a 100 W, 110 V lamp is to be varied by controlling firing angle of SCR full-wave circuit; the r.m.s. value of a.c. voltage appearing across each SCR being 110 V. Find the r.m.s. voltage and current in the lamp at firing angle of 60°.*

Solution. Let $v = V_m \sin\theta$ be the alternating voltage that appears between centre tap and either end of the secondary. Let α be the firing angle as shown in Fig. 20.16. This means that *SCR* will conduct at θ = α. Clearly, *SCR* circuit will conduct from α to 180°.

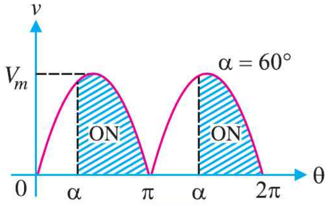


Fig. 20.16

$$E^2_{r.m.s.} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2\theta\, d\theta$$

$$= V_m^2\ {}^{*}\frac{2(\pi - \alpha) + \sin 2\alpha}{4\pi}$$

$$\therefore \qquad E_{r.m.s.} = V_m\sqrt{\frac{2(\pi - \alpha) + \sin 2\alpha}{4\pi}}$$

Here $V_m = 110 \times \sqrt{2} = 156\text{V}; \alpha = 60°$

$$\therefore \qquad E_{r.m.s.} = 156\sqrt{\frac{2(\pi - \pi/3) + \sin 120°}{4\pi}} = \mathbf{98.9V}$$

$$\text{Lamp resistance, } R_L = \frac{V^2}{P} = \frac{(110)^2}{100} = 121\Omega$$

$$\therefore \qquad I_{r.m.s.} = \frac{E_{r.m.s.}}{R_L} = \frac{98.9}{121} = \mathbf{0.82\ A}$$

20.11 Single-Phase SCR Inverter Circuit

SCR inverter provides an efficient and economical way of converting direct current or voltage into alternating current or voltage. In this application, *SCR* acts as a controlled switch, alternately opening and closing a d.c. circuit. Fig. 20.17 shows the basic inverter circuit. Here, a.c. voltage is generated by alternately closing and opening switches S_1 and S_2. Replacing, the mechanical switches

---

* On carrying out the integration.

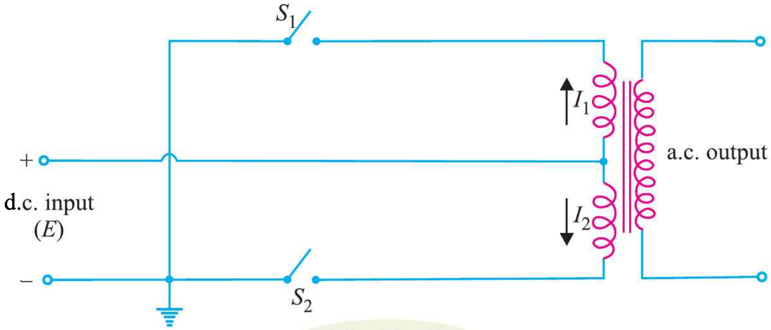


Fig. 20.17

with *SCR*s, whose gates are triggered by an external pulse generator, we get the practical *SCR* inverter as shown in Fig. 20.18.

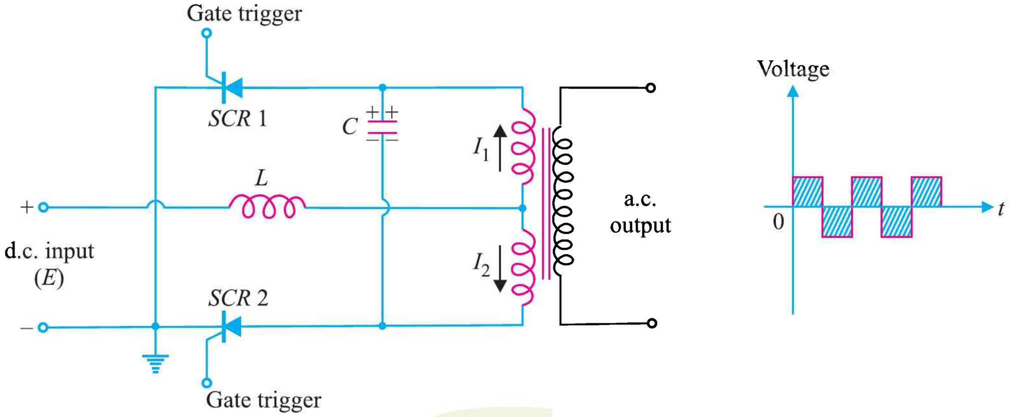


Fig. 20.18

Circuit Action

The circuit action is as under :

(*i*) When conduction is initiated by applying a positive trigger pulse to *SCR* 1 (*SCR* 2 is assumed *OFF*), the voltage across *SCR* decreases rapidly as the current through it increases. At the same time, the capacitor *C* charges through *SCR* 1 in the polarity shown. The load current flows through inductor *L*, upper half of the transformer primary winding and *SCR*1.

(*ii*) When a firing pulse is applied to the gate of *SCR* 2, this *SCR* turns on and conducts current. At this instant, capacitor *C* begins to discharge through *SCR* 1 and *SCR* 2. This discharge current flows through *SCR* 1 in a *reverse* direction. This reverse current turns off *SCR*1. At this time, with *SCR* 1 turned off, the capacitor voltage (approximately–*2*E*) appears across *SCR* 1 as a reverse voltage, long enough for this *SCR* to recover for forward blocking.

Simultaneously, during this interval, conducting *SCR* 2 allows the capacitor to discharge through the transformer primary winding and inductor *L*. The function of *L* is to control the discharge rate of *C* to allow sufficient time for *SCR* 1 to turn *OFF*. Capacitor *C* discharges rapidly from – 2*E* to zero and then charges up in the opposite direction to + 2*E*. The load current is now carried through the second half of the transformer primary winding and *SCR* 2.

(*iii*) When trigger pulse is applied to the gate of *SCR* 1, this device will conduct and *SCR* 2 will turn off by the process just described. In this way, *SCR* 1 and *SCR* 2 alternately turn *ON* and *OFF*. Consequently, a.c. output is obtained as shown in Fig. 20.18.

---

* The capacitor voltage will charge to double the suppply voltage (*E*) as a result of transformer action between the two primary windings.

The a.c. waveform produced by a single-phase inverter is a poor version of sine wave and would not be suitable for most industrial, commercial and domestic loads. More complex inverters using multiple *SCR*s and sophisticated triggering circuits are capable of generating a.c. voltages that are extremely close to a pure sine wave.

20.12 Applications of SCR

The ability of an *SCR* to control large currents in a load by means of small gate current makes this device useful in switching and control applications. Some of the important applications of *SCR* are discussed below :

(*i*) **SCR as static contactor.** An important application of *SCR* is for switching operations. As *SCR* has no moving parts, therefore, when it is used as a switch, it is often called a *static contactor.*

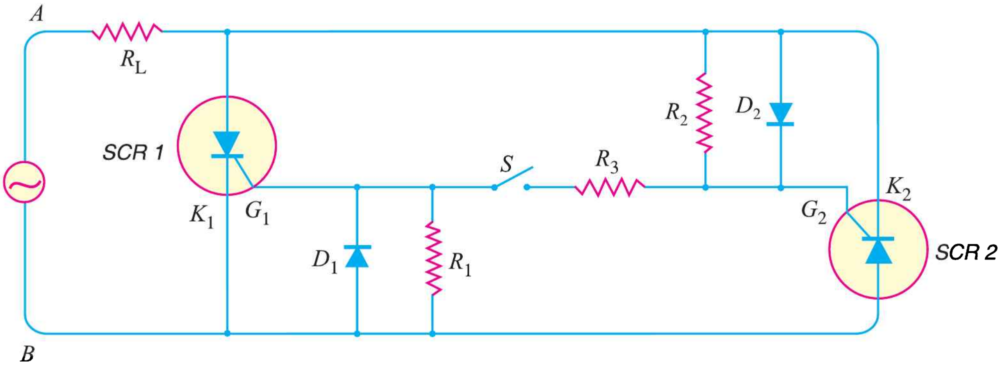


Fig. 20.19

Fig. 20.19 shows the use of *SCR* to switch *ON* or *OFF* a.c. power to a load R_L. Resistances R_1 and R_2 are for the protection of diodes D_1 and D_2 respectively. Resistance R_3 is the gate current limiting resistor. To start the circuit, switch is closed. During the positive half-cycle of a.c. supply, end *A* is positive and end *B* is negative. Then diode D_2 sends gate current through *SCR*1. Therefore *SCR*1 is turned *ON* while *SCR*2 remains *OFF* as its anode is negative *w.r.t.* cathode. The current conduction by *SCR*1 follows the path AR_LK_1BA. Similarly, in the next half-cycle, *SCR*2 is turned *ON* and conducts current through the load. It may be seen that switch *S* handles only a few mA of gate current to switch *ON* several hundred amperes in the load R_L. This is a distinct advantage over a mechanical switch.

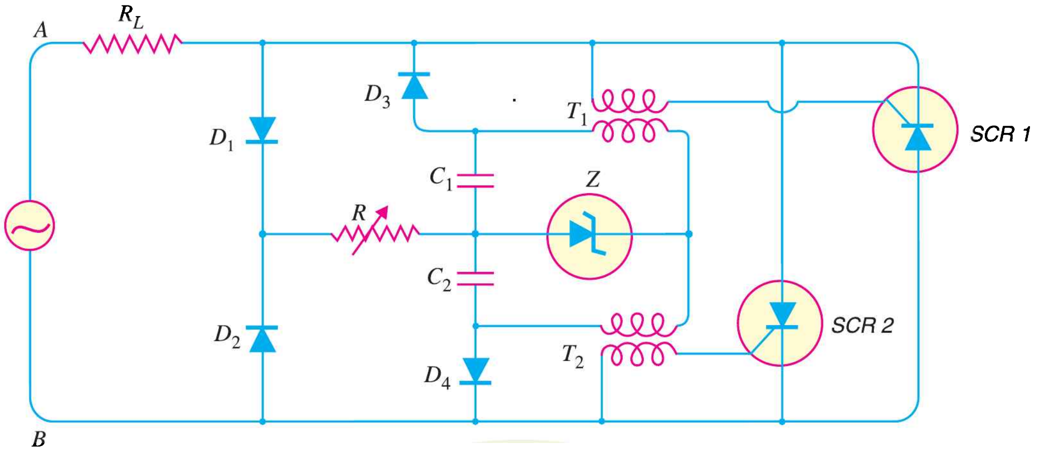


Fig. 20.20

(*ii*) **SCR for power control.** It is often necessary to control power delivered to some load such as the heating element of a furnace. Series resistances or potentiometers cannot be used because they waste power in high power circuits. Under such conditions, silicon controlled rectifiers are used which are capable of adjusting the transmitted power with little waste. Fig. 20.20 shows a common circuit for controlling power in the load R_L. During the positive half-cycle of a.c. supply, end A is positive and end B is negative. Therefore, capacitor C_2 is charged through $AD_1\ RC_2\ D_4B$. The charge on the capacitor C_2 depends upon the value of potentiometer R. When the capacitor C_2 is charged through a sufficient voltage, it discharges through the zener Z. This gives a pulse to the primary and hence secondary of transformer T_2. This turns on $SCR2$ which conducts currents through the load R_L. During negative half-cycle of supply, the capacitor C_1 is charged. It discharges through the zener and fires $SCR1$ which conducts current through the load.

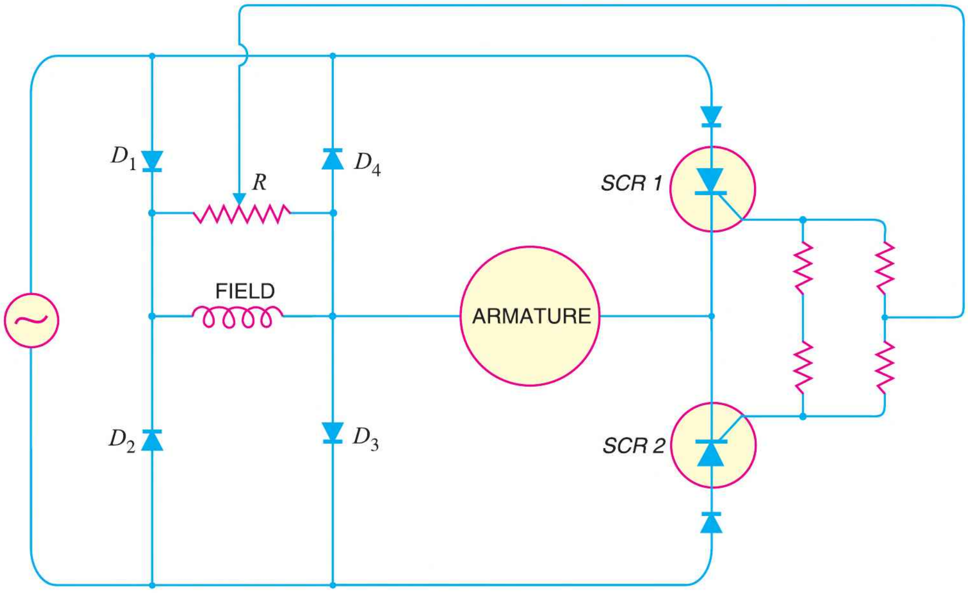
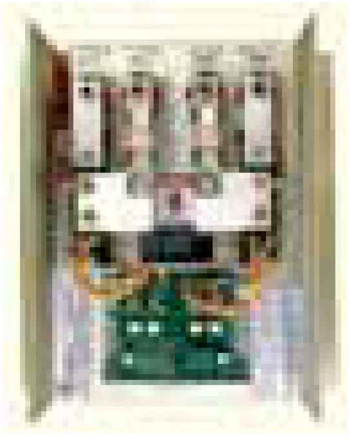


Fig. 20.21

The angle of conduction can be controlled by the potentiometer R. The greater the resistance of R, lesser is the voltage across C_1 or C_2 and hence smaller will be the time during which $SCR1$ and $SCR2$ will conduct in a full cycle. In this way, we can control a large power of several kW in the load R_L with the help of a small potentiometer R.



SCR Power Control

(*iii*) **SCRs for speed control of d.c. shunt motor.** The conventional method of speed control of d.c. shunt motor is to change the field excitation. But change in field excitation changes the motor torque also. This drawback is overcome in SCR control as shown in Fig. 20.21. Diodes D_1, D_2, D_3 and D_4 form the bridge. This bridge circuit converts a.c. into d.c. and supplies it to the field winding of the motor. During the positive half-cycle of a.c. supply, $SCR1$ conducts because it gets gate current from bridge circuit as well as its anode is positive *w.r.t.* cathode. The armature winding of the motor gets current. The angle of conduction can be changed by varying the gate current. During the negative half-cycle of a.c. supply, *SCR*2 provides current to the armature winding. In this way, the voltage fed to the motor armature and hence the speed can be controlled.

(*iv*) **Overlight detector.** Fig. 20.22 shows the use of *SCR* for overlight detection. The resistor *R* is a photo-resistor, a device whose resistance decreases with the increase in light intensity. When the light falling on *R* has normal intensity, the value of *R* is high enough and the voltage across R_1 is insufficient to trigger the *SCR*. However, when *R* is in strong light, its resistance decreases and the voltage drop across R_1 becomes high enough to trigger the *SCR*. Consequently, the buzzer sounds the alarm. It may be noted that even if the strong light disappears, the buzzer continues to sound the alarm. It is because once the *SCR* is fired, the gate loses all control.

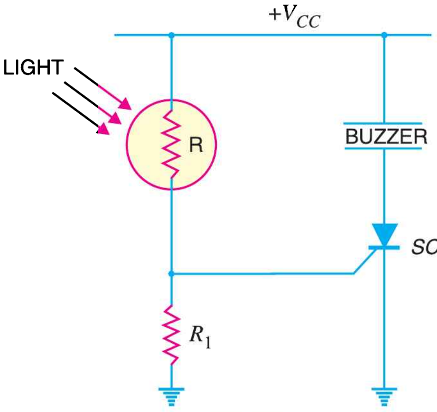


Fig. 20.22

(*v*) **SCR Crowbar.** A crowbar is a circuit that is used to protect a voltage-sensitive load from excessive d.c. power supply output voltages. Fig. 20.23 shows the *SCR* crowbar circuit. It consists of a zener diode, a gate resistor R_G and an *SCR*. It also contains a *snubber to prevent false triggering.

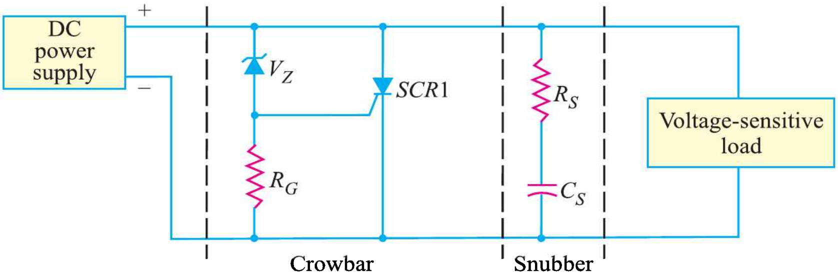


Fig. 20.23

Operation. The circuit action is as under:

(*a*) Under normal conditions, the zener diode and the *SCR* are *OFF*. With zener diode being in cutoff, there is no current through R_G and no voltage drop occurs across this resistor. This means that the gate of *SCR* is at 0V so that the *SCR* is in the off state. Therefore, as long as zener diode is off, the *SCR* behaves as an open and will not affect either the d.c. power supply or the load.

(*b*) Suppose the output voltage from the d.c. power supply suddenly *increases*. This causes the zener diode to break down and conduct current. As the current flows through the zener diode, voltage is developed across resistor R_G which causes the *SCR* to conduct current. When the *SCR* conducts, the voltage source is shorted by the *SCR*. The supply voltage fuse blows out and the load is protected from overvoltage.

20.13 Light-Activated SCR

The light-activated *SCR* (*LASCR*) is the light sensitive equivalent of the normal *SCR* and is shown in Fig. 20.24. As the name suggests, its state is controlled by the light falling on depletion layers. In a normal *SCR*, gate current

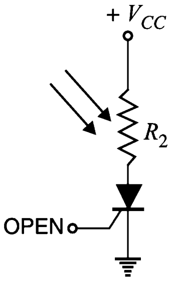


Fig. 20.24

---

* It is an *RC* circuit connected between the *SCR* anode and cathode to eliminate false triggering.

turns on the device. In the **LASCR*, instead of having the external gate current applied, light shinning on the device turns it *ON*. Just as a normal *SCR*, the *LASCR* will continue to conduct even if the light source is removed. The *LASCRs* find many applications including optical light controls, relays, phase control, motor control and a large number of computer applications. The maximum current (r.m.s.) and power (gate) ratings for *LASCRs* commercially available today are about 3A and 0.1W. It may be noted that *LASCR* is most sensitive to light when the gate terminal is open. Its sensitivity can be reduced and controlled by the insertion of a gate resistor.

Example 20.12. *The SCR of Fig. 20.25 has gate trigger voltage $V_T = 0.7V$, gate trigger current $I_T = 7$ mA and holding current $I_H = 6$ mA.*

(*i*) *What is the output voltage when the SCR is off ?*

(*ii*) *What is the input voltage that triggers the SCR ?*

(*iii*) *If V_{CC} is decreased until the SCR opens, what is the value of V_{CC} ?*

Solution.

(*i*) When the *SCR* is off (*i.e.* it is not conducting), there is no current through the 100Ω resistor.

$$\therefore \quad V_{out} = \text{Supply voltage } V_{CC} = \mathbf{15V}$$

(*ii*) The input voltage V_{in} must overcome V_T(=0.7V) and also cause 7 mA to flow through 1 kΩ resistor.

$$\therefore \quad V_{in} = V_T + I_T R = 0.7 + (7 \text{ mA})(1 \text{ k}\Omega) = \mathbf{7.7V}$$

(*iii*) In order to open the *SCR*, the V_{CC} must be reduced so that anode current is equal to I_H.

$$\therefore \quad I_H = \frac{V_{CC} - V_T}{100\ \Omega}$$

$$\text{or} \quad V_{CC} = (100\Omega)(I_H) + V_T = (100\Omega)(6 \text{ mA}) + 0.7 = \mathbf{1.3V}$$

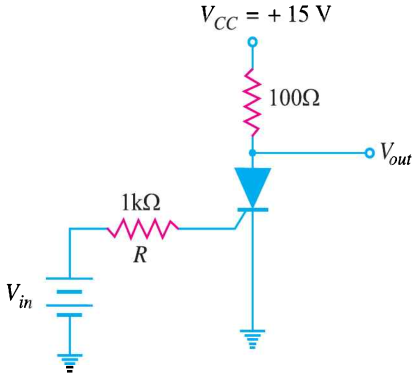


Fig. 20.25

Example 20.13. *In Fig. 20.26, the SCR has a trigger voltage of 0.7 V. Calculate the supply voltage that turns on the crowbar. Ignore zener diode resistance.*

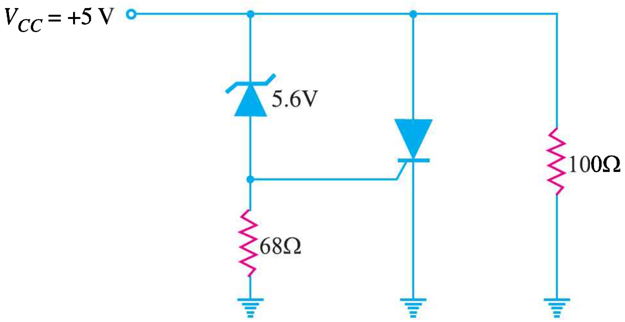


Fig. 20.26

Solution. The breakdown voltage of the zener is 5.6V. To turn on the *SCR*, the voltage across 68Ω has to be equal to V_T (= 0.7V).

$$\therefore \quad V_{CC} = V_Z + V_T = 5.6 + 0.7 = \mathbf{6.3V}$$

---

* For maximum sensitivity to light, the gate is left open.

When the supply voltage becomes 6.3 V, the zener breaks down and starts conducting. The voltage V_T (= 0.7V) across 68Ω forces the *SCR* into conduction. When the *SCR* conducts, the supply voltage is shorted by the *SCR* and the fuse in the supply voltage burns out. Thus the load (100Ω) is protected from overvoltage.

Example. 20.14. *The zener diode of Fig. 20.27 has a tolerance of ± 10% and the trigger voltage can be as high as 1.5V. What is the maximum supply voltage where crowbarring takes place?*

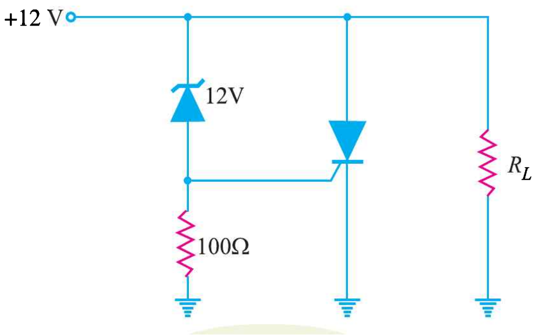


Fig. 20.27

Solution. The breakdown voltage of the zener diode is 12V and it has a tolerance of ± 10%. It means that breakdown voltage of zener can vary from 10.8V to 13.2V. Since the trigger voltage of *SCR* has a maximum value of 1.5 V,

∴ Maximum value of supply voltage for crowbarring

$= 13.2\text{V} + 1.5\text{V} = \mathbf{14.7V}$

Example. 20.15. ***The circuit of Fig. 20.28 is in a dark room. When a bright light is turned on, the LASCR fires. What is the approximate output voltage? If the bright light is turned off, what is the output voltage?***

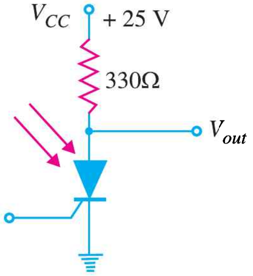


Fig. 20.28

Solution. Fig. 20.28 shows a light-activated *SCR*, also known as a photo-*SCR*. When light falls on the device, it starts conducting and the output voltage is ideally,

$$V_{out} = \mathbf{0V}$$

However, if we take into account anode-cathode drop, $V_{out} = 0.7\text{V}$.

When light is turned off, the *LASCR* stops conducting and the output voltage is equal to the supply voltage V_{CC} *i.e.*

$$V_{out} = V_{CC} = \mathbf{+ 25V}$$

Example 20.16. *Give a simple method for testing an SCR.*

Solution. Fig. 20.29 shows a simple circuit for testing an *SCR*. The test lamp serves two purposes. First, it is a visual indicator of current conduction. Secondly, it limits current through the *SCR*.

(*i*) When switch *S* is closed, the lamp should not light for the *SCR* to be good. It is because voltage is *applied only between anode and cathode but there is no trigger voltage. If the lamp lights, the *SCR* is *shorted.*

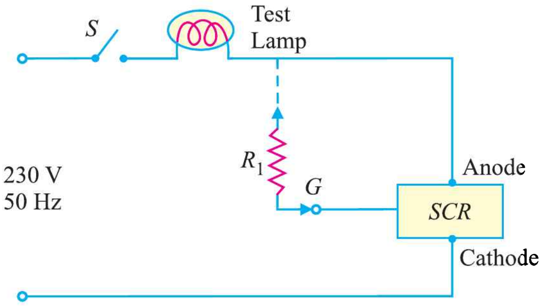


Fig. 20.29

---

* It is understood that the applied voltage is less than the breakover voltage of the *SCR*.

(*ii*) Now touch R_1 momentarily between gate and anode terminals. For the *SCR* to be good, the lamp should light and *continue to light. If it does not, the *SCR* is *open*.

Note that the lamp will be on at half brilliance because the *SCR* conducts only every other half-cycle.

MULTIPLE-CHOICE QUESTIONS

1. An *SCR* has .... *pn* junctions.
(*i*) two (*ii*) three
(*iii*) four (*iv*) none of the above

2. An *SCR* is a solid state equivalent of ....
(*i*) triode (*ii*) pentode
(*iii*) gas-filled triode (*iv*) tetrode

3. An *SCR* has .... semiconductor layers.
(*i*) two (*ii*) three
(*iii*) four (*iv*) none of the above

4. An *SCR* has three terminals *viz.* ....
(*i*) cathode, anode, gate
(*ii*) anode, cathode, grid
(*iii*) anode, cathode, drain
(*iv*) none of the above

5. An *SCR* behaves as a .... switch.
(*i*) unidirectional (*ii*) bidirectional
(*iii*) mechanical (*iv*) none of the above

6. An *SCR* is sometimes called ....
(*i*) triac
(*ii*) diac
(*iii*) unijunction transistor
(*iv*) thyristor

7. An *SCR* is made of ....
(*i*) germanium (*ii*) silicon
(*iii*) carbon (*iv*) none of the above

8. In the normal operation of an *SCR*, anode is .... *w.r.t.* cathode.
(*i*) at zero potential
(*ii*) negative
(*iii*) positive
(*iv*) none of the above

9. In normal operation of an *SCR*, gate is .... *w.r.t.* cathode.
(*i*) positive
(*ii*) negative
(*iii*) at zero potential
(*iv*) none of the above

10. An *SCR* combines the features of ....
(*i*) a rectifier and resistance
(*ii*) a rectifier and transistor
(*iii*) a rectifier and capacitor
(*iv*) none of the above

11. The control element in an *SCR* is ....
(*i*) cathode (*ii*) anode
(*iii*) anode supply (*iv*) gate

12. The normal way to turn on an *SCR* is by ....
(*i*) breakover voltage
(*ii*) appropriate anode current
(*iii*) appropriate gate current
(*iv*) none of the above

13. An *SCR* is turned off by ....
(*i*) reducing anode voltage to zero
(*ii*) reducing gate voltage to zero
(*iii*) reverse biasing the gate
(*iv*) none of the above

14. An *SCR* is a .... triggered device.
(*i*) voltage
(*ii*) current
(*iii*) voltage as well as current
(*iv*) none of the above

15. In an *SCR* circuit, the supply voltage is generally .... that of breakover voltage.
(*i*) equal to (*ii*) less than
(*iii*) greater than (*iv*) none of the above

16. When an *SCR* is turned on, the voltage across it is about ....
(*i*) zero (*ii*) 10 V
(*iii*) 0.1 V (*iv*) 1V

17. An *SCR* is made of silicon and not germanium because silicon ....
(*i*) is inexpensive
(*ii*) is mechanically strong
(*iii*) has small leakage current
(*iv*) is tetravalent

18. An *SCR* is turned off when ....
(*i*) anode current is reduced to zero
(*ii*) gate voltage is reduced to zero
(*iii*) gate is reverse biased
(*iv*) none of the above

---

* Recall that once the *SCR* is fired by the gate voltage, it continues to conduct current even if the gate voltage is removed.

19. In an *SCR* circuit, the angle of conduction can be changed by ....
- (*i*) changing anode voltage
- (*ii*) changing gate voltage
- (*iii*) reverse biasing the gate
- (*iv*) none of the above

20. If firing angle in an *SCR* circuit is increased, the output ....
- (*i*) remains the same
- (*ii*) is increased
- (*iii*) is decreased
- (*iv*) none of the above

21. If gate current is increased, then anode-cathode voltage at which *SCR* closes ....
- (*i*) is decreased
- (*ii*) is increased
- (*iii*) remains the same
- (*iv*) none of the above

22. When *SCR* is *OFF*, the current in the circuit is ....
- (*i*) exactly zero
- (*ii*) small leakage current
- (*iii*) large leakage current
- (*iv*) none of the above

23. An *SCR* can exercise control over .... of a.c. supply.
- (*i*) positive half-cycles only
- (*ii*) negative half-cycles only
- (*iii*) both positive and negative half-cycles
- (*iv*) positive or negative half-cycles

24. We can control a.c. power in a load by connecting ....
- (*i*) two *SCRs* in series
- (*ii*) two *SCRs* in parallel
- (*iii*) two *SCRs* in parallel opposition
- (*iv*) none of the above

25. When *SCR* starts conducting, then .... loses all control.
- (*i*) gate
- (*ii*) cathode
- (*iii*) anode
- (*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iii*)	**3.** (*iii*)	**4.** (*i*)	**5.** (*i*)
6. (*iv*)	**7.** (*ii*)	**8.** (*iii*)	**9.** (*i*)	**10.** (*ii*)
11. (*iv*)	**12.** (*iii*)	**13.** (*i*)	**14.** (*ii*)	**15.** (*ii*)
16. (*iv*)	**17.** (*iii*)	**18.** (*i*)	**19.** (*ii*)	**20.** (*iii*)
21. (*i*)	**22.** (*ii*)	**23.** (*iv*)	**24.** (*iii*)	**25.** (*i*)

Chapter Review Topics

1. Explain the construction and working of an *SCR*.
2. Draw the equivalent circuit of an *SCR* and explain its working from this equivalent circuit.
3. Explain the terms breakover voltage, holding current and forward current rating as used in connection with *SCR* analysis.
4. Draw the *V-I* characteristics of an *SCR*. What do you infer from them ?
5. Explain the action of an *SCR* as a switch. What are the advantages of *SCR* switch over a mechanical or electro-mechanical switch ?
6. Discuss some important applications of *SCR*.

Problems

1. An *SCR* has a breakover voltage of 450 V, a trigger current of 15 mA and holding current of 10 mA. What do you infer from it?
2. An *SCR* in a circuit is subjected to a 50 A current surge that lasts for 10 ms. Determine whether or not this surge will destroy the device. Given that circuit fusing rating of *SCR* is 90 A^{2}s. **[will not be destroyed]**
3. An *SCR* has a circuit fusing rating of 70 A^{2}s. The device is being used in a circuit where it could be subjected to a 100 A surge. Determine the limit on the duration of such a surge. **[7ms]**
4. An *SCR* has a circuit fusing rating of 60 A^{2}s. Determine the highest surge current value that *SCR* can withstand for a period of 20 ms. **[54.77A]**

5. In Fig. 20.30, what value of input voltage would be required to cause the *SCR* to break down if the gate current required for firing is 10 mA ? **[3.7V]**

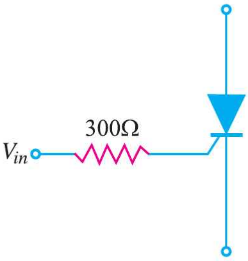


Fig. 20.30

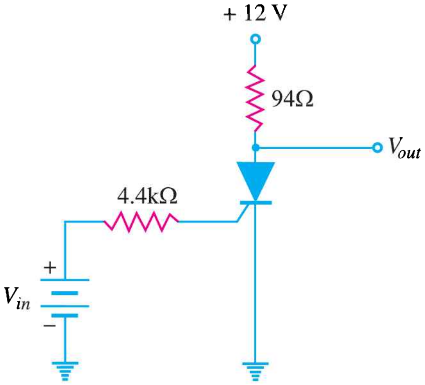


Fig. 20.31

6. In Fig. 20.31, if the trigger current of the *SCR* is 1.5 mA, what is the input voltage that triggers the *SCR*? Given $V_T = 0.7V$. **[7.3V]**
7. A 24V r.m.s. supply is connected to a half-wave *SCR* circuit that is triggered at 50°. What is the d.c. voltage delivered to the load ? **[8.88V]**

Discussion Questions

1. How does *SCR* differ from an ordinary rectifier ?
2. Why is *SCR* always turned on by gate current ?
3. Why *SCR* cannot be used as a bidirectional switch ?
4. How does *SCR* control the power fed to the load ?
5. Why are *SCRs* usually used in a.c. circuits?
6. Name three thyristor devices.
7. Why is *SCR* turned on by high-frequency radiation ?

21

Power Electronics

21.1 Power Electronics
21.2 The Triac
21.3 Triac Construction
21.4 SCR Equivalent Circuit of Triac
21.5 Triac Operation
21.6 Triac Characteristics
21.7 Triac Phase Control Circuit
21.8 Applications of Triac
21.9 The Diac
21.10 Applications of Diac
21.11 Unijunction Transistor (UJT)
21.12 Equivalent Circuit of a UJT
21.13 Characteristics of UJT
21.14 Advantages of UJT
21.15 Applications of UJT

INTRODUCTION

Since the 1950'*s* there has been a great upsurge in the development, production and applications of semiconductor devices. Today there are well over 100 million semiconductor devices manufactured in a year. These figures alone indicate how important semiconductor devices have become to the electrical industry. In fact, the present day advancement in technology is largely attributed to the widespread use of semiconductor devices in the commercial and industrial fields.

One major field of application of semiconductor devices in the recent years has been to control large blocks of power flow in a system. This has led to the development of a new branch of engineering called power electronics. The purpose of this chapter is to acquaint the readers with some important switching devices much used in power electronics.

21.1 Power Electronics

The branch of electronics which deals with the control of power at 50 Hz (i.e. supply frequency) is known as **power electronics**.

There are many applications where it is desired to control (or regulate) the power fed to a load *e.g.* to change the speed of a fan or motor. So far we have been using electrical methods to exercise such a control. However, electrical methods do not permit a *fine control over the flow of power in a system. Moreover, there is a considerable wastage of power. In the recent years, such semiconductor devices have been developed which can exercise fine control over the flow of large blocks of power in a system. Such devices act as controlled switches and can perform the duties of controlled rectification, inversion and regulation of power in a load. The important semiconductor switching devices are :

(*i*) Silicon controlled rectifier (*SCR*)
(*ii*) Triac
(*iii*) Diac
(*iv*) Unijunction transistor (*UJT*)

The silicon controlled rectifier (*SCR*) has already been discussed in the previous chapter. Therefore, we shall deal with the other three switching devices in the following discussion.

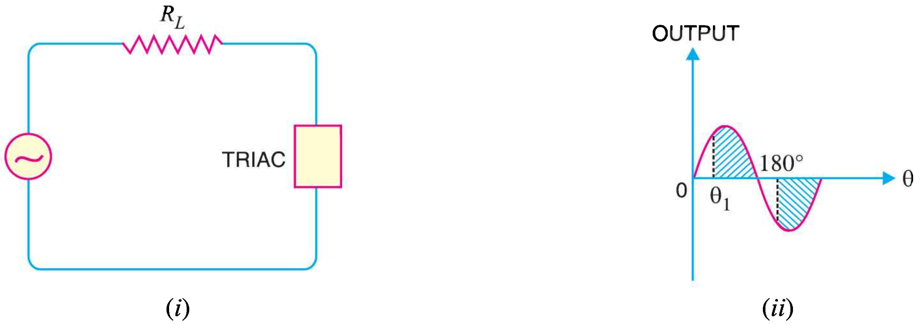
21.2 The Triac

The major drawback of an *SCR* is that it can conduct current in one direction only. Therefore, an *SCR* can only control d.c. power or forward biased half-cycles of a.c. in a load. However, in an a.c. system, it is often desirable and necessary to exercise control over both positive and negative half-cycles. For this purpose, a semiconductor device called *triac* is used.

A **triac** *is a three-terminal semiconductor switching device which can control alternating current in a load.*

Triac is an abbreviation for *triode a.c. switch*. 'Tri'– indicates that the device has three terminals and 'ac' means that the device controls alternating current or can conduct current in either direction.

The key function of a triac may be understood by referring to the simplified Fig. 21.1. The **control circuit of triac can be adjusted to pass the desired portions of positive and negative half-cycle of a.c. supply through the load R_L. Thus referring to Fig. 21.1 (*ii*), the triac passes the positive half-cycle of the supply from θ_1 to 180° *i.e.* the shaded portion of positive half-cycle. Similarly, the shaded portion of negative half-cycle will pass through the load. In this way, the alternating current and hence a.c. power flowing through the load can be controlled.



(*i*) (*ii*)

Fig. 21.1

Since a triac can control conduction of both positive and negative half-cycles of a.c. supply, it is sometimes called a bidirectional semi-conductor triode switch. The above action of a triac is certainly not a rectifying action (as in an **SCR*) so that the triac makes no mention of rectification in its name.

---

* For example, the speed of a ceiling fan can be changed in four to five steps by electrical method.

** Although it appears that 'triac' has two terminals, there is also third terminal connected to the control circuit.

21.3 Triac Construction

A triac is a three-terminal, five-layer semiconductor device whose forward and reverse characteristics are indentical to the forward characteristics of the SCR. The three terminals are designated as main terminal *MT*1, main terminal *MT*2 and gate *G*.

Fig. 21.2 (*i*) shows the basic structure of a triac. As we shall see, a triac is equivalent to two separate *SCR*s connected in inverse parallel (*i.e.* anode of each connected to the cathode of the other) with gates commoned as shown in Fig. 21.2 (*ii*). Therefore, a triac acts like a bidirectional switch *i.e.* it can conduct current in either direction. This is unlike an *SCR* which can conduct current only in one direction. Fig. 21.2 (*iii*) shows the schematic symbol of a triac. The symbol consists of two parallel diodes connected in opposite directions with a single gate lead. It can be seen that even the symbol of triac indicates that it can conduct current for either polarity of the main terminals (*MT*1 and *MT*2) *i.e.* it can act as a bidirectional switch. The gate provides control over conduction in either direction.

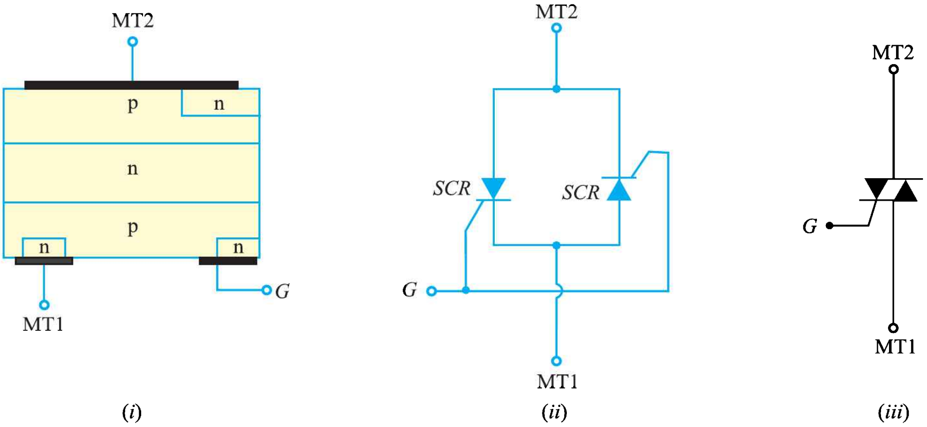


Fig. 21.2

The following points many be noted about the triac :

(*i*) The triac can conduct current (of course with proper gate current) regardless of the polarities of the main terminals *MT*1 and *MT*2. Since there is no longer a specific anode or cathode, the main leads are referred to as *MT*1 and *MT*2.

(*ii*) A triac can be turned on either with a positive or negative voltage at the gate of the device.

(*iii*) Like the *SCR*, once the triac is fired into conduction, the gate loses all control. The triac can be turned off by reducing the circuit current to the value of holding current.

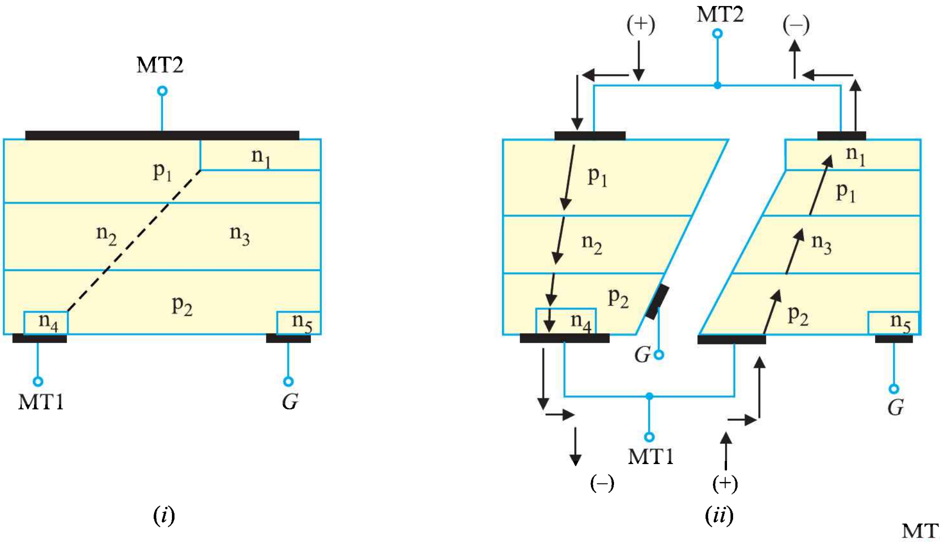
(*iv*) The main disadvantage of triacs over *SCR*s is that triacs have considerably lower current-handling capabilities. Most triacs are available in ratings of less than 40A at voltages up to 600V.

21.4 SCR Equivalent Circuit of Triac

We shall now see that a triac is equivalent to two separate *SCRs* connected in inverse parallel (*i.e.* anode of each connected to the cathode of the other) with gates commoned. Fig. 21.3 (*i*) shows the basic structure of a triac. If we split the basic structure of a triac into two halves as shown in Fig. 21.3 (*ii*), it is easy to see that we have two *SCR*s connected in inverse parallel. The left half in Fig. 21.3 (*ii*) consists of a *pnpn* device ($p_1n_2\,p_2n_4$) having three *pn* junctions and constitutes *SCR*1. Similarly, the right half in Fig. 21.3 (*ii*) consists of *pnpn* device ($p_2n_3p_1n_1$) having three *pn* junctions and constitutes *SCR*2. The *SCR* equivalent circuit of the triac is shown in Fig. 21.4.

---

* *SCR* is a controlled rectifier. It is a unidirectional switch and can conduct only in one direction. Therefore, it can control only one half-cycle (positive or negative) of a.c. supply.



(*i*) (*ii*)

Fig. 21.3

Suppose the main terminal *MT*2 is positive and main terminal *MT*1 is negative. If the triac is now fired into conduction by proper gate current, the triac will conduct current following the path (left half) shown in Fig. 21.3 (*ii*). In relation to Fig. 21.4, the *SCR*1 is *ON* and the *SCR*2 is *OFF*. Now suppose that *MT*2 is negative and *MT*1 is positive. With proper gate current, the triac will be fired into conduction. The current through the devices follows the path (right half) as shown in Fig. 21.3 (*ii*). In relation to Fig. 21.4, the *SCR*2 is *ON* and the *SCR*1 is *OFF*. Note that the triac will conduct current in the appropriate direction as long as the current through the device is greater than its holding current.

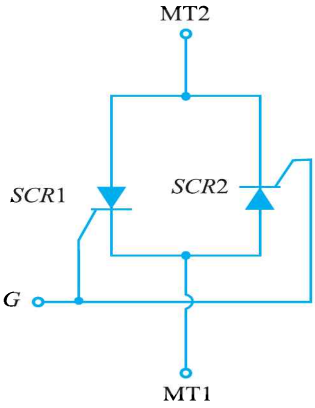


Fig. 21.4

21.5 Triac Operation

Fig. 21.5 shows the simple triac circuit. The a.c. supply to be controlled is connected across the main terminals of triac through a load resistance R_L. The gate circuit consists of battery, a current limiting resistor R and a switch S. The circuit action is as follows :

(*i*) With switch *S* open, there will be no gate current and the triac is cut off. Even with no gate current, the triac can be turned on provided the supply voltage becomes equal to the breakover voltage of triac. However, the normal way to turn on a triac is by introducing a proper gate current.

(*ii*) When switch *S* is closed, the gate current starts flowing in the gate circuit. In a similar manner to *SCR*, the breakover voltage of the triac can be varied by making proper gate current to flow. With a few milliamperes introduced at the gate, the triac will start conducting whether terminal *MT*2 is positive or negative *w.r.t.* *MT*1.

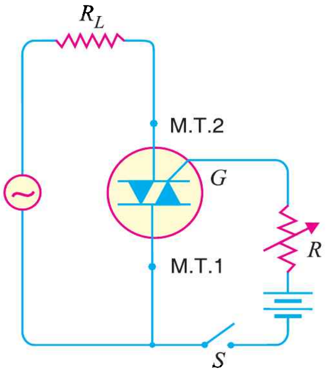


Fig. 21.5

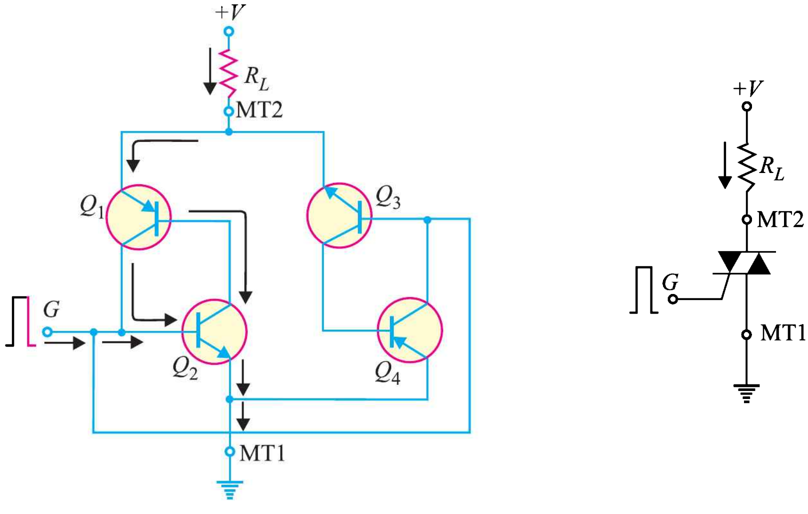
(*iii*) If terminal *MT*2 is positive *w.r.t.* *MT*1, the triac turns on and the conventional current will flow from *MT*2 to *MT*1. If the terminal *MT*2 is negative *w.r.t.* *MT*1, the triac is again turned on but this time the conventional current flows from *MT*1 to *MT*2.

The above action of triac reveals that it can act as an *a.c.* contactor to switch on or off alternating current to a load. The additional advantage of triac is that by adjusting the gate current to a proper value, any portion of both positive and negative half-cycles of *a.c.* supply can be made to flow through the load. This permits to adjust the transfer of a.c. power from the source to the load.

Example 21.1. *Draw the transistor equivalent circuit of a triac and explain its operation from this equivalent circuit.*

Solution. We have seen that transistor equivalent circuit of an *SCR* is composed of ***pnp*** transistor and ***npn*** transistor with collector of each transistor coupled to the base of the other. Since a triac is equivalent to two *SCR*s connected in inverse parallel (Refer back to Fig. 21.4), the transistor equivalent circuit of triac will be composed of four transistors arranged as shown in Fig. 21.6 (*i*). The transistors Q_1 and Q_2 constitute the equivalent circuit of *SCR*1 while the transistors Q_3 and Q_4 constitute the equivalent circuit of *SCR*2. We can explain the action of triac from its transistor equivalent circuit as under :

(*i*) When *MT*2 is positive w.r.t. *MT*1 and appropriate gate current is allowed in the gate circuit, *SCR*1 is turned *ON* while *SCR*2 remains *OFF*. In terms of transistor equivalent circuit, Q_1 and Q_2 are forward biased while Q_3 and Q_4 are reverse biased. Therefore, transistors Q_1 and Q_2 conduct current as shown in Fig. 21.6 (*i*). Since Q_1 and Q_2 form a positive feedback, both transistors are quickly driven to stauration and a large current flows through the load R_L. This is as if switch between *MT*2 and *MT*1 were closed.



(*i*) (*ii*)

Fig. 21.6

Fig. 21.6 (*ii*) shows the action of triac (*MT*2 positive w.r.t. *MT*1) by replacing the triac with its symbol.

(*ii*) When *MT*2 is negative w.r.t. *MT*1 and appropriate gate current is allowed in the gate circuit, *SCR*2 is turned *ON* and *SCR*1 is *OFF*. In terms of transistor equivalent circuit, Q_3 an Q_4 are forward biased while Q_1 and Q_2 are reverse biased. Therefore, transistors Q_3 and Q_4 will conduct as shown in Fig. 21.7 (*i*). As explained above, the current in load R_L will quickly attain a large value. The circuit will behave as if a switch is closed between *MT*2 and *MT*1.

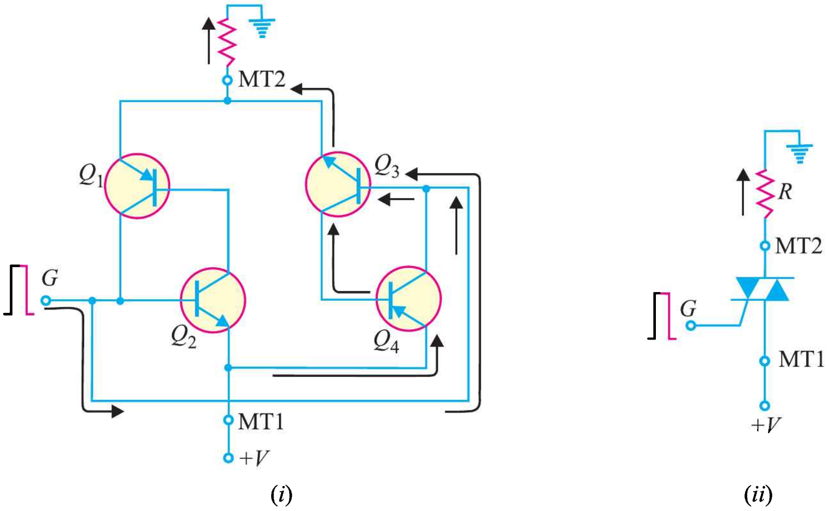


Fig. 21.7

Fig. 21.7 (*ii*) shows the action of triac (*MT*2 negative w.r.t. *MT*1) by replacing the triac with its symbol.

21.6 Traic Characteristics

Fig. 21.8 shows the *V-I* characteristics of a triac. Because the triac essentially consists of two *SCRs* of opposite orientation fabricated in the same crystal, its operating characteristics in the first and third quadrants are the same except for the direction of applied voltage and current flow. The following points may be noted from the triac characteristics :

(*i*) The *V-I* characteristics for triac in the Ist and IIIrd quadrants are essentially identical to those of an *SCR* in the Ist quadrant.

(*ii*) The triac can be operated with either positive or negative *gate* control voltage but in *normal operation usually the gate voltage is positive in quadrant I and negative in quadrant III.

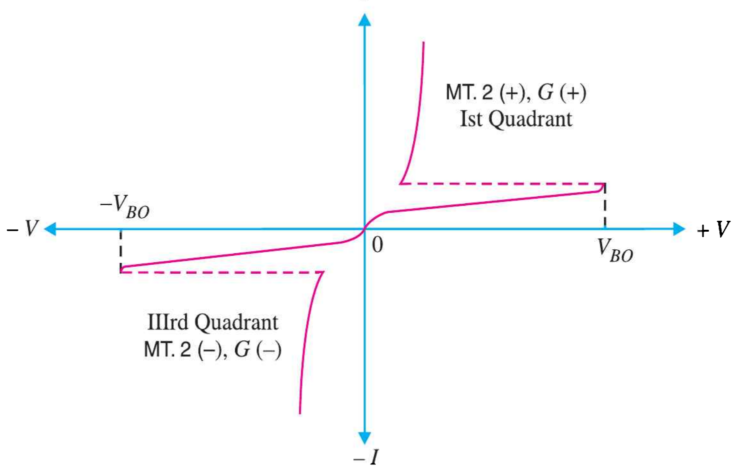


Fig. 21.8

---

* With this arrangement, less charge is required to turn on the triac.

(*iii*) The supply voltage at which the triac is turned *ON* depends upon the gate current. The greater the gate current, the smaller the supply voltage at which the triac is turned on. This permits to use a triac to control a.c. power in a load from zero to full power in a smooth and continuous manner with no loss in the controlling device.

21.7 Triac Phase Control Circuit

A *triac can be used to control the average a.c. power to a load by passing a portion of positive and negative half-cycles of input a.c. This is achieved by changing the conduction angle through the load. Fig. 21.9 shows the basic triac phase control circuit. This circuit uses a capacitor C and variable resistance R_1 to shift the phase angle of the gate signal. Because of this phase shift, the gate voltage lags the line voltage by an angle between 0° and 90°. By adjusting the variable resistance R_1, the conduction angle through the load can be changed. Thus any portion of positive and negative half-cycles of the a.c. can be passed through the load. This action of triac permits it to be used as a *controlled ** bidirectional switch.*

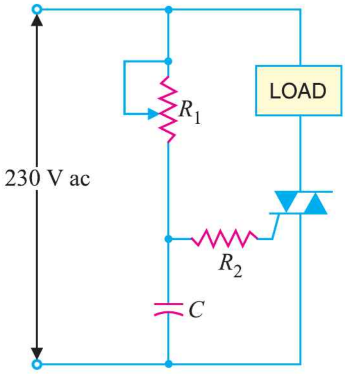


Fig. 21.9

Circuit action. The operation of triac phase control circuit is as under :

(*i*) During each positive half-cycle of the a.c., the triac is off for a certain interval, called *firing angle* α (measured in degrees) and then it is triggered on and conducts current through the load for the remaining portion of the positive half-cycle, called the *conduction angle* θ_C. The value of firing angle α (and hence θ_C)can be changed by adjusting the variable resistance R_1. If R_1 is increased, the capacitor will charge more slowly, resulting in the triac being triggered later in the cycle *i.e.* firing angle α is increased while conduction angle θ_C is decreased. As a result, smaller a.c. power is fed to the load. Reverse happens if the resistance R_1 is decreased.

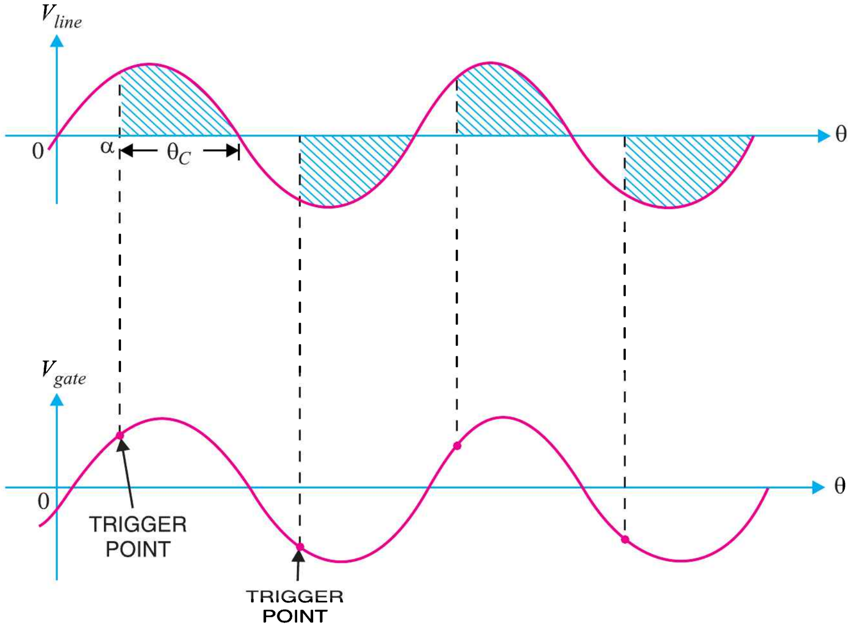


Fig. 21.10

---

* An *SCR* can only control the positive half-cycle or negative half-cycle of a.c.

** An *SCR* is a controlled unidirectional switch because it can conduct only in one direction.

(*ii*) During each negative half-cycle of the a.c., a similar action occurs except that now current in the load is in the opposite direction.

Fig. 21.10 shows the waveforms of the line voltage and gate voltage. Only the shaded portion of the positive and negative half-cycles pass through the load. We can change the phase angle of gate voltage by adjusting the variable resistance R_1. Thus a triac can control the a.c. power fed to a load. This control of a.c. power is useful in many applications such as industrial heating, lighting etc.

21.8 Applications of Triac

As low gate currents and voltages can be used to control large load currents and voltages, therefore, triac is often used as an electronic on/off switch controlled by a low-current mechanical switch.

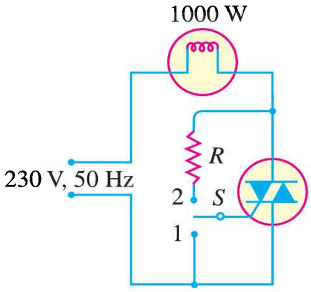


Fig. 21.11

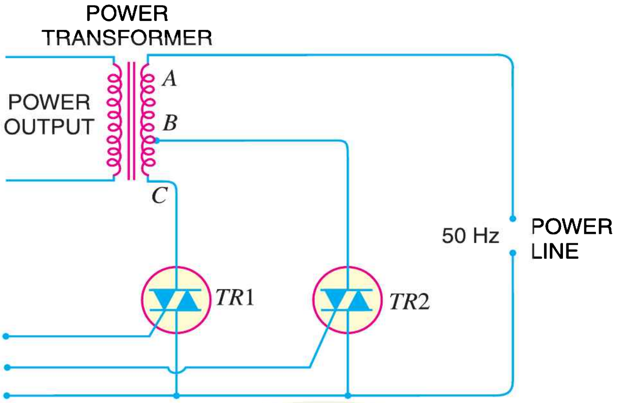


Fig. 21.12

(*i*) **As a high-power lamp switch.** Fig. 21.11 shows the use of a triac as an *a.c.* on/off switch. When switch *S* is thrown to position 1, the triac is cut off and the output power of lamp is zero. But as the switch is thrown to position 2, a small gate current (a few mA) flowing through the gate turns the triac on. Consequently, the lamp is switched on to give full output of 1000 watts.

(*ii*) **Electronic change over of transformer taps.** Fig. 21.12 shows the circuit of electronic change over of power transformer input taps. Two triacs *TR*1 and *TR*2 are used for the purpose. When triac *TR*1 is turned on and *TR*2 is turned off, the line input is connected across the full transformer primary *AC*. However, if it is desired to change the tapping so that input appears across part *AB* of the primary, then *TR*2 is turned on and *TR*1 is turned off. The gate control signals are so controlled that both triacs are never switched on together. This avoids a dangerous short circuit on the section *BC* of the primary.

Triac as an a.c. switch

Example 21.2. *Give a simple method for testing a triac.*

Solution. Fig. 21.13 shows a simple circuit for testing a triac. The test lamp serves two purposes. First, it is a visual indicator of current conduction. Secondly, it limits current through the triac.

(*i*) When switch *S* is closed, the lamp should not light for the triac to be good. It is because voltage is *applied only between *MT*2 and *MT*1 but there is no trigger voltage. If the lamp lights, the triac is *shorted.*

---

* It is understood that the applied voltage is less than the breakover voltage of the triac.

(*ii*) Now touch R_1 momentarily between gate and *MT*2 terminal. For the triac to be good, the lamp should light and *continue to light. If it does not, the triac is *open*.

Note that the lamp is on at full brilliance because the triac conducts both half-cycles (positive and negative) of a.c. This method of triac testing has two main advantages. First, it is a very simple method. Secondly, it does not require expensive apparatus.

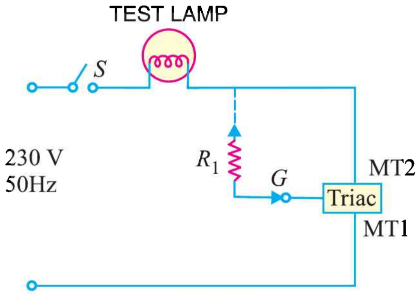


Fig. 21.13

Example 21.3. *The triac shown in Fig. 21.14 can be triggered by the gate triggering voltage* $V_{GT} = \pm 2V$*. How will you trigger the triac by (i) only a positive gate voltage (ii) only a negative gate voltage ?*

Solution. In Fig. 21.14, the triac will be triggered into conduction for $V_{GT} = \pm 2V$.

(*i*) In order that the triac is triggered only by a positive gate voltage, we can use the method shown in Fig. 21.15. In this circuit, diode D_1 is forward biased when V_{GT} is positive and reverse biased when V_{GT} is negative. Since D_1 will conduct only when V_{GT} is positive, the triac can only be triggered by a positive gate signal. The voltage V_A required to trigger the device is equal to the sum of V_F for diode D_1 and the required gate triggering voltage *i.e.*

$$V_A = V_F + V_{GT} = 0.7V + 2V = 2.7V$$

(*ii*) In order that the triac is triggered only by the negative voltage, reverse the direction of diode D_1.

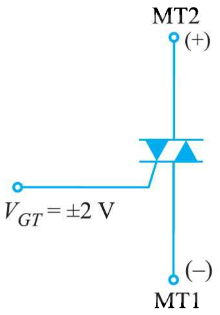


Fig. 21.14

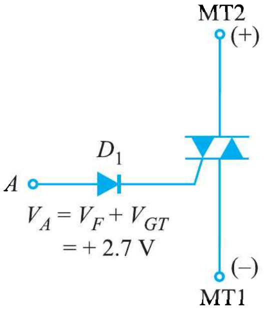


Fig. 21.15

Example 21.4. *In Fig. 21.16, the switch is closed. If the triac has fired, what is the current through 50Ω resistor when (i) triac is ideal (ii) triac has a drop of 1V ?*

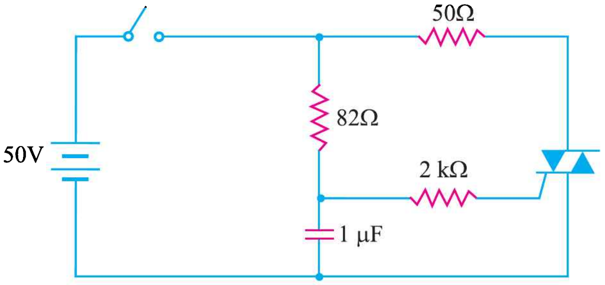


Fig. 21.16

Solution.

(*i*) Since the triac is ideal and it is fired into conduction, the voltage across triac is 0V. Therefore, the entire supply voltage of 50V appears across 50Ω resistor.

---

* Recall that once the triac is fired by the gate voltage, it continues to conduct even if the gate voltage is removed.

$\therefore$ Current in 50Ω $= \dfrac{50\text{V}}{50\Omega} = \mathbf{1\,A}$

(*ii*) When triac is fired into conduction, voltage across 50Ω resistor = 50V – 1V = 49V.

$\therefore$ Current in 50Ω $= \dfrac{49\text{V}}{50\Omega} = \mathbf{0.98\,A}$

21.9 The Diac

A **diac** *is a two-terminal, three layer bidirectional device which can be switched from its OFF state to ON state for either polarity of applied voltage.*

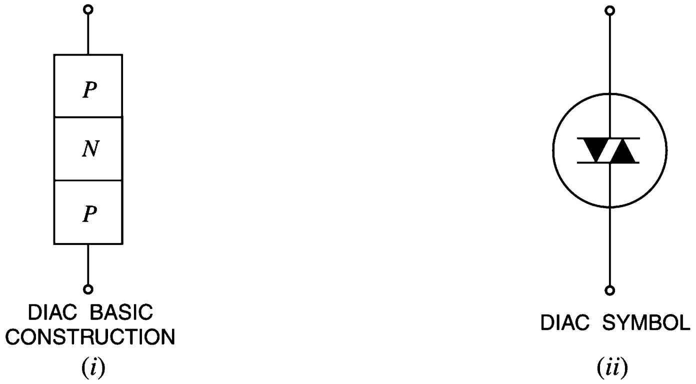


Fig. 21.17

The diac can be constructed in either *npn* or *pnp* form. Fig. 21.17 (*i*) shows the basic structure of a diac in *pnp* form. The two leads are connected to *p*-regions of silicon separated by an *n*-region. The structure of diac is very much similar to that of a transistor. However, there are several imporant differences:

(*i*) There is no terminal attached to the base layer.

(*ii*) The three regions are nearly identical in size.

(*iii*) The doping concentrations are identical (unlike a bipolar transistor) to give the device symmetrical properties.

Fig. 21.17 (*ii*) shows the symbol of a diac.

Operation. When a positive or negative voltage is applied across the terminals of a diac, only a small leakage current I_{BO} will flow through the device. As the applied voltage is increased, the leakage current will continue to flow until the voltage reaches the breakover voltage V_{BO}. At this point, avalanche breakdown of the reverse-biased junction occurs and the device exhibits negative resistance *i.e.* current through the device increases with the decreasing values of applied voltage. The voltage across the device then drops to 'breakback' voltage V_W.

Fig. 21.18 shows the *V-I* characteristics of a diac. For applied positive voltage less than $+ V_{BO}$ and negative voltage less than $- V_{BO}$, a small leakage current ($\pm I_{BO}$) flows through the device. Under such conditions, the diac blocks the flow of current and effectively behaves as an open circuit. The voltages $+ V_{BO}$ and $- V_{BO}$ are the breakdown voltages and usually have a range of 30 to 50 volts.

When the positive or negative applied voltage is equal to or greater than the breakdown voltage, diac begins to conduct and the voltage drop across it becomes a few volts. Conduction then continues until the device current drops below its holding current. Note that the breakover voltage and holding current values are identical for the forward and reverse regions of operation.

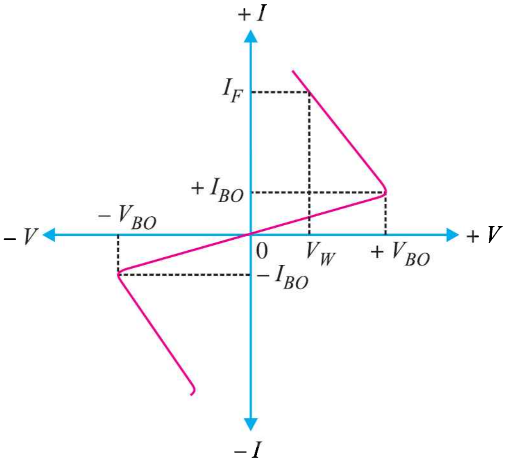


Fig. 21.18

Diacs are used primarily for triggering of triacs in adjustable phase control of a.c. mains power. Some of the circuit applications of diac are (*i*) light dimming (*ii*) heat control and (*iii*) universal motor speed control.

21.10 Applications of Diac

Although a triac may be fired into the conducting state by a simple resistive triggering circuit, more reliable and faster turn-on may be had if a switching device is used in series with the gate. One of the switching devices that can trigger a triac is the diac. This is illustrated in the following applications.

(*i*) Lamp dimmer. Fig. 21.19 shows a typical circuit that may be used for smooth control of a.c. power fed to a lamp. This permits to control the light output from the lamp. The basic control is by an *RC* variable gate voltage arrangement. The series $R_4 - C_1$ circuit across the triac is designed to limit the rate of voltage rise across the device during switch off.

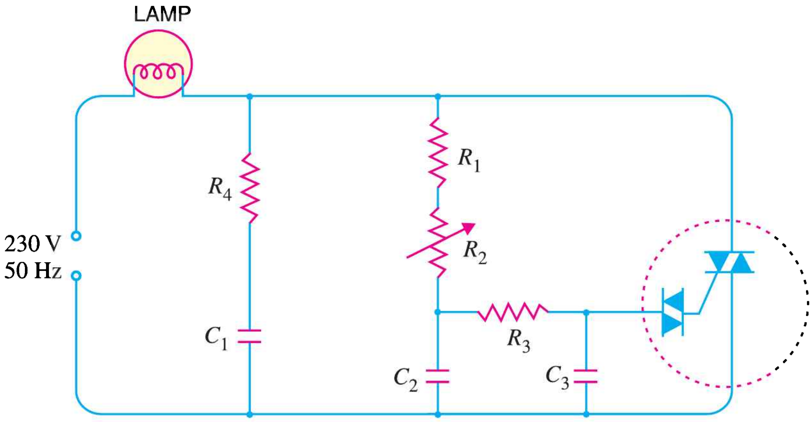


Fig. 21.19

The circuit action is as follows : As the input voltage increases positively or negatively, C_1 and C_2 charge at a rate determined primarily by R_2. When the voltage across C_3 exceeds the breakover voltage of the diac, the diac is fired into the conducting state. The capacitor C_3 discharges through the conducting diac into the gate of the triac. Hence, the triac is turned on to pass the a.c. power to the lamp. By adjusting the value of R_2, the rate of charge of capacitors and hence the point at which triac will trigger on the positive or negative half-cycle of input voltage can be controlled. Fig. 21.20 shows the waveforms of supply voltage and load voltage in the diac-triac control circuit

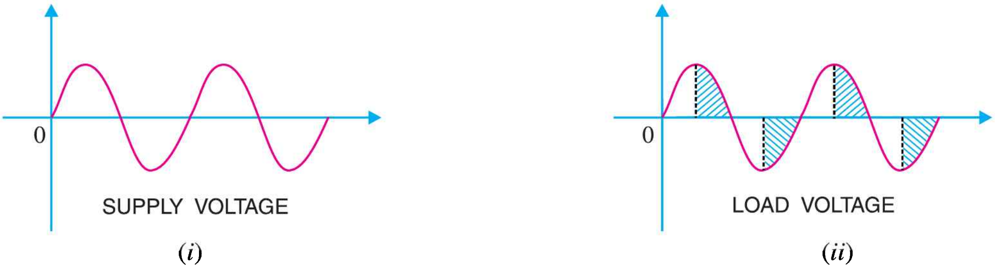


Fig. 21.20

The firing of triac can be controlled upto a maximum of 180°. In this way, we can provide a continuous control of load voltage from practically zero to full *r.m.s.* value.

***(ii)* Heat control.** Fig. 21.21 shows a typical diac-triac circuit that may be used for the smooth control of a.c. power in a heater. This is similar to the circuit shown in Fig. 21.19. The capacitor C_1 in series with choke L across the triac helps to slow-up the voltage rise across the device during switch-off. The resistor R_4 in parallel with the diac ensures smooth control at all positions of variable resistance R_2.

The circuit action is as follows : As the input voltage increases positively or negatively, C_1 and C_2 charge at a rate determined primarily by R_2. When the voltage across C_3 exceeds the breakover voltage of the diac, the diac conducts. The capacitor C_3 discharges through the conducting diac into the gate of the triac. This turns on the triac and hence a.c. power to the heater. By adjusting the value of R_2, any portion of positive and negative half-cycles of the supply voltage can be passed through the heater. This permits a smooth control of the heat output from the heater.

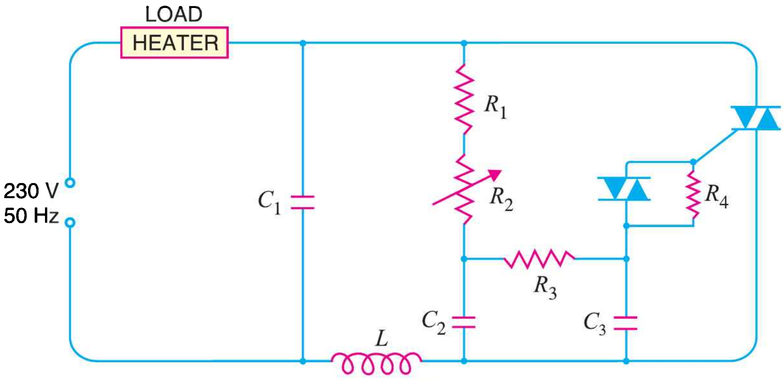


Fig. 21.21

Example 21.5. *We require a small gate triggering voltage V_{GT} (say ± 2V) to fire a triac into conduction. How will you raise the trigger level of the triac ?*

Solution. The rated values of V_{GT} for triacs are generally low. For example, the traic shown in Fig. 21.22 (*i*) has $V_{GT} = \pm 2V$. However, we can raise the triggering level of the triac by using a *diac* in the gate circuit as shown in Fig. 21.22 (*ii*). With the diac present, the triac can still be triggered by both positive and negative gate voltages. However, to fire the triac into conduction, the potential V_A at point A in Fig. 21.22 (*ii*) must overcome the V_{BO} (breakover voltage) for the diac plus V_{GT} *i.e.*

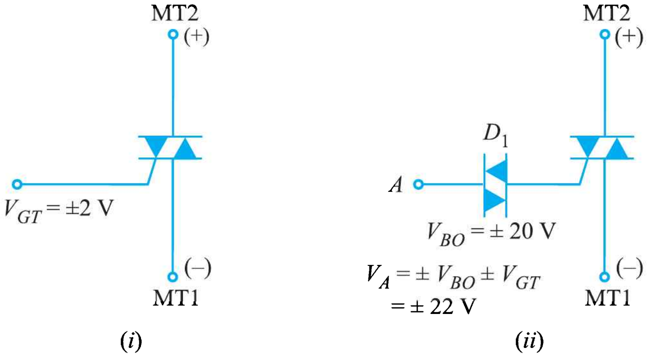


Fig. 21.22

$$\begin{aligned} V_A &= \pm V_{BO} \pm V_{GT} \\ &= \pm 20\text{V} \pm 2\text{V} = \pm 22\text{V} \end{aligned}$$

Therefore, in order to turn on the triac, the gate trigger signal V_A must be ± 22V. Note that triac triggering control is the primary function of a diac.

Example 21.6. *In Fig. 21.23, the switch is closed. A diac with breakover voltage $V_{BO} = 30V$ is connected in the circuit. If the triac has a trigger voltage of 1V and a trigger current of 10 mA, what is the capacitor voltage that triggers the triac ?*

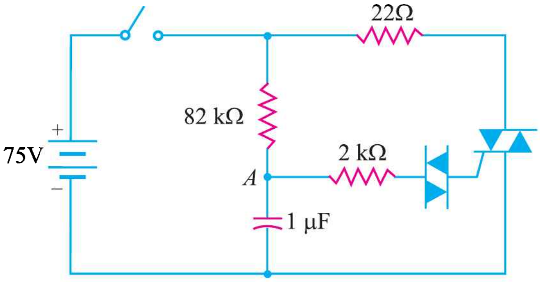


Fig. 21.23

Solution. When switch is closed, the capacitor starts charging and voltage at point *A* increases. When voltage V_A at point *A* becomes equal to V_{BO} of diac plus gate triggering voltage V_{GT} of the triac, the triac is fired into conduction.

$$\therefore \quad V_A = V_{BO} + V_{GT} = 30\text{V} + 1\text{V} = \mathbf{31V}$$

This is the minimum capacitor voltage that will trigger the triac.

21.11 Unijunction Transistor (UJT)

A unijunction transistor (abbreviated as *UJT*) is a three-terminal semiconductor switching device. This device has a unique characteristic that when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply. Due to this characteristic, the unijunction transistor can be employed in a variety of applications *e.g.*, switching, pulse generator, saw-tooth generator etc.

Construction. Fig. 21.24 (*i*) shows the basic *structure of a unijunction transistor. It consists of an *n*-type silicon bar with an electrical connection on each end. The leads to these connections are

---

* Note that structure of *UJT* is very much similar to that of the *n*-channel *JFET*. The only difference in the two components is that *p*-type (gate) material of the *JFET surrounds* the *n*-type (channel) material.

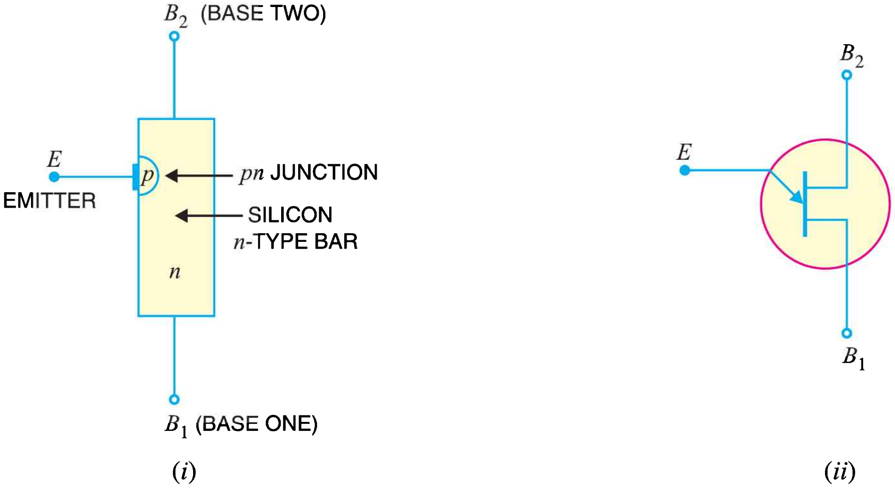


Fig. 21.24

called base leads *base-one* B_1 and *base two* B_2. Part way along the bar between the two bases, nearer to B_2 than B_1, a *pn* junction is formed between a *p*-type emitter and the bar. The lead to this junction is called the *emitter lead E*. Fig. 21.24 (*ii*) shows the symbol of unijunction transistor. Note that emitter is shown closer to B_2 than B_1. The following points are worth noting :

(*i*) Since the device has one *pn* junction and three leads, it is *commonly called a unijunction transistor (*uni* means single).

(*ii*) With only one *pn*-junction, the device is really a form of diode. Because the two base terminals are taken from one section of the diode, this device is also called *double-based diode*.

(*iii*) The emitter is heavily doped having many holes. The *n* region, however, is lightly doped. For this reason, the resistance between the base terminals is very high (5 to 10 kΩ) when emitter lead is open.

Operation. Fig. 21.25 shows the basic circuit operation of a unijunction transistor. The device has normally B_2 positive *w.r.t.* B_1.

(*i*) If voltage V_{BB} is applied between B_2 and B_1 with emitter open [See Fig. 21.25 (*i*)], a voltage gradient is established along the *n*-type bar. Since the emitter is located nearer to B_2, more than **half of V_{BB} appears between the emitter and B_1. The voltage V_1 between emitter and B_1 establishes a

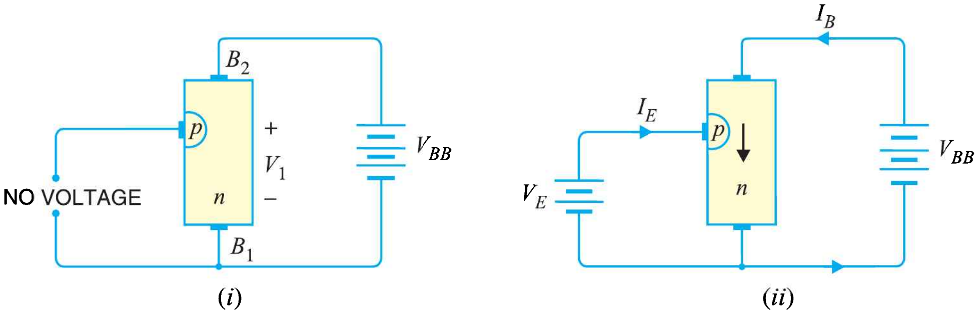


Fig. 21.25

---

* In packaged form, a *UJT* looks very much like a small signal transistor. As a *UJT* has only one *pn* junction, therefore, naming it a 'transistor' is really a misnomer.

** The *n*-type silicon bar has a high resistance. The resistance between emitter and B_1 is greater than between B_2 and emitter. It is because emitter is nearer to B_2 than B_1.

reverse bias on the *pn* junction and the emitter current is cut off. Of course, a small leakage current flows from B_2 to emitter due to minority carriers.

(*ii*) If a positive voltage is applied at the emitter [See Fig. 21.25 (*ii*)], the *pn* junction will remain reverse biased so long as the input voltage is less than V_1. If the input voltage to the emitter exceeds V_1, the *pn* junction becomes *forward biased. Under these conditions, holes are injected from *p*-type material into the *n*-type bar. These holes are repelled by positive B_2 terminal and they are attracted towards B_1 terminal of the bar. This accumulation of holes in the emitter to B_1 region results in the decrease of resistance in this section of the bar. The result is that internal voltage drop from emitter to B_1 is decreased and hence the emitter current I_E increases. As more holes are injected, a condition of saturation will eventually be reached. At this point, the emitter current is limited by emitter power supply only. The device is now in the *ON* state.

(*iii*) If a negative pulse is applied to the emitter, the *pn* junction is reverse biased and the emitter current is cut off. The device is then said to be in the *OFF* state.

21.12 Equivalent Circuit of a UJT

Fig. 21.26 shows the equivalent circuit of a *UJT*. The resistance of the silicon bar is called the inter-base resistance R_{BB}. The inter-base resistance is represented by two resistors in series *viz.*

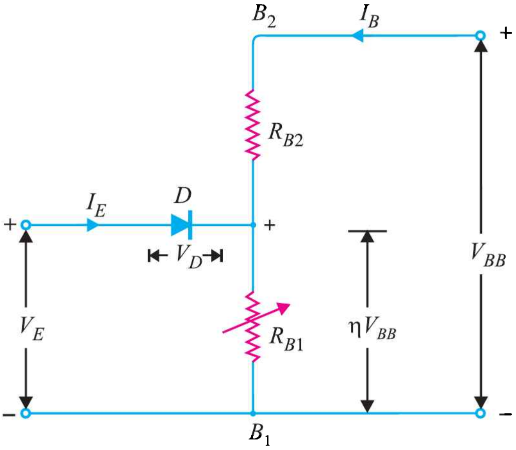


Fig. 21.26

(*a*) R_{B2} is the resistance of silicon bar between B_2 and the point at which the emitter junction lies.

(*b*) R_{B1} is the resistance of the bar between B_1 and emitter junction. This resistance is shown variable because its value depends upon the bias voltage across the *pn* junction.

The *pn* junction is represented in the emitter by a diode *D*.

The circuit action of a *UJT* can be explained more clearly from its equivalent circuit.

(*i*) With no voltage applied to the *UJT*, the inter-base resistance is given by ;

$$R_{BB} = R_{B1} + R_{B2}$$

The value of R_{BB} generally lies between 4 kΩ and 10 kΩ.

(*ii*) If a voltage V_{BB} is applied between the bases with emitter open, the voltage will divide up across R_{B1} and R_{B2}.

$$\text{Voltage across } R_{B1},\ V_1 = \frac{R_{B1}}{R_{B1} + R_{B2}} V_{BB}$$

---

* The main operational difference between the *JFET* and the *UJT* is that the *JFET* is normally operated with the gate junction reverse biased whereas the useful behaviour of the *UJT* occurs when the emitter is forward biased.

or $$V_1/V_{BB} = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

The ratio V_1/V_{BB} is called *intrinsic stand-off ratio* and is represented by Greek letter η.

$$\text{Obviously, } \eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

The value of η usually lies between 0.51 and 0.82.

$\therefore$ Voltage across $R_{B1} = \eta\, V_{BB}$

The voltage $\eta\, V_{BB}$ appearing across R_{B1} reverse biases the diode. Therefore, the emitter current is zero.

(*iii*) If now a progressively rising positive voltage is applied to the emitter, the diode will become forward biased when input voltage exceeds $\eta\, V_{BB}$ by V_D, the forward voltage drop across the silicon diode *i.e.*

$$V_P = \eta\, V_{BB} + V_D$$

where V_P = 'peak point voltage'

V_D = forward voltage drop across silicon diode ($\simeq$ 0.7 V)

When the diode D starts conducting, holes are injected from p-type material to the n-type bar. These holes are swept down towards the terminal B_1. This decreases the resistance between emitter and B_1 (indicated by variable resistance symbol for R_{B1}) and hence the internal drop from emitter to B_1. The emitter current now increases regeneratively until it is limited by the emitter power supply.

Conclusion. The above discussion leads to the conclusion that when input positive voltage to the emitter is less than peak-point voltage V_P, the *pn*-junction remains reverse biased and the emitter current is practically zero. However, when the input voltage exceeds V_P, R_{B1} falls from several thousand ohms to a small value. The diode is now forward biased and the emitter current quickly reaches to a saturation value limited by R_{B1} (about 20 Ω) and forward resistance of *pn*-junction (about 200 Ω).

21.13 Characteristics of UJT

Fig. 21.27 shows the curve between emitter voltage (V_E) and emitter current (I_E) of a *UJT* at a given voltage V_{BB} between the bases. This is known as the emitter characteristic of *UJT*. The following points may be noted from the characteristics :

(*i*) Initially, in the cut-off region, as V_E increases from zero, slight leakage current flows from terminal B_2 to the emitter. This current is due to the minority carriers in the reverse biased diode.

(*ii*) Above a certain value of V_E, forward I_E begins to flow, increasing until the peak voltage V_P and current I_P are reached at point P.

(*iii*) After the peak point P, an attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E. This is a *negative resistance* portion of the curve because with increase in I_E, V_E decreases. The device, therefore, has a negative resistance region which is stable enough to be used with a great deal of reliability in many areas *e.g.*, trigger circuits, saw-tooth generators, timing circuits .

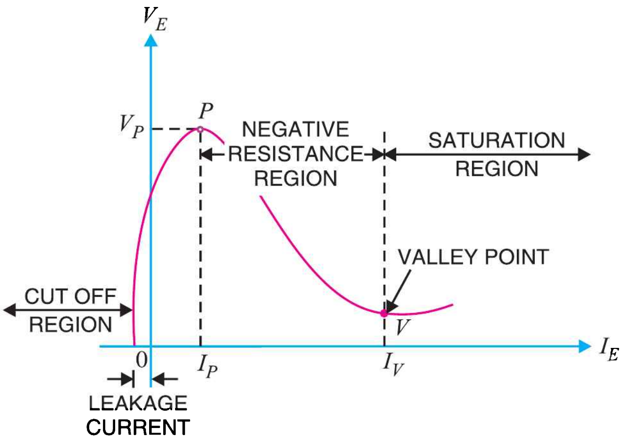


Fig. 21.27

(*iv*) The negative portion of the curve lasts until the valley point *V* is reached with valley-point voltage V_V and valley-point current I_V. After the valley point, the device is driven to saturation.

Fig. 21.28 shows the typical family of V_E/I_E characteristics of a *UJT* at different voltages between the bases. It is clear that peak-point voltage ($= \eta V_{BB} + V_D$) falls steadily with reducing V_{BB} and so does the valley point voltage V_V. The difference $V_P - V_V$ is a measure of the switching efficiency of *UJT* and can be seen to fall off as V_{BB} decreases. For a general purpose *UJT*, the peak - point current is of the order of 1 μA at $V_{BB} = 20$ V with a valley-point voltage of about 2.5 V at 6 mA.

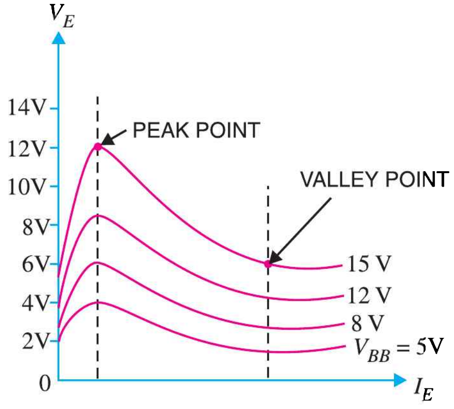


Fig. 21.28

Example 21.7. *The intrinsic stand-off ratio for a UJT is determined to be 0.6. If the inter-base resistance is 10 kΩ, what are the values of R_{B1} and R_{B2} ?*

Solution. $R_{BB} = 10\ \text{k}\Omega,\quad \eta = 0.6$

Now $R_{BB} = R_{B1} + R_{B2}$

or $10 = R_{B1} + R_{B2}$

Also
$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

or
$$0.6 = \frac{R_{B1}}{10} \qquad (\because R_{B1} + R_{B2} = 10\ \text{k}\Omega)$$

$\therefore$ $R_{B1} = 10 \times 0.6 = \mathbf{6\ k\Omega}$

and $R_{B2} = 10 - 6 = \mathbf{4\ k\Omega}$

Example 21.8. *A unijunction transistor has 10 V between the bases. If the intrinsic stand off ratio is 0.65, find the value of stand off voltage. What will be the peak-point voltage if the forward voltage drop in the pn junction is 0.7 V ?*

Solution. $V_{BB} = 10\text{ V};\quad \eta = 0.65;\quad V_D = 0.7\text{ V}$

Stand off voltage $= \eta V_{BB} = 0.65 \times 10 = \mathbf{6.5\ V}$

Peak-point voltage, $V_P = \eta V_{BB} + V_D = 6.5 + 0.7 = \mathbf{7.2\ V}$

Example 21.9. *Determine the maximum and minimum peak-point voltage for a UJT with V_{BB} = 25 V. Given that UJT has a range of η = 0.74 to 0.86.*

Solution.

$$V_{BB} = 25\text{ V};\ \eta_{max} = 0.86\ ;\ \eta_{min} = 0.74$$

$$\therefore \quad V_{P(max)} = \eta_{max} V_{BB} + V_D = (0.86)(25\text{V}) + 0.7\text{ V} = \mathbf{22.2\ V}$$

$$V_{P(min)} = \eta_{min} V_{BB} + V_D = (0.74)(25\text{ V}) + 0.7\text{ V} = \mathbf{19.2\ V}$$

Example 21.10. *Fig. 21.29 (i) shows the UJT circuit. The parameters of UJT are η = 0.65 and R_{BB} = 7 kΩ. Find (i) R_{B1} and R_{B2} (ii) $V_{B1\,B2}$ and V_P.*

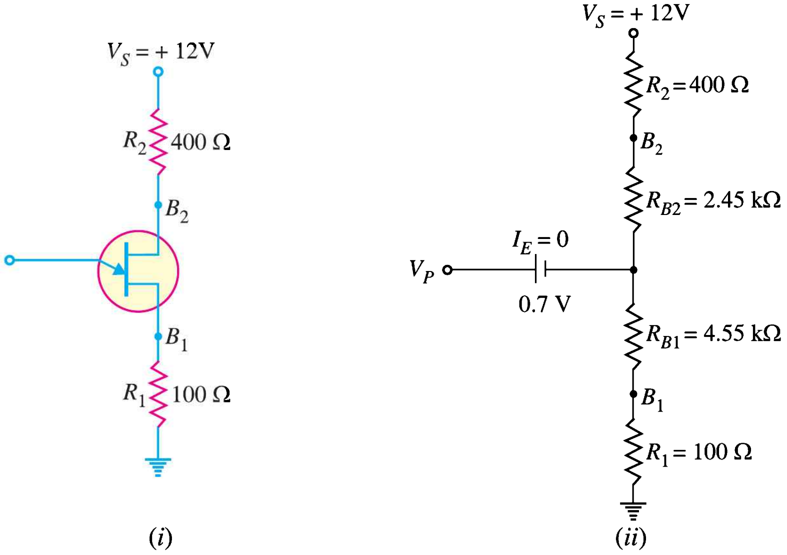


Fig. 21.29

Solution.

$\eta = 0.65\ ;\ V_S = 12\ \text{V}\ ;\ R_{BB} = 7\ \text{k}\Omega$

(*i*)
$$\eta = \frac{R_{B1}}{R_{BB}} \qquad \therefore \quad R_{B1} = \eta\, R_{BB} = 0.65 \times 7\ \text{k}\Omega = \mathbf{4.55\ k\Omega}$$

$$\text{Also } R_{B2} = R_{BB} - R_{B1} = 7\ \text{k}\Omega - 4.55\ \text{k}\Omega = \mathbf{2.45\ k\Omega}$$

(*ii*) Fig. 21.29 (*ii*) shows the *UJT* circuit model. Because *UJT* is *OFF*, $I_E = 0$. We can find V_{B2B1} by the voltage-divider rule.

$$V_{B2\,B1} = \frac{V_S}{R_1 + R_2 + R_{BB}} \times R_{BB}$$

$$= \frac{12\text{V}}{(100 + 400 + 7000)\Omega} \times 7000\Omega = \mathbf{11.2V}$$

The voltage V_P required to turn on the *UJT* is

$$V_P = \eta V_{B2B1} + V_D = 0.65 \times 11.2\ \text{V} + 0.7\ \text{V} = \mathbf{7.98V}$$

21.14 Advantages of UJT

The *UJT* was introduced in 1948 but did not become commercially available until 1952. Since then, the device has achieved great popularity due to the following reasons :

(*i*) It is a low cost device.

(*ii*) It has excellent characteristics.

(*iii*) It is a low-power absorbing device under normal operating conditions.

Due to above reasons, this device is being used in a variety of applications. A few include oscillators, trigger circuits, saw-tooth generators, bistable network etc.

21.15 Applications of UJT

Unijunction transistors are used extensively in oscillator, pulse and voltage sensing circuits. Some of the important applications of *UJT* are discussed below :

(*i*) UJT relaxation oscillator. Fig. 21.30 shows *UJT* relaxation oscillator where the discharging of a capacitor through *UJT* can develop a saw-tooth output as shown.

When battery V_{BB} is turned on, the capacitor C charges through resistor R_1. During the charging period, the voltage across the capacitor rises in an exponential manner until it reaches the peak - point voltage. At this instant of time, the *UJT* switches to its low resistance conducting mode and the capacitor is discharged between E and B_1. As the capacitor voltage flys back to zero, the emitter ceases to conduct and the *UJT* is switched off. The next cycle then begins, allowing the capacitor C to charge again. The frequency of the output saw-tooth wave can be varied by changing the value of R_1 since this controls the time constant R_1C of the capacitor charging circuit.

The time period and hence the frequency of the saw-tooth wave can be calculated as follows. Assuming that the capacitor is initially uncharged, the voltage V_C across the capacitor prior to breakdown is given by :

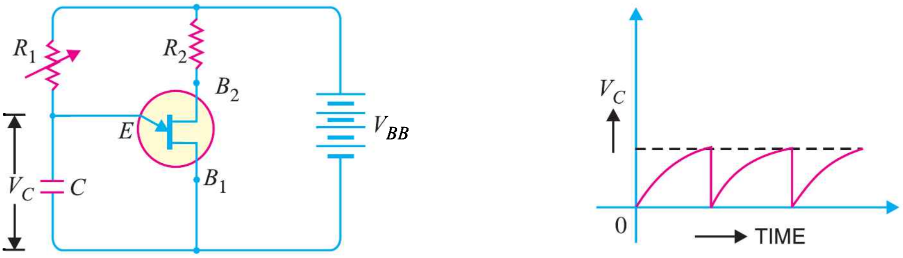


Fig. 21.30

$$V_C = V_{BB}(1 - e^{-t/R_1C})$$

where R_1C = charging time constant of resistor-capacitor circuit

t = time from the commencement of waveform.

The discharge of the capacitor occurs when V_C is equal to the *peak-point voltage $\eta\, V_{BB}$ *i.e.*

$$\eta\, V_{BB} = V_{BB}(1 - e^{-t/R_1C})$$

or $$\eta = 1 - e^{-t/R_1C}$$

or $$e^{-t/R_1C} = 1 - \eta$$

or $$t = R_1\, C \log_e \frac{1}{1-\eta}$$

$\therefore$ $$\text{Time period, } t = 2.3\, R_1\, C \log_{10} \frac{1}{1-\eta}$$

$$\text{Frequency of saw-tooth wave, } f = \frac{1}{t \text{ in seconds}} \text{ Hz}$$

(*ii*) Overvoltage detector. Fig. 21.31 shows a simple d.c. over-voltage indicator. A warning pilot - lamp L is connected between the emitter and B_1 circuit. So long as the input voltage is less than the peak-point voltage (V_P) of the *UJT*, the device remains switched off. However, when the input voltage exceeds V_P, the *UJT* is switched on and the capacitor discharges through the low resistance path between terminals E and B_1. The current flowing in the pilot lamp L lights it, thereby indicating the overvoltage in the circuit.

---

* Actually, peak point voltage, $V_P = \eta V_{BB} + V_D$. As V_D, the forward voltage drop across emitter diode is generally small, it can be neglected with reasonable accuracy.

$\therefore$ $$V_P = \eta\, V_{BB}$$

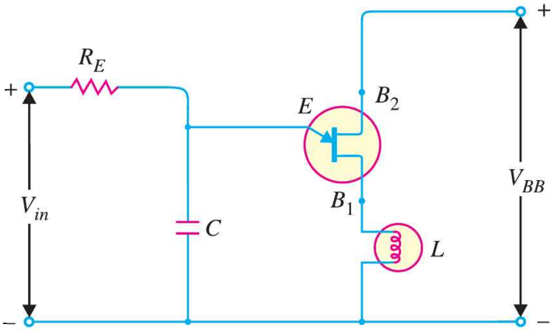


Fig. 21.31

Example 21.11. *The circuit shown in Fig. 21.32 uses variable resistor R_E to change the frequency of pulses delivered at V_{out}. The variable resistor is initially set at 5 kΩ and is then adjusted to 10kΩ. Determine the frequency of the voltage spikes produced for (i) 5 kΩ setting and (ii) 10 kΩ setting.*

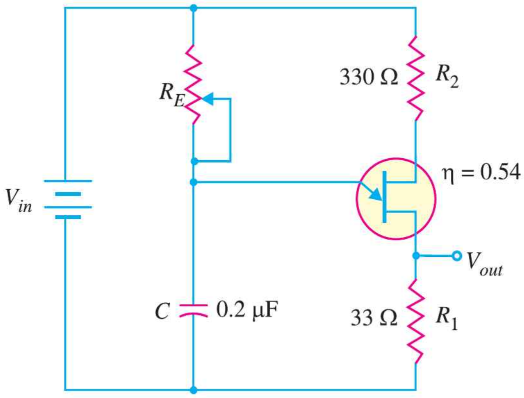


Fig. 21.32

Solution.

(*i*) Time period, $t = R_E C \log_e \frac{1}{1-\eta}$

Here $R_E = 5\text{ k}\Omega = 5 \times 10^3\Omega$; $C = 0.2\ \mu\text{F} = 0.2 \times 10^{-6}\text{ F}$; $\eta = 0.54$

$\therefore$ $t = (5 \times 10^3)(0.2 \times 10^{-6}) \log_e \frac{1}{1-0.54}$

$= 0.78 \times 10^{-3}\text{s} = 0.78\text{ ms}$

$\therefore$ Frequency, $f = 1/t = 1/0.78 \times 10^{-3}\text{s} = \mathbf{1282\ Hz}$

(*ii*) $t = (10 \times 10^3)(0.2 \times 10^{-6}) \log_e \frac{1}{1-0.54}$

$= 1.55 \times 10^{-3}\text{s} = 1.55\text{ ms}$

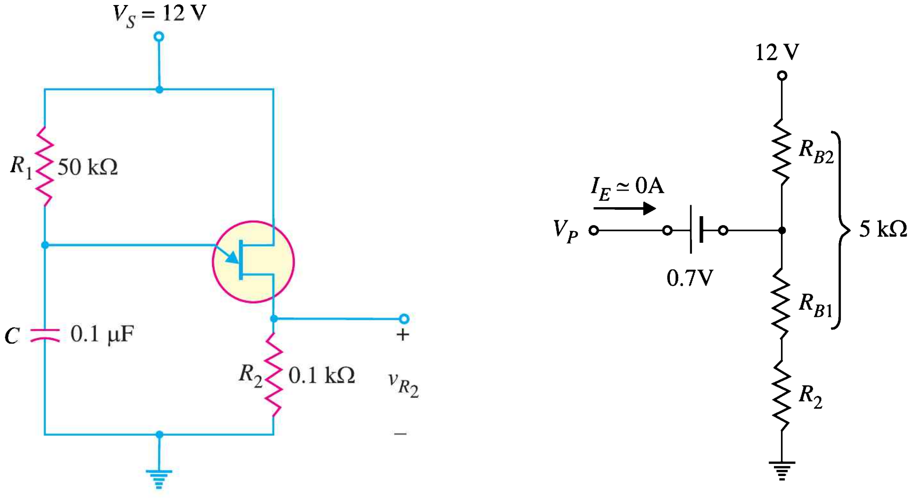
$\therefore$ Frequency, $f = 1/t = 1/1.55 \times 10^{-3}\text{s} = \mathbf{645\ Hz}$

Example 21.12. *Fig. 21.33 (i) shows the relaxation oscillator. The parameters of the UJT are R_{BB} = 5 kΩ and η = 0.6.*

(*i*) *Determine R_{B1} and R_{B2} at $I_E = 0$.*

(*ii*) *Calculate the voltage V_P necessary to turn on the UJT.*

(*iii*) *Determine the frequency of oscillations.*



(*i*) (*ii*)

Fig. 21.33

Solution.

$V_S = 12$ V ; $R_{BB} = 5$ kΩ ; $\eta = 0.6$

(*i*) $$\eta = \frac{R_{B1}}{R_{BB}} \quad \text{or} \quad R_{B1} = \eta\, R_{BB} = 0.6 \times 5\text{ k}\Omega = \mathbf{3\ k\Omega}$$

Also $$R_{B2} = R_{BB} - R_{B1} = 5\text{ k}\Omega - 3\text{ k}\Omega = \mathbf{2\ k\Omega}$$

(*ii*) The voltage V_P required to turn on the *UJT* can be found from the *UJT* circuit model shown is Fig. 21.33 (*ii*). Referring to Fig. 21.33 (*ii*), we have,

$$V_P = V_D + \text{Voltage drop across } (R_{B1} + R_2)$$

$$= V_D + \frac{V_S}{R_{BB} + R_2} \times (R_{B1} + R_2)$$

$$= 0.7\text{V} + \frac{12\text{V}}{5\text{ k}\Omega + 0.1\text{ k}\Omega} \times (3 + 0.1)\text{ k}\Omega$$

$$= 0.7\text{V} + 7.294\text{ V} \simeq \mathbf{8V}$$

(*iii*) Time period, $$t = R_1 C \log_e \frac{1}{1-\eta}$$

Here $R_1 = 50\text{ k}\Omega = 50 \times 10^3\ \Omega$; $C = 0.1\ \mu\text{F} = 0.1 \times 10^{-6}\text{F}$; $\eta = 0.6$

$$\therefore \quad t = (50 \times 10^3)(0.1 \times 10^{-6}) \log_e \frac{1}{1-0.6}$$

$$= 4.58 \times 10^{-3}\text{s} = 4.58\text{ ms}$$

$$\therefore \quad \text{Frequency, } f = \frac{1}{t} = \frac{1}{4.58 \times 10^{-3} s} = \mathbf{218\ Hz}$$

MULTIPLE-CHOICE QUESTIONS

1. A triac has three terminals *viz.* ....

(*i*) drain, source, gate
(*ii*) two main terminal and a gate terminal
(*iii*) cathode, anode, gate
(*iv*) none of the above

2. A triac is equivalent to two *SCRs* ....

(*i*) in parallel
(*ii*) in series
(*iii*) in inverse-parallel
(*iv*) none of the above

3. A triac is a .... switch.

(*i*) bidirectional
(*ii*) undirectional
(*iii*) mechanical
(*iv*) none of the above

4. The *V-I* characteristics for a triac in the first and third quadrants are essentially identical to those of .... in the first quadrant.

(*i*) transistor (*ii*) *SCR*
(*iii*) *UJT* (*iv*) none of the above

5. A triac can pass a portion of .... half-cycle through the load.

(*i*) only positive
(*ii*) only negative
(*iii*) both positive and negative
(*iv*) none of the above

6. A diac has .... terminals.

(*i*) two (*ii*) three
(*iii*) four (*iv*) none of the above

7. A triac has .... semiconductor layers.

(*i*) two (*ii*) three
(*iii*) four (*iv*) five

8. A diac has .... *pn* junctions.

(*i*) four (*ii*) two
(*iii*) three (*iv*) none of the above

9. The device that does not have the gate terminal is ....

(*i*) triac (*ii*) *FET*
(*iii*) *SCR* (*iv*) diac

10. A diac has .... semiconductor layers.

(*i*) three (*ii*) two
(*iii*) four (*iv*) none of the above

11. A *UJT* has ....

(*i*) two *pn* junctions
(*ii*) one *pn* junction
(*iii*) three *pn* junctions
(*iv*) none of the above

12. The normal way to turn on a diac is by ....

(*i*) gate current
(*ii*) gate voltage
(*iii*) breakover voltage
(*iv*) none of the above

13. A diac is .... switch.

(*i*) an a.c. (*ii*) a d.c.
(*iii*) a mechanical (*iv*) none of the above

14. In a *UJT*, the *p*-type emitter is .... doped.

(*i*) lightly (*ii*) heavily
(*iii*) moderately (*iv*) none of the above

15. Power electronics essentially deals with control of a.c. power at ....

(*i*) frequencies above 20 kHz
(*ii*) frequencies above 1000 kHz
(*iii*) frequencies less than 10 Hz
(*iv*) 50 Hz frequency

16. When the emitter terminal of a *UJT* is open, the resistance between the base terminals is generally ....

(*i*) high (*ii*) low
(*iii*) extremely low (*iv*) none of the above

17. When a *UJT* is turned *ON*, the resistance between emitter terminal and lower base terminal ....

(*i*) remains the same
(*ii*) is decreased
(*iii*) is increased
(*iv*) none of the above

18. To turn on *UJT*, the forward bias on the emitter diode should be .... the peak point voltage.

(*i*) less than (*ii*) equal to
(*iii*) more than (*iv*) none of the above

19. A *UJT* is sometimes called .... diode.

(*i*) low resistance (*ii*) high resistance
(*iii*) single-base (*iv*) double-based

20. When the temperature increases, the inter-base resistance (R_{BB}) of a *UJT* ....
(*i*) increases
(*ii*) decreases
(*iii*) remains the same
(*iv*) none of the above

21. The intrinsic stand off ratio (η) of a *UJT* is given by ....
(*i*) $R_{B1} + R_{B2}$ (*ii*) $\dfrac{R_{B1} + R_{B2}}{R_{B1}}$
(*iii*) $\dfrac{R_{B1}}{R_{B1} + R_{B2}}$ (*iv*) $\dfrac{R_{B1} + R_{B2}}{R_{B2}}$

22. When the temperature increases, the intrinsic stand off ratio ....
(*i*) increases
(*ii*) decreases
(*iii*) essentially remains the same
(*iv*) none of the above

23. Between the peak point and the valley point of *UJT* emitter characteristics we have .... region.
(*i*) saturation (*ii*) negative resistance
(*iii*) cut-off (*iv*) none of the above

24. A diac is turned on by ....
(*i*) breakover voltage
(*ii*) gate voltage
(*iii*) gate current
(*iv*) none of the above

25. The device that exhibits negative resistance region is ....
(*i*) diac (*ii*) triac
(*iii*) transistor (*iv*) *UJT*

26. The *UJT* may be used as ....
(*i*) an amplifier
(*ii*) a sawtooth generator
(*iii*) a rectifier
(*iv*) none of the above

27. A diac is simply ....
(*i*) a single junction device
(*ii*) a three junction device
(*iii*) a triac without gate terminal
(*iv*) none of the above

28. After peak point, the *UJT* operates in the .... region.
(*i*) cut-off
(*ii*) saturation
(*iii*) negative resistance
(*iv*) none of the above

29. Which of the following is *not* a characteristic of *UJT* ?
(*i*) intrinsic stand off ratio
(*ii*) negative resistance
(*iii*) peak-point voltage
(*iv*) bilateral conduction

30. The triac is ....
(*i*) like a bidirectional *SCR*
(*ii*) a four-terminal device
(*iii*) not a thyristor
(*iv*) answers (*i*) and (*ii*)

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iii*)	**3.** (*i*)	**4.** (*ii*)	**5.** (*iii*)
6. (*i*)	**7.** (*iii*)	**8.** (*ii*)	**9.** (*iv*)	**10.** (*i*)
11. (*ii*)	**12.** (*iii*)	**13.** (*i*)	**14.** (*ii*)	**15.** (*iv*)
16. (*i*)	**17.** (*ii*)	**18.** (*iii*)	**19.** (*iv*)	**20.** (*i*)
21. (*iii*)	**22.** (*iii*)	**23.** (*ii*)	**24.** (*i*)	**25.** (*iv*)
26. (*ii*)	**27.** (*iii*)	**28.** (*iii*)	**29.** (*iv*)	**30.** (*i*)

Chapter Review Topics

1. Discuss the importance of power electronics.
2. Explain the construction and working of a triac.

3. Sketch the *V-I* characteristics of a triac. What do you infer from them ?
4. Describe some important applications of a triac.
5. Explain the construction and working of a diac.
6. Discuss the applications of a diac.
7. Explain the construction and working of a *UJT*.
8. Draw the equivalent circuit of a *UJT* and discuss its working from the circuit.
9. Describe some important applications of a *UJT*.
10. Write short notes on the following :

    (*i*) *UJT* relaxation oscillator (*ii*) Triac as an a.c. switch (*iii*) Diac as a triggering device

Problems

1. The intrinsic stand off ratio for a *UJT* is determined to be 0.6. If the inter-base resistance is 5 kΩ, what are the values of R_{B1} and R_{B2} ? **[R_{B1} = 3 kΩ ; R_{B2} = 2 kΩ]**
2. A unijunction transistor has 18 V between the bases. If the intrinsic stand off ratio is 0.8, find the value of stand off voltage. What will be the peak point voltage if the forward voltage drop in the *pn* junction is 0.7 V ? **[14.4 V ; 15.1 V]**
3. In a unijunction transistor, $\eta = 0.8$, $V_P = 10.3$ V and $R_{B2} = 5$ kΩ. Determine R_{B1} and V_{BB}. **[20 kΩ ; 12 V]**
4. The instrinsic stand-off ratio for a *UJT* is 0.75 and $V_{BB} = 12$ V. If the forward drop in the *pn*-junction is 0.7 V, find the peak point voltage. **[9.7 V]**
5. A unijunction transistor has 12 V between the bases. If the intrinsic stand off ratio is 2/3, find the value of stand-off voltage. What will be the peak point voltage if the forward drop in the *pn* junction is 0.7 V? **[8 V ; 8.7 V]**
6. In Fig. 21.34, the switch is closed. If the triac has fired, what is the current through the 22Ω ? **[3.41 A]**

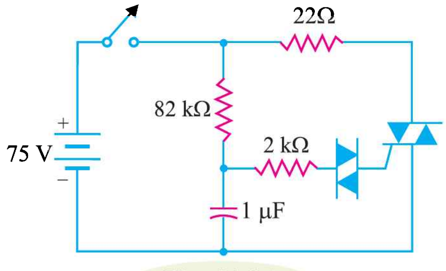


Fig. 21.34

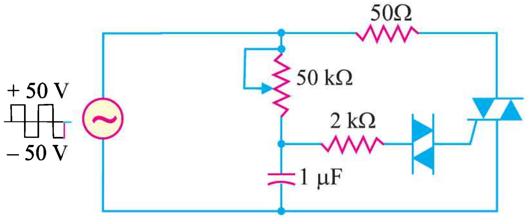


Fig. 21.35

7. If the triac of Fig. 21.35 has 1 V across it when it is conducting, what is the maximum current through the 50Ω ? **[0.98 A]**

Discussion Questions

1. What are the advantages of a triac over an *SCR* ?
2. Why is diac preferred to trigger a triac ?
3. Why is power electronics so important ?
4. Why is diac used to trigger a triac ?
5. Is the name *UJT* appropriate?
6. What is the most common application of diac?
7. What are the symptoms of a *shorted* diac or triac?
8. What are the symptoms of an *open* diac or triac?
9. For what are *UJTs* used?

22

Electronic Instruments

22.1 Electronic Instruments
22.3 Applications of Multimeter
22.5 Merits and Demerits of Multimeter
22.7 Electronic Voltmeters
22.9 Applications of VTVM
22.11 Transistor Voltmeter Circuit
22.13 Cathode Ray Oscilloscope
22.15 Deflection Sensitivity of CRT
22.17 Display of Signal Waveform on CRO
22.19 Various Controls of CRO

INTRODUCTION

In recent years, the rapid strides and remarkable advances in the field of electronics is partly due to modern electronic instruments. By using these instruments, we can gather much information regarding the performance of specific electronic circuit. Electronic instruments are also used for trouble shooting since they permit readings to be taken so that circuit faults can be located by ascertaining which component values do not coincide with the pre-established values indicated by the manufacturer. In fact, electronic instruments are playing a vital role in the fast developing field of electronics. It is with this view that they have been treated in a separate chapter.

22.1 Electronic Instruments

Those instruments which employ electronic devices for measuring various electrical quantities (*e.g. voltage, current, resistance etc.*) *are known as* **electronic instruments**.

There are a large number of electronic instruments available for completion of various tests and measurements. However, in this chapter, we shall confine our attention to the following electronic instruments :

(*i*) Multimeter

(*ii*) Electronic Voltmeters

(*iii*) Cathode ray oscilloscope

The knowledge of the manner in which each instrument is used plus an understanding of the applications and limitations of each instrument will enable the reader to utilise such instruments successfully.

22.2 Multimeter

A *multimeter* is an electronic instrument which can measure resistances, currents and voltages. It is an indispensable instrument and can be used for measuring d.c. as well as a.c. voltages and currents. Multimeter is the most inexpensive equipment and can make various electrical measurements with reasonable accuracy.

Construction. A multimeter consists of an ordinary pivoted type of moving coil galvanometer. This galvanometer consists of a coil pivoted on jeweled bearings between the poles of a permanent magnet. The indicating needle is fastened to the coil. When electric current is passed through the coil, mechanical force acts and the pointer moves over the scale.

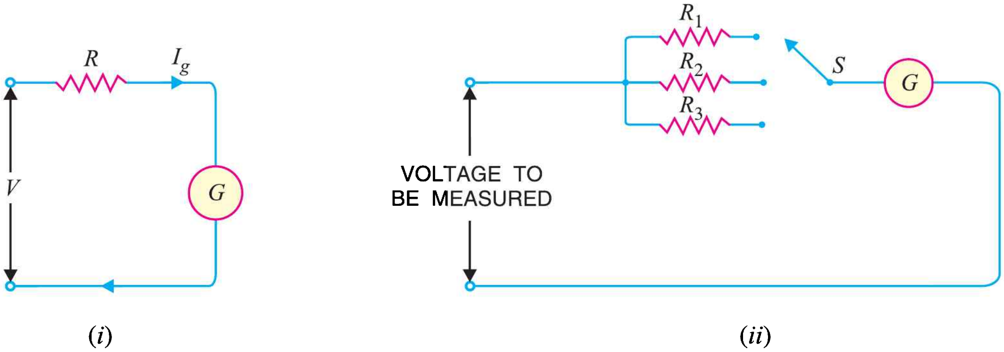
Functions. A multimeter can measure voltages, currents and resistances. To achieve this objective, proper circuits are incorporated with the galvanometer. The galvanometer in a multimeter is always of *left zero type i.e.* normally its needle rests in extreme left position as compared to centre zero position of ordinary galvanometers.

(*i*) **Multimeter as voltmeter.** When a high resistance is connected in series with a galvanometer, it becomes a voltmeter. Fig. 22.1 (*i*) shows a high resistance R connected in series with the galvanometer of resistance G. If I_g is the *full scale deflection current*, then the galvanometer becomes a voltmeter of range 0 – V volts. The required value of series resistance R is given by :

$$V = I_g R + I_g G$$

or $$V/I_g = R + G$$

or $$R = V/I_g - G$$



(*i*) (*ii*)

Fig. 22.1

For maximum accuracy, a multimeter is always provided with a number of voltage ranges. This is achieved by providing a number of high resistances in the multimeter as shown in Fig. 22.1 (*ii*). Each resistance corresponds to one voltage range. With the help of selector switch S, we can put any resistance (R_1, R_2 and R_3) in series with the galvanometer. When d.c. voltages are to be measured, the multimeter switch is turned on to d.c. position. This puts the circuit shown in Fig. 22.1 (*ii*) in action. By throwing the range selector switch S to a suitable position, the given d.c. voltage can be measured.

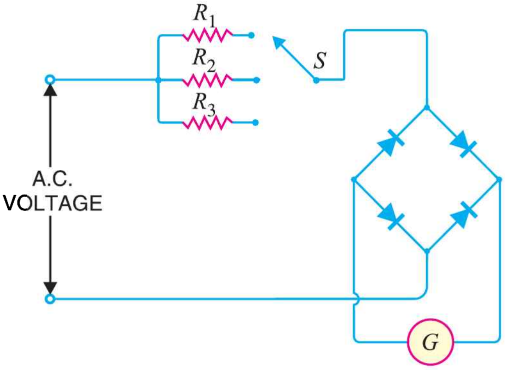


Fig. 22.2

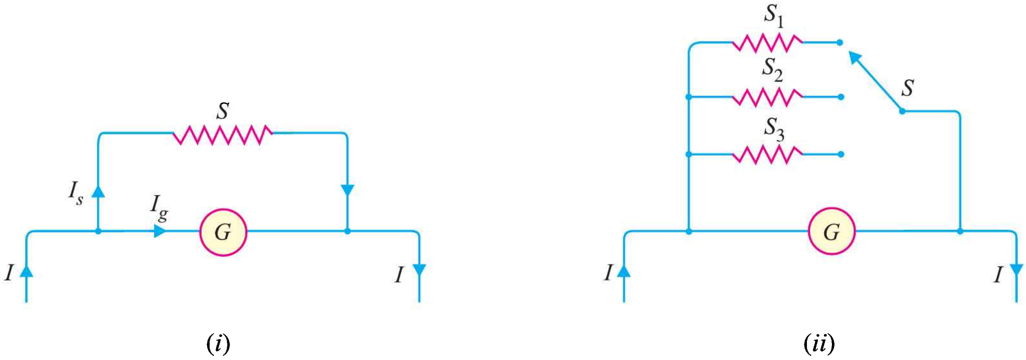
The multimeter can also measure a.c. voltages. To permit it to perform this function, a full-wave rectifier is used as shown in Fig. 22.2. The rectifier converts a.c. into d.c. for application to the galvanometer. The desired a.c. voltage range can be selected by the switch S. When a.c. voltage is to be measured, the multimeter switch is thrown to a.c. position. This puts the circuit shown in Fig. 22.2 in action. By throwing the range selector switch S to a suitable position, the given a.c. voltage can be measured. It may be mentioned here that a.c. voltage scale is calibrated in r.m.s. values. Therefore, the meter will give the r.m.s. value of the a.c. voltage under measurement.

(*ii*) Multimeter as ammeter. When low resistance is connected in parallel with a galvanometer, it becomes an ammeter. Fig. 22.3 (*i*) shows a low resistance S (generally called *shunt*) connected in parallel with the galvanometer of resistance G. If I_g is the full scale deflection current, then the galvanometer becomes an ammeter of range 0 – I amperes. The required value of shunt resistance S is given by :

$$I_s S = I_g G$$

or $$I_s/I_g = G/S \quad \text{or} \quad \frac{I_s}{I_g} + 1 = \frac{G}{S} + 1$$

or $$\frac{I_s + I_g}{I_g} = \frac{G+S}{S} \quad \text{or} \quad \frac{I}{I_g} = \frac{G+S}{S}$$



(*i*) (*ii*)

Fig. 22.3

In practice, a number of low resistances are connected in parallel with the galvanometer to provide a number of current ranges as shown in Fig. 22.3 (*ii*). With the help of range selector switch S, any shunt can be put in parallel with the galvanometer. When d.c. current is to be measured, the multimeter switch is turned on to d.c. position. This puts the circuit shown in Fig. 22.3 (*ii*) in action. By throwing the range selector switch S to a suitable position, the desired d.c. current can be measured.

The multimeter can also be used to measure alternating current. For this purpose, a full - wave rectifier is used as shown in Fig. 22.4. The rectifier converts a.c. into d.c. for application to the galvanometer. The desired current range can be selected by switch S. By throwing the range selector switch S to a suitable position, the given a.c. current can be measured. Again, the a.c. current scale is calibrated in r.m.s. values so that the instrument will give r.m.s. value of alternating current under measurement.

(*iii*) Multimeter as ohmmeter. Fig. 22.5 (*i*) shows the circuit of ohmmeter. The multimeter employs the internal battery. A fixed resistance R and a variable resistance r are connected in series with the battery and galvanometer. The fixed resistance R limits the current within the range desired and variable resistance r is for zero-adjustment reading. The resistance to be measured is connected between terminals A and B. The current flowing through the circuit will depend upon the value of resistor connected across the terminals. The ohmmeter scale is calibrated in terms of ohms. The ohmmeter is generally made multirange instrument by using different values of R as shown in Fig. 22.5 (*ii*).

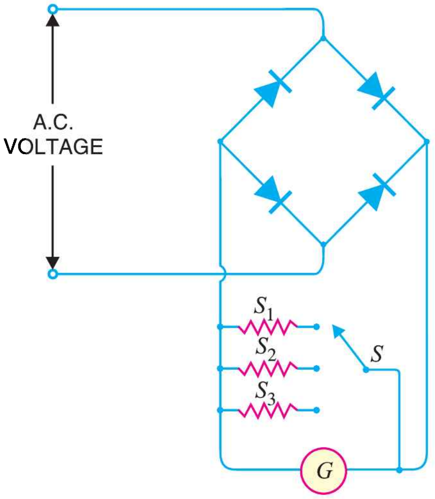
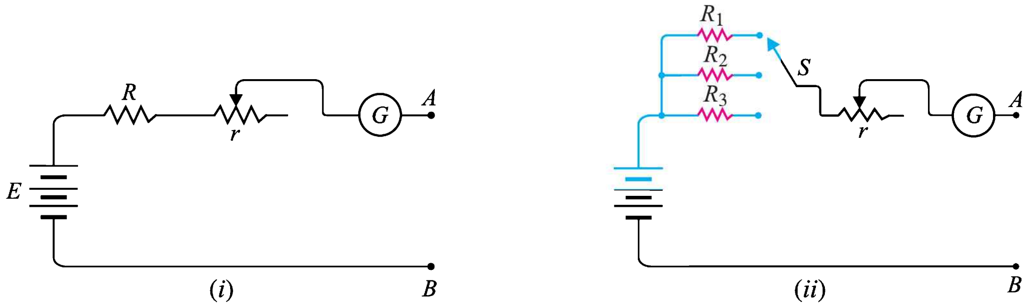


Fig. 22.4

To use ohmmeter, terminals A and B are shorted and resistance r is adjusted to give full scale deflection of the galvanometer. Under this condition, the resistance under measurement is zero. Because the needle deflects to full scale, the ohmmeter scale must then indicate *full scale deflection as zero ohm*. Then probes A and B are connected across the resistance to be measured. If the resistance to be measured is high, lower current flows through the circuit and the meter will indicate lower reading. It may be mentioned here that each time the ohmmeter is used, it is first shorted across AB and r is adjusted to zero the meter. This calibrates the meter and accommodates any decrease in the terminal voltage of the battery with age.



(*i*) (*ii*)

Fig. 22.5

Typical multimeter circuit. Fig 22.6 shows a typical multimeter circuit incorporating three voltage and current ranges.

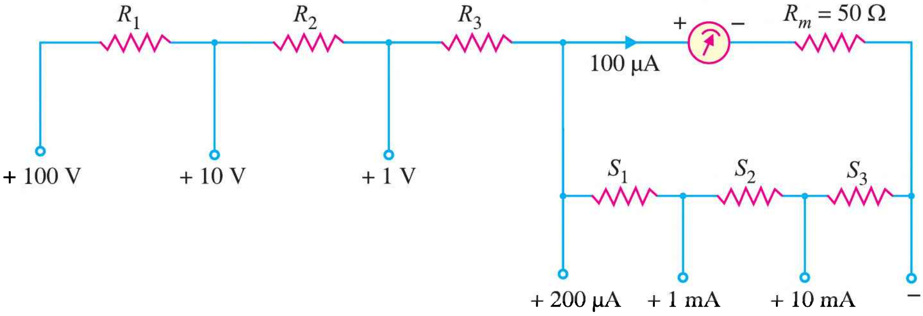


Fig. 22.6

Here the full-scale deflection (*f.s.d.*) current of the meter is 100 μA and meter resistance is 50 Ω. The design of this multimeter means finding the values of various resistances.

22.3 Applications of Multimeter

A multimeter is an extremely important electronic instrument and is extensively used for carrying out various tests and measurements in electronic circuits. It is used :

(*i*) For checking the circuit continuity. When the multimeter is employed as continuity-checking device, the ohmmeter scale is utilised and the equipment to be checked is shut off or disconnected from the power mains.

(*ii*) For measuring d.c. current flowing through the cathode, plate, screen and other vacuum tube circuits.

(*iii*) For measuring d.c. voltages across various resistors in electronic circuits.

Checking the circuit continuity by multimeter

(*iv*) For measuring a.c. voltages across power supply transformers.

(*v*) For ascertaining whether or not open or short circuit exists in the circuit under study.

22.4 Sensitivity of Multimeter

The resistance offered per volt of full scale deflection by the multimeter is known as **multimeter sensitivity.**

Multimeter sensitivity indicates the internal resistance of the multimeter. For example, if the total resistance of the meter is 5000 ohms and the meter is to read 5 volts full scale, then internal resistance of the meter is 1000 Ω per volt *i.e.* meter sensitivity is 1000 Ω per volt. Conversely, if the meter sensitivity is 400 Ω per volt which reads from 0 to 100 V, then meter resistance is 40,000 ohms. If the meter is to read V volts and I_g is the full scale deflection current, then,

$$\text{Meter resistance} = \frac{V}{I_g}$$

$$\text{Meter sensitivity} = \text{Resistance per volt full scale deflection}$$

$$= \frac{V}{I_g}\Big/V = \frac{1}{I_g}$$

Sensitivity is the most important characteristic of a multimeter. If the sensitivity of a multimeter is high, it means that it has high internal resistance. When such a meter is connected in the circuit to read voltage, it will draw a very small current. Consequently, there will be no change in the circuit current due to the introduction of the meter. Hence, it will measure the voltage correctly. On the other hand, if the sensitivity of multimeter is low, it would cause serious error in voltage measurement. The sensitivity of multimeters available in the market range from 5 kΩ per volt to 20 kΩ per volt.

22.5 Merits and Demerits of Multimeter

Although multimeter is widely used for manufacturing and servicing of electronics equipment, it has its own merits and demerits.

Merits

(*i*) It is a single meter that performs several measuring functions.

(*ii*) It has a small size and is easily portable.

(*iii*) It can make measurements with reasonable accuracy.

Demerits

(*i*) It is a costly instrument. The cost of a multimeter having sensitivity of 20 kΩ per volt is about Rs. 1000.

(*ii*) It cannot make precise and accurate measurements due to the loading effect.

(*iii*) Technical skill is required to handle it.

22.6 Meter Protection

It is important to provide protection for the meter in the event of an accidental overload. This is achieved by connecting a diode in parallel with the voltmeter as shown in Fig. 22.7.

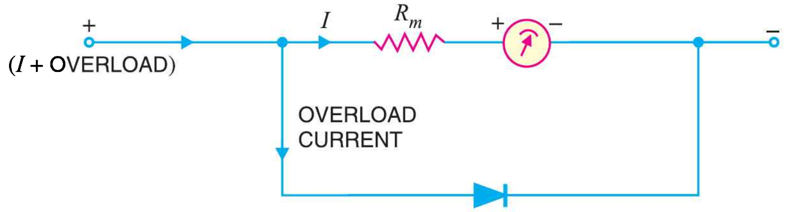


Fig. 22.7

Let us see how diode across the meter enables it to withstand overload without destroying the expensive movement. If I is the normal *f.s.d.* current, a potential difference of IR_m is developed across the diode. The circuit is so designed that IR_m does not turn on the diode. In the event of an accidental overload (say 5 I), the voltage across diode becomes 5 times greater and it is immediately turned on. Consequently, diode diverts most of the overload current in the same manner as a shunt. Thus protection of the meter against overload is ensured. Silicon diodes are perhaps the best to use in such circuits.

Example 22.1. *A multimeter has full scale deflection current of 1 mA. Determine its sensitivity.*

Solution. Full scale deflection current, I_g = 1 mA = 10^{-3} A

∴ Multimeter sensitivity = $1/I_g$ = $1/10^{-3}$ = **1000 Ω per volt**

Example 22.2. *A multimeter has a sensitivity of 1000 Ω per volt and reads 50 V full scale. If the meter is to be used to measure the voltage across 50000 Ω resistor, will it read correctly ?*

Solution. Meter sensitivity = 1000 Ω per volt

Full scale volts = 50 V

∴ Meter resistance = 50 × 1000 = 50,000 Ω

When the meter is used to measure the voltage across the resistance as shown in Fig. 22.8, the total resistance of the circuit is a parallel combination of two 50,000 Ω resistors. Therefore, the circuit resistance would be reduced to 25000 Ω and double the amount of current would be drawn than would otherwise be the case.

∴ *Meter will give highly incorrect reading.*

Comments. This example shows the limitation of multimeter. The multimeter will read correctly only if its resistance is very high as compared to the resistance across which voltage is to be measured.

As a rule, the resistance of the multimeter should be atleast 100 times the resistance across which voltage is to be measured.

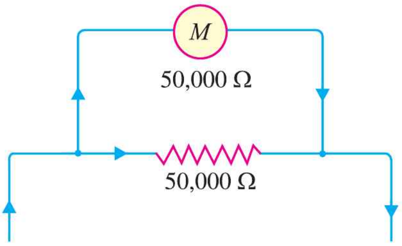


Fig. 22.8

Example 22.3. *In the circuit shown in Fig. 22.9 (i), it is desired to measure the voltage across 10 kΩ resistance. If a multimeter of sensitivity 4 kΩ/volt and range 0-10 V is used for the purpose, what will be the reading ?*

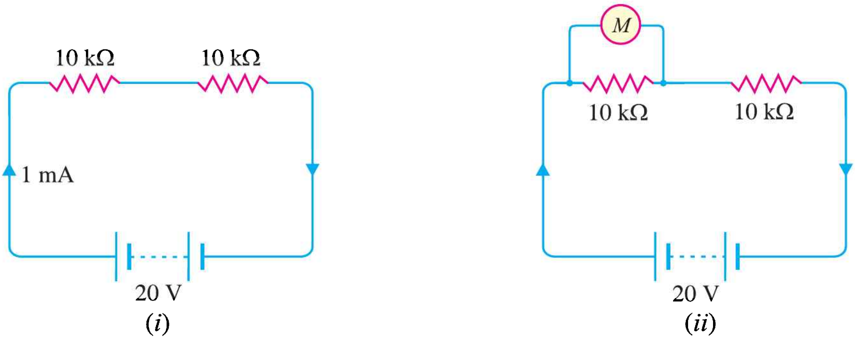
Solution. In the circuit shown in Fig. 22.9 (*i*), the circuit current by Ohm's law is 1 mA. Therefore, voltage across 10 kΩ resistance is 10 V. Let us see whether the given multimeter reads this value. Fig. 22.9 (*ii*) shows the multimeter connected across 10 kΩ resistance. The introduction of multimeter will change the circuit resistance and hence circuit current.

$$\text{Resistance of meter} = 4\text{ k}\Omega \times 10 = 40\text{ k}\Omega$$

$$\text{Total circuit resistance} = 40\text{ k}\Omega \parallel 10\text{ k}\Omega + 10\text{ k}\Omega$$

$$= \frac{40\times10}{40+10} + 10 = 8 + 10 = 18\text{ k}\Omega$$

$$\therefore \quad \text{Circuit current} = \frac{20\,V}{18\text{ k}\Omega} = 1.11\text{ mA}$$



(*i*) (*ii*)

Fig. 22.9

$$\text{Voltage read by multimeter} = 8\text{ k}\Omega \times 1.11\text{ mA} = \mathbf{8.88\ V}$$

Example 22.4. *If in the above example, a multimeter of sensitivity 20 kΩ per volt is used, what will be the reading ?*

Solution. $$\text{Meter resistance} = 20\text{ k}\Omega \times 10 = 200\text{ k}\Omega$$

$$\text{Total circuit resistance} = 200\text{ k}\Omega \parallel 10\text{ k}\Omega + 10\text{ k}\Omega$$

$$= \frac{200\times10}{200+10} + 10 = 9.5 + 10 = 19.5\text{ k}\Omega$$

$$\text{Circuit current} = \frac{20\,V}{19.5\text{ k}\Omega} = 1.04\text{ mA}$$

$$\therefore \quad \text{Voltage read by multimeter} = 9.5\text{ k}\Omega \times 1.04\text{ mA} = \mathbf{9.88\ V}$$

A comparison of examples 22.3 and 22.4 shows that a multimeter with higher sensitivity gives more correct reading.

Example 22.5. *In the circuit shown in Fig. 22.10, find the voltage at points A, B, C and D (i) before the meter is connected and (ii) after the meter is connected. Explain why the meter readings differ from those without the meter connected.*

Solution. (*i*) **When meter is not connected.** When meter is not connected in the circuit, the circuit is a simple series circuit consisting of resistances 20 kΩ, 20 kΩ, 30 kΩ and 30 kΩ.

$$\text{Total circuit resistance} = 20 + 20 + 30 + 30 = 100 \text{ k}\Omega$$

$$\therefore \quad \text{Circuit current} = \frac{100\,V}{100\text{ k}\Omega} = 1\text{ mA}$$

$$\text{Voltage at point } A = \mathbf{100\ V}$$

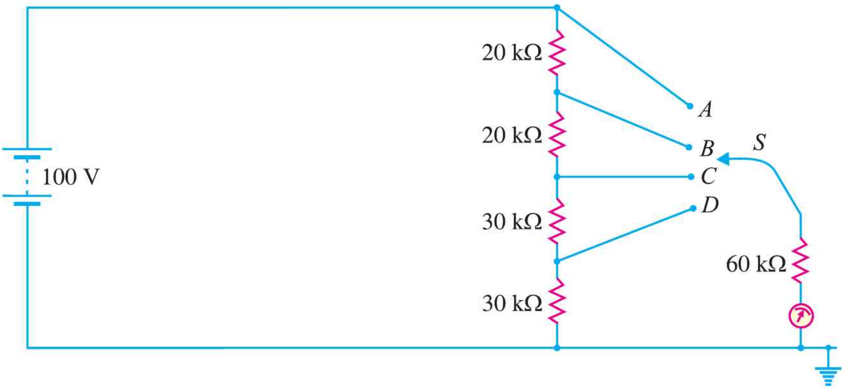


Fig. 22.10

$$\text{Voltage at point } B = 100 - 1\text{ mA} \times 20\text{ k}\Omega = \mathbf{80\ V}$$

$$\text{Voltage at point } C = 100 - 1\text{ mA} \times 40\text{ k}\Omega = \mathbf{60V}$$

$$\text{Voltage at point } D = 100 - 1\text{ mA} \times 70\text{ k}\Omega = \mathbf{30V}$$

(*ii*) **When meter is connected.** When meter is connected in the circuit, the circuit becomes a series-parallel circuit. The total circuit resistance would depend upon the position of switch *S*.

(***a***) *When switch is at position A*

The voltage at point *A* is 100 V because point *A* is directly connected to the voltage source.

$$\therefore \quad \text{Voltage at point } A = \mathbf{100\ V}$$

(***b***) *When switch is at position B*

$$\text{Total circuit resistance} = 20 + \frac{80 \times 60}{80 + 60} = 20 + 34.28 = 54.28 \text{ k}\Omega$$

$$\therefore \quad \text{Circuit current} = \frac{100\,V}{54.28\text{ k}\Omega}$$

$$\therefore \quad \text{Voltage at point } B = \frac{100\text{ V}}{54.28\text{ k}\Omega} \times 34.28\text{ k}\Omega = \mathbf{63\ V}$$

(***c***) *When switch is at point C*

$$\text{Total circuit resistance} = 40 + \frac{60 \times 60}{60 + 60} = 40 + 30 = 70 \text{ k}\Omega$$

$$\therefore \quad \text{Circuit current} = \frac{100\text{ V}}{70\text{ k}\Omega}$$

$$\therefore \qquad \text{Voltage at point } C = \frac{100\text{ V}}{70\text{ k}\Omega} \times 30\text{ k}\Omega = \mathbf{42.8\ V}$$

(*d*) *When switch is at point D*

$$\text{Total circuit resistance} = 70 + \frac{30 \times 60}{30 + 60} = 70 + 20 = 90\text{ k}\Omega$$

$$\therefore \qquad \text{Circuit current} = \frac{100\text{ V}}{90\text{ k}\Omega}$$

$$\therefore \qquad \text{Voltage at point } D = \frac{100\text{ V}}{90\text{ k}\Omega} \times 20\text{ k}\Omega = \mathbf{22.2\ V}$$

Comments. Note that potential measurements are being made in a high-impedance circuit; the circuit resistance is comparable to meter resistance. As a rule, the resistance of the voltmeter should be 100 times the resistance across which voltage is to be measured. Since such a condition is not realised in this problem, the meter readings differ appreciably from those without the meter connected.

22.7 Electronic Voltmeters

The electromagnetic and electrostatic voltmeters have two main drawbacks. First, the input resistance/impedance of these instruments is not very high so that there is a considerable *loading effect of the instrument. Secondly, considerable power is drawn from the circuit under measurement. Both these drawbacks are overcome in electronic voltmeters. The electronic devices (*e.g.* vacuum tubes, transistors etc.) have very high input resistance/impedance and possess the property of amplification. The latter property permits the input signal to be amplified so that the power to operate the indicating mechanism comes from a source other than the measured circuit. There are a large number of electronic voltmeters. However, we shall discuss the following three types of electronic voltmeters :

(*i*) Vacuum Tube Voltmeter (*VTVM*)

(*ii*) Transistor Voltmeter

(*iii*) Bridge Rectifier Voltmeter

22.8 Vacuum Tube Voltmeter (VTVM)

A vacuum tube voltmeter consists of any ordinary voltmeter and electron tubes. It is extensively used for measuring both a.c. and d.c. voltages. The vacuum tube voltmeter has high internal resistance ($> 10\text{ M}\Omega$) and draws extremely small current from the circuit across which it is connected. In other words, the loading effect of this instrument is very small. Therefore, a *VTVM* measures the exact voltage even across a high resistance. In fact, the ability of *VTVM* to measure the voltages accurately has made this instrument the most popular with technicians for trouble shooting radio and television receivers as well as for laboratory work involving research and design.

(*i*) **Simple VTVM circuit.** Fig. 22.11 shows the simple circuit of a vacuum tube voltmeter. It consists of a triode having meter *M* connected in the plate circuit. The meter is calibrated in volts. R_1 is the grid leak resistor. The voltage to be measured is applied at the grid of triode in such a way that grid is always negative *w.r.t.* cathode. This voltage at the grid is transformed by the triode into corresponding plate current. The meter *M* connected in the plate circuit directly gives the value of the voltage under measurement. It may be seen that as grid draws extremely small current ($< 1\ \mu$A), therefore, internal resistance of *VTVM* is very large. This circuit has the disadvantage that if the applied voltages change (especially filament voltage), the plate current will also change. Consequently, the meter will give wrong reading.

---

* When a voltmeter is connected across a resistance *R* to measure voltage, the measured voltage will be less than the actual value. It is because the resistance *R* is shunted by the voltmeter. This is called loading effect of the meter. The greater the input resistance of voltmeter, the smaller will be the loading effect and more accurate is the reading.

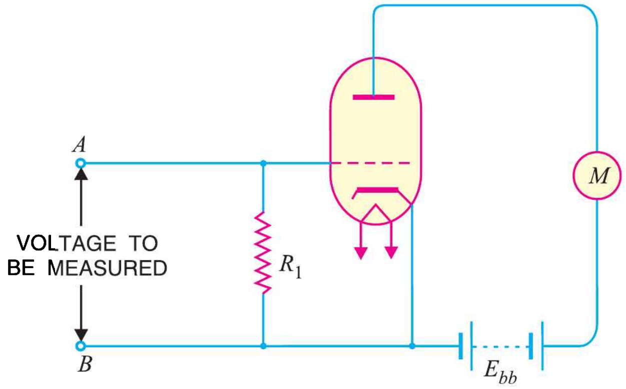


Fig. 22.11

(*ii*) **Balanced bridge Type VTVM.** The disadvantage of above circuit is overcome in the balanced bridge type *VTVM* shown in Fig. 22.12. Here, two similar triodes V_1 and V_2 are used. The meter *M* is connected between the plates of triodes and indicates the voltage to be measured. The variable resistance *r* in the plate circuit of V_2 is for zero adjustment of the meter. The voltage to be measured is applied at the grid of triode V_1 in such a way that grid is always negative with respect to cathode.

Operation. When no voltage is applied at the input terminals *AB*, the plate currents flowing in both valves are equal as the triodes are similar. Therefore, plates of both valves are at the same potential. Consequently, the current through the meter *M* is zero and the meter reads zero volt. However, in actual practice, there are always some constructional differences in plates, grids and cathodes of the two valves. The result is that two plate currents differ slightly and the meter may give some reading. In such a case, the meter needle is brought to zero by changing resistance *r*.

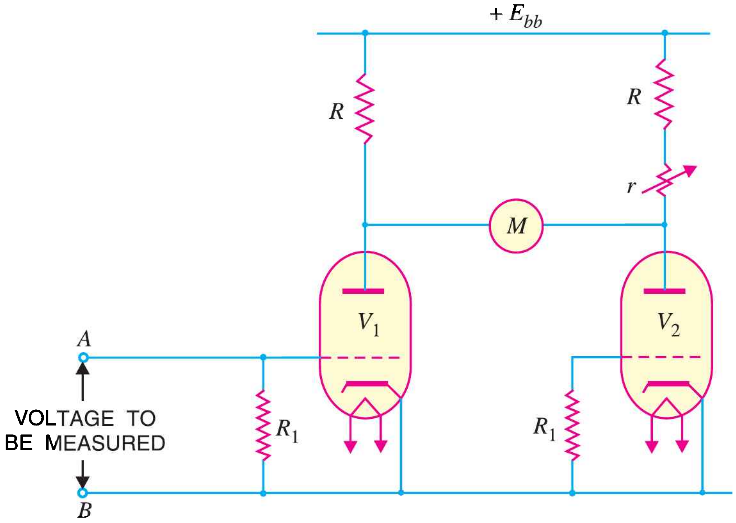


Fig. 22.12

The voltage to be measured is applied at the grid of triode V_1, making the grid negative *w.r.t.* cathode. This changes the plate current of triode V_1 and the plates of two valves no longer remain at the same potential. Therefore, a small current flows through the meter *M* which directly gives the value of the voltage being measured. It may be noted that actually triode V_1 is used for voltage measurement, the purpose of V_2 is simply to prevent zero drift. By using two similar tubes, any change in plate current due to supply fluctuations will equally affect the two plate currents. Therefore, net change in potential drop across voltmeter is zero.

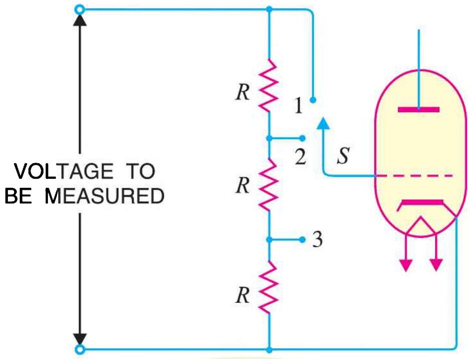


Fig. 22.13

VTVM

Range selection. In practice, a *VTVM* is made a multirange instrument by employing a potentiometer at the input circuit as shown in Fig. 22.13. By throwing the range selector switch *S* to a suitable position, the desired voltage range can be obtained. Thus when the range selector switch *S* is thrown to position 1, the voltage applied to the grid is three times as compared to position 3. Although only three voltage ranges have been considered, a commercial *VTVM* may have more ranges.

22.9 Applications of VTVM

A *VTVM* is far superior to a multimeter and performs a number of measuring functions. A few important applications of *VTVM* are discussed below :

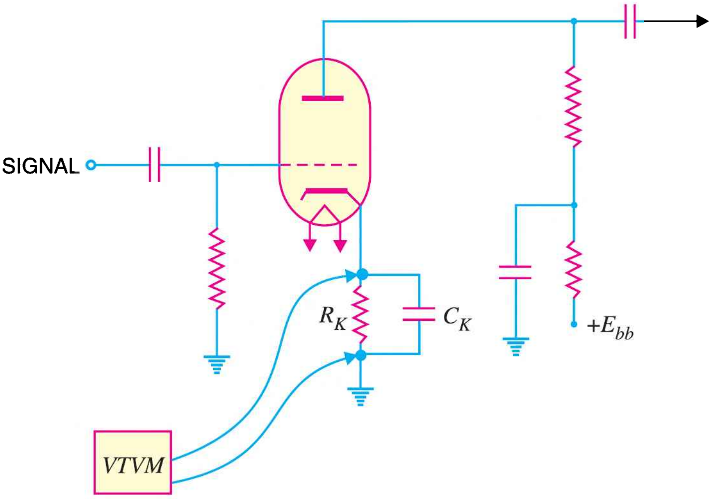


Fig. 22.14

(*i*) **d.c. voltage measurements.** A *VTVM* can accurately measure the d.c. voltages in an electronic circuit. The d.c. voltage to be measured is applied at the input (*i.e.* grid of V_1) terminals in such a way that grid of the input valve V_1 is always negative. Fig. 22.14 shows the circuit of an amplifier stage and measurement of d.c. voltage across cathode resistor R_K.

(*ii*) **d.c. current measurements.** A conventional *VTVM* does not incorporate a current scale. However, current values can be found indirectly. For instance, in Fig. 22.14, the d.c. current through R_K can be found by noting the voltage across R_K and dividing it by the resistance R_K.

(*iii*) **a.c. voltage measurements.** For measuring a.c. voltage, a rectifier is used in conjunction with a *VTVM*. The rectifier converts a.c. into d.c. for application to the grid of valve V_1. In fact, rectifier circuit is a part of *VTVM*. Fig. 22.15 shows the transistor power amplifier stage and measurement of a.c. voltage across the speaker.

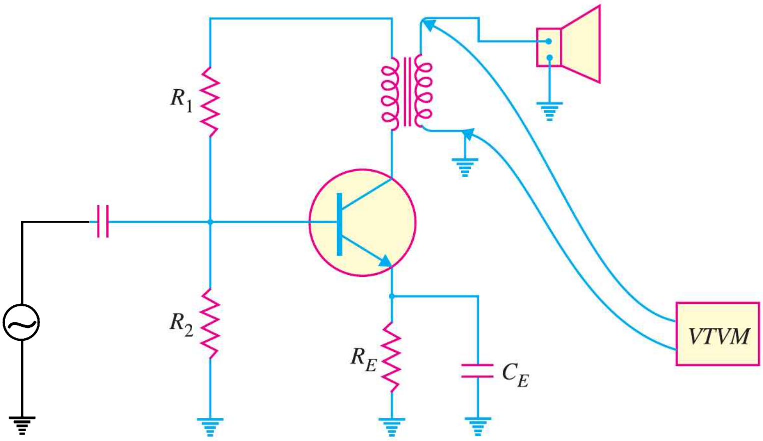


Fig. 22.15

(*iv*) **Resistance measurements.** A *VTVM* can be used to measure resistances and has the ability to measure resistances upto 1000 megaohms whereas the ordinary ohmmeter will measure only upto about 10 megaohms. Fig. 22.16 shows the circuit of *VTVM* ohmmeter. By throwing the selector switch *S* to any suitable position, the desired resistance range can be obtained. The unknown resistor whose value is to be measured is connected between points *A* and *B*. If the unknown resistance has high value, a higher negative bias will be applied to triode V_1. Reverse will happen if the unknown

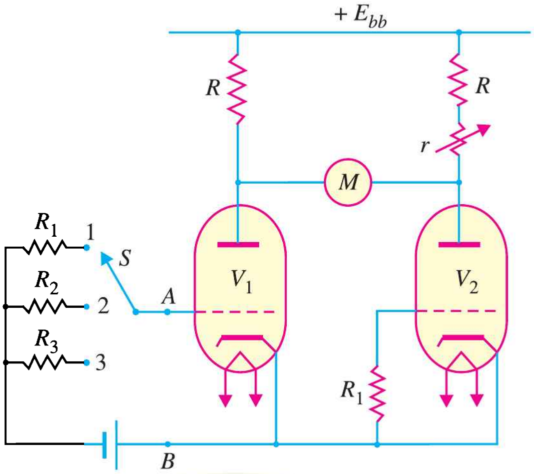


Fig. 22.16

resistance has low value. The imbalance in the plate currents of the two valves will cause a current through the meter M which will directly give the value over the resistance scale of the meter.

22.10 Merits and Demerits of VTVM

A *VTVM* is an extremely important electronic equipment and is widely used for making different measurements in electronic circuits.

Merits

(*i*) A *VTVM* draws extremely small current from the measuring circuit. Therefore, it gives accurate readings.

(*ii*) There is little effect of temperature variations.

(*iii*) Because a *VTVM* uses triodes, the voltage to be measured is amplified. This permits the use of less sensitive meter.

(*iv*) It has a wide frequency response.

Demerits

(*i*) It cannot make current measurements directly.

(*ii*) Accurate readings can be obtained only for sine waves.

22.11 Transistor Voltmeter Circuit

Since vacuum tubes have become obsolete, these have been replaced by transistors and other semiconductor devices. Fig. 22.17 shows the circuit of an emitter-follower voltmeter. The voltage E to be measured is applied between base and emitter. A permanent-magnet moving coil (PMMC) instrument and a multiplier resistor R_S are connected in series with the transistor emitter. The circuit measures the voltage quite accurately because the emitter follower offers high input resistance to the voltage being measured and provides a low output resistance to drive current through the coil of PMMC meter.

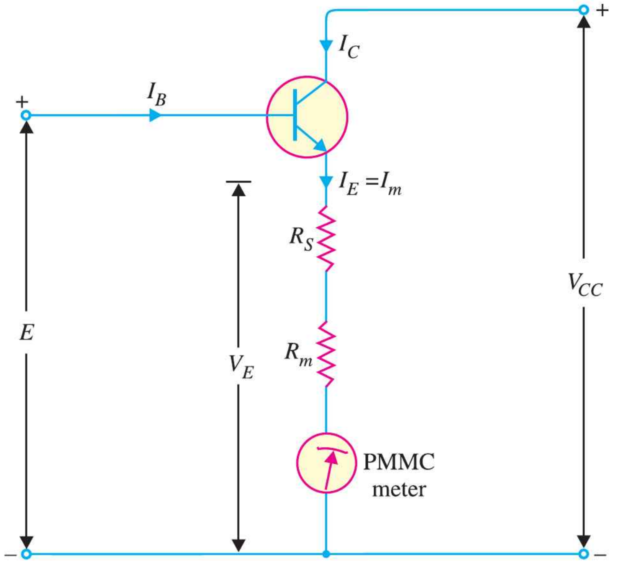


Fig. 22.17

Operation. The voltage E to be measured is applied between base and emitter of the transistor and causes a base current I_B to flow through the base circuit. Therefore, collector current $I_C = \beta I_B$ where β is the current amplification factor of the transistor. Since $I_E \simeq I_C$ and the meter is connected in the emitter, the meter current $I_m = I_E = \beta I_B$. Now the meter current I_m depends upon the input voltage to be measured. Therefore, the PMMC meter can be calibrated to read the input voltage directly.

$$\text{Emitter voltage, } V_E = E - V_{BE}$$

$$\text{Meter current, } I_m = \frac{V_E}{R_S + R_m}$$

Here R_S = multiplier resistor ; R_m = meter resistance

Input resistance of voltmeter, $R_i = \frac{E}{I_B}$

Example 22.6. *The emitter follower circuit shown in Fig. 22.17 has V_{CC} = 12 V ; R_m = 1kΩW and a 2 mA meter. If transistor β = 80, calculate (i) the suitable resistance for R_S to give full -scale deflection when E = 5V (ii) the voltmeter input resistance.*

Solution.

$$\text{Meter resistance, } R_m = 1\text{ k}\Omega$$

$$\text{F.S.D. current of meter,} I_{m\,(f.s.d.)} = 2\text{ mA} = 2 \times 10^{-3}\text{A}$$

(*i*) $$\text{Emitter voltage, } V_E = E - V_{BE} = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

$$\therefore \quad I_{m\,(f.s.d.)} = \frac{V_E}{R_S + R_m}$$

$$\text{or} \quad 2 \times 10^{-3} = \frac{4.3\text{V}}{1000\Omega + R_S} \qquad \therefore\ R_S = \mathbf{1150\ \Omega}$$

(*ii*) $$\text{Base current, } I_B = \frac{I_{m\,(f.s.d.)}}{\beta} = \frac{2\ mA}{80} = 0.025\text{ mA}$$

$$\therefore \quad \text{Input resistance of voltmeter, } R_i = \frac{E}{I_B} = \frac{5\text{V}}{0.025\text{ mA}} = \mathbf{200\ k\Omega}$$

Example 22.7. *The emitter-follower voltmeter circuit in Fig. 22.17 has V_{CC} = 20 V, $R_S + R_m$ = 9.3 kΩ, I_m = 1 mA and transistor β = 100.*

(*i*) *Calculate the meter current when E = 10V.*

(*ii*) *Determine the voltmeter input resistance with and without the transistor.*

Solution.

(*i*) $$\text{Emitter voltage, } V_E = E - V_{BE} = 10\text{V} - 0.7\text{ V} = 9.3\text{ V}$$

$$\therefore \quad \text{Meter current, } I_m = \frac{V_E}{R_S + R_m} = \frac{9.3\text{ V}}{9.3\text{ k}\Omega} = \mathbf{1\ mA}$$

(*ii*) $$\text{Base current, } I_B = \frac{I_m}{\beta} = \frac{1\text{ mA}}{100} = 0.01\text{ mA}$$

$$\text{With transistor, } R_i = \frac{E}{I_B} = \frac{10\text{ V}}{0.01\text{ mA}} = 1000\text{ k}\Omega = \mathbf{1\ M\Omega}$$

$$\text{Without transistor, } R_i = R_S + R_m = \mathbf{9.3\ k\Omega}$$

Note that without transistor, the voltmeter input resistance = $R_S + R_m$ = 9.3 kΩ. However, with transistor, the voltmeter input resistance = 1 MΩ = 1000 kΩ. The obvious advantage of the electronic voltmeter is that its loading effect in voltage measurement will be very small.

Example 22.8. *In the above example, if E = 5V, all other values remaining the same, what will be the value of meter current? Comment on the result.*

Solution.

$$\text{Meter current, } I_m = \frac{E - V_{BE}}{R_S + R_m} = \frac{5\text{V} - 0.7\text{V}}{9.3\text{ k}\Omega} = \frac{4.3\text{V}}{9.3\text{ k}\Omega} = \mathbf{0.46\ mA}$$

With $E = 5$V, the meter should read half of full-scale reading *i.e.* 0.5 mA. However, the meter current is actually 0.46 mA. This error is due to V_{BE} and can be eliminated by the modification of the circuit.

22.12 Bridge Rectifier Voltmeter

A permanent-magnet moving coil (PMMC) instrument responds to *average* or d.c. value of current through the moving coil. If alternating current is passed through the moving coil, the driving torque would be *zero. It is because the average value of a sine wave over one cycle is zero. Therefore, a PMMC instrument connected directly to measure a.c. indicates zero reading. In order to measure a.c. with a PMMC instrument, the given a.c. is converted into d.c. by using a bridge rectifier. The instrument is then called rectifier type instrument.

Circuit details. Fig. 22.18 shows bridge rectifier voltmeter for the measurement of a.c. voltages. A multiplier resistor R_S is connected in **series with the PMMC instrument having resistance R_m. When a.c. voltage to be measured is applied to the circuit, full-wave rectification will be obtained as shown in Fig. 22.19. The meter deflection will be proportional to the †average current. Since there is a definite relationship between the average value and r.m.s. value of a sine-wave (r.m.s. value = 1.11 × average value), the meter scale can be calibrated to read the r.m.s. value directly.

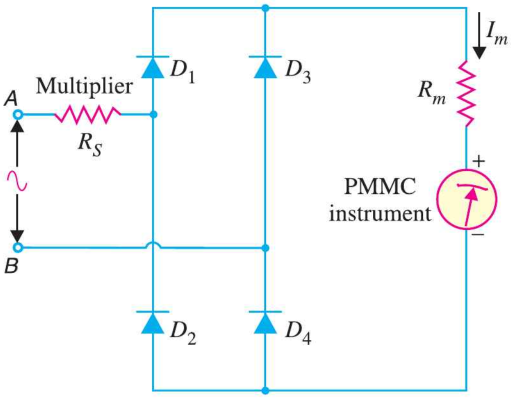


Fig. 22.18

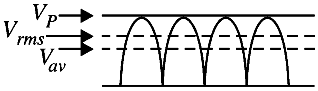


Fig. 22.19

Operation. When a.c. voltage to be measured is applied to the circuit, it passes the positive half-cycles of the input and inverts the negative half-cycles.

(*i*) During the positive half-cycle of the a.c. input voltage, point *A* is positive w.r.t. point *B*. Therefore, diodes D_1 and D_4 are forward biased while diodes D_2 and D_3 are reverse biased. As a result, diodes D_1 and D_4 conduct and the current follows the path $R_S - D_1$ – PMMC meter – D_4 – back to point *B*. Note that multiplier resistor R_S and the meter are in series.

(*ii*) During the negative half-cycle of the a.c. input voltage, diodes D_2 and D_3 are forward biased while diodes D_1 and D_4 are reverse biased. As a result, diodes D_2 and D_3 conduct and the current follows path D_3 – PMMC meter – $D_2 - R_S$ back to point *A*. Note that current through the meter is in the same direction as for the positive half-cycle. Consequently, full-wave rectification results.

---

* The driving torque would be in one direction for the positive half-cycle and in the other direction for the negative half-cycle. The inertia of the coil is so great that at supply frequency (50 Hz),the pointer cannot follow the rapid reversals of the driving torque. Therefore, pointer of the meter remians stationary at zero mark.

** If you see carefully, the four diodes (D_1, D_2, D_3 and D_4) form the bridge. Note that the same current flows through the R_S and R_m.

† Note that a voltmeter is a current-operated device.

The scale of the PMMC meter is calibrated to read directly the r.m.s. value of a.c. voltage being measured. It may be noted that rectifier voltmeter can be used only to measure pure sine-wave voltages. When other than pure sine-waves are applied, the meter will *not* indicate the r.m.s. voltage.

Example 22.9. *A PMMC instrument with a full-scale deflection (f.s.d.) current of 100 μA and R_m = 1 kΩ is to be used as a voltmeter of range 0 – 100 V (r.m.s.). The diodes used in the bridge rectifier circuit are of silicon. Calculate the value of multiplier resistor R_S required.*

Solution. Note that 100 μA is the average current.

F.S.D. current of meter, $I_{m\,(f.s.d.)} = 100\ \mu\text{A} = 100 \times 10^{-6}\ \text{A} = 10^{-4}\ \text{A}$

Total circuit resistance, $R_T = R_S + R_m = (R_S + 1000)\ \Omega$

Peak value of applied voltage, $V_m = \sqrt{2}\ V_{r.m.s.} = \sqrt{2} \times 100\ \text{V} = 141.4\text{V}$

* Total rectifier drop $= 2\ V_F = 2 \times 0.7 = 1.4\text{V}$

$$\text{Peak f.s.d. current of meter} = \frac{\text{Peak applied voltage} - \text{Rectifier Drop}}{\text{Total circuit resistance}}$$

or $$\frac{10^{-4}}{0.637} = \frac{141.4 - 1.4}{R_S + 1000} \qquad \left(\because I_{peak} = \frac{I_{av.}}{0.637}\right)$$

∴ $$R_S = \mathbf{890.7\ k\Omega}$$

Example 22.10. *An a.c. voltmeter uses a bridge rectifier with silicon diodes and a PMMC instrument with f.s.d. current of 75 μA. If meter coil resistance is 900Ω and the multiplier resistor is 708 kΩ, calculate the applied r.m.s. voltage when the meter reads f.s.d.*

Solution. The PMMC meter reads average value.

∴ $$\text{Peak f.s.d. meter current} = \frac{75 \times 10^{-6}}{0.637}\ \text{A} \qquad \left(\because I_{peak} = \frac{I_{av.}}{0.637}\right)$$

$$\text{Now Peak f.s.d. meter current} = \frac{\text{Peak applied voltage} - \text{Rectifier drop}}{\text{Total circuit resistance}}$$

or $$\frac{75 \times 10^{-6}}{0.637} = \frac{\sqrt{2}\,V_{r.m.s.} - 2 \times 0.7}{R_S + R_m}$$

or $$117.74 \times 10^{-6} = \frac{1.414\,V_{r.m.s} - 1.4}{708 \times 10^3 + 900}$$

∴ $$V_{r.m.s.} = \frac{(117.74 \times 10^{-6})(708 \times 10^3 + 900) + 1.4}{1.414} = \mathbf{60V}$$

22.13 Cathode Ray Oscilloscope

The cathode ray oscilloscope (commonly abbreviated as *CRO*) is an electronic device which is capable of giving a visual indication of a signal waveform. No other instrument used in the electronic industry is as versatile as the cathode ray oscilloscope. It is widely used for trouble shooting radio and television receivers as well as for laboratory work involving research and design. With an oscilloscope, the wave-shape of a signal can be studied with respect to amplitude distortion and deviation from the normal. In addition, the oscilloscope can also be used for measuring voltage, frequency and phase shift.

In an oscilloscope, the electrons are emitted from a cathode accelerated to a high velocity and brought to focus on a fluorescent screen. The screen produces a visible spot where the electron beam strikes. By deflecting the electron beam over the screen in response to the electrical signal, the electrons can be made to act as an *electrical pencil of light* which produces a spot of light wherever it strikes. An oscilloscope obtains its remarkable properties as a measuring instrument from the fact that it uses as an indicating needle a beam of electrons. As electrons have negligible mass, therefore, they respond almost instantaneously when acted upon by an electrical signal and can trace almost any electrical variation no matter how rapid. A cathode ray oscilloscope contains a *cathode ray tube* and necessary power equipment to make it operate.

---

* During positive or negative half-cycle of input a.c. voltage, two diodes (D_1 and D_4 or D_2 and D_3) are in series.

22.14 Cathode Ray Tube

A cathode ray tube (commonly abbreviated as *CRT*) is the heart of the oscilloscope. It is a vacuum tube of special geometrical shape and converts an electrical signal into visual one. A cathode ray tube makes available plenty of electrons. These electrons are accelerated to high velocity and are brought to focus on a fluorescent screen. The electron beam produces a spot of light wherever it strikes. The electron beam is deflected on its journey in response to the electrical signal under study. The result is that electrical signal waveform is displayed visually. Fig. 22.20 shows the various parts of cathode ray tube.

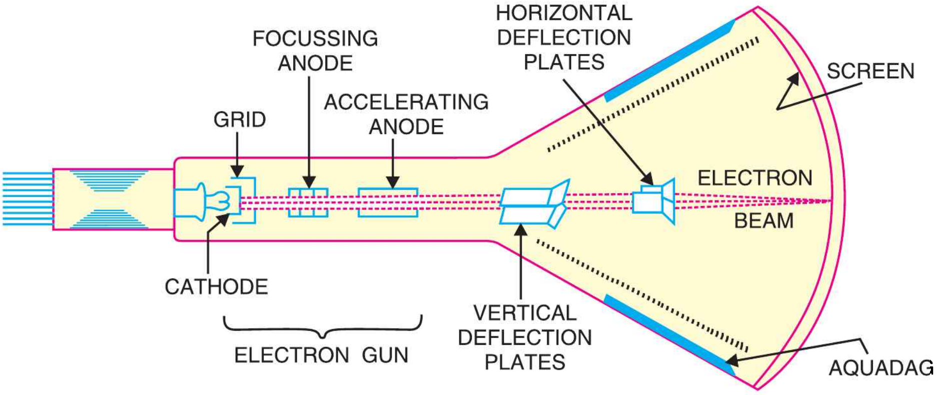


Fig. 22.20

(*i*) **Glass envelope.** It is conical highly evacuated glass housing and maintains vacuum inside and supports the various electrodes. The inner walls of *CRT* between neck and screen are usually coated with a conducting material, called *aquadag*. This coating is electrically connected to the accelerating anode so that electrons which accidentally strike the walls are returned to the anode. This prevents the walls of the tube from charging to a high negative potential.

(*ii*) **Electron gun assembly.** The arrangement of electrodes which produce a focussed beam of electrons is called the *electron gun*. It essentially consists of an indirectly heated *cathode*, a *control grid*, a *focussing anode* and an *accelerating anode*. The control grid is held at negative potential *w.r.t.* cathode whereas the two anodes are maintained at high positive potential *w.r.t.* cathode.

The cathode consists of a nickel cylinder coated with oxide coating and provides plenty of electrons. The control grid encloses the cathode and consists of a metal cylinder with a tiny circular opening to keep the electron beam small in size. The focussing anode focuses the electron beam into a sharp pin-point by controlling the positive potential on it. The positive potential (about 10,000 V) on the accelerating anode is much higher than on the focusing anode. For this reason, this anode accelerates the narrow beam to a high velocity. Therefore, the electron gun assembly forms a narrow, accelerated beam of electrons which produces a spot of light when it strikes the screen.

(*iii*) **Deflection plate assembly.** The deflection of the beam is accomplished by two sets of deflecting plates placed within the tube beyond the accelerating anode as shown in Fig. 22.20. One set is the *vertical deflection plates* and the other set is the *horizontal deflection plates*.

The vertical deflection plates are mounted horizontally in the tube. By applying proper potential to these plates, the electron beam can be made to move up and down vertically on the fluorescent screen. The horizontal deflection plates are mounted in the vertical plane. An appropriate potential on these plates can cause the electron beam to move right and left horizontally on the screen.

(iv) **Screen.** The screen is the inside face of the tube and is coated with some fluorescent material such as zinc orthosilicate, zinc oxide etc. When high velocity electron beam strikes the screen, a spot of light is produced at the point of impact. The colour of the spot depends upon the nature of fluorescent material. If zinc orthosilicate is used as the fluorescent material, green light spot is produced.

Action of CRT. When the cathode is heated, it emits plenty of electrons. These electrons pass through control grid on their way to screen. The control grid influences the amount of current flow as in standard vacuum tubes. If negative potential on the control grid is high, fewer electrons will pass through it and the electron beam on striking the screen will produce a dim spot of light. Reverse will happen if the negative potential on the control grid is reduced. Thus, the intensity of light spot on the screen can be changed by changing the negative potential on the control grid. As the electron beam leaves the control grid, it comes under the influence of focussing and accelerating anodes. As the two anodes are maintained at high positive potential, therefore, they produce a field which acts as an *electrostatic lens* to converge the electron beam at a point on the screen.

As the electron beam leaves the accelerating anode, it comes under the influence of vertical and horizontal deflection plates. If no voltage is applied to the deflection plates, the electron beam will produce spot of light at the centre (point O in Fig. 22.21) of the screen. If the voltage is applied to vertical plates *only* as shown in Fig. 22.21, the electron beam and hence the spot of light will be deflected upwards (point O_1). The spot of light will be deflected downwards (point O_2) if the potential on the plates is reversed. Similarly, the spot of light can be moved horizontally by applying voltage across the horizontal plates.

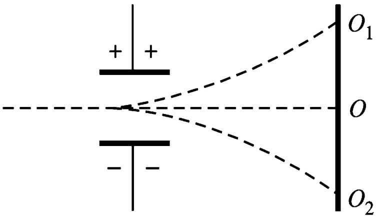


Fig. 22.21

22.15 Deflection Sensitivity of CRT

The shift of the spot of light on the screen per unit change in voltage across the deflection plates is known as *deflection sensitivity* of *CRT*. For instance, if a voltage of 100 V applied to the vertical plates produces a vertical shift of 3 mm in the spot, then deflection sensitivity is 0.03 mm/V. In general,

Spot deflection = Deflection sensitivity × Applied voltage

The deflection sensitivity depends not only on the design of the tube but also on the voltage applied to the accelerating anode. The deflection sensitivity is low at high accelerating voltages and vice-versa.

Example 22.11. *The deflection sensitivity of a CRT is 0.01 mm/V. Find the shift produced in the spot when 400 V are applied to the vertical plates.*

Solution. As voltage is applied to the vertical plates only, therefore, the spot will be shifted vertically.

$$\text{Spot shift} = \text{deflection sensitivity} \times \text{applied voltage}$$

$$= 0.01 \times 400 = \mathbf{4\ mm}$$

Example 22.12. *The deflection sensitivity of a CRT is 0.03 mm/V. If an unknown voltage is applied to the horizontal plates, the spot shifts 3 mm horizontally. Find the value of unknown voltage.*

Solution. Deflection sensitivity = 0.03 mm/V

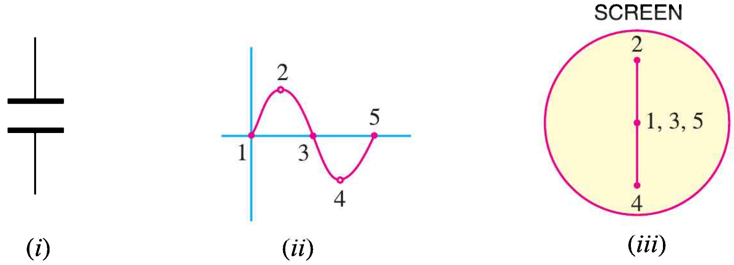
Spot shift = 3 mm

Now, spot shift = deflection sensitivity × applied voltage

$$\therefore \qquad \text{Applied voltage} = \frac{\text{spot shift}}{\text{deflection sensitivity}} = \frac{3 \text{ mm}}{0.03 \text{ mm/V}} = \mathbf{100\ V}$$

22.16 Applying Signal Across Vertical Plates

If a sinusoidal voltage is applied to the vertical deflection plates, it will make the plates alternately positive and negative. Thus, in the positive half of the signal, upper plate will be positive and lower plate negative while in the negative half-cycle, the plate polarities will be reversed.



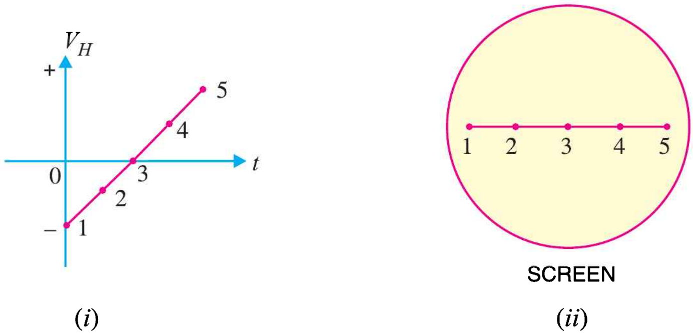
(*i*) (*ii*) (*iii*)

Fig. 22.22

The result is that the spot moves up and down at the same rate as the frequency of the applied voltage. As the frequency of applied voltage is 50 Hz, therefore, due to persistence of vision, we will see a continuous vertical line 2 - 1 - 4 on the screen as shown in Fig. 22.22 (*iii*). The line gives no indication of the manner in which the voltage is alternating since it does not reveal the waveform.

22.17 Display of Signal Waveform on CRO

One interesting application of *CRO* is to present the wave shape of the signal on the screen. As discussed before, if sinusoidal signal is applied to the vertical deflection plates, we get a vertical line. However, it is desired to see the signal voltage variations with time on the screen. This is possible only if we could also move the beam horizontally from left to right at a uniform speed while it is moving up and down. Further, as soon as a full cycle of the signal is traced, the beam should return quickly to the left hand side of the screen so that it can start tracing the second cycle.



(*i*) (*ii*)

Fig. 22.23

In order that the beam moves from left to right at a uniform rate, a voltage that varies linearly with time should be applied to the horizontal plates. This condition is exactly met in the saw tooth wave shown in Fig. 22.23 (*i*).

When time $t = 0$, the negative voltage on the horizontal plates keep the beam to the extreme left on the screen as shown in Fig. 22.23 (*ii*). As the time progresses, the negative voltage decreases linearly with time and the beam moves towards right forming a horizontal line. In this way, the saw-tooth wave applied to horizontal plates moves the beam from left to right at a uniform rate.

22.18 Signal Pattern on Screen

If the signal voltage is applied to the vertical plates and saw-tooth wave to the horizontal plates, we get the exact pattern of the signal as shown in Fig. 22.24. When the signal is at the instant 1, its amplitude is zero. But at this instant, maximum negative voltage is applied to horizontal plates. The result is that the beam is at the extreme left on the screen as shown. When the signal is at the instant 2, its amplitude is maximum. However, the negative voltage on the horizontal plates is decreased. Therefore, the beam is deflected upwards by the signal and towards the right by the saw tooth wave. The result is that the beam now strikes the screen at point 2. On similar reasoning, the beam strikes the screen at points 3, 4 and 5. In this way, we have the exact signal pattern on the screen.

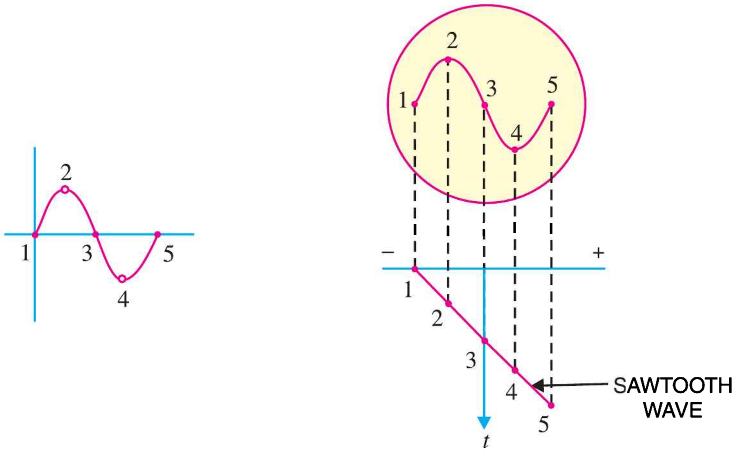


Fig. 22.24

22.19 Various Controls of CRO

In order to facilitate the proper functioning of *CRO*, various controls are provided on the face of *CRO*. A few of them are given below:

(*i*) ***Intensity control.*** The knob of intensity control regulates the bias on the control grid and affects the electron beam intensity. If the negative bias on the grid is increased, the intensity of electron beam is decreased, thus reducing the brightness of the spot.

(*ii*) ***Focus control.*** The knob of focus control regulates the positive potential on the focussing anode. If the positive potential on this anode is increased, the electron beam becomes quite narrow and the spot on the screen is a pin-point.

(*iii*) ***Horizontal position control.*** The knob of horizontal position control regulates the amplitude of d.c. potential which is applied to the horizontal deflection plates, in addition to the usual saw-tooth wave. By adjusting this control, the spot can be moved to right or left as required.

(*iv*) ***Vertical position control.*** The knob of vertical position control regulates the amplitude of d.c. potential which is applied to the vertical deflection plates in addition to the signal. By adjusting this control, the image can be moved up or down as required.

22.20 Applications of CRO

The modern cathode ray oscilloscope provides a powerful tool for solving problems in electrical measurements. Some important applications of *CRO* are :

1. Examination of waveforms
2. Voltage measurement
3. Frequency measurement

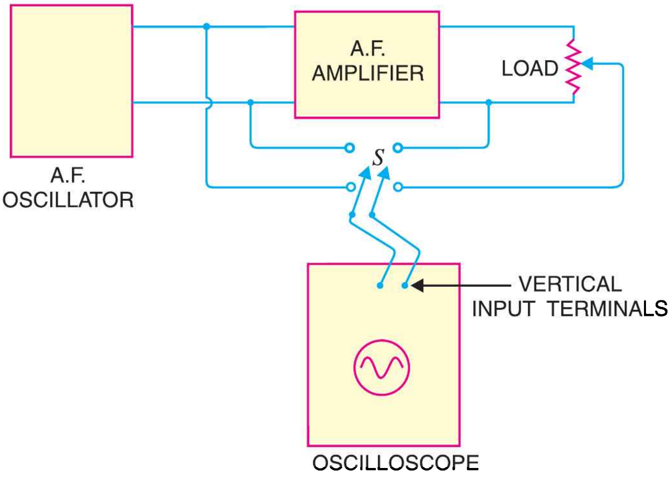


Fig. 22.25

1. Examination of waveform. One of the important uses of *CRO* is to observe the wave shapes of voltages in various types of electronic circuits. For this purpose, the signal under study is applied to vertical input (*i.e.*, vertical deflection plates) terminals of the oscilloscope. The sweep circuit is set to internal so that sawtooth wave is applied to the horizontal input *i.e.* horizontal deflection plates. Then various controls are adjusted to obtain sharp and well defined signal waveform on the screen.

Fig. 22.25 shows the circuit for studying the performance of an audio amplifier. With the help of switch *S*, the output and input of amplifier is applied in turn to the vertical input terminals. If the waveforms are identical in shape, the fidelity of the amplifier is excellent.

2. Voltage measurement. As discussed before, if the signal is applied to the vertical deflection plates only, a vertical line appears on the screen. The height of the line is proportional to peak-to-peak voltage of the applied signal. The following procedure is adopted for measuring voltages with *CRO*.

(*i*) Shut off the internal horizontal sweep generator.

(*ii*) Attach a transparent plastic screen to the face of oscilloscope. Mark off the screen with vertical and horizontal lines in the form of graph.

(*iii*) Now, calibrate the oscilloscope against a known voltage. Apply the known voltage, say 10 V, to the vertical input terminals of the oscilloscope. Since the sweep circuit is shut off, you will get a vertical line. Adjust the vertical gain till a good deflection is obtained. Let the deflection sensitivity be V volts/mm.

(*iv*) Keeping the vertical gain unchanged, apply the unknown voltage to be measured to the vertical input terminals of *CRO*.

(*v*) Measure the length of the vertical line obtained. Let it be l mm.

Then, Unknown voltage $= l \times V$ volts

3. Frequency measurement. The unknown frequency can be accurately determined with the help of a *CRO*. The steps of the procedure are as under :

(*i*) A known frequency is applied to horizontal input and unknown frequency to the vertical input.

(*ii*) The various controls are adjusted.

(*iii*) A pattern with loops is obtained.

(*iv*) The number of loops cut by the horizontal line gives the frequency on the vertical plates (f_v) and the number of loops cut by the vertical line gives the frequency on the horizontal plates (f_H).

$$\therefore \quad \frac{f_v}{f_H} = \frac{\text{No. of loops cut by horizontal line}}{\text{No. of loops cut by vertical line}}$$

For instance, suppose during the frequency measurement test, a pattern shown in Fig. 22.26 is obtained. Let us further assume that frequency applied to horizontal plates is 2000 Hz. If we draw horizontal and vertical lines, we find that one loop is cut by the horizontal line and two loops by the vertical line. Therefore,

$$\frac{f_v}{f_H} = \frac{\text{No. of loops cut by horizontal line}}{\text{No. of loops cut by vertical line}}$$

$$\text{or} \quad \frac{f_v}{2000} = \frac{1}{2}$$

$$\text{or} \quad f_v = 2000 \times 1/2 = 1000 \text{ Hz}$$

i.e. Unknown frequency is 1000 Hz.

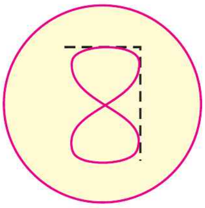


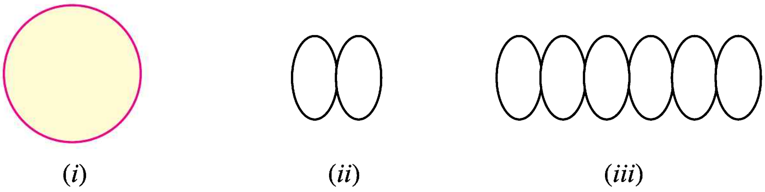
Fig. 22.26

Example 22.13. *In an oscilloscope, 200 V, 50 Hz signal produces a deflection of 2 cm corresponding to a certain setting of vertical gain control. If another voltage produces 3 cm deflection, what is the value of this voltage ?*

Solution. Deflection sensitivity = 200 V/2 cm = 100 V/cm

Unknown voltage = D. S. × deflection = 100 × 3 = **300 V**

Example 22.14. *When signals of different frequencies were applied to the vertical input terminals of oscilloscope, the patterns shown in Fig. 22.27 were obtained. If the frequency applied to horizontal plates in each case is 1000Hz, determine the unknown frequency.*



(*i*) (*ii*) (*iii*)

Fig. 22.27

Solution.

(*i*) The number of loops cut by horizontal and vertical line is one.

$$\therefore \quad \frac{f_v}{f_H} = \frac{1}{1} \quad \text{or} \quad f_v = f_H = \mathbf{1000\ Hz}$$

(*ii*) The number of loops cut by horizontal line is 2 and the number of loops cut by vertical line is 1.

$$\therefore \quad \frac{f_v}{f_H} = \frac{2}{1} \quad \text{or} \quad f_v = 2 \times f_H = 2 \times 1000 = \mathbf{2000\ Hz}$$

(*iii*) The number of loops cut by the horizontal line is 6 and that by vertical line is 1.

$$\therefore \quad \frac{f_v}{f_H} = \frac{6}{1}$$

$$\text{or} \quad f_v = 6 f_H = 6 \times 1000 = \mathbf{6000\ Hz}$$

MULTIPLE-CHOICE QUESTIONS

1. An ammeter is connected in .... with the circuit element whose current we wish to measure.

(*i*) series
(*ii*) parallel
(*iii*) series or parallel
(*iv*) none of the above

2. A galvanometer in series with a high resistance is called ....

(*i*) an ammeter (*ii*) a voltmeter
(*iii*) a wattmeter (*iv*) none of the above

3. An ammeter should have .... resistance.

(*i*) infinite (*ii*) very large
(*iii*) very low (*iv*) none of the above

4. A voltmeter is connected in .... with the circuit component across which potential difference is to be measured.

(*i*) parallel
(*ii*) series
(*iii*) series or parallel
(*iv*) none of the above

5. A voltmeter should have .... resistance.

(*i*) zero (*ii*) very high
(*iii*) very low (*iv*) none of the above

6. The sensitivity of a multimeter is given in ....

(*i*) Ω (*ii*) amperes
(*iii*) kΩ/V (*iv*) none of the above

7. If the full-scale deflection current of a multimeter is 50 μA, its sensitivity is ....

(*i*) 10 kΩ/V (*ii*) 100 kΩ/V
(*iii*) 50 kΩ/V (*iv*) 20 kΩ/V

8. If a multimeter has a sensitivity of 1000 Ω per volt and reads 50 V full scale, its internal resistance is..............

(*i*) 20 kΩ (*ii*) 50 kΩ
(*iii*) 10 kΩ (*iv*) none of the above

9. A *VTVM* has .... input resistance than that of a multimeter.

(*i*) more (*ii*) less
(*iii*) same (*iv*) none of the above

10. The input resistance of a *VTVM* is about ....

(*i*) 1000 Ω (*ii*) 10 kΩ
(*iii*) 20 kΩ (*iv*) 10 MΩ

11. If the negative potential on the control grid of *CRT* is increased, the intensity of spot ....

(*i*) is increased
(*ii*) is decreased
(*iii*) remains the same
(*iv*) none of the above

12. For display of signal pattern .... voltage is applied to the horizontal plates of a *CRO*.

(*i*) sinusoidal (*ii*) rectangular
(*iii*) sawtooth (*iv*) none of the above

13. Two multimeters *A* and *B* have sensitivities of 10 kΩ/V and 30 kΩ/V respectively. Then ....

(*i*) multimeter *A* is more sensitive
(*ii*) multimeter *B* is more sensitive
(*iii*) both are equally sensitive
(*iv*) none of the above

14. A galvanometer of resistance *G* is shunted by a very small resistance *S*. The resistance of the resulting ammeter is ....

(*i*) $\frac{GS}{G+S}$ (*ii*) $G + S$
(*iii*) $G - S$ (*iv*) none of the above

15. A *VTVM* is never used to measure ....

(*i*) voltage (*ii*) current
(*iii*) resistance (*iv*) none of the above

16. The sensitivity of a voltmeter which uses a 100 μA meter movement is ....

(*i*) 1 kΩ/V (*ii*) 10 kΩ/V
(*iii*) 5 kΩ/V (*iv*) data insufficient

17. What is the total resistance of a voltmeter on the 10 V range when the meter movement is rated for 50 μA of full-scale current ?

(*i*) 10 kΩ (*ii*) 20 kΩ
(*iii*) 200 kΩ (*iv*) none of the above

18. The material used to coat inside face of *CRT* is ....

(*i*) carbon (*ii*) sulphur
(*iii*) silicon (*iv*) phosphorus

19. When an ammeter is inserted in the circuit, the circuit current will ....

(*i*) increase
(*ii*) decrease
(*iii*) remain the same
(*iv*) none of the above

20. A series ohmmeter circuit uses a 3 V battery and a 1 mA meter movement. What is the half-scale resistance for this movement ?

(*i*) 3 kΩ (*ii*) 1.5 kΩ
(*iii*) 4.5 kΩ (*iv*) 6 kΩ

21. The most accurate device for measuring voltage is ....

(*i*) voltmeter (*ii*) multimeter
(*iii*) *CRO* (*iv*) *VTVM*

22. The horizontal plates of a *CRO* are supplied with .... to observe the waveform of a signal.

(*i*) sinusoidal wave
(*ii*) cosine wave
(*iii*) sawtooth wave
(*iv*) none of the above

23. A *CRO* is used to measure ....

(*i*) voltage (*ii*) frequency
(*iii*) phase (*iv*) all of above

24. If 2 % of the main current is to be passed through a galvanometer of resistance *G*, then resistance of the shunt required is ....

(*i*) $G/50$ (*ii*) $G/49$
(*iii*) $49\,G$ (*iv*) $50\,G$

25. Which of the following is likely to have the largest resistance ?

(*i*) voltmeter of range 10 V
(*ii*) moving coil galvanometer
(*iii*) ammeter of range 1 A
(*iv*) a copper wire of length 1 m and diameter 3 mm

26. An ideal ammeter has .... resistance.

(*i*) low (*ii*) infinite
(*iii*) zero (*iv*) high

27. The resistance of an ideal voltmeter is ....

(*i*) low (*ii*) infinite
(*iii*) zero (*iv*) high

28. To send 10% of the main current through a moving coil galvanometer of resistance 99 Ω, the shunt required is ....

(*i*) 11 Ω (*ii*) 9.9 Ω
(*iii*) 100 Ω (*iv*) 9 Ω

29. A voltmeter has a resistance of *G* ohms and range *V* volts. The value of resistance required in series to convert it into voltmeter of range ***nV*** is ....

(*i*) nG (*ii*) $\frac{G}{n}$
(*iii*) $\frac{G}{n-1}$ (*iv*) $(n-1)\,G$

30. An ammeter has a resistance of *G* ohms and range of *I* amperes. The value of resistance required in parallel to convert it into an ammeter of range ***nI*** is ....

(*i*) nG (*ii*) $(n-1)\,G$
(*iii*) $\frac{G}{n-1}$ (*iv*) $\frac{G}{n}$

Answers to Multiple-Choice Questions

1. (*i*)	**2.** (*ii*)	**3.** (*iii*)	**4.** (*i*)	**5.** (*ii*)
6. (*iii*)	**7.** (*iv*)	**8.** (*ii*)	**9.** (*i*)	**10.** (*iv*)
11. (*ii*)	**12.** (*iii*)	**13.** (*ii*)	**14.** (*i*)	**15.** (*ii*)
16. (*ii*)	**17.** (*iii*)	**18.** (*iv*)	**19.** (*ii*)	**20.** (*i*)
21. (*iii*)	**22.** (*iii*)	**23.** (*iv*)	**24.** (*ii*)	**25.** (*i*)
26. (*iii*)	**27.** (*ii*)	**28.** (*i*)	**29.** (*iv*)	**30.** (*iii*)

Chapter Review Topics

1. What is a multimeter ? How does it work ?
2. What type of measurements can be made with a multimeter ? Explain with suitable diagrams.
3. Briefly explain the advantages of 20 kΩ/volt multimeter as compared to a 10 kΩ/volt multimeter.
4. What are the applications of a multimeter ?
5. Discuss the advantages and disadvantages of a multimeter.
6. What is a *VTVM* ? Explain balanced bridge Type *VTVM* with a neat circuit diagram.
7. What are the applications of *VTVM* ?
8. Discuss the advantages and disadvantages of *VTVM*.
9. Briefly explain the differences between a *VTVM* and a multimeter.
10. Explain the construction and working of a cathode ray tube.
11. How will you make the following measurements with a *CRO* :
    (*i*) voltage (*ii*) frequency ?
12. Write short notes on the following :
    - (*i*) Limitations of multimeter
    - (*ii*) Advantages of oscilloscope
    - (*iii*) Vacuum tube voltmeter
    - (*iv*) Oscilloscope controls

Problems

1. A voltmeter is used to measure voltage across 20 kΩ resistor as shown in Fig. 22.28. What will be the voltage value if (*i*) voltmeter has infinite resistance (*ii*) voltmeter has a sensitivity of 1000 Ω per volt and reads 100 V full scale ? **[(*i*) 50 V (*ii*) 45 V]**

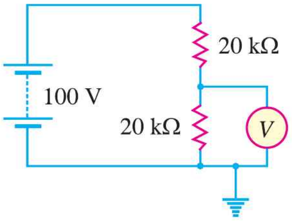


Fig. 22.28

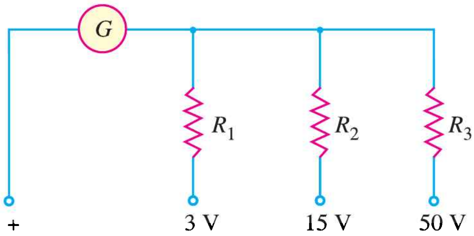


Fig. 22.29

2. The three range voltmeter is arranged as shown in Fig. 22.29. The ranges are 0 to 3 V, 0 to 15 V and 0 to 50 V as marked. If the full scale deflection current is 10 mA, what should be the values of R_1, R_2 and R_3 ? The resistance of the meter is 5 Ω. **[305 Ω, 1505 Ω, 5005 Ω]**
3. If the sensitivity of voltmeter in Fig. 22.28 is 500 Ω/volt (Full-scale reading being 100 V), what will be the reading of the voltmeter ? **[41.7 V]**
4. What is the lowest full-scale voltage that could be displayed with a 100 μA meter movement with an internal resistance of 150 Ω ? What would be the sensitivity of this meter in ohms per volt ? **[15 mV, 10,000 Ω/V]**
5. If a 20,000 Ω/V meter with 5 kΩ internal resistance is used in an ohmmeter with a 3-V-battery, what internal resistance is required in the meter to produce proper zeroing? **[60 kΩ]**
6. A PMMC instrument with f.s.d. = 100 μA and R_m = 1 kΩ is to be used as an a.c. voltmeter with f.s.d. = 100 V (r.m.s.) as shown in Fig. 22.18. Silicon diodes are used in the bridge rectifier circuit. Calculate the pointer indications for the voltmeter when the r.m.s. input voltage is (*i*) 75 V (*ii*) 50V. **[0.75 f.s.d. ; 0.5 f.s.d.]**
7. In the above example, calculate the voltmeter sensitivity. **[9 kΩ/V]**

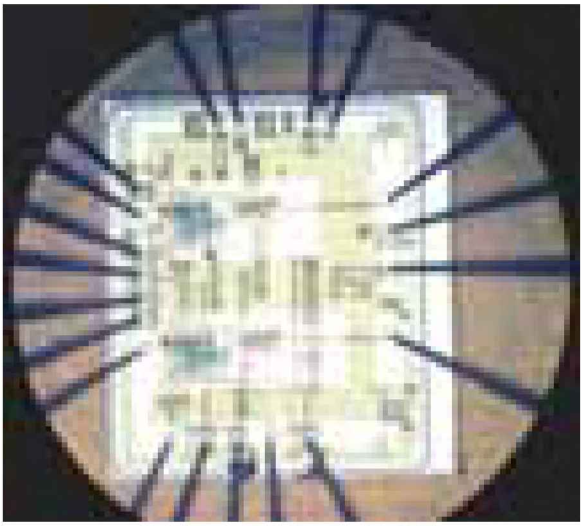
Discussion Questions

1. Why is sensitivity of best multimeter not more than 20 kΩ per volt ?
2. Why do we generally prefer *VTVM* to multimeter for measurements in electronic circuits ?
3. Why does oscilloscope give more accurate measurements than a *VTVM* ?
4. What is the basic difference between vacuum tubes and cathode ray tube ?
5. How can a multimeter be used for continuity checking ?
6. Which would usually have more linear scales, dc or ac meters ?
7. Which is more sensitive, a 0 – 59 μA or a 0 – 1 mA meter ?
8. On a multirange ohmmeter, where is 0 Ω mark ?
9. What component prevents meter damage in a *VTVM*?
10. Could a 0 – 1 mA-movement 100 – V voltmeter and a 0 – 50 μA – movement 100 – V voltmeter be used in series across 125 V ?

23

Integrated Circuits

23.1 Integrated Circuit
23.2 Advantages and Disadvantages of Integrated Circuits
23.3 Inside an IC Package
23.4 IC Classifications
23.5 Making Monolithic IC
23.6 Fabrication of Components on Monolithic IC
23.7 Simple Monolithic *ICs*
23.8 *IC* Packings
23.9 *IC* Symbols
23.10 Scale of Integration
23.11 Some Circuits Using ICs



INTRODUCTION

The circuits discussed so far in the text consisted of separately manufactured components (*e.g.* resistors, capacitors, diodes, transistors *etc.*) joined by wires or plated conductors on printed boards. Such circuits are known as *discrete circuits* because each component added to the circuit is discrete (*i.e.* distinct or separate) from the others. Discrete circuits have two main disadvantages. Firstly, in a large circuit (*e.g.* TV circuit, computer circuit) there may be hundreds of components and consequently discrete assembly would occupy a large space. Secondly, there will be hundreds of soldered points posing a considerable problem of reliability. To meet these problems of space conservation and reliability, engineers started a drive for miniaturized circuits. This led to the development of *microelectronics* in the late 1950*s*.

Microelectronics is the branch of electronics engineering which deals with micro-circuits. A micro-circuit is simply a miniature assembly of electronic components. One type of such circuit is the *integrated circuit*, generally abbreviated as *IC*. An integrated circuit has various components such as resistors, capacitors, diodes, transistors etc. fabricated on a small semiconductor chip. How circuits containing hundreds of components are fabricated on a small semiconductor chip to produce an *IC* is a fascinating feat of microelectronics. This has not only fulfilled the everincreasing demand of industries for electronic equipment of smaller size, lighter weight and low power requirements, but it has also resulted in high degree of reliability. In this chapter, we shall focus our attention on the various aspects of integrated circuits.

23.1 Integrated Circuit

An **integrated circuit** *is one in which circuit components such as transistors, diodes, resistors, capacitors etc. are automatically part of a small semiconductor chip.*

An integrated circuit consists of a number of circuit components (*e.g.* transistors, diodes, resistors etc.) and their inter connections in a single small package to perform a complete electronic function. These components are formed and connected within a small chip of semiconductor material. The following points are worth noting about integrated circuits :

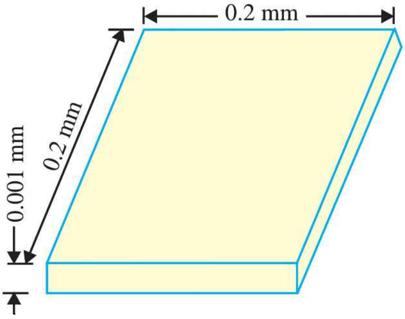


Fig. 23.1

(*i*) In an *IC*, the various components are automatically part of a small semi-conductor chip and the individual components cannot be removed or replaced. This is in contrast to discrete assembly in which individual components can be removed or replaced if necessary.

(*ii*) The size of an **IC* is extremely small. In fact, *ICs* are so small that you normally need a microscope to see the connections between the components. Fig. 23.1 shows a typical semi-conductor chip having dimensions 0.2 mm × 0.2 mm × 0.001 mm. It is possible to produce circuits containing many transistors, diodes, resistors etc. on the surface of this small chip.

(*iii*) No components of an *IC* are seen to project above the surface of the chip. This is because all the components are formed within the chip.

23.2 Advantages and Disadvantages of Integrated Circuits

Integrated circuits free the equipment designer from the need to construct circuits with individual discrete components such as transistors, diodes and resistors. With the exception of a few very simple circuits, the availability of a large number of low-cost integrated circuits have largely rendered discrete circuitry obsolete. It is, therefore, desirable to mention the significant advantages of integrated circuits over discrete circuits. However, integrated circuits have some disadvantages and continuous efforts are on to overcome them.

Integrated circuits

Advantages : Integrated circuits possess the following advantages over discrete circuits :

(*i*) Increased reliability due to lesser number of connections.

(*ii*) Extremely small size due to the fabrication of various circuit elements in a single chip of semi-conductor material.

(*iii*) Lesser weight and **space requirement due to miniaturized circuit.

---

* Since it combines both active (*e.g.*, transistors, diodes etc.) and passive elements (*e.g.*, resistors, capacitors etc.) in a monolithic structure, the complete unit is called an integrated circuit.

** Typically, this is about 10% of the space required by comparable discrete assembly.

(*iv*) Low power requirements.

(*v*) Greater ability to operate at extreme values of temperature.

(*vi*) Low cost because of simultaneous production of hundreds of alike circuits on a small semi-conductor wafer.

(*vii*) The circuit lay out is greatly simplified because integrated circuits are constrained to use minimum number of external connections.

Disadvantages : The disadvantages of integrated circuits are :

(*i*) If any component in an *IC* goes out of order, the whole *IC* has to be replaced by the new one.

(*ii*) In an *IC*, it is neither convenient nor economical to fabricate capacitances exceeding 30 *pF*. Therefore, for high values of capacitance, discrete components exterior to *IC* chip are connected.

(*iii*) It is not possible to fabricate inductors and transformers on the surface of semi-conductor chip. Therefore, these components are connected exterior to the semi-conductor chip.

(*iv*) It is not possible to produce high power *ICs* (greater than 10 W).

(*v*) There is a lack of flexibility in an *IC* *i.e.*, it is generally not possible to modify the parameters within which an integrated circuit will operate.

23.3 Inside an IC Package

The *IC* units are fast replacing the discrete components in all electronic equipment. These are similar to the discrete circuits that they replaced. However, there are some points to be noted. An integrated circuit (*IC*) usually contains only transistors, diodes and resistors. It is usually very difficult to form inductors in an *IC*. Also, only very small capacitors, in the picofarad range, can be included. When inductors and large values of *C* are needed, they are connected externally to an *IC*. The various components in an *IC* are so small that they cannot be seen with a naked eye. Therefore, individual components cannot be removed or replaced. If a single component within an *IC* fails, the complete *IC* is replaced. When studying circuits using *IC*s, we are more concerned with the external connections to the *IC*s than with what is actually going on inside. We cannot get into an *IC* to repair its internal circuitry.

23.4 IC Classifications

Four basic types of constructions are employed in the manufacture of integrated circuits, namely ;

(*i*) mono-lithic (*ii*) thin-film (*iii*) thick-film (*iv*) hybrid.

Monolithic *ICs* are by far the most common type used in practice. Therefore, in this chapter we shall confine our attention to the construction of this type of *ICs* only. It may be worthwhile to mention here that regardless of the type of method used to fabricate active and passive components, the basic characteristics and circuit operation of an *IC* are the same as for any of their counterparts in a similar circuit using separate circuit components.

23.5 Making Monolithic IC

A **monolithic IC** *is one in which all circuit components and their inter-connections are formed on a single thin wafer called the substrate.*

The word monolithic is from Greek and means "one stone." The word is appropriate because all the components are part of one chip. Although we are mainly interested in using *ICs*, yet it is profitable to know something about their fabrication. The basic production processes for the monolithic *ICs* are as follow :

(*i*) **p-Substrate.** This is the first step in the making of an *IC*. A cylindrical *p*-type *silicon crystal is grown having typical dimensions 25 cm long and 2.5 cm diameter [See Fig. 23.2 (*i*)]. The crystal is then cut by a diamond saw into many thin wafers like Fig. 23.2 (*ii*), the typical thickness of the wafer being 200 μm. One side of wafer is polished to get rid of surface imperfections. This wafer is called the substrate. The *ICs* are produced on this wafer.

---

* Since silicon possesses characteristics which are best suited to *IC* manufacturing processes.

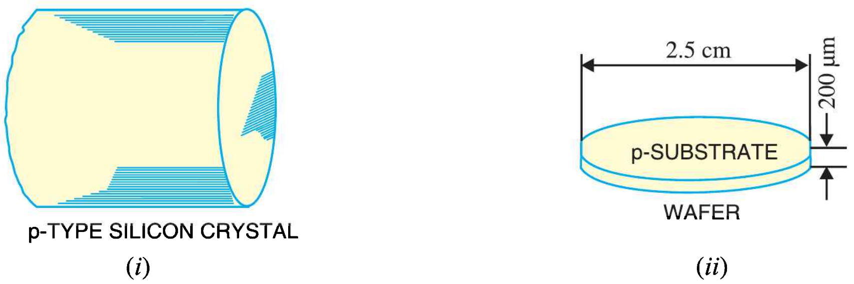


Fig. 23.2

(*ii*) **Epitaxial n layer.** The next step is to put the wafers in a diffusion furnace. A gas mixture of silicon atoms and pentavalent atoms is passed over the wafers. This forms a thin layer of *n*-type semi-conductor on the heated surface of substrate [See Fig. 23.3 (*i*)]. This thin layer is called the **epitaxial layer* and is about 10 μm thick. It is in this layer that the whole integrated circuit is formed.

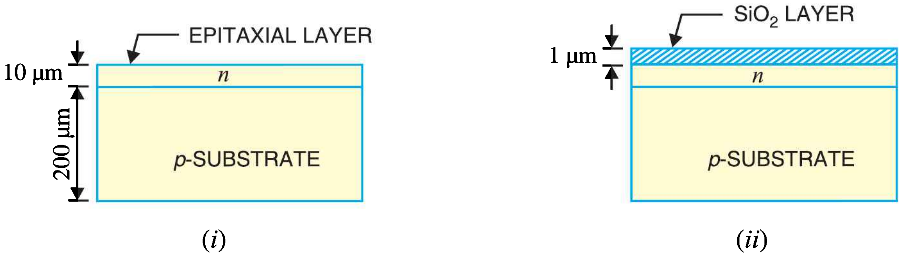


Fig. 23.3

(*iii*) **Insulating layer.** In order to prevent the contamination of the epitaxial layer, a thin SiO_2 layer about 1μm thick is deposited over the entire surface as shown in Fig. 23.3 (*ii*). This is achieved by passing pure oxygen over the epitaxial layer. The oxygen atoms combine with silicon atoms to form a layer of silicon dioxide (SiO_2).

(*iv*) **Producing components.** By the process of **diffusion, appropriate materials are added to the substrate at specific locations to produce diodes, transistors, resistors and capacitors. The production of these components on the wafer is discussed in Art 23.6.

(*v*) **Etching.** Before any impurity is added to the substrate, the oxide layer (*i.e.* SiO_2 layer) is etched. The process of etching exposes the epitaxial layer and permits the production of desired components. The terminals are processed by etching the oxide layer at the desired locations.

(*vi*) **Chips.** In practice, the wafer shown in Fig. 23.4 is divided into a large number of areas. Each of these areas will be a separate chip. The manufacturer produces hundreds of alike *ICs* on the wafer over each area. To separate the individual *ICs*, the

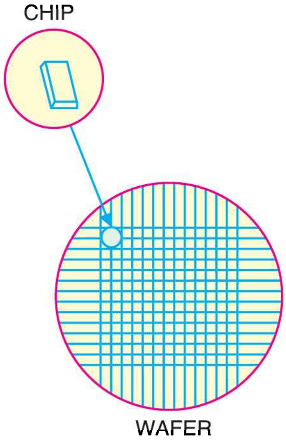


Fig. 23.4

---

* The word "epitaxial" is derived from the Greek language and means arranged upon.

** In *IC* construction, diffusion is the process of deliberately adding controlled impurities at specific locations of substrate by thermal processes.

wafer is divided into small chips by a process similar to glass cutting. This is illustrated in Fig. 23.4. It may be seen that hundreds of alike *ICs* can be produced from a small wafer. This simultaneous mass production is the reason for the low cost of integrated circuits.

After the chip is cut, it is bonded to its mounting and connections are made between the *IC* and external leads. The *IC* is then encapsulated to prevent it from becoming contaminated by the surrounding atmosphere.

23.6 Fabrication of Components on Monolithic IC

The notable feature of an *IC* is that it comprises a number of circuit elements inseparably associated in a single small package to perform a complete electronic function. This differs from discrete assembly where separately manufactured components are joined by wires. We shall now see how various circuit elements (*e.g.* diodes, transistors, resistors etc.) can be constructed in an *IC* form.

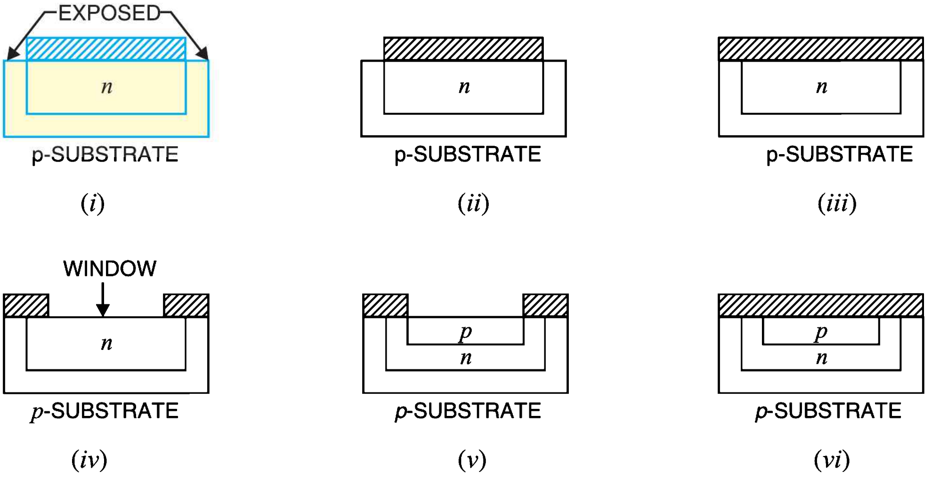
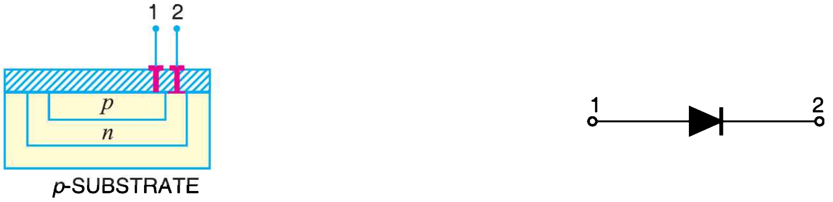


Fig. 23.5

(*i*) **Diodes.** One or more diodes are formed by diffusing one or more small *n*-type deposits at appropriate locations on the substrate. Fig. 23.5 shows how a diode is formed on a portion of substrate of a monolithic *IC*. Part of SiO_2 layer is etched off, exposing the epitaxial layer as shown in Fig. 23.5 (*i*). The wafer is then put into a furnace and trivalent atoms are diffused into the epitaxial layer. The trivalent atoms change the exposed epitaxial layer from *n*-type semi-conductor to *p*-type. Thus we get an island of *n*-type material under the SiO_2 layer as shown in Fig. 23.5 (*ii*).

Next pure oxygen is passed over the wafer to form a complete SiO_2 layer as shown in Fig. 23.5 (*iii*). A hole is then etched at the centre of this layer ; thus exposing the *n*-epitaxial layer [See Fig. 23.5 (*iv*)]. This hole in SiO_2 layer is called a **window**. Now we pass trivalent atoms through the window. The trivalent atoms diffuse into the epitaxial layer to form an island of *p*-type material as shown in Fig. 23.5 (*v*). The SiO_2 layer is again formed on the wafer by blowing pure oxygen over the wafer [See Fig. 23.5 (*vi*)]. Thus a *p-n* junction diode is formed on the substrate.

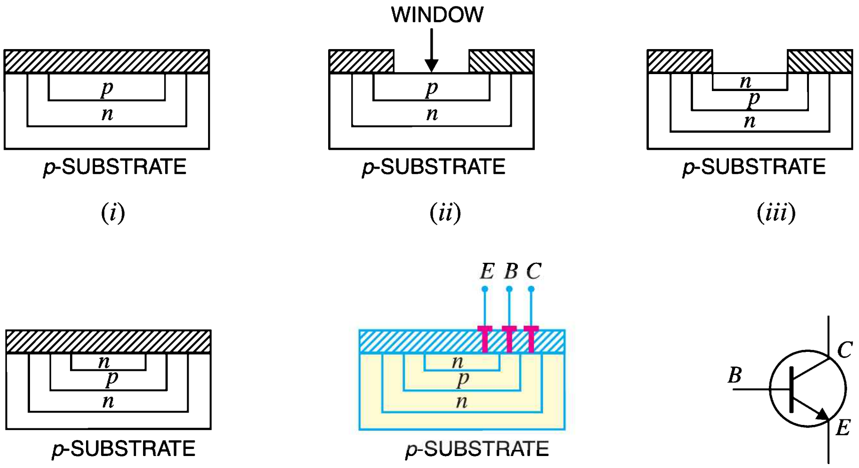
The last step is to attach the terminals. For this purpose, we etch the SiO_2 layer at the desired locations as shown in Fig 23.6 (*i*). By depositing metal at these locations, we make electrical contact with the anode and cathode of the integrated diode. Fig. 23.6 (*ii*) shows the electrical circuit of the diode.



(*i*) (*ii*)

Fig. 23.6

(*ii*) Transistors. Transistors are formed by using the same principle as for diodes. Fig. 23.7 shows how a transistor is formed on a portion of the substrate of a monolithic *IC*. For this purpose, the steps used for fabricating the diode are carried out upto the point where *p* island has been formed and sealed off [See Fig. 23.5 (*vi*) above]. This Fig. is repeated as Fig. 23.7 (*i*) and shall be taken as the starting point in order to avoid repetition.



(*i*) (*ii*) (*iii*)

(*iv*) (*v*) (*vi*)

Fig. 23.7

A window is now formed at the centre of SiO_2 layer, thus exposing the *p*-epitaxial layer as shown in Fig. 23.7(*ii*). Then we pass pentavalent atoms through the window. The pentavalent atoms diffuse into the epitaxial layer to form an island of *n*-type material as shown in Fig. 23.7 (*iii*). The SiO_2 layer is re-formed over the wafer by passing pure oxygen [See Fig. 23.7 (*iv*)]. The terminals are processed by etching the SiO_2 layer at appropriate locations and depositing the metal at these locations as shown in Fig. 23.7 (*v*). In this way, we get the integrated transistor. Fig. 23.7 (*vi*) shows the electrical circuit of a transistor.

(*iii*) Resistors. Fig. 23.8 shows how a resistor is formed on a portion of the substrate of a monolithic *IC*. For this purpose, the steps used for fabricating diode are carried out upto the point where *n* island has been formed and sealed off [Refer back to Fig. 23.5 (*iii*)]. This figure is repeated as Fig. 23.8 (*i*) and shall be taken as the starting point in order to avoid repetition.

A window is now formed at the centre of SiO_2 layer, thus exposing the *n*-epitaxial layer as shown in Fig. 23.8 (*ii*). Then we diffuse a *p*-type material into the *n*-type area as shown in Fig. 23.8 (*iii*). The SiO_2 layer is re-formed over the wafer by passing pure oxygen [See Fig. 23.8 (*iv*)]. The terminals are processed by etching SiO_2 layer at two points above the *p* island and depositing the metal at these locations [See Fig. 23.8 (*v*)]. In this way, we get an integrated resistor. Fig. 23.8 (*vi*) shows the electrical circuit of a resistor.

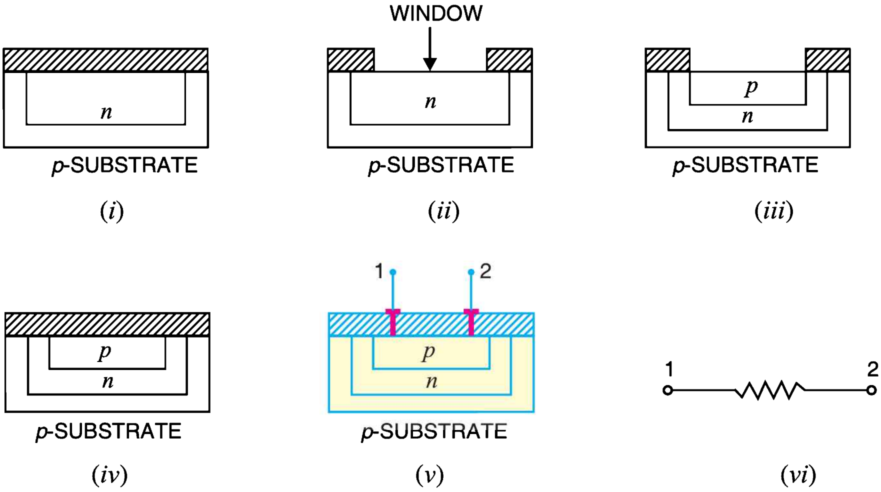


Fig. 23.8

The value of resistor is determined by the material, its length and area of cross-section. The high-resistance resistors are long and narrow while low-resistance resistors are short and of greater cross-section.

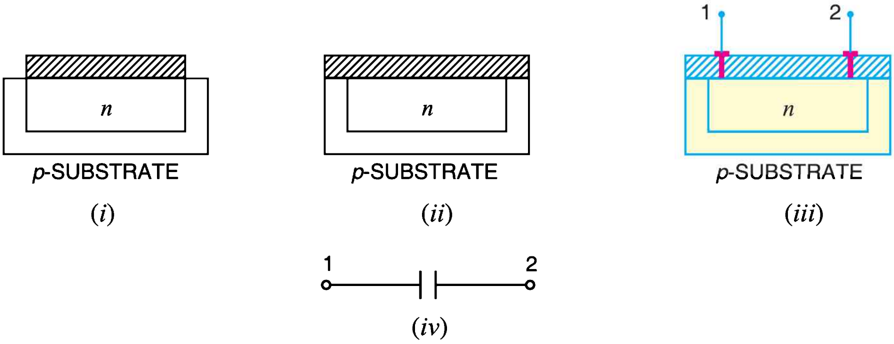


Fig. 23.9

***(iv)* Capacitors.** Fig. 23.9 shows the process of fabricating a capacitor in the monolithic *IC*. The first step is to diffuse an *n*-type material into the substrate which forms one plate of the capacitor as shown in Fig. 23.9 (*i*). Then SiO_2 layer is re-formed over the wafer by passing pure oxygen as shown in Fig. 23.9 (*ii*).

The SiO_2 layer formed acts as the dielectric of the capacitor. The oxide layer is etched and terminal 1 is added as shown in Fig. 23.9 (*iii*). Next a large (compared to the electrode at terminal 1) metallic electrode is deposited on the SiO_2 layer and forms the second plate of the capacitor. The oxide layer is etched and terminal 2 is added. This gives an integrated capacitor. The value of capacitor formed depends upon the dielectric constant of SiO_2 layer, thickness of SiO_2 layer and the area of cross-section of the smaller of the two electrodes.

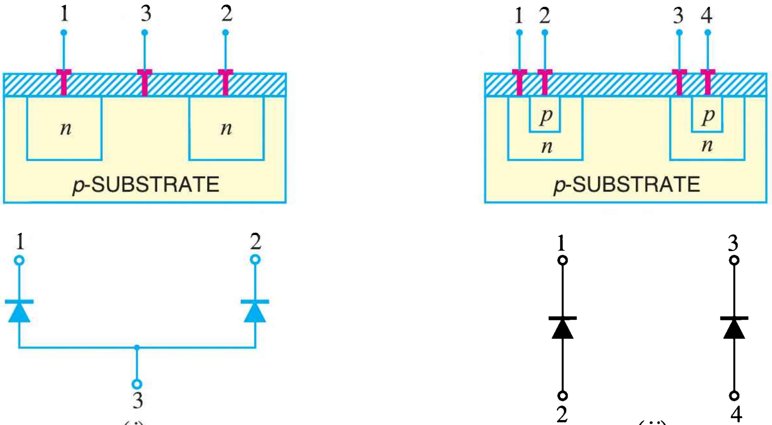
23.7 Simple Monolithic *ICs*

It has been seen above that individual components can be integrated in a monolithic *IC*. We shall now see how an electronic circuit comprising different components is produced in an *IC* form. The key point to keep in mind is that regardless of the complexity of the circuit, it is mainly a process of etching windows, forming *p* and *n* islands, and connecting the integrated components.

(*i*) **Two-diode IC.** Fig. 23.10 (*i*) shows a two-diode *IC* with a common anode whereas Fig. 23.10 (*ii*) shows a two-diode *IC* with individual anode.

Two points are worth noting. Firstly, any circuit [like the one shown in Fig 23.10 (*i*) or Fig 23.10 (*ii*)] is not integrated individually ; rather hundreds of alike circuits are simultaneously fabricated on a wafer. The wafer is then cut into chips so that each chip area represents one circuit. This is the key factor for low cost of *ICs* and is exerting considerable influence on electronics engineers to switch over to *IC* technology. Secondly, *ICs* are usually not as simple as shown in Fig. 23.10. In fact, actual *ICs* contain a large number of components.

Monolithic IC



(*i*) (*ii*)

Fig. 23.10

(*ii*) **Another simple IC.** Fig.23.11 shows an *IC* consisting of a capacitor, resistor, diode and transistor connected in series. The interconnection of the circuit elements is accomplished by extending the metallic deposits from terminal to terminal of adjacent components.

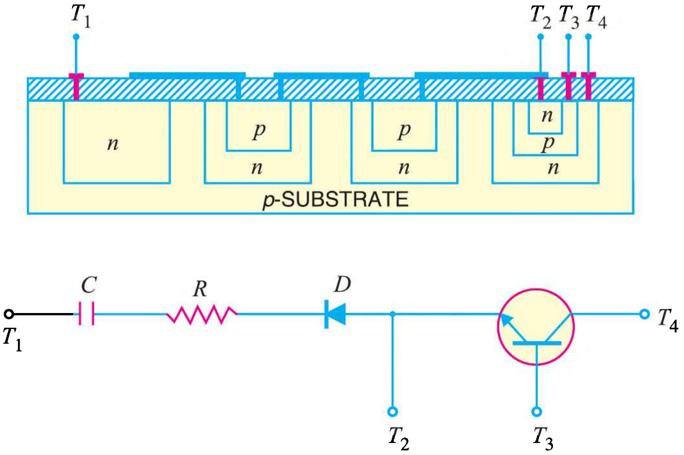
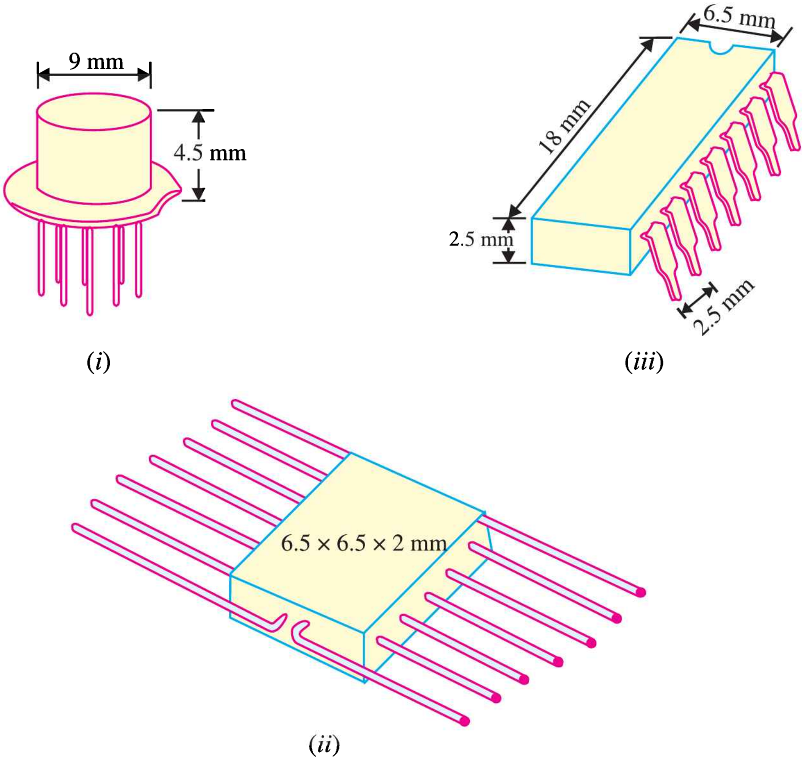


Fig. 23.11

It is interesting to see that p substrate isolates the integrated components from each other. Thus referring to Fig. 23.11, depletion layers exist between p substrate and the four n islands touching it. As the depletion layers have virtually no current carriers, therefore, the integrated components are insulated from each other.

23.8 *IC* Packings

In order to protect *ICs* from external environment and to provide mechanical protection, various forms of encapsulation are used for integrated circuits. Just as with semi-conductor devices, *IC* packages are of two types *viz.*



(*i*) (*iii*)

(*ii*)

Fig. 23.12

(***i***) hermatic (metal or ceramic with glass) (***ii***) non-hermatic (plastics)

Plastics are cheaper than hermatic but are still not regarded as satisfactory in extremes of temperature and humidity. Although *ICs* appeared in the market several years ago, yet the standardisation of packages started only in the recent years. The three most popular types of *IC* packages are shown in Fig. 23.12.

(***i***) Fig. 23.12 (*i*) shows *TO-5 package** which resembles a small signal transistor in both appearance and size but differs in that it has either 8, 10 or 12 pigtail-type leads. The close leads spacing and the difficulty of removal from a printed circuit board has diminished the popularity of this package with the users.

(***ii***) Fig. 23.12 (*ii*) shows a *flat pack* container with 14 leads, seven on each side.

(***iii***) Fig. 23.12 (*iii*) shows the *dual-in-line* (**DIL**) pack in 14-lead version. The 14-pin DIL is the most popular form and has seven connecting pairs per side. The pairs of pins of this pack are in line with one another, the pins being 2.5 mm apart to allow *IC* to be fitted directly into the standard printed circuit boards.

---

* This was the earliest type of package and it was natural for the semi-conductor manufactures to use modified transistor cases.

23.9 *IC* Symbols

In general, no standard symbols exist for *ICs*. Often the circuit diagram merely shows a block with numbered terminals. However, sometimes standard symbols are used for operational amplifiers or digital logic gates. Some of the symbols used with *ICs* are shown below.

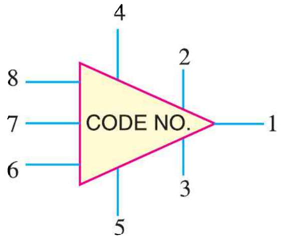


Fig. 23.13

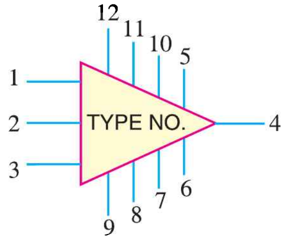


Fig. 23.14

Fig. 23.13 shows the symbol of an *IC r-f* amplifier containing 3 transistors, 3 resistors and 8 terminals. Similarly, Fig. 23.14 shows an *IC* audio amplifier which contain 6 transistors, 2 diodes, 17 resistors and has 12 terminals.

23.10 Scale of Integration

An *IC* chip may contain as large as 100,000 semiconductor devices or other components. The relative number of these components within the chip is given by referring to its scale of integration. The following terminology is commonly used.

Scale of integration	Abbreviation	Number of components
Small	*SSI	1 to 20
Medium	MSI	20 to 100
Large	LSI	100 to 1000
Very large	VLSI	1000 to 10,000
Super large	SLSI	10,000 to 100,000

23.11 Some Circuits Using ICs

Integrated circuits are fairly complex because they contain a large number of circuit components within a small semiconductor chip. While studying circuits using *ICs*, we are more concerned with the external connections to the *IC* rather than what is actually going on inside.

(*i*) **IC Fixed 5-volt Voltage Regulator.** The *IC* voltage regulator is a device that is used to hold the output voltage from a dc power supply constant as the input voltage or load current changes. For example, LM 309 (fixed postive) provides a + 5 V d.c. output. This regulator is frequently used in digital circuits. Fig. 23.15 shows the circuit of the voltage regulator using LM 309. It is a three terminal device with terminals labelled as input, output and ground terminal. It provides a fixed 5 V between the output and ground terminals.

---

* SSI stands for small scale integration.

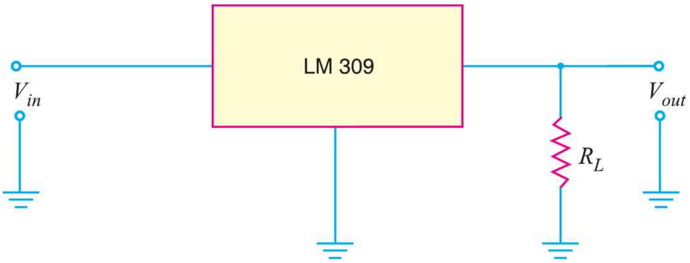


Fig. 23.15

The LM 309 has a number of advantages over the zener diode. First, it is much more accurate than the zener diode. Secondly, there is built-in overload protection. The LM 309 also has overheating protection. If the internal temperature becomes excessive, it shuts off until the temperature is reduced, at which point it will start up again.

(*ii*) **IC Adjustable Voltage Regulator.** Sometimes, we want a voltage regulator whose voltage we can vary. An example of such a voltage regulator is LM 317 whose schematic diagram is shown in Fig. 23.16. By varying the value of R_2, the output voltage of the regulator can be adjusted. The following equation is used to determine the regulated d.c. output voltage for an LM 317 regulator circuit :

$$V_{out} = 1.25\left(\frac{R_2}{R_1} + 1\right)$$

Example 23.1. *In LM 317 voltage regulator shown in Fig. 23.16, R_2 is adjusted to 2.4 kΩ. If the value of R_1 is 240 Ω, determine the regulated d.c. output voltage for the circuit.*

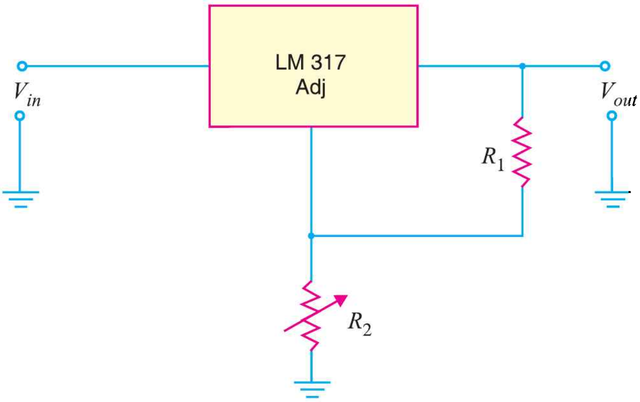


Fig. 23.16

Solution.

$$V_{out} = 1.25\left(\frac{R_2}{R_1} + 1\right)$$

$$= 1.25\left(\frac{2.4\ \text{k}\Omega}{240\ \Omega} + 1\right) = \mathbf{13.75\ V}$$

(*iii*) **The 555 Timer as monostable multivibrator.** Fig. 23.17 shows the circuit of the 555 timer as a monostable multivibrator. The R and C are the external components whose values determine the time T (in seconds) for which the circuit is on. This time is given by ;

$$T = 1.1\ RC$$

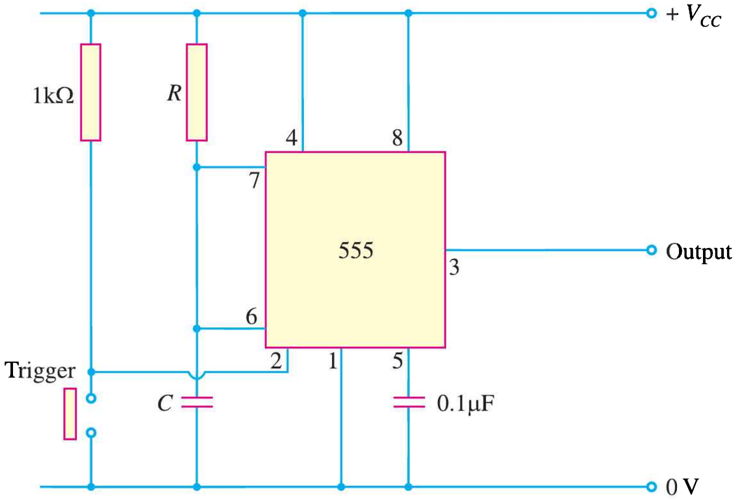

+ V_{CC}
1kΩ
R
4
8
7
555
Output
3
6
Trigger
2
1
5
C
0.1μF
0 V

Fig. 23.17

Example 23.2. *The monostable multivibrator like the one in Fig. 23.17 has the values of R = 1.2 kΩ and C = 0.1 μF. Determine the time T for which the circuit is on.*

Solution. The time T for which the circuit is on is given by ;

$$T = 1.1\,RC = 1.1(1.2 \times 10^{3})\,(0.1 \times 10^{-6})$$

$$= 132 \times 10^{-6}\text{s} = \mathbf{132\ \mu s}$$

(*iv*) The 555 Timer as astable multivibrator. Fig. 23.18 shows the 555 timer as an astable multibrator. Note that the circuit contains *two resistors (R_1 and R_2) and one capacitor (C)* and *does not have an input from any other circuit.* The lack of a triggering signal from an external source is the circuit recognition feature of the astable multivibrator.

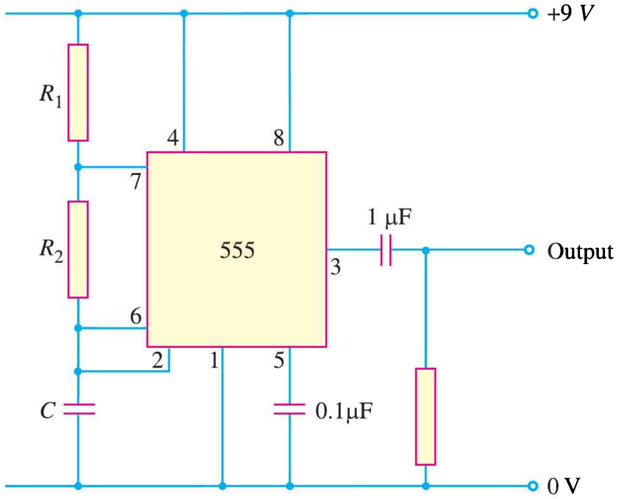

+9 V
R_1
4
8
7
1 μF
R_2
555
3
Output
6
2
1
5
C
0.1μF
0 V

Fig. 23.18

The time T_1 for which the output is 'high' is given by ;

$$T_1 = 0.694\,(R_1 + R_2)\,C$$

The time T_2 for which the output is 'low' is given by ;

$$T_2 = 0.694\, R_2C$$

∴ Total period T for the oscillation is

$$T = T_1 + T_2 = 0.694\,(R_1 + 2\,R_2)\,C$$

The frequency f of the astable multivibrator is given by ;

$$f = \frac{1}{T} = \frac{1}{0.694\,(R_1 + 2R_2)\,C} = \frac{1.44}{(R_1 + 2R_2)\,C}$$

Note that f will be in Hz if resistance is in ohms and capacitance in farads.

Example 23.3. *Determine the frequency of the circuit shown in Fig. 23.18. Given that $R_1 = 3\ k\Omega$; $R_2 = 2.7\ k\Omega$ and $C = 0.033\ \mu F$.*

Solution. The frequency of the circuit is given by ;

$$f = \frac{1.44}{(R_1 + 2R_2)\,C}$$

Here
$$R_1 + 2R_2 = 3\ \text{k}\Omega + 2 \times 2.7\ \text{k}\Omega = 8.4 \times 10^3\Omega\ ;$$
$$C = 0.033\ \mu\text{F} = 0.033 \times 10^{-6}\ \text{F}$$

∴
$$f = \frac{1.44}{(8\cdot4 \times 10^3)\,(0.033 \times 10^{-6})} = 5.19 \times 10^3\ \text{Hz} = \mathbf{5.19\ kHz}$$

(*v*) Op-Amp Half-wave Rectifier. Fig. 23.19 shows the half-wave rectifier using an *Op-Amp. The use of Op-Amp greatly reduces the effect of diode offset voltage and allows the circuit to be used in the millivolt region.

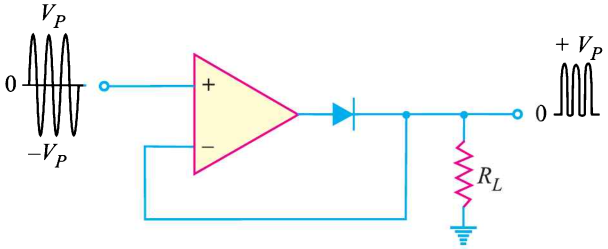


Fig. 23.19

When the input signal goes positive, the output of Op-Amp goes positive and turns on the diode. The circuit then acts like a voltage follower and the positive half-cycle appears across the load resistor R_L. On the other hand, when the input goes negative, the Op-Amp output goes negative and turns off the diode. Since the diode is open, no voltage appears across the load resistor R_L. Therefore, the voltage across R_L is almost a perfect half-wave signal.

(*vi*) Logarithmic amplifier. A *logarithmic amplifier* produces an output voltage that is proportional to the logarithm of the input voltage. If you place a **diode in the feedback loop of an Op-Amp as shown in Fig. 23.20, you have a log amplifier. The output is limited to a maximum value of about 0.7V because the diodes logarithmic characteristic is limited to voltages below 0.7V.

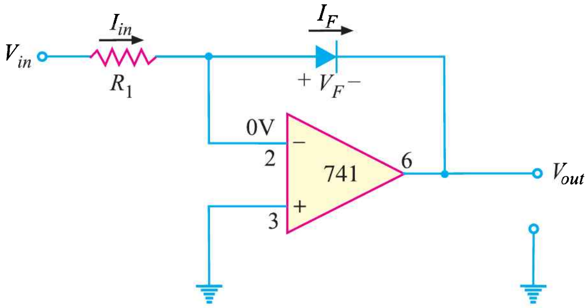


Fig. 23.20

---

* Now-a-days, Op-Amp is produced as an *IC*.

** The forward characteristic of a diode is logarithmic upto a forward voltage of about 0.7V.

Also, the input must be positive when the diode is connected in the direction shown in Fig. 23.20. To handle negative inputs, you should reverse the direction of the diode. It can be shown that the output voltage of the circuit shown is given by ;

$$V_{out} = -(0.025\text{ V})\log_e\left(\frac{V_{in}}{I_R\,R_1}\right)$$

where I_R = reverse leakage current of the diode

For example, if $V_{in} = +2$ V, $R_1 = 100$ kΩ and $I_R = 50$ nA, then,

$$V_{out} = -(0.025)\log_e\left(\frac{2V}{(50\times10^{-9})\,(100\times10^3)}\right)$$

$$= -(0.025)\log_e(400) = -0.15\text{ V}$$

(*vii*) Constant-current source. A constant current source delivers a load current I_L that remains constant when the load resistance R_L changes. Fig. 23.21 shows the basic circuit of a constant current source. Since the inverting (–) input of the Op-Amp is at virtual ground (0V), the value of I_i is determined by V_{in} and R_i *i.e.*

$$I_i = \frac{V_{in}}{R_i}$$

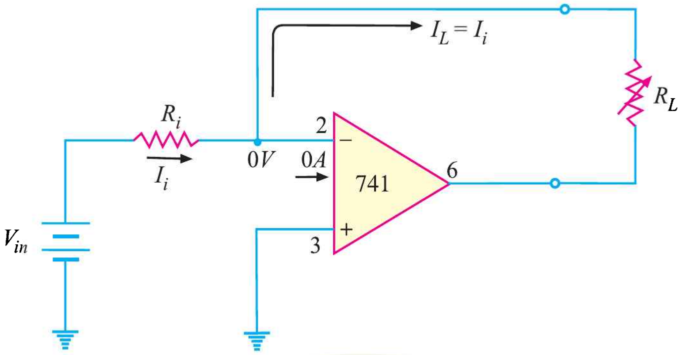


Fig. 23.21

The internal impedance of Op-Amp is extremely high (ideally infinite) so that practically all of I_i flows through R_L. Since $I_i = I_L$,

$$\therefore \quad I_L = \frac{V_{in}}{R_i}$$

Note that load resistance R_L does not appear in this equation. Therefore, the load current (I_L) is independent of load resistance R_L. If R_L changes, I_L remains constant as long as V_{in} and R_i are held constant. In other words, the load is driven by a constant current source.

MULTIPLE-CHOICE QUESTIONS

1. An *IC* has .... size.

(*i*) very large
(*ii*) large
(*iii*) extremely small
(*iv*) none of the above

2. *ICs* are generally made of ....

(*i*) silicon (*ii*) germanium
(*iii*) copper (*iv*) none of the above

3. .... *ICs* are the most commonly used.

(*i*) thin film (*ii*) monolithic
(*iii*) hybrid (*iv*) none of the above

4. The most popular form of *IC* package is ....

(*i*) DIL (*ii*) flatpack
(*iii*) TO-5 (*iv*) none of the above

5. .... cannot be fabricated on an *IC*.

(*i*) transistors (*ii*) diodes
(*iii*) resistors
(*iv*) large inductors and transformers

6. An audio amplifier is an example of ....

(*i*) digital *IC* (*ii*) linear *IC*
(*iii*) both digitial and linear *IC*
(*iv*) none of the above

7. The active components in an *IC* are ....

(*i*) resistors (*ii*) capacitors
(*iii*) transistors and diodes
(*iv*) none of the above

8. We use .... *ICs* in computers.

(*i*) digital (*ii*) linear
(*iii*) both digital and linear
(*iv*) none of the above

9. The SiO_2 layer in an *IC* acts as ....

(*i*) a resistor
(*ii*) an insulating layer
(*iii*) mechanical output
(*iv*) none of the above

10. *ICs* are used in ....

(*i*) linear devices only
(*ii*) digital devices only
(*iii*) both linear and digital devices
(*iv*) none of the above

11. A transistor takes .... inductor on a silicon *IC* chip.

(*i*) less space than
(*ii*) more space than
(*iii*) same space as (*iv*) none of the above

12. The most popular types of *ICs* are ....

(*i*) thin-film (*ii*) hybrid
(*iii*) thick-film (*iv*) monolithic

13. Digital *ICs* process ....

(*i*) linear signals only
(*ii*) digital signals only
(*iii*) both digital and linear signals
(*iv*) none of the above

14. Operational amplifiers use ....

(*i*) linear *ICs* (*ii*) digital *ICs*
(*iii*) both linear and digital *ICs*
(*iv*) none of the above

15. Which of the following is most difficult to fabricate in an *IC* ?

(*i*) diode (*ii*) transistor
(*iii*) *FET* (*iv*) capacitor

Answers to Multiple-Choice Questions

1.	(*iii*)	**2.**	(*i*)	**3.**	(*ii*)	**4.**	(*ii*)	**5.**	(*iv*)
6.	(*ii*)	**7.**	(*iii*)	**8.**	(*i*)	**9.**	(*ii*)	**10.**	(*iii*)
11.	(*i*)	**12.**	(*iv*)	**13.**	(*iii*)	**14.**	(*ii*)	**15.**	(*iv*)

Chapter Review Topics

1. What is an integrated circuit ? Discuss the relative advantages and disadvantages of *ICs* over discrete assembly.
2. How will you make a monolithic *IC* ?
3. Explain how (*i*) a diode (*ii*) a transistor (*iii*) a resistor and (*iv*) a capacitor can be constructed in a monolithic integrated circuit.
4. Explain how electronic circuit consisting of different components can be constructed in a monolithic *IC*.
5. Write short notes on the following :
   (*i*) Epitaxial layer (*ii*) *IC* packages (*iii*) *IC* symbols

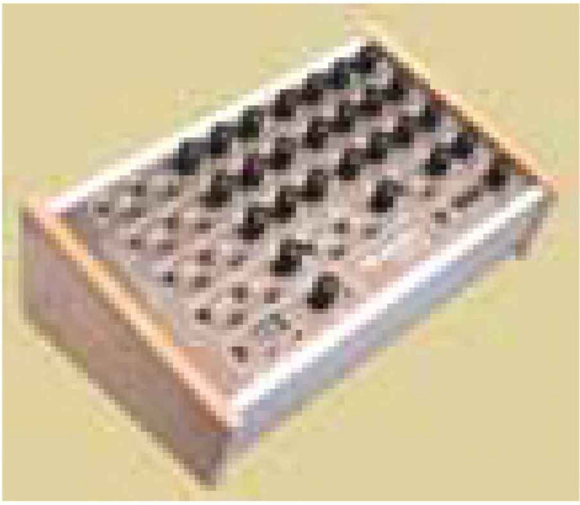
Discussion Questions

1. Why are *ICs* so cheap ?
2. Why do *ICs* require low power ?
3. Why cannot we produce *ICs* of greater power ?
4. Why are *ICs* more reliable than discrete assembly ?
5. Why is DIL *IC* package the most popular ?

24

Hybrid Parameters

24.1 Hybrid Parameters
24.2 Determination of *h* Parameters
24.3 *h* Parameter Equivalent Circuit
24.4 Performance of a Linear Circuit in *h* Parameters
24.5 The *h* Parameters of a Transistor
24.6 Nomenclature for Transistor *h* Parameters
24.7 Transistor Circuit Performance in *h* Parameters
24.8 Approximate Hybrid Formulas for Transistor Amplifier
24.9 Experimental Determination of Transistor *h* Parameters
24.10 Limitations of *h* Parameters



INTRODUCTION

In order to predict the behaviour of a small-signal transistor amplifier, it is important to know its operating characteristics *e.g.*, input impedance, output impedance, voltage gain *etc.* In the text so far, these characteristics were determined by using *β and circuit resistance values. This method of analysis has two principal advantages. Firstly, the values of circuit components are readily available and secondly the procedure followed is easily understood. However, the major drawback of this method is that accurate results cannot be obtained. It is because the input and output circuits of a transistor amplifier are not completely independent. For example, output current is affected by the value of load resistance rather than being constant at the value βI_b. Similarly, output voltage has an effect on the input circuit so that changes in the output cause changes in the input.

---

* Since transistor is generally connected in *CE* arrangement, current amplification factor β is mentioned here.

One of the methods that takes into account all the effects in a transistor amplifier is the hybrid parameter approach. In this method, four parameters (one measured in ohm, one in mho, two dimensionless) of a transistor are measured experimentally. These are called hybrid or *h* parameters of the transistor. Once these parameters for a transistor are known, formulas can be developed for input impedance, voltage gain etc.in terms of *h* parameters. There are two main reasons for using *h* parameter method in describing the characteristics of a transistor. Firstly, it yields exact results because the inter-effects of input and output circuits are taken into account. Secondly, these parameters can be measured very easily. To begin with, we shall apply *h* parameter approach to general circuits and then extend it to transistor amplifiers.

24.1 Hybrid Parameters

*Every *linear circuit having input and output terminals can be analysed by four parameters (one measured in ohm, one in mho and two dimensionless) called* **hybrid** *or* ***h*** **Parameters.**

Hybrid means "mixed". Since these parameters have mixed dimensions, they are called hybrid parameters. Consider a linear circuit shown in Fig. 24.1. This circuit has input voltage and current labelled v_1 and i_1. This circuit also has output voltage and current labelled v_2 and i_2. Note that both input and output currents (i_1 and i_2) are assumed to flow *into* the box ; input and output voltages (v_1 and v_2) are assumed *positive* from the upper to the lower terminals. These are standard conventions and do not necessarily correspond to the actual directions and polarities. When we analyse circuits in which the voltages are of opposite polarity or where the currents flow out of the box, we simply treat these voltages and currents as negative quantities.

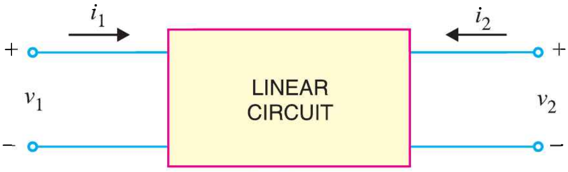


Fig. 24.1

It can be proved by advanced circuit theory that voltages and currents in Fig. 24.1 can be related by the following sets of equations :

$$v_1 = h_{11} i_1 + h_{12} v_2 \qquad ...(i)$$

$$i_2 = h_{21} i_1 + h_{22} v_2 \qquad ...(ii)$$

In these equations, the *hs* are fixed constants for a given circuit and are called *h* parameters. Once these parameters are known, we can use equations (*i*) and (*ii*) to find the voltages and currents in the circuit. If we look at *eq*.(*i*), it is clear that **h_{11} has the dimension of ohm and h_{12} is dimensionless. Similarly, from *eq*. (*ii*), h_{21} is dimensionless and h_{22} has the dimension of mho. The following points may be noted about *h* parameters :

(*i*) Every linear circuit has four *h* parameters ; one having dimension of ohm, one having dimension of mho and two dimensionless.

(*ii*) The *h* parameters of a given circuit are constant. If we change the circuit, *h* parameters would also change.

(*iii*) Suppose that in a particular linear circuit, voltages and currents are related as under:

$$v_1 = 10i_1 + 6v_2$$

$$i_2 = 4i_1 + 3v_2$$

---

* A linear circuit is one in which resistances, inductances and capacitances remain fixed when voltage across them changes.

** The two parts on the R.H.S. of *eq*. (*i*) must have the unit of voltage. Since current (amperes) must be multiplied by resistance (ohms) to get voltage (volts), h_{11} should have the dimension of resistance *i.e.* ohms.

Here we can say that the circuit has h parameters given by $h_{11} = 10\ \Omega$; $h_{12} = 6$; $h_{21} = 4$ and $h_{22} = 3\ ℧$.

24.2 Determination of *h* Parameters

The major reason for the use of h parameters is the relative ease with which they can be measured. The h parameters of a circuit shown in Fig. 24.1 can be found out as under :

(*i*) If we short-circuit the output terminals (See Fig. 24.2), we can say that output voltage $v_2 = 0$. Putting $v_2 = 0$ in equations (*i*) and (*ii*), we get,

$$v_1 = h_{11}\, i_1 + h_{12} \times 0$$
$$i_2 = h_{21}\, i_1 + h_{22} \times 0$$
$$\therefore \quad h_{11} = \frac{v_1}{i_1} \quad \text{for } v_2 = 0 \text{ i.e. output shorted}$$
$$\text{and} \quad h_{21} = \frac{i_2}{i_1} \quad \text{for } v_2 = 0 \text{ i.e. output shorted}$$

Let us now turn to the physical meaning of h_{11} and h_{21}. Since h_{11} is a ratio of voltage and current (*i.e.* v_1/i_1), it is an impedance and is called * "*input impedance with output shorted*". Similarly, h_{21} is the ratio of output and input current (*i.e.*, i_2/i_1), it will be dimensionless and is called "*current gain with output shorted*".

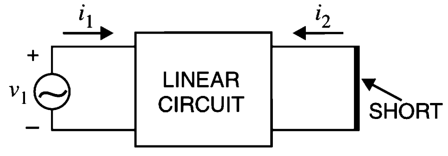


Fig. 24.2

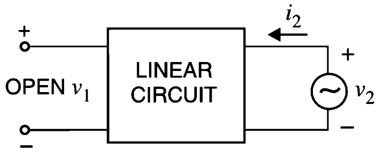


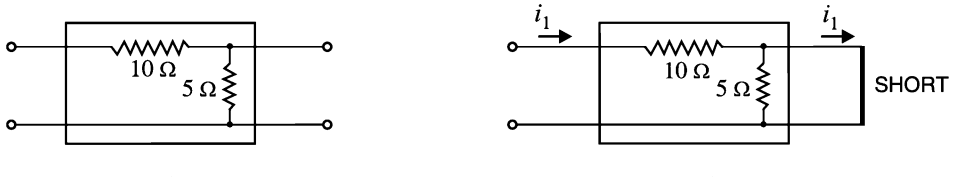
Fig. 24.3

(*ii*) The other two h parameters (*viz* h_{12} and h_{22}) can be found by making $i_1 = 0$. This can be done by the arrangement shown in Fig. 24.3. Here, we drive the output terminals with voltage v_2, keeping the input terminals open. With this set up, $i_1 = 0$ and the equations become :

$$v_1 = h_{11} \times 0 + h_{12}\, v_2$$
$$i_2 = h_{21} \times 0 + h_{22}\, v_2$$
$$\therefore \quad h_{12} = \frac{v_1}{v_2} \quad \text{for } i_1 = 0 \text{ i.e. input open}$$
$$\text{and} \quad h_{22} = \frac{i_2}{v_2} \quad \text{for } i_1 = 0 \text{ i.e. input open}$$

Since h_{12} is a ratio of input and output voltages (*i.e.* v_1/v_2), it is dimensionless and is called "*voltage feedback ratio with input terminals open*". Similarly, h_{22} is a ratio of output current and output voltage (*i.e.* i_2/v_2), it will be admittance and is called "*output admittance with input terminals open*".

Example. 24.1. *Find the h parameters of the circuit shown in Fig. 24.4 (i).*



(*i*) (*ii*)

Fig. 24.4

---

* Note that v_1 is the input voltage and i_1 is the input current. Hence v_1/i_1 is given the name input impedance.

Solution. The *h* parameters of the circuit shown in Fig. 24.4 (*i*) can be found as under :

To find h_{11} and h_{21}, short - circuit the output terminals as shown in Fig. 24.4 (*ii*). It is clear that input impedance of the circuit is 10 Ω because 5 Ω resistance is shorted out.

$$\therefore \qquad h_{11} = \mathbf{10\ \Omega}$$

Now current i_1 flowing into the box will flow through 10 Ω resistor and then through the shorted path as shown. It may be noted that in our discussion, i_2 is the output current flowing into the box. Since output current in Fig. 24.4 (*ii*) is actually flowing out of the box, i_2 is negative *i.e.*,

$$i_2 = -i_1$$

$$\therefore \qquad h_{21} = \frac{i_2}{i_1} = \frac{-i_1}{i_1} = \mathbf{-1}$$

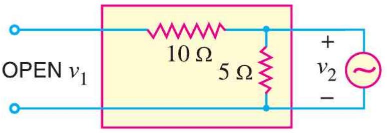


Fig. 24.4 (*iii*)

To find h_{12} and h_{22}, make the arrangement as shown in Fig. 24.4 (*iii*). Here we are driving the output terminals with a voltage v_2. This sets up a current i_2. Note that input terminals are open. Under this condition, there will be no current in 10Ω resistor and, therefore, there can be no voltage drop across it. Consequently, all the voltage appears across input terminals *i.e.*

$$v_1 = v_2$$

$$\therefore \qquad h_{12} = \frac{v_1}{v_2} = \frac{v_2}{v_2} = \mathbf{1}$$

Now the output impedance looking into the output terminals with input terminals open is simply 5 Ω. Then h_{22} will be the reciprocal of it because h_{22} is the output admittance with input terminals open.

$$\therefore \qquad h_{22} = 1/5 = \mathbf{0.2\mho}$$

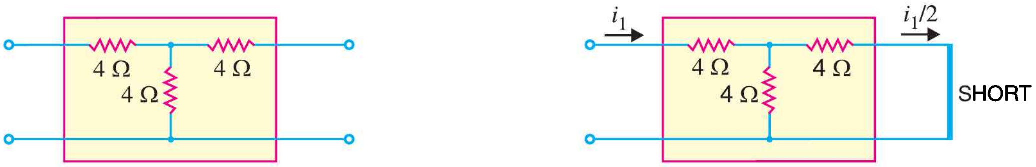
The *h* parameters of the circuit are :

$$h_{11} = 10\ \Omega\ ;\ h_{21} = -1$$

$$h_{12} = 1\ ;\ h_{22} = 0.2\ \mho$$

It may be mentioned here that in practice, dimensions are not written with *h* parameters. It is because it is understood that h_{11} is always in ohms, h_{12} and h_{21} are dimensionless and h_{22} is in mhos.

Example 24.2. *Find the h parameters of the circuit shown in Fig. 24.5 (i).*



(*i*) **Fig. 24.5** (*ii*)

Solution. First of all imagine that output terminals are short-circuited as shown in Fig. 24.5 (*ii*). The input impedance under this condition is the parameter h_{11}.

$$\text{Obviously,} \qquad h_{11} = 4 + 4 \parallel 4$$

$$= 4 + \frac{4 \times 4}{4+4} = \mathbf{6\ \Omega}$$

Now the input current i_1 in Fig. 24.5 (*ii*) will divide equally at the junction of 4 Ω resistors so that output current is $i_1/2$ *i.e.*

$$i_2 = -i_1/2 = -0.5\, i_1$$

$$\therefore \quad h_{21} = \frac{i_2}{i_1} = \frac{-0.5\, i_1}{i_1} = \mathbf{-0.5}$$

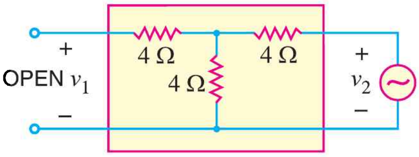


Fig. 24.5 (*iii*)

In order to find h_{12} and h_{22}, imagine the arrangement as shown in Fig. 24.5 (*iii*). Here we are driving the output terminals with voltage v_2, keeping the input terminals open. Under this condition, any voltage v_2 applied to the output will divide by a factor 2 *i.e.*

$$v_1 = \frac{v_2}{2} = 0.5\, v_2$$

$$\therefore \quad h_{12} = \frac{v_1}{v_2} = \frac{0.5\, v_2}{v_2} = \mathbf{0.5}$$

Now the output impedance looking into the output terminals with input terminals open is simply 8 Ω. Then h_{22} will be the reciprocal of this *i.e.*

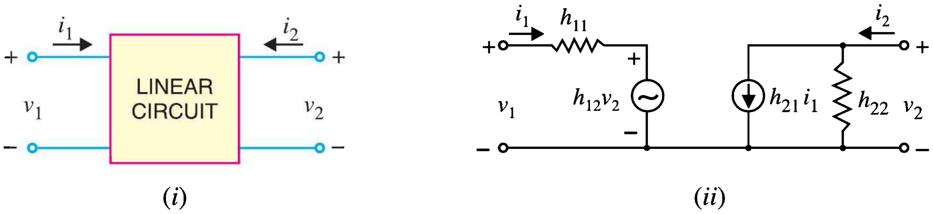
$$h_{22} = \frac{1}{8} = \mathbf{0.125\ ℧}$$

24.3 *h* Parameter Equivalent Circuit

Fig. 24.6 (*i*) shows a linear circuit. It is required to draw the *h* parameter equivalent circuit of Fig. 24.6 (*i*). We know that voltages and currents of the circuit in Fig. 24.6 (*i*) can be expressed in terms of *h* parameters as under :

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2 \qquad ...(i)$$

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2 \qquad ...(ii)$$



(*i*) (*ii*)

Fig. 24.6

Fig. 24.6 (*ii*) shows *h* parameter equivalent circuit of Fig. 24.6 (*i*) and is derived from equations (*i*) and (*ii*). The *input circuit* appears as a resistance h_{11} in series with a voltage generator $h_{12}\, v_2$. This circuit is derived from equation (*i*). The *output circuit* involves two components ; a current generator $h_{21}\, i_1$ and shunt resistance h_{22} and is derived from equation (*ii*). The following points are worth noting about the *h* parameter equivalent circuit [See Fig. 24.6 (*ii*)] :

(*i*) This circuit is called hybrid equivalent because its input portion is a Thevenin equivalent, or voltage generator with series resistance, while output side is Norton equivalent, or current generator with shunt resistance. Thus it is a mixture or a hybrid. The symbol '*h*' is simply the abbreviation of the word hybrid (hybrid means "mixed").

(*ii*) The different hybrid parameters are distinguished by different number subscripts. The notation shown in Fig. 24.6 (*ii*) is used in general circuit analysis. The first number designates the circuit in which the effect takes place and the second number designates the circuit from which the effect comes. For instance, h_{21} is the "short-circuit forward current gain" or the ratio of the current in the output (*circuit* 2) to the current in the input (*circuit* 1).

(*iii*) The equivalent circuit of Fig. 24.6 (*ii*) is extremely useful for two main reasons. First, it isolates the input and output circuits, their interaction being accounted for by the two controlled sources. Thus, the effect of output upon input is represented by the equivalent voltage generator $h_{12}v_2$ and its value depends upon output voltage. Similarly, the effect of input upon output is represented by current generator $h_{21}i_1$ and its value depends upon input current. Secondly, the two parts of the circuit are in a form which makes it simple to take into account source and load circuits.

24.4 Performance of a Linear Circuit in *h* Parameters

We have already seen that any linear circuit with input and output has a set of *h* parameters. We shall now develop formulas for input impedance, current gain, voltage gain etc.of a linear circuit in terms of *h* parameters.

(*i*) **Input impedance.** Consider a linear circuit with a load resistance r_L across its terminals as shown in Fig. 24.7. The input impedance Z_{in} of this circuit is the ratio of input voltage to input current *i.e.*

$$Z_{in} = \frac{v_1}{i_1}$$

Now $v_1 = h_{11}\,i_1 + h_{12}\,v_2$ in terms of *h* parameters. Substituting the value of v_1 in the above expression, we get,

$$Z_{in} = \frac{h_{11}\,i_1 + h_{12}\,v_2}{i_1} = h_{11} + \frac{h_{12}\,v_2}{i_1} \qquad ...(i)$$

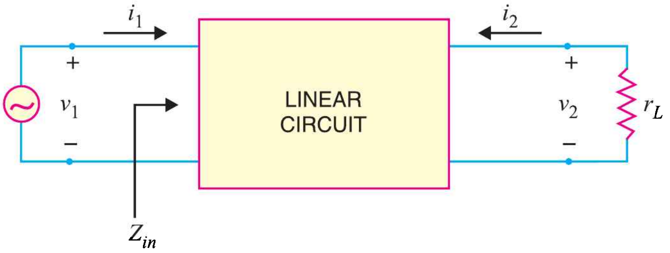


Fig. 24.7

Now, $i_2 = h_{21}\,i_1 + h_{22}\,v_2$ in terms of *h* parameters. Further from Fig. 24.7, it is clear that $i_2 = -\,v_2/r_L$. The minus sign is used here because the actual load current is opposite to the direction of i_2.

$$\therefore \qquad \frac{-\,v_2}{r_L} = h_{21}\,i_1 + h_{22}\,v_2 \qquad \left[\because i_2 = \frac{-\,v_2}{r_L}\right]$$

$$\text{or} \qquad -\,h_{21}\,i_1 = h_{22}\,v_2 + \frac{v_2}{r_L} = v_2\left(h_{22} + \frac{1}{r_L}\right)$$

$$\therefore \qquad \frac{v_2}{i_1} = \frac{-\,h_{21}}{h_{22} + \dfrac{1}{r_L}} \qquad ...(ii)$$

Substituting the value of v_2/i_1 from exp. (*ii*) into exp. (*i*), we get,

$$\mathbf{Z_{in}} = \boldsymbol{h_{11} - \frac{h_{12}\,h_{21}}{h_{22} + \dfrac{1}{r_L}}} \qquad ...(iii)$$

This is the expression for input impedance of a linear circuit in terms of *h* parameters and load connected to the output terminals. If either h_{12} or r_L is very small, the second term in exp. (*iii*) can be neglected and input impedance becomes :

$$\mathbf{Z_{in}} \simeq \boldsymbol{h_{11}}$$

(*ii*) **Current Gain.** Referring to Fig. 24.7, the current gain A_i of the circuit is given by :

$$A_i = \frac{i_2}{i_1}$$

Now $\quad i_2 = h_{21}\, i_1 + h_{22}\, v_2$

and $\quad v_2 = -\, i_2\, r_L$

$\therefore \quad i_2 = h_{21}\, i_1 - h_{22}\, i_2\, r_L$

or $\quad i_2\,(1 + h_{22}\, r_L) = h_{21}\, i_1$

or $\quad \dfrac{i_2}{i_1} = \dfrac{h_{21}}{1 + h_{22}\, r_L}$

But $i_2/i_1 = A_i$, the current gain of the circuit.

$$\therefore \quad \mathbf{A_i = \frac{h_{21}}{1 + h_{22}\, r_L}}$$

If $h_{22}\, r_L << 1$, then $A_i \simeq h_{21}$.

The expression $A_i \simeq h_{21}$ is often useful. To say that $h_{22}\, r_L << 1$ is the same as saying that $r_L << 1/h_{22}$. This occurs when r_L is much smaller than the output resistance ($1/h_{22}$), shunting $h_{21}\, i_1$ generator. Under such condition, most of the generator current bypasses the circuit output resistance in favour of r_L. This means that $i_2 \simeq h_{21}\, i_1$ or $i_2/i_1 \simeq h_{21}$.

(*iii*) **Voltage gain.** Referring back to Fig. 24.7, the voltage gain of the circuit is given by :

$$A_v = \frac{v_2}{v_1}$$

$$= \frac{v_2}{i_1\, Z_{in}} \qquad (\because\ v_1 = i_1 Z_{in}) \qquad \text{...(iv)}$$

While developing expression for input impedance, we found that :

$$\frac{v_2}{i_1} = \frac{-\,h_{21}}{h_{22} + \dfrac{1}{r_L}}$$

Substituting the value of v_2/i_1 in exp. (*iv*), we get,

$$\mathbf{A_v = \frac{-\,h_{21}}{Z_{in}\left(h_{22} + \dfrac{1}{r_L}\right)}}$$

(*iv*) **Output impedance.** In order to find the output impedance, remove the load r_L, set the signal voltage v_1 to zero and connect a generator of voltage v_2 at the output terminals. Then *h* parameter equivalent circuit becomes as shown in Fig. 24.8. By definition, the output impedance Z_{out} is

$$Z_{out} = \frac{v_2}{i_2}$$

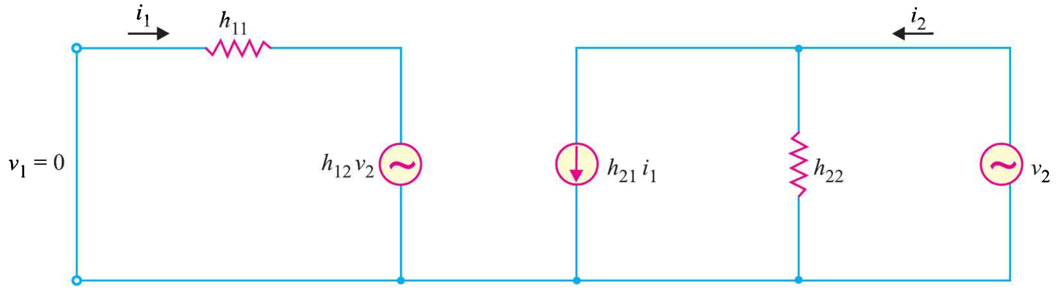


Fig. 24.8

With $v_1 = 0$ and applying Kirchhoff's voltage law to the input circuit, we have,

$$0 = i_1 h_{11} + h_{12} v_2$$

$$\therefore \quad i_1 = -\frac{h_{12} v_2}{h_{11}}$$

Now
$$i_2 = h_{21} i_1 + h_{22} v_2$$

Putting the value of i_1 $(= -h_{12} v_2 / h_{11})$ in this equation, we get,

$$i_2 = h_{21}\left(-\frac{h_{12} v_2}{h_{11}}\right) + h_{22} v_2$$

or
$$i_2 = -\frac{h_{21} h_{12} v_2}{h_{11}} + h_{22} v_2$$

Dividing throughout by v_2, we have,

$$\frac{i_2}{v_2} = \frac{-h_{21} h_{12}}{h_{11}} + h_{22}$$

$$\therefore \quad Z_{out} = \frac{\boldsymbol{v_2}}{\boldsymbol{i_2}} = \frac{\mathbf{1}}{\boldsymbol{h_{22}} - \dfrac{\boldsymbol{h_{21} h_{12}}}{\boldsymbol{h_{11}}}}$$

Example 24.3. *Find the (i) input impedance and (ii) voltage gain for the circuit shown in Fig. 24.9.*

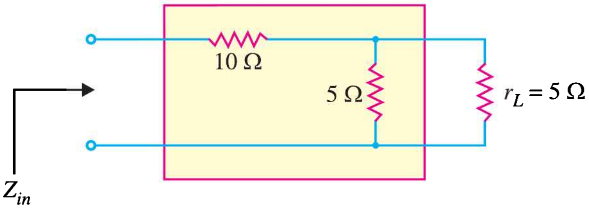


Fig. 24.9

Solution. The *h* parameters of the circuit inside the box are the same as those calculated in example 24.1 *i.e.*

$$h_{11} = 10\ ; \qquad h_{21} = -1$$

$$h_{12} = 1 \text{ and } h_{22} = 0.2$$

(*i*) Input impedance is given by :

$$Z_{in} = h_{11} - \frac{h_{12} h_{21}}{h_{22} + \dfrac{1}{r_L}} = 10 - \frac{1 \times -1}{0.2 + \dfrac{1}{5}}$$

$$= 10 + 2.5 = \mathbf{12.5\ \Omega}$$

By inspection, we can see that input impedance is equal to 10 Ω plus two 5 Ω resistances in parallel *i.e.*

$$Z_{in} = 10 + 5 \parallel 5$$

$$= 10 + \frac{5 \times 5}{5 + 5} = 12.5\ \Omega$$

(*ii*) Voltage gain,
$$A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \dfrac{1}{r_L}\right)} = \frac{1}{12.5\left(0.2 + \dfrac{1}{5}\right)} = \mathbf{\frac{1}{5}}$$

It means that output voltage is one-fifth of the input voltage. This can be readily established by inspection of Fig. 24.9. The two 5 Ω resistors in parallel give a net resistance of 2.5 Ω. Therefore, we have a voltage divider consisting of 10 Ω resistor in series with 2.5 Ω resistor.

$$\therefore \quad \text{Output voltage} = \frac{2.5}{12.5} \times \text{Input voltage}$$

$$\text{or} \quad \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{2.5}{12.5} = \frac{1}{5}$$

$$\text{or} \quad A_v = \frac{1}{5}$$

Comments. The reader may note that in a simple circuit like that of Fig. 24.9, it is not advisable to use *h* parameters to find the input impedance and voltage gain. It is because answers of such circuits can be found directly by inspection. However, in complicated circuits, inspection method becomes cumbersome and the use of *h* parameters yields quick results.

24.5 The *h* Parameters of a Transistor

It has been seen in the previous sections that every linear circuit is associated with *h* parameters. When this linear circuit is terminated by load r_L, we can find input impedance, current gain, voltage gain, etc. in terms of *h* parameters. Fortunately, for ***small*** a.c. signals, the transistor behaves as a linear device because the output a.c. signal is directly proportional to the input a.c. signal. Under such circumstances, the a.c. *operation* of the transistor can be described in terms of *h* parameters. The expressions derived for input impedance, voltage gain *etc.* in the previous section shall hold good for transistor amplifier except that here r_L is the a.c. load seen by the transistor.

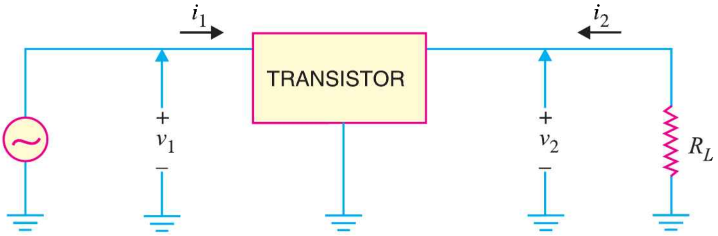


Fig. 24.10

Fig. 24.10 shows the transistor amplifier circuit. There are four quantities required to describe the external behaviour of the transistor amplifier. These are v_1, i_1, v_2 and i_2 shown on the diagram of Fig. 24.10. These voltages and currents can be related by the following sets of equations :

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2$$

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2$$

The following points are worth noting while considering the behaviour of transistor in terms of *h* parameters :

(*i*) For small a.c. signals, a transistor behaves as a linear circuit. Therefore, its a.c. operation can be described in terms of *h* parameters.

(*ii*) The value of *h* parameters of a transistor will depend upon the transistor connection (*i.e. CB, CE* or *CC*) used. For instance, a transistor used in *CB* arrangement may have $h_{11} = 20\ \Omega$. If we use the same transistor in *CE* arrangement, h_{11} will have a different value. Same is the case with other *h* parameters.

(*iii*) The expressions for input impedance, voltage gain etc. derived in Art. 24.4 are also applicable to transistor amplifier except that r_L is the a.c. load seen by the transistor *i.e.*

$$r_L = R_C \parallel R_L$$

(*iv*) The values of *h* parameters depend upon the operating point. If the operating point is changed, parameter values are also changed.

(*v*) The notations v_1, i_1, v_2 and i_2 are used for general circuit analysis. In a transistor amplifier, we use the notation depending upon the configuration in which transistor is used. Thus for *CE* arrangement,

$$v_1 = V_{be} \quad ; \quad i_1 = I_b \quad ; \quad v_2 = V_{ce} \quad ; \quad i_2 = I_c$$

Here V_{be}, I_b, V_{ce} and I_c are the R.M.S. values.

24.6 Nomenclature for Transistor *h* Parameters

The numerical subscript notation for *h* parameters (*viz.* h_{11}, h_{21}, h_{12} and h_{22}) is used in general circuit analysis. However, this nomenclature has been modified for a transistor to indicate the nature of parameter and the transistor configuration used. The *h* parameters of a transistor are represented by the following notation :

(*i*) The numerical subscripts are replaced by letter subscripts.

(*ii*) The first letter in the double subscript notation indicates the nature of parameter.

(*iii*) The second letter in the double subscript notation indicates the circuit arrangement (*i.e. CB, CE* or *CC*) used.

Table below shows the *h* parameter nomenclature of a transistor :

S.No.	*h* parameter	Notation in CB	Notation in CE	Notation in CC
1.	h_{11}	h_{ib}	h_{ie}	h_{ic}
2.	h_{12}	h_{rb}	h_{re}	h_{rc}
3.	h_{21}	h_{fb}	h_{fe}	h_{fc}
4.	h_{22}	h_{ob}	h_{oe}	h_{oc}

Note that first letter *i*, *r*, *f* or *o* indicates the nature of parameter. Thus h_{11} indicates input impedance and this parameter is designated by the subscript *i*. Similarly, letters *r*, *f* and *o* respectively indicate reverse voltage feedback ratio, forward current transfer ratio and output admittance. The second letters *b*, *e* and *c* respectively indicate *CB*, *CE* and *CC* arrangement.

24.7 Transistor Circuit Performance in *h* Parameters

The expressions for input impedance, voltage gain etc. in terms of *h* parameters derived in Art. 24.4 for general circuit analysis apply equally for transistor analysis. However, it is profitable to rewrite them in standard transistor *h* parameter nomenclature.

(*i*) **Input impedance.** The general expression for input impedance is

$$Z_{in} = h_{11} - \frac{h_{12}\,h_{21}}{h_{22} + \frac{1}{r_L}}$$

Using standard *h* parameter nomenclature for transistor, its value for *CE* arrangement will be :

$$Z_{in} = h_{ie} - \frac{h_{re}\,h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

Similarly, expressions for input impedance in *CB* and *CC* arrangements can be written. It may be noted that r_L is the a.c. load seen by the transistor.

(*ii*) **Current gain.** The general expression for current gain is

$$A_i = \frac{h_{21}}{1 + h_{22}\,r_L}$$

Using standard transistor *h* parameter nomenclature, its value for *CE* arrangement is

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

The reader can readily write down the expressions for *CB* and *CC* arrangements.

(*iii*) **Voltage gain.** The general expression for voltage gain is

$$A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_L}\right)}$$

Using standard transistor *h* parameter nomenclature, its value for *CE* arrangement is

$$A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

In the same way, expressions for voltage gain in *CB* and *CC* arrangement can be written.

(*iv*) **Output impedance.** The general expression for output impedance is

$$Z_{out} = \frac{1}{h_{22} - \frac{h_{21}\, h_{12}}{h_{11}}}$$

Using standard transistors *h* parameter nomenclature, its value for *CE* arrangement is

$$Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}\, h_{re}}{h_{ie}}}$$

In the same way, expression for output impedance in *CB* and *CC* arrangements can be written.

The above expression for Z_{out} is for the transistor. If the transistor is connected in a circuit to form a single stage amplifier, then output impedance of the stage = $Z_{out} \parallel r_L$ where $r_L = R_C \parallel R_L$.

Example 24.4. *A transistor used in CE arrangement has the following set of h parameters when the d.c. operating point is* V_{CE} = *10 volts and* I_C = *1 mA :*

$h_{ie} = 2000\ \Omega$; $h_{oe} = 10^{-4}$ mho; $h_{re} = 10^{-3}$; $h_{fe} = 50$

Determine (i) input impedance (ii) current gain and (iii) voltage gain. The a.c. load seen by the transistor is $r_L = 600\ \Omega$. *What will be approximate values using reasonable approximations?*

Solution. (*i*) Input impedance is given by :

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 2000 - \frac{10^{-3} \times 50}{10^{-4} + \frac{1}{600}} \quad \text{.... }(i)$$

$$= 2000 - 28 = \mathbf{1972\ \Omega}$$

The second term in eq. (*i*) is quite small as compared to the first.

$\therefore \quad Z_{in} \simeq h_{ie} = \mathbf{2000\ \Omega}$

(*ii*) Current gain, $A_i = \dfrac{h_{fe}}{1 + h_{oe} \times r_L} = \dfrac{50}{1 + (600 \times 10^{-4})} = \mathbf{47}$

If $h_{oe}\, r_L << 1$, then $A_i \simeq h_{fe} = \mathbf{50}$

(*iii*) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)} = \dfrac{-50}{1972\left(10^{-4} + \frac{1}{600}\right)} = \mathbf{-14.4}$

The negative sign indicates that there is 180° phase shift between input and output. The magnitude of gain is 14.4. In other words, the output signal is 14.4 times greater than the input and it is 180° out of phase with the input.

Example 24.5. *A transistor used in CE connection has the following set of h parameters when the d.c. operating point is* V_{CE} = *5 volts and* I_C = *1 mA :*

$h_{ie} = 1700\ \Omega;\ h_{re} = 1.3 \times 10^{-4};\ h_{fe} = 38;\ h_{oe} = 6 \times 10^{-6}\ \mho$

If the a.c. load r_L *seen by the transistor is 2 kΩ, find (i) the input impedance (ii) current gain and (iii) voltage gain.*

Solution. (*i*) The input impedance looking into the base of transistor is

$$Z_{in} = h_{ie} - \frac{h_{re}\,h_{fe}}{h_{oe} + \dfrac{1}{r_L}} = 1700 - \frac{1.3 \times 10^{-4} \times 38}{6 \times 10^{-6} + \dfrac{1}{2000}} \simeq \mathbf{1690\ \Omega}$$

(*ii*) Current gain,

$$A_i = \frac{h_{fe}}{1 + h_{oe} r_L} = \frac{38}{1 + 6 \times 10^{-6} \times 2000} = \frac{38}{1.012} \simeq \mathbf{37.6}$$

(*iii*) Voltage gain,

$$A_v = \frac{-\,h_{fe}}{Z_{in}\left(h_{oe} + \dfrac{1}{r_L}\right)} = \frac{-\,38}{1690\left(6 \times 10^{-6} + \dfrac{1}{2000}\right)} = \mathbf{44.4}$$

Example 24.6. *Fig. 24.11 shows the transistor amplifier in CE arrangement. The h parameters of transistor are as under :*

$h_{ie} = 1500\ \Omega;\ h_{fe} = 50;\ h_{re} = 4 \times 10^{-4};\ h_{oe} = 5 \times 10^{-5}\ \mho$

Find (i) a.c. input impedance of the amplifier (ii) voltage gain and (iii) output impedance.

Solution. The a.c. load r_L seen by the transistor is equivalent of the parallel combination of R_C (= 10 kΩ) and R_L (= 30 kΩ) *i.e.*

$$r_L = \frac{R_C\,R_L}{R_C + R_L} = \frac{10 \times 30}{10 + 30} = 7.5\ \text{k}\Omega = 7500\ \Omega$$

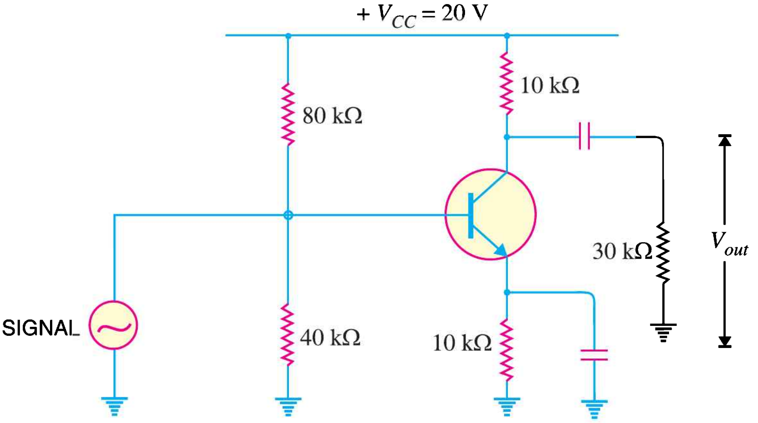


Fig. 24.11

(*i*) The input impedance looking into the base of transistor is given by :

$$Z_{in} = h_{ie} - \frac{h_{re}\,h_{fe}}{h_{oe} + \dfrac{1}{r_L}} = 1500 - \frac{4 \times 10^{-4} \times 50}{5 \times 10^{-5} + \dfrac{1}{7500}} = 1390\ \Omega$$

This is only the input impedance looking into the base of transistor. The a.c. input impedance of the entire stage will be Z_{in} in parallel with bias resistors *i.e.*

Input impedance of stage $= 80 \times 10^3 \parallel 40 \times 10^3 \parallel 1390 = \mathbf{1320\ \Omega}$

(*ii*) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \dfrac{1}{r_L}\right)} = \dfrac{-50}{1390\left(5 \times 10^{-5} + \dfrac{1}{7500}\right)} = \mathbf{-196}$

The negative sign indicates phase reversal. The magnitude of gain is 196.

(*iii*) Output impedance of transistor is

$$Z_{out} = \frac{1}{h_{oe} - \dfrac{h_{fe}\, h_{re}}{h_{ie}}}$$

$$= \frac{1}{5 \times 10^{-5} - \dfrac{50 \times 4 \times 10^{-4}}{1500}} = 27270\ \Omega = 27.27\ \text{k}\Omega$$

∴ Output impedance of the stage

$$= Z_{out} \parallel R_L \parallel R_C$$

$$= 27.27\ \text{k}\Omega \parallel 30\ \text{k}\Omega \parallel 10\ \text{k}\Omega = \mathbf{5.88\ k\Omega}$$

Example 24.7. *Find the value of current gain for the circuit shown in Fig. 24.12. The h-parameter values of the transistor are given alongside the figure.*

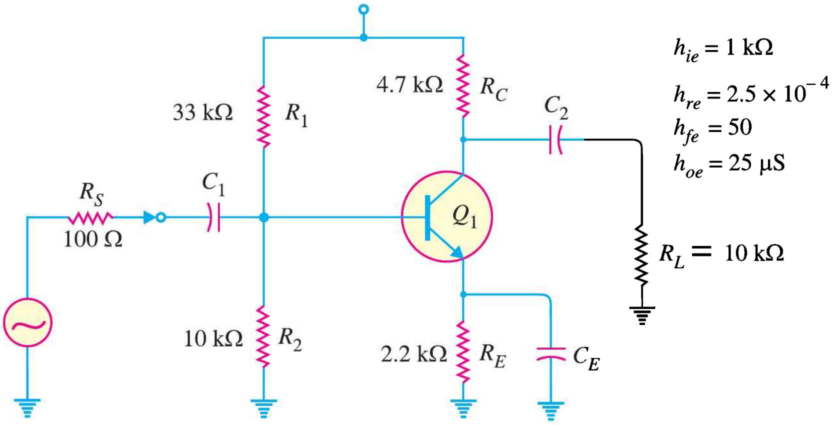


Fig. 24.12

Solution. The current gain A_i for the circuit is given by ;

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

Here $r_L = R_C \parallel R_L = 4.7\ \text{k}\Omega \parallel 10\ \text{k}\Omega = 3.2\ \text{k}\Omega$

∴ $$A_i = \frac{50}{1 + (25 \times 10^{-6})(3.2 \times 10^3)} = \mathbf{46.3}$$

Note that current gain of the circuit is very close to the value h_{fe}. The reason for this is that $h_{oe}\, r_L << 1$. Since this is normally the case, $A_i \simeq h_{fe}$.

Example 24.8. *In the above example, determine the output impedance of the transistor.*

Solution. Note that the signal source (See Fig. 24.12) has resistance $R_S = 100\ \Omega$.

∴ Output impedance Z_{out} of the transistor is

$$Z_{out} = \frac{1}{h_{oe} - \left(\frac{h_{fe}\,h_{re}}{h_{ie} + R_S}\right)}$$

$$= \frac{1}{(25 \times 10^{-6}) - \frac{(50)\,(2.5 \times 10^{-4})}{(1 \times 10^{3}) + 100}} = 73{\cdot}3 \times 10^{3}\ \Omega = \mathbf{73.3\ k\Omega}$$

24.8 Approximate Hybrid Formulas for Transistor Amplifier

The *h*-parameter formulas (*CE* configuration) covered in Art. 24.7 can be approximated to a form that is easier to handle. While these approximate formulas will not give results that are as accurate as the original formulas, they can be used for many applications.

(*i*) Input impedance

$$\text{Input impedance, } Z_{in} = h_{ie} - \frac{h_{re}\,h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

In actual practice, the second term in this expression is very small as compared to the first term.

$$\therefore \qquad Z_{in} = h_{ie} \qquad \text{... approximate formula}$$

(*ii*) Current gain

$$\text{Current gain, } A_i = \frac{h_{fe}}{1 + h_{oe}\,r_L}$$

In actual practice, $h_{oe}\,r_L$ is very small as compared to 1.

$$\therefore \qquad A_i = h_{fe} \qquad \text{... approximate formula}$$

(*iii*) Voltage gain

$$\text{Voltage gain, } A_v = \frac{-\,h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

$$= \frac{-\,h_{fe}\,r_L}{Z_{in}\,(h_{oe}\,r_L + 1)}$$

Now approximate formula for Z_{in} is h_{ie}. Also $h_{oe}\,r_L$ is very small as compared to 1.

$$\therefore \qquad A_v = -\frac{h_{fe}\,r_L}{h_{ie}} \qquad \text{... approximate formula}$$

(*iv*) Output impedance

$$\text{Output impedance of transistor, } Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}\,h_{re}}{h_{ie}}}$$

The second term in the denominator is very small as compared to h_{oe}.

$$\therefore \qquad Z_{out} = \frac{1}{h_{oe}} \qquad \text{... approximate formula}$$

The output impedance of transistor amplifier

$$= Z_{out} \parallel r_L \qquad \text{where } {}^{*}r_L = R_C \parallel R_L$$

---

* If the amplifier is unloaded (*i.e.* $R_L = \infty$), $r_L = R_C$.

Example 24.9. *For the circuit shown in Fig. 24.13, use approximate hybrid formulas to determine (i) the input impedance (ii) voltage gain. The h parameters of the transistor are* h_{ie} *= 1.94 kΩ and* h_{fe} *= 71.*

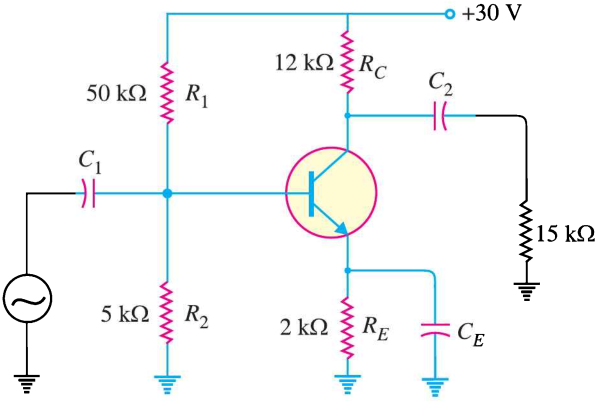


Fig. 24.13

Solution.

$$\text{a.c. collector load, } r_L = R_C \| R_L = 12\text{ k}\Omega \| 15\text{ k}\Omega = 6.67\text{ k}\Omega$$

(*i*) Transistor input impedance is

$$Z_{in\,(base)} = h_{ie} = 1.94\text{ k}\Omega$$

$$\therefore \quad \text{Circuit input impedance} = Z_{in\,(base)} \| R_1 \| R_2$$

$$= 1.94\text{ k}\Omega \| 50\text{ k}\Omega \| 5\text{ k}\Omega = \mathbf{1.35\text{ k}\Omega}$$

(*ii*) $$\text{Voltage gain, } A_v = \frac{h_{fe}\, r_L}{h_{ie}} = \frac{71 \times 6.67\text{ k}\Omega}{1.94\text{ k}\Omega} = 244$$

Example 24.10. *A transistor used in an amplifier has h-parameter values of* h_{ie} *= 600 Ω to 800Ω and* h_{fe} *= 110 to 140. Using approximate hybrid formula, determine the voltage gain for the circuit. The a.c. collector load,* r_L *= 460 Ω.*

Solution. When *minimum* and *maximum h*-parameter values are given, we should determine the *geometric average* of the two values. Thus the values that we would use in the analysis of circuit are found as under :

$$h_{ie} = \sqrt{h_{ie\,(min)} \times h_{ie\,(max)}}$$

$$= \sqrt{(600\ \Omega)\ (800\ \Omega)} = 693\Omega$$

$$h_{fe} = \sqrt{h_{fe\,(min)} \times h_{fe\,(max)}}$$

$$= \sqrt{(110)\ (140)} = 124$$

$$\text{Voltage gain, } A_v = \frac{h_{fe}\, r_L}{h_{ie}} = \frac{(124)\ (460)}{693} = \mathbf{82.3}$$

24.9 Experimental Determination of Transistor *h* Parameters

The determination of *h* parameters of a general linear circuit has already been discussed in Art. 24.2. To illustrate how such a procedure is carried out for a *CE* transistor amplifier, consider the circuit of Fig. 24.14. The R.M.S. values will be considered in the discussion. Using standard transistor nomenclature :

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \qquad \text{...}(i)$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \qquad \text{...}(ii)$$

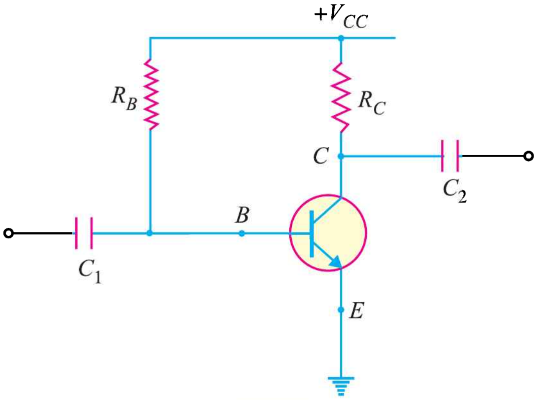


Fig. 24.14

(*i*) **Determination of $\mathbf{h_{fe}}$ and $\mathbf{h_{ie}}$.** In order to determine these parameters, the output is a.c. short circuited as shown in Fig. 24.15 (*i*). This is accomplished by making the capacitance of C_2 deliberately large. The result is that changing component of collector current flows through C_2 instead of R_C and a.c. voltage developed across C_2 is zero *i.e.* *$V_{ce} = 0$.

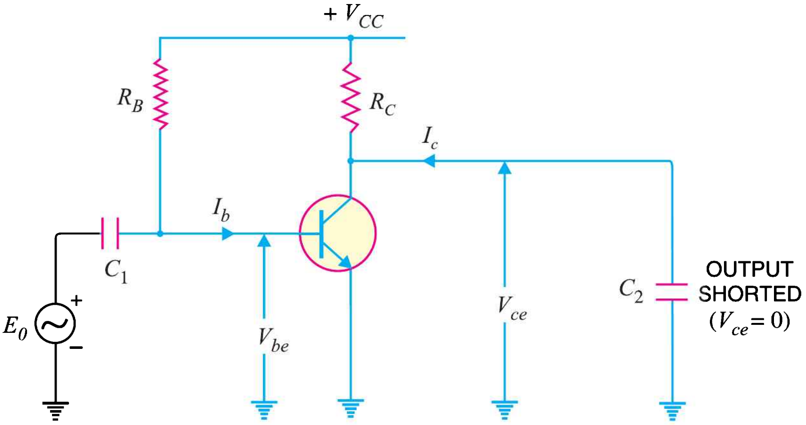


Fig. 24.15 (*i*)

Substituting $V_{ce} = 0$ in equations (*i*) and (*ii*) above, we get,

$$V_{be} = h_{ie} I_b + h_{re} \times 0$$

$$I_c = h_{fe} I_b + h_{oe} \times 0$$

$$\therefore \qquad h_{fe} = \frac{I_c}{I_b} \quad \text{for} \quad V_{ce} = 0$$

$$\text{and} \qquad h_{ie} = \frac{V_{be}}{I_b} \quad \text{for } V_{ce} = 0$$

Note that I_c and I_b are the a.c. R.M.S. collector and base currents respectively. Also V_{be} is the a.c. R.M.S. base-emitter voltage.

---

* Note that setting $V_{ce} = 0$ does not mean that V_{CE} (the d.c. collector-emitter voltage) is zero. Only a.c. output is short-circuited.

(*ii*) **Determination of h_{re} and h_{oe}.** In order to determine these two parameters, the input is a.c. open-circuited, a signal generator is applied across the output and resulting V_{be}, V_{ce} and I_c are measured. This is illustrated in Fig 24.15 (*ii*). A large inductor L is connected in series with R_B. Since the d.c. resistance of inductor is very small, it does not disturb the operating point. Again, a.c. current cannot flow through R_B because of large reactance of inductor. Further, the voltmeter used to measure V_{be} has a high input impedance and hence there are no paths connected to the base with any appreciable a.c. current. This means that base is *effectively a.c. open-circuited *i.e.* $I_b = 0$.

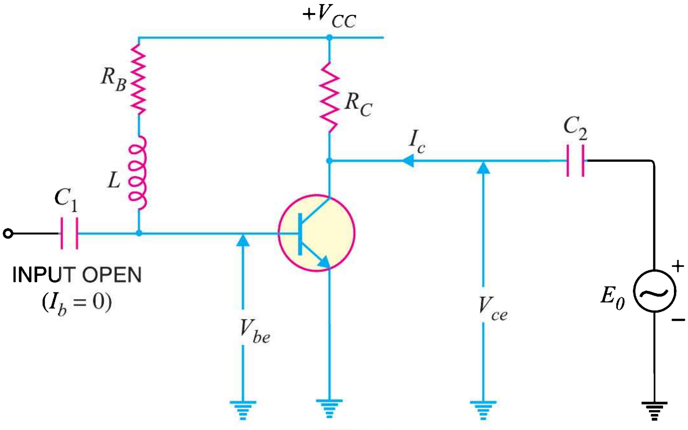


Fig. 24.15 (*ii*)

Substituting $I_b = 0$ in equations (*i*) and (*ii*), we get,

$$V_{be} = h_{ie} \times 0 + h_{re} V_{ce}$$

$$I_c = h_{fe} \times 0 + h_{oe} V_{ce}$$

$$\therefore \qquad h_{re} = \frac{V_{be}}{V_{ce}} \text{ for } I_b = 0$$

$$\text{and} \qquad h_{oe} = \frac{I_c}{V_{ce}} \text{ for } I_b = 0$$

Example 24.11. *The following quantities are measured in a CE amplifier circuit :*

(*a*) *With output a.c. short-circuited (i.e.* $V_{ce} = 0$*)*

$$I_b = 10\,\mu A;\ I_c = 1\ mA;\ V_{be} = 10\ mV$$

(*b*) *With input a.c. open-circuited (i.e.* $I_b = 0$*)*

$$V_{be} = 0.65\ mV;\ I_c = 60\,\mu A;\ V_{ce} = 1\ V$$

Determine all the four h parameters.

Solution.

$$h_{ie} = \frac{V_{be}}{I_b} = \frac{10 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{1000\ \Omega}$$

$$h_{fe} = \frac{I_c}{I_b} = \frac{1 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{100}$$

$$h_{re} = \frac{V_{be}}{V_{ce}} = \frac{0.65 \times 10^{-3}}{1} = \mathbf{0.65 \times 10^{-3}}$$

---

* How effectively the base is a.c. open-circuited depends upon the reactance L and the input impedance of the voltmeter used to measure V_{be}.

$$h_{oe} = \frac{I_c}{V_{ce}} = \frac{60 \times 10^{-6}}{1} = 60\ \mu\text{mho}$$

24.10 Limitations of *h* Parameters

The *h* parameter approach provides accurate information regarding the current gain, voltage gain, input impedance and output impedance of a transistor amplifier. However, there are two major limitations on the use of these parameters.

(*i*) It is very difficult to get the exact values of *h* parameters for a particular transistor. It is because these parameters are subject to considerable variation—unit to unit variation, variation due to change in temperature and variation due to change in operating point. In predicting an amplifier performance, care must be taken to use *h* parameter values that are correct for the operating point being considered.

(*ii*) The *h* parameter approach gives correct answers for small a.c. signals only. It is because a transistor behaves as a linear device for small signals only.

MULTIPLE-CHOICE QUESTIONS

1. Hybrid means ....
(*i*) mixed (*ii*) single
(*iii*) unique (*iv*) none of the above

2. There are .... *h* parameters of a transistor.
(*i*) two (*ii*) four
(*iii*) three (*iv*) none of the above

3. The *h* parameter approach gives correct results for ....
(*i*) large signals only
(*ii*) small signals only
(*iii*) both small and large signals
(*iv*) none of the above

4. A transistor behaves as a linear device for ....
(*i*) small signals only
(*ii*) large signals only
(*iii*) both small and large signals
(*iv*) none of the above

5. The parameter h_{ie} stands for input impedance in ....
(*i*) *CB* arrangement with output shorted
(*ii*) *CC* arrangement with output shorted
(*iii*) *CE* arrangement with output shorted
(*iv*) none of the above

6. The dimensions of h_{ie} parameter are ....
(*i*) mho (*ii*) ohm
(*iii*) farad (*iv*) none of the above

7. The parameter h_{fe} is called .... in *CE* arrangement with output shorted.
(*i*) voltage gain
(*ii*) current gain
(*iii*) input impedance
(*iv*) none of the above

8. If the operating point changes, the *h* parameters of a transistor ....
(*i*) also change
(*ii*) do not change
(*iii*) may or may not change
(*iv*) none of the above

9. The values of *h* parameter of a transistor in *CE* arrangement are .... arrangement.
(*i*) the same as for *CB*
(*ii*) the same as for *CC*
(*iii*) different from that in *CB*
(*iv*) none of the above

10. In order to determine h_{fe} and h_{ie} parameters of a transistor, ... is a.c. short-circuited.
(*i*) input
(*ii*) output
(*iii*) input as well as output
(*iv*) none of the above

11. If temperature changes, *h* parameters of a transistor ....
(*i*) may or may not change
(*ii*) do not change
(*iii*) also change
(*iv*) none of the above

12. In *CE* arrangement, the value of input impedance is approximately equal to ....

(*i*) h_{ie} (*ii*) h_{oe}

(*iii*) h_{re} (*iv*) none of the above

13. Using standard transistor *h* parameter nomenclature, the voltage gain in *CE* arrangement is ....

(*i*) $\dfrac{-h_{fe}}{Z_{in}\left(h_{oe}+\dfrac{1}{r_L}\right)}$

(*ii*) $\dfrac{-h_{fe}}{Z_{out}\left(h_{oe}+1\right)}$

(*iii*) $\dfrac{-h_{fe}}{h_{oe}+h_{re}}$

(*iv*) none of the above

14. $Z_{in} = h_{ie} - \dfrac{\cdots\cdots}{h_{oe}+\dfrac{1}{r_L}}$

(*i*) $h_{re}\,h_{oe}$ (*ii*) $h_{re}\,h_{fe}$

(*iii*) $r_L\,h_{oe}$ (*iv*) none of the above

15. .... *h* parameters of a transistor are dimensionless.

(*i*) four (*ii*) three

(*iii*) two (*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*i*)	**2.** (*ii*)	**3.** (*ii*)	**4.** (*i*)	**5.** (*iii*)
6. (*ii*)	**7.** (*ii*)	**8.** (*i*)	**9.** (*iii*)	**10.** (*ii*)
11. (*iii*)	**12.** (*i*)	**13.** (*i*)	**14.** (*ii*)	**15.** (*iii*)

Chapter Review Topics

1. What do you understand by hybrid parameters ? What are their dimensions ?
2. How will you measure *h* parameters of a linear circuit ?
3. Draw the *h* parameter equivalent circuit of a linear circuit.
4. What is the physical meaning of *h* parameters ?
5. Derive the general formula for :
   (*i*) input impedance (*ii*) current gain and (*iii*) voltage gain in terms of *h* parameters and the load.
6. What are the notations for *h* parameters of a transistor when used in (*i*) *CB* (*ii*) *CE* and (*iii*) *CC* arrangement ?
7. How are *h* parameters of a transistor measured ?
8. What are the drawbacks of *h* parameter approach in the design of a transistor amplifier ?

Problems

1. Determine the *h*-parameter values for the circuit shown in Fig. 24.16.

[$h_{11} = 8\Omega$; $h_{21} = -0.5$; $h_{12} = 0.5$; $h_{22} = 0.125$ ℧]

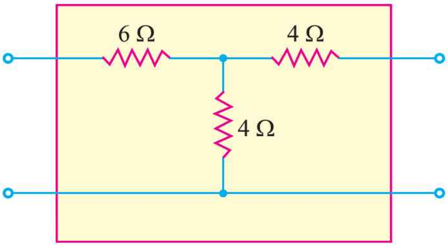


Fig. 24.16

2. Measurement of a circuit gives the following *h*-parameters :

$h_{11} = 10\ \text{k}\Omega$; $h_{12} = 0.5$; $h_{21} = 100$; $h_{22} = 2$ mS

Find v_1 and i_2 if $i_1 = 1$ mA and $v_2 = 2$V.

[$v_1 = 11$V ; $i_2 = 14$ mA]

3. A *CE* amplifier has h_{ie} = 1000Ω, h_{re} = 10^{-4}, h_{fe} = 100 and h_{oe} = 12 × 10^{-6}S. The load resistance = 2000 Ω. Find (*i*) current gain (*ii*) voltage gain (*iii*) output resistance.

[(*i*) 97.7 (*ii*) – 199.2 (*iii*) 5 × 10^5Ω]

4. A *CE* amplifier has h_{ie} = 1500Ω, h_{fe} = – 60 and h_{oe} = 12.5 × 10^{-6}S. The load resistance varies between 5 × 10^3Ω and 10 × 10^3Ω. Find the maximum and minimum values of (*i*) current gain (*ii*) voltage gain.

[(*i*) 36.9, 26.7 (*ii*) 178, 123]

5. An amplifier has values of R_C = 12 kΩ, R_L = 4.7 kΩ, R_1 = 33 kΩ, R_2 = 4.7 kΩ and I_C = 1 mA. At 1 mA, the transistor has *h*-parameter values of h_{ie} = 1 kΩ to 5 kΩ and h_{fe} = 70 to 350. Determine the values of (*i*) input impedance (*ii*) voltage gain for the circuit. Use approximate hybrid formulas.

[(*i*) 1.45 kΩ (*ii*) 236.9]

Discussion Questions

1. What is the origin of the name hybrid ?
2. How can we obtain an effective a.c. short-circuit across the output of an amplifier ? Does this affect d.c. operating conditions ?
3. When *h* parameters are specified for a particular transistor, the operating point is usually given. Why is this necessary ?
4. How can we obtain an effective a.c. open circuit at the input to an amplifier ? Does this affect d.c. operating conditions ?
5. Under what condition is the input impedance of a transistor equal to h_{ie} ?

25

Operational Amplifiers

25.1 Operational Amplifier
25.3 Basic Circuit of Differential Amplifier
25.5 Common-mode and Differential-mode signals
25.7 Voltage Gains of DA
25.9 D.C. Analysis of Differential Amplifier (DA)
25.11 Parameters of DA (or Op–amp) due to Mismatch of Transistors
25.13 A.C. Analysis of Differential Amplifier
25.15 Operational Amplifier (OP- Amp)
25.17 Output Voltage from Op-Amp
25.19 Bandwidth of an OP-Amp
25.21 Frequency Response of an OP-Amp
25.23 Applications of OP-Amps
25.25 Input and Output Impedance of Inverting Amplifier
25.27 Voltage Follower
25.29 Effect of Negative Feedback on OP-Amp impedances
25.31 Summary of OP-AMP Configurations
25.33 Applications of Summing Amplifiers
25.35 OP-Amp Integrator
25.37 OP-Amp Differentiator
25.39 Comparator Circuits

INTRODUCTION

Historically, an operational amplifier (*OP*-Amp) was designed to perform such mathematical operations as addition, subtraction, integration and differentiation. Hence, the name operational amplifier. An operational amplifier is a multistage amplifier and consists of a differential amplifier stage, a high-gain *CE* amplifier stage and class *B* push-pull emitter follower. An operational amplifier (*OP*-Amp) is an *integrated circuit and is widely used in computers, as video and audio amplifiers in communication electronics. Because of their multi-purpose use, *OP*-Amps are used in all branches of electronics, both digital and linear circuits. In this chapter, we shall discuss the various aspects of operational amplifiers.

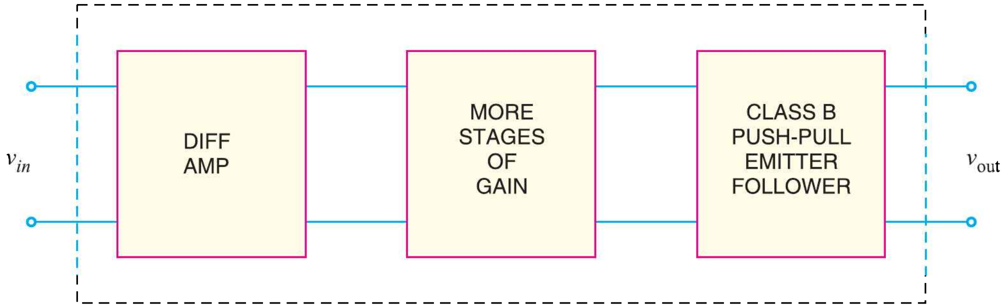
---

* All the components of an *OP*-Amp (*e.g.*, transistors, resistors etc.) are fabricated on a small chip called integrated circuit.

25.1 Operational Amplifier

An **operational amplifier** *(OP-Amp) is a circuit that can perform such mathematical operations as addition, subtraction, integration and differentiation.*

Fig. 25.1 shows the block diagram of an operational amplifier. Note that *OP*-Amp is a multistage amplifier. The three stages are : differential amplifier input stage followed by a high-gain *CE* amplifier and finally the output stage. *The key electronic circuit in an OP-Amp is the* **differential amplifier.** A differential amplifier (*DA*) can accept two input signals and amplifies the difference between these two input signals.



Block diagram of OP-Amp

Fig. 25.1

The following points may be noted about operational amplifiers (*OP*-Amps) :

(*i*) The input stage of an *OP*-Amp is a *differential amplifier* (*DA*) and the output stage is typically a class *B* push-pull emitter follower.

(*ii*) The internal stages of an *OP*-Amp are *direct-coupled i.e.*, no coupling capacitors are used. The direct coupling allows the *OP*-Amp to amplify d.c. as well as a.c. signals.

(*iii*) An OP-Amp has *very high input impedance* (ideally infinite) and *very low output impedance* (ideally zero). The effect of high input impedance is that the amplifier will draw a very small current (ideally zero) from the signal source. The effect of very low output impedance is that the amplifier will provide a constant output voltage independent of current drawn from the source.

(*iv*) An OP-Amp has *very high *open-loop voltage gain* (ideally infinite); typically more than 200,000.

(*v*) The OP-Amps are almost always operated with negative feedback. It is because the open-loop voltage gain of these amplifiers is very high and we can sacrifice the gain to achieve the advantages of negative feedback including large bandwidth (*BW*) and gain stability (Refer to chapter 13 of the book).

---

* The gain of an OP-Amp without feedback circuit is called open-loop gain. The gain of an *OP*-Amp with feedback circuit is called closed-loop gain. These terms were discussed in Chapter 13.

25.2 Differential Amplifier (DA)

Since differential amplifier (*DA*) is key to the operation of *OP*-Amp, we shall discuss this circuit in detail. So far in the book we have considered general-purpose amplifiers. In these conventional amplifiers, the signal (generally single input) is applied at the input terminals and amplified output is obtained at the output terminals. However, we can design an amplifier circuit that accepts two input signals and amplifies the difference between these two signals. Such an amplifier is called a **differential amplifier* (*DA*).

A **differential amplifier** *is a circuit that can accept two input signals and amplify the difference between these two input signals.*

Fig. 25.2 shows the block diagram of an ordinary amplifier. The input voltage v is amplified to Av where A is the voltage gain of the amplifier. Therefore, the ouput voltage is $v_0 = Av$.

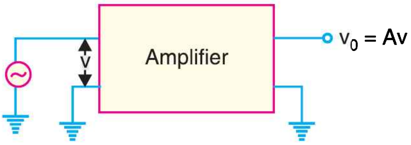


Fig. 25.2

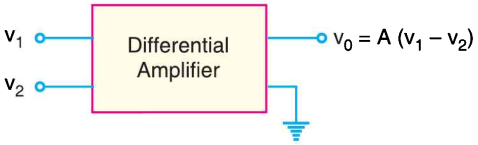


Fig.25.3

Fig. 25.3 shows the block diagram of a differential amplifier. There are two input voltages v_1 and v_2. This amplifier amplifies the difference between the two input voltages. Therefore, the output voltage is $v_0 = A(v_1 - v_2)$ where A is the voltage gain of the amplifier.

Example 25.1. *A differential amplifier has an open-circuit voltage gain of 100. The input signals are 3.25 V and 3.15V. Determine the output voltage.*

Solution.

Output voltage, $v_0 = A(v_1 - v_2)$

Here, $A = 100$; $v_1 = 3.25$ V : $v_2 = 3.15$V

$\therefore$ $v_0 = 100(3.25 - 3.15) = \textbf{10V}$

25.3 Basic Circuit of Differential Amplifier

Fig. 25.4(*i*) shows the basic circuit of a differential amplifier. It consists of two transistors Q_1 and Q_2 that have identical (ideally) characteristics. They share a common positive supply **V_{CC}, common emitter resistor R_E and common negative supply V_{EE}. Note that the circuit is symmetrical. Fig. 25.4(*ii*) shows the symbol of differential amplifier.

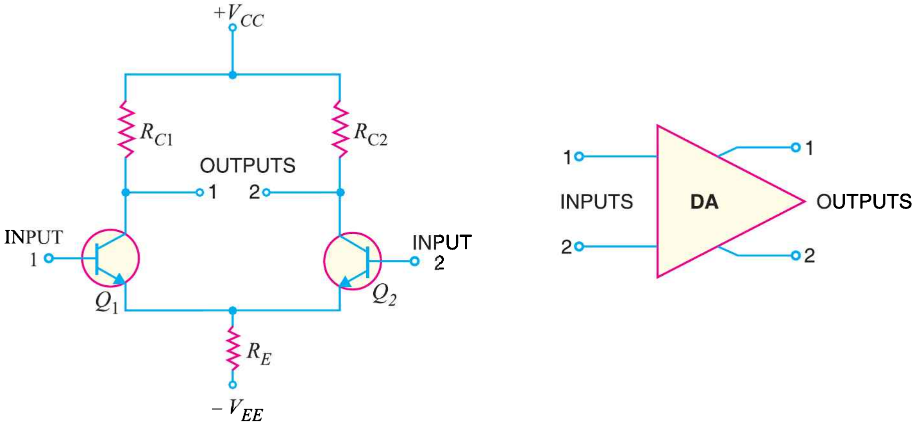
The following points may be noted about the differential amplifier :

(*i*) The differential amplifier (*DA*) is a two-input terminal device using atleast two transistors. There are two output terminals marked 1 ($v_{out\ 1}$) and 2($v_{out\ 2}$).

---

* The name is appropriate because the amplifier is amplifying the difference between the two input signals.

** Note that for this circuit, we need two supply voltages viz. + V_{CC} and $-V_{EE}$. The negative terminal of V_{CC} is grounded and positive terminal of V_{EE} is grounded.



(*i*) (*ii*)

Fig. 25.4

(***ii***) The *DA* transistors Q_1 and Q_2 are matched so that their characteristics are the same. The collector resistors (R_{C1} and R_{C2}) are also equal. The equality of the matched circuit components makes the *DA* circuit arrangement completely symmetrical.

(***iii***) We can apply signal to a differential amplifier (*DA*) in the following two ways :

(***a***) The signal is applied to one input of *DA* and the other input is grounded. In that case, it is called *single-ended input* arrangement.

(***b***) The signals are applied to both inputs of *DA*. In that case, it is called *dual-ended* or *double-ended input* arrangement.

(***iv***) We can take output from *DA* in the following two ways :

(***a***) The output can be taken from one of the output terminals and the ground. In that case, it is called *single-ended output* arrangement.

(***b***) The output can be taken between the two output terminals (*i.e.*, between the collectors of Q_1 and Q_2). In that case, it is called *double-ended output* arrangement or *differential output*.

(***v***) *Generally, the differential amplifier (DA) is operated for single-ended output.* In other words, we take the output either from output terminal 1 and ground or from output terminal 2 and ground. Any input/output terminal that is grounded is at *0V*.

25.4 Operation of Differential Amplifier

For *simplicity, we shall discuss the operation of single-ended input (*i.e.*, signal is applied to one input of *DA* and the other input is grounded) and double-ended output *DA*.

(***i***) Suppose the signal is applied to input 1 (*i.e.*, base of transistor Q_1) and input 2 (*i.e.*, base of transistor Q_2) is grounded as shown in Fig. 25.5. The transistor Q_1 will act in two ways : as a common emitter amplifier and as a common collector amplifier. As a common emitter amplifier, the input signal to Q_1 (input 1) will appear at output 1 (*i.e.*, collector of Q_1) as amplified inverted signal as shown in Fig. 25.5. As a common collector amplifier, the signal appears on the emitter of Q_1 in phase with the input and only slightly smaller. Since the emitters of Q_1 and Q_2 are common, the emitter signal becomes input to Q_2. Therefore, Q_2 functions as a *common base amplifier. As a result, the signal on the emitter of Q_2 will be amplified and appears on output 2 (*i.e.*, collector of Q_2) in phase with the emitter signal and hence in phase with the input signal (signal at input 1). This is illustrated in Fig. 25.5.

---

* The operation of double-ended input *DA* will then be easier to understand.

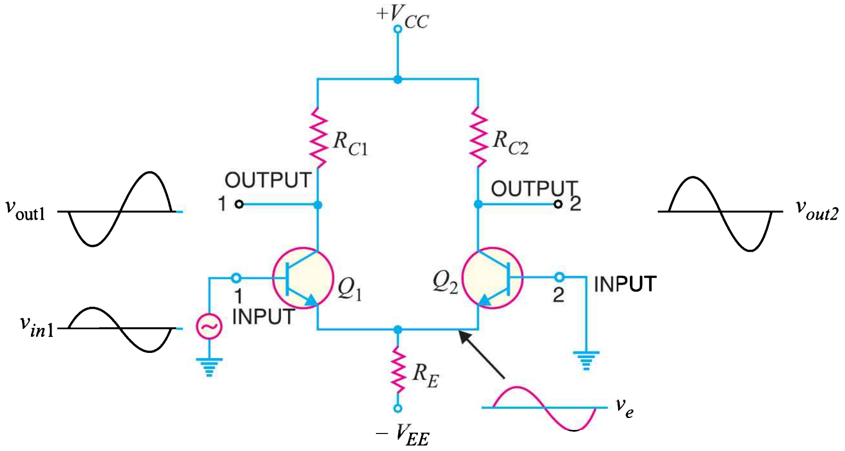


Fig. 25.5

(*ii*) Now suppose the signal is applied to input 2(*i.e.*, base of transistor Q_2) and input 1(base of transistor Q_1) is grounded. As explained above, now Q_2 acts as a common emitter amplifier and common collector amplifier while Q_1 functions as a common base amplifier. Therefore, an inverted and amplified signal appears at output 2 (*i.e.*, at collector of Q_2) and non-inverted, amplified signal appears at output 1(*i.e.*, at collector of Q_1). This is illustrated in Fig. 25.6.

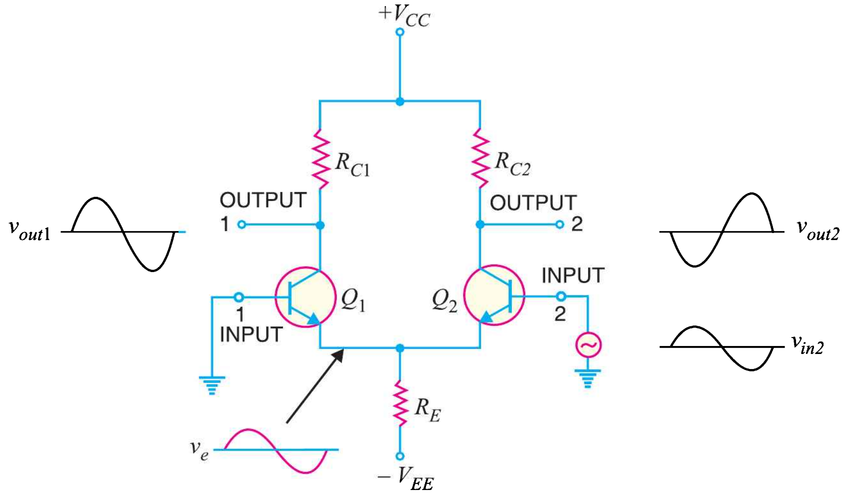


Fig. 25.6

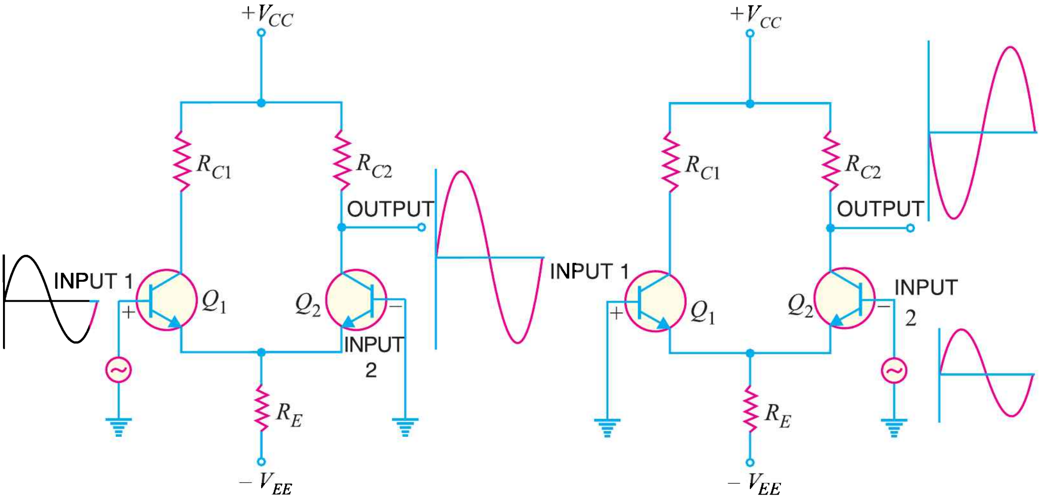
The following points are worth noting about single-ended input *DA* :

(*a*) When signal is applied to input 1 (*i.e.*, base of transistor Q_1 in Fig. 25.5), an inverted, amplified signal appears at output 1 and non-inverted, amplified signal appears at output 2. Reverse happens when signal is applied to input 2 and input 1 is grounded.

---

* In a common base amplifier, output signal is in phase with the input signal. Recall that only in *CE* amplifier, the output voltage is 180° out of phase with the input voltage.

(*b*) When only one output terminal is available, the phase of the output of single-ended input *DA* depends on which input receives the input signal. This is illustrated in Fig. 25.7.



(*i*) Noninverting input (*ii*) Inverting input

Fig. 25.7

When signal applied to the input of *DA* produces no phase shift in the output, it is called *noninverting input* [See Fig. 25.7 (*i*)]. In other words, for noninverting input, the output signal is in phase with the input signal. When the signal applied to the input of *DA* produces 180° phase shift, it is called *inverting input* [See Fig. 25.7 (*ii*)]. In other words, for inverting input, the output signal is 180° out of phase with the input signal. Since inverting input provides 180° phase shift, it is often identified with –sign. The noninverting input is then represented by +*sign. It may be noted that terms noninverting input and inverting input are meaningful when only one output terminal of *DA* is available.

25.5 Common-mode and Differential-mode Signals

The importance of a differential amplifier lies in the fact that the outputs are proportional to the *difference* between the two input signals. Thus the circuit can be used to amplify the difference between the two input signals or amplify only one input signal simply by grounding the other input. The input signals to a *DA* are defined as :

(*i*) Common-mode signals (*ii*) Differential-mode signals

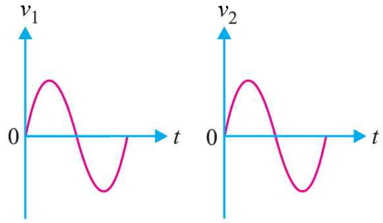
(*i*) Common-mode signals : When the input signals to a *DA* are in phase and exactly equal in amplitude, they are called *common-mode signals* as shown in Fig. 25.8. The common-mode signals are rejected (not amplified) by the differential amplifier. It is because a differential amplifier amplifies the difference between the two signals ($v_1 - v_2$) and for common-mode signals, this difference is zero. Note that for common-mode operations, $v_1 = v_2$.

(*ii*) Differential-mode signals. When the input signals to a *DA* are 180° out of phase and exactly equal in amplitude, they are called *differential-mode signals* as shown in Fig. 25.9.

The differential-mode signals are amplified by the differential amplifier. It is because the difference in the signals is twice the value of each signal. For differential-mode signals, $v_1 = -v_2$.

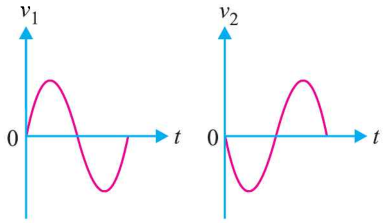
---

* Note that in Fig. 25.7, the noninverting input terminal is given the +ve sign while the inverting input terminal is given the –ve sign.



Common-mode signals

Fig. 25.8



Differential-mode signals

Fig. 25.9

Thus we arrive at a very important conclusion that a differential amplifier will amplify the differential-mode signals while it will reject the common-mode signals.

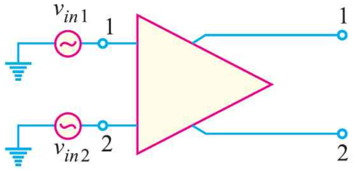
25.6 Double-ended Input Operation of DA

A differential amplifier (*DA*) has two inputs so that it can simultaneously receive two signals. The input signals to a *DA* are defined as :

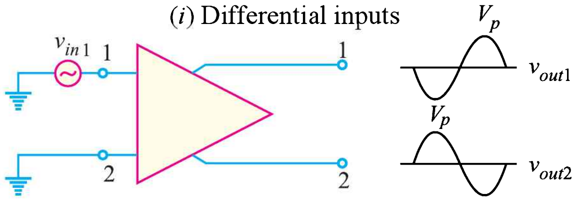
(*i*) Differential-mode signals **(*ii*)** Common-mode signals

The differential-mode signals are equal in amplitude but 180° out of phase. The common-mode signals are equal in magnitude and have the same phase.

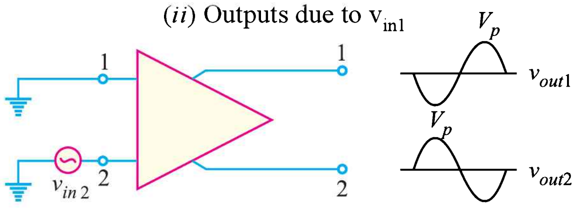
(*i*) Differential input. In this mode (arrangement), two opposite-polarity (180° out of phase) signals are applied to the inputs of *DA* as shown in Fig. 25.10 (*i*).



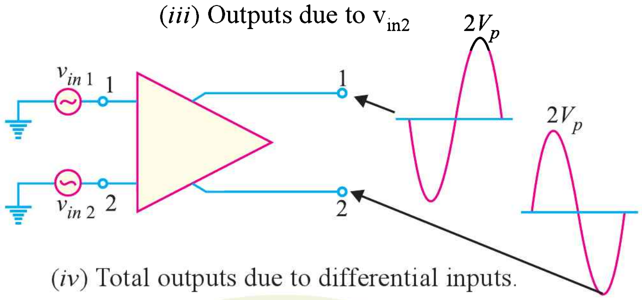
(*i*) Differential inputs



(*ii*) Outputs due to v_{in1}



(*iii*) Outputs due to v_{in2}

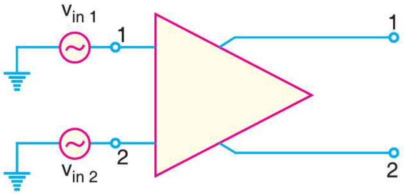


(*iv*) Total outputs due to differential inputs.

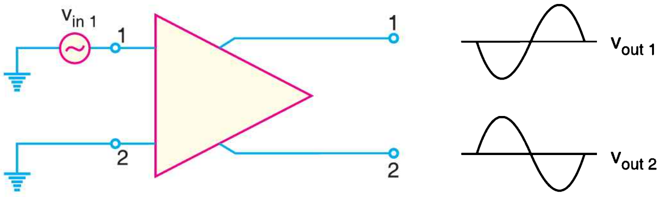
Fig. 25.10

As we shall see, each input affects the *outputs. Fig. 25.10 (*ii*) shows the output signals due to the signal on input 1 acting alone as a single-ended input. Fig. 25.10 (*iii*) shows the output signals due to the signal on **input 2 acting alone as a single-ended input. Note that in Figs. 25.10 (*ii*) and (*iii*), the signals on output 1 are of the same polarity. The same is also true for output 2. By superimposing both output 1 signals and both output 2 signals, we get the total outputs due to differential inputs [See Fig. 25.10(*iv*)].

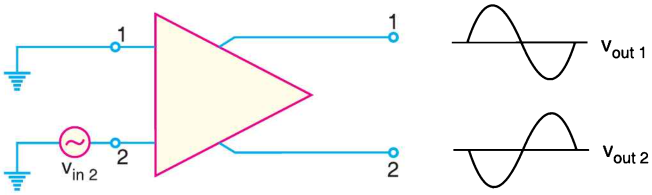
(*ii*) Common-mode input. In this mode, two signals equal in amplitude and having the same phase are applied to the inputs of *DA* as shown in Fig. 25.11(*i*).



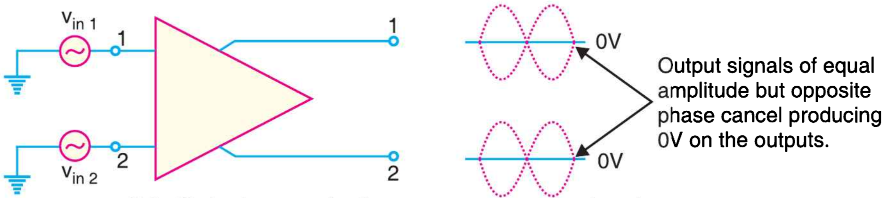
(*i*) Common-mode inputs



(*ii*) Outputs due to v_{in1}



(*iii*) Outputs due to v_{in2}



Output signals of equal amplitude but opposite phase cancel producing 0V on the outputs.

(*iv*) Outputs cancel when common-mode signals are applied.

Fig. 25.11

---

* Note that in all the Figures in Fig. 25.10, the phase of the input signal is given in the circle and the phase shift in the output signal is given at the output terminals. Thus in Fig. 25.10 (*ii*), the output signal at terminal 1 is 180° out of phase with the input signal. On the other hand, the output signal at terminal 2 is in phase with the input signal.

** Note that a *DA* amplifies $(v_1 - v_2)$. For Fig. 25.10 (*ii*), $v_{in1} - v_{in2} = v_{in1} - 0 = v_{in1}$. For Fig. 25.10 (*iii*), $v_{in1} - v_{in2} = 0 - v_{in2} = -v_{in2}$.

Again, by considering each input signal acting alone, the basic operation of *DA* in this mode can be explained. Fig. 25.11 (*ii*) shows the output signals due to the signal on only input 1 while Fig. 25.11 (*iii*) shows the output signals due to the signal on only input 2. Note that the corresponding signals on output 1 are of the opposite polarity and so are the ones on output 2. When these are superimposed, they cancel, resulting in zero output voltage as shown in Fig. 25.11 (*iv*).

It is important to note that common-mode signals are rejected by *DA*. This action is called *common-mode rejection.* Most of noises and other unwanted signals are common-mode signals. When these unwanted signals appear on the inputs of a *DA*, they are virtually eliminated on the output.

25.7 Voltage Gains of DA

The voltage gain of a *DA* operating in differential mode is called *differential-mode voltage gain* and is denoted by A_{DM}. The voltage gain of *DA* operating in common-mode is called *common-mode voltage gain* and is denoted by A_{CM}.

Ideally, a *DA* provides a very high voltage gain for differential-mode signals and zero gain for common-mode signals. However, practically, differential amplifiers do exhibit a very small common-mode gain (usually much less than 1) while providing a high differential voltage gain (usually several thousands). The higher the differential gain w.r.t. the common-mode gain, the better the performance of the *DA* in terms of rejection of common-mode signals.

25.8 Common-mode Rejection Ratio (CMRR)

A differential amplifier should have high differential voltage gain (A_{DM}) and very low common-mode voltage gain (A_{CM}). The ratio A_{DM}/A_{CM} is called common-mode rejection ratio (*CMRR*) *i.e.*,

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

Very often, the *CMRR* is expressed in decibels (*dB*). The decibel measure for *CMRR* is given by;

$$CMRR_{dB} = 20\log_{10}\frac{A_{DM}}{A_{CM}} = 20\log_{10} CMRR$$

The following table shows the relation between the two measurements :

CMRR	$CMRR_{dB}$
10	20dB
10^3	60dB
10^5	100dB
10^7	140dB

Importance of CMRR. The *CMRR* is the ability of a *DA* to reject the common-mode signals. The larger the *CMRR*, the better the *DA* is at eliminating common-mode signals. Let us illustrate this point. Suppose the differential amplifier in Fig. 25.12 has a differential voltage gain of 1500 (*i.e.*, A_{DM} = 1500) and a common-mode gain of 0.01 (*i.e.*, A_{CM} = 0.01).

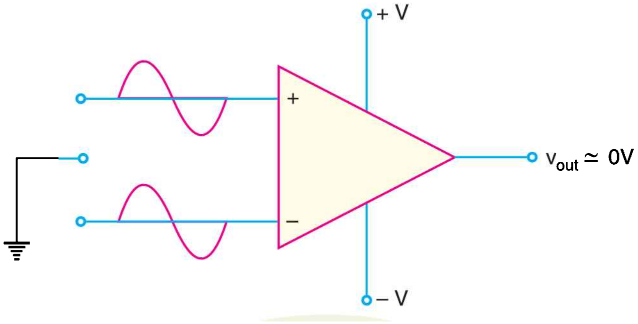


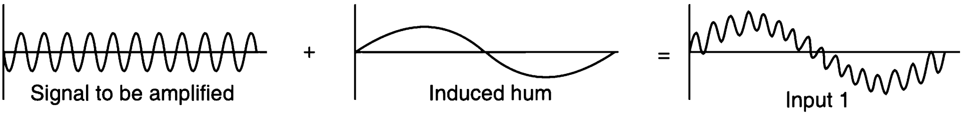
Fig. 25.12

$$\therefore \qquad CMRR = \frac{1500}{0.01} = 150{,}000$$

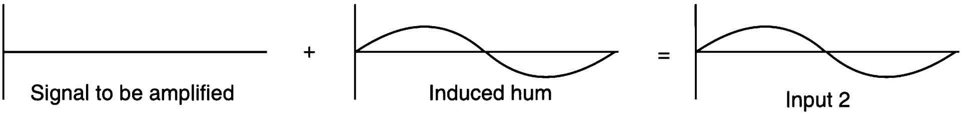
This means that the output produced by a difference between the inputs would be 150,000 times as great as an output produced by a common-mode signal.

The ability of the *DA* to reject common-mode signals is one of its main advantages. Common-mode signals are usually ***undesired signals*** caused by external interference. For example, any *RF* signals picked up by the *DA* inputs would be considered undesirable. The *CMRR* indicates the *DA*'s ability to reject such unwanted signals.

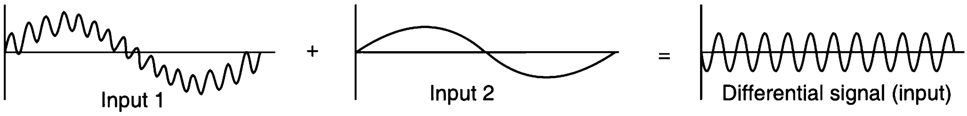
Practical Illustrations. Fig. 25.13 shows how a differential amplifier (*DA*) rejects hum and static voltages induced into its input leads.



(*i*) Signal input to input 1



(*ii*) Signal input to input 2



(*iii*) Differential input signal

Fig. 25.13

(*i*) In Fig. 25.13(*i*), the signal is applied to input 1 of the *DA*. However, a low frequency *hum* voltage is also induced into the lead wire. This hum is produced due to building and collapsing magnetic field generated by adjacent conductor carrying 50Hz current. The resultant waveform is shown in Fig. 25.13 (*i*). If this waveform is amplified by a conventional amplifier, the 50 Hz hum in the output will be stronger than the desired signal.

Low voltage differential amplifier for test and measurement applications.

(*ii*) However, a *DA* also has second input (input 2). Therefore, the lead of second input has the same phase 50 Hz hum induced into it. This is the only voltage (*i.e.*, hum) applied to input 2 as shown in Fig. 25.13(*ii*).

(*iii*) As shown in Fig. 25.13 (*iii*), the hum components of the two inputs form a common-mode signal which is largely rejected by the *DA*. If the input hum signals are equal at the input, then differential input to *DA* will be devoid of hum. Therefore, the amplified output of *DA* will be free from the hum.

Note : We have considered the ideal case *i.e.* $A_{CM} = 0$. Even in a practical case, the value of A_{CM} is less than 1 while A_{DM} is over 200. This means that the desired signal would be over 200 times larger than the hum at the output terminal.

Example 25.2. *A certain differential amplifier has a differential voltage gain of 2000 and a common mode gain of 0.2. Determine CMRR and express it in dB.*

Solution.

$$CMRR = \frac{A_{DM}}{A_{CM}} = \frac{2000}{0.2} = \mathbf{10{,}000}$$

$$CMRR_{dB} = 20 \log_{10} 10{,}000 = \mathbf{80dB}$$

Example 25.3. *A differential amplifier has an output of 1V with a differential input of 10 mV and an output of 5 mV with a common-mode input of 10 mV. Find the CMRR in dB.*

Solution. Differential gain, $A_{DM} = 1\text{V}/10\text{ mV} = 100$

Common-mode gain, $A_{CM} = 5\text{ mV}/10\text{ mV} = 0.5$

$$\therefore \quad CMRR_{dB} = 20 \log_{10} (100/0.5) = \mathbf{46\ dB}$$

Example 25.4. *A differential amplifier has a voltage gain of 150 and a CMRR of 90 dB. The input signals are 50 mV and 100 mV with 1 mV of noise on each input. Find (i) the output signal (ii) the noise on the output.*

Solution.

(*i*) Output signal, $v_{out} = A_{DM}(v_1 - v_2) = 150\ (100\text{ mV} - 50\text{ mV}) = \mathbf{7.5\ V}$

(*ii*) $CMRR_{dB} = 20 \log_{10} (150/A_{CM})$

or $90 = 20 \log_{10} (150/A_{CM})$

$\therefore \quad A_{CM} = 4.7 \times 10^{-3}$

Noise on output $= A_{CM} \times 1\text{ mV} = 4.7 \times 10^{-3} \times 1\text{mV} = \mathbf{4.7 \times 10^{-6}\ V}$

Example 25.5. *The differential amplifier shown in Fig. 25.14 has a differential voltage gain of 2500 and a CMRR of 30,000. A single-ended input signal of 500 µV r.m.s. is applied. At the same time, 1V, 50 Hz interference signal appears on both inputs as a result of radiated pick-up from the a.c. power system.*

(*i*) *Determine the common-mode gain.*

(*ii*) *Express the CMRR in dB.*

(*iii*) *Determine the r.m.s. output signal.*

(*iv*) *Determine the r.m.s. interference voltage on the output.*

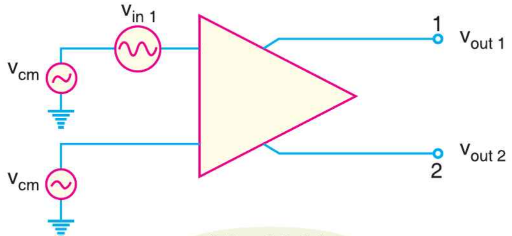


Fig. 25.14

Solution. (*i*) $$CMRR = \frac{A_{DM}}{A_{CM}}$$

$$\therefore \quad A_{CM} = \frac{A_{DM}}{CMRR} = \frac{2500}{30{,}000} = \mathbf{0.083}$$

(*ii*) $$CMRR_{dB} = 20\log_{10}(30{,}000) = \mathbf{89.5\ dB}$$

(*iii*) In Fig. 25.14, the differential input voltage is the difference between the voltages on input 1 and that on input 2. Since input 2 is grounded, its voltage is zero.

$\therefore$ Differential input voltage = 500 μV – 0 = 500 μV

The output signal in this case is taken at output 1.

$$\therefore \quad v_{out1} = A_{DM} \times (500\ \mu V) = (2500 \times 500)\ \mu V = \mathbf{1.25\ V}$$

(*iv*) The common-mode input is 1 V r.m.s. and the common-mode gain is $A_{CM} = 0.083$.

$\therefore$ Noise on the output = $A_{CM} \times (1\text{ V}) = (0.083)\,(1\text{ V}) = \mathbf{83\ mV}$

25.9 D.C. Analysis of Differential Amplifier (DA)

When no signal is applied to a *DA*, d.c. or quiescent conditions prevail in the circuit. From the transistor circuit theory, we can find *bias voltages and bias currents in the circuit. Fig. 25.15 shows the basic arrangement for an *npn* differential amplifier. Typical circuit values have been assumed to make the treatment illustrative. The circuit is symmetrical *i.e.*, the transistors Q_1 and Q_2 are identical; collector loads are equal ($R_{C1} = R_{C2}$) and base resistors R_B are equal. We assume that base current is very small so that we can ignore the voltage drops across base resistors *i.e.*,

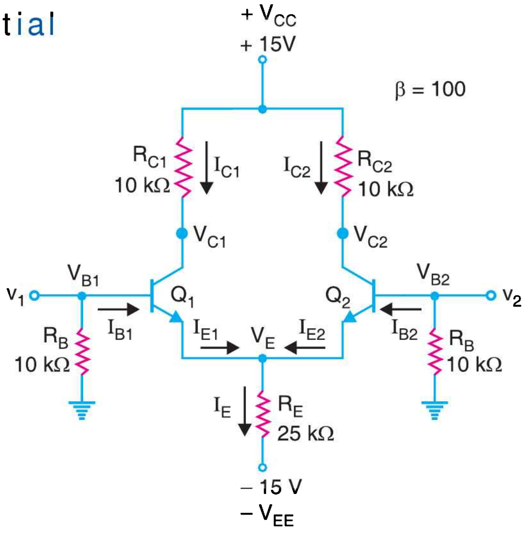


Fig. 25.15

$$V_{B1} = V_{B2} \simeq {**}0V$$

Now $$V_E = V_{B1} - 0.7 = V_{B2} - 0.7 = {***}0 - 0.7 = -0.7\ \text{V}$$

$$\therefore \quad V_{E1} = V_{E2} = V_E = \mathbf{-0.7\ V}$$

$$\dagger\ \text{Voltage across } R_E = V_{EE} - V_{BE}$$

$$\text{Current in } R_E,\ I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

---

* Bias voltages and currents mean d.c. values.

** As we shall see, for the considered circuit values, $I_{B1} = I_{B2} = 2.86\ \mu A$.

$\therefore$ Base voltage, $V_B = I_B \times R_B = 2.86\ \mu A \times 10\ k\Omega = 28.6\ mV$. Compared to the –15V of V_{EE}, this is a negligible amount of voltage.

*** $V_{BE} = 0.7$ V. There is a plus-to-minus drop in going from the base to emitter. Since base voltage is 0V, $V_E = -0.7$ V.

† Applying Kirchhoff's voltage law to the loop consisting of V_{EE}, the base-emitter junction of Q_1 and R_B, we have,

$$V_{RE} = V_{EE} - V_{BE} - V_{RB} = V_{EE} - V_{BE} - 0 = V_{EE} - V_{BE}$$

The current through the emitter resistor R_E is called †**tail current.** For the circuit values considered in Fig.25.15, we have,

$$\text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{(15 - 0.7)\text{V}}{25\text{ k}\Omega} = \mathbf{0.572\ mA}$$

Because of the symmetry in the circuit, I_E must split equally between Q_1 and Q_2.

$$\therefore \qquad I_{E1} = I_{E2} = \frac{I_E}{2} = \frac{0.572\text{ mA}}{2} = \mathbf{0.286\ mA}$$

$$\text{Now} \qquad I_{C1} \simeq I_{E1} = \mathbf{0.286\ mA}\ ;\ I_{C2} \simeq I_{E2} = \mathbf{0.286\ mA}$$

$$\text{Also} \qquad I_{B1} = \frac{I_{C1}}{\beta} = \frac{0.286\text{ mA}}{100} = \mathbf{2.86\ \mu A}\ ;\ I_{B2} = \frac{I_{C2}}{\beta} = \mathbf{2.86\ \mu A}$$

$$V_{C1} = V_{CC} - I_{C1}R_{C1} = 15\text{ V} - 0.286\text{ mA} \times 10\text{ k}\Omega = \mathbf{12.1\ V}$$

$$V_{C2} = V_{CC} - I_{C2}R_{C2} = 15\text{ V} - 0.286\text{ mA} \times 10\text{ k}\Omega = \mathbf{12.1\ V}$$

Note that bold type results are bias voltages or bias currents. An important point to see is that $V_{C1} = V_{C2} = 12.1$ V. It means that there is no potential difference between the collectors. Therefore, the differential d.c. output for a balanced *DA* is zero.

Example 25.6. *Find the bias voltages and currents for the differential amplifier circuit shown in Fig. 25.16.*

Solution. Note that there is no resistor in the collector circuit of Q_1. This makes no difference in the values of the two collector currents because the collector currents are determined by the emitter circuit, not the collector circuit. This arrangement will only affect V_{C1}. Because of symmetry in the base-emitter circuits of Q_1 and Q_2, we have,

$$I_{E1} = I_{E2} = \frac{I_E}{2}$$

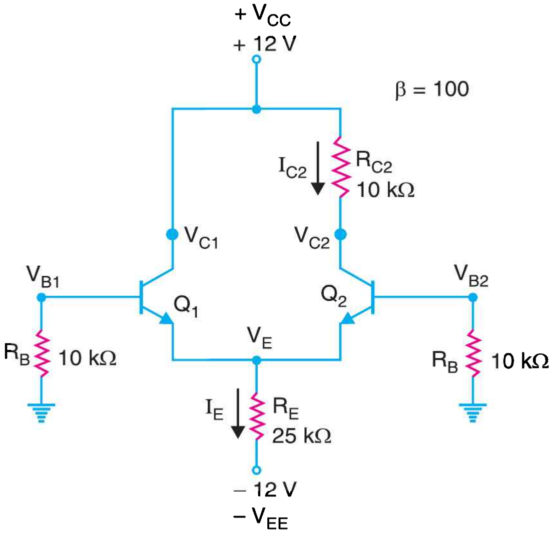


Fig. 25.16

Ignoring the base current, the emitter voltage for both transistors is $V_E = \mathbf{-\ 0.7\ V.}$

$$\text{Now,} \qquad \text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{(12 - 0.7)V}{25\text{ k}\Omega} = \mathbf{0.452\ mA}$$

$$\therefore \qquad I_{E1} = I_{E2} = I_E/2 = 0.452\text{ mA}/2 = \mathbf{0.226\ mA}$$

---

† If you look at the circuit, you can see that emitter resistor R_E is like a tail.

Now, $I_{C1} = I_{C2} = \mathbf{0.226\ mA}$ $(\because I_{C1} \simeq I_{E1} \text{ and } I_{C2} \simeq I_{E2})$

$\therefore$ $I_{B1} = I_{B2} = 0.226\ \text{mA}/\beta = 0.226\ \text{mA}/100 = \mathbf{2.26\ \mu A}$

$V_{C1} = V_{CC} = \mathbf{12V}\ ;\ V_{C2} = V_{CC} - I_{C2}R_{C2} = 12 - 0.226\ \text{mA} \times 10\ \text{k}\Omega = \mathbf{9.7V}$

Example 25.7. *In Fig. 25.17, the transistors are identical with β_{dc} = 100. Find the output voltage.*

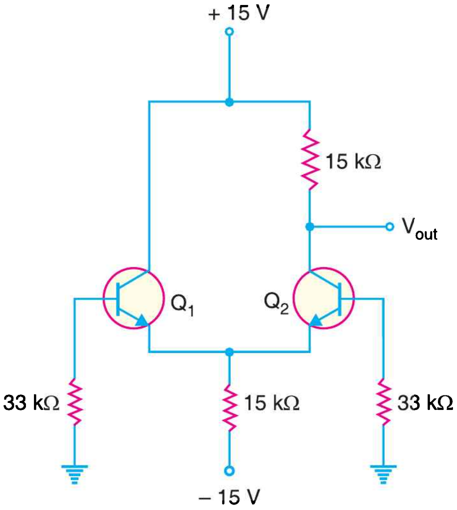


Fig. 25.17

Solution. Tail current, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{(15 - 0.7)V}{15\ \text{k}\Omega} = 0.953\ \text{mA}$

Since the transistors are identical, the tail current I_E splits equally between the two transistors. Therefore, emitter current of each transistor = 0.953 mA/2 = 0.477 mA.

Since $I_C \simeq I_E = 0.477$ mA, $V_{out} = V_{CC} - I_C R_C = 15 - 0.477\ \text{mA} \times 15\ \text{k}\Omega = \mathbf{7.85\ V}$

Example 25.8. *In Fig. 25.17, the transistors are identical except for β_{dc}. The left transistor has β_{dc} = 90 and the right transistor has β_{dc} = 110. Find (i) base currents (ii) base voltages. Assume V_{BE} = 0V.*

Solution. (*i*) Tail current, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{(15 - 0)V}{15\ \text{k}\Omega} = 1\text{mA}$

Therefore, the emitter current in each transistor = 1/2 = 0.5 mA.

The base current in the left transistor is

$$I_{B1} = 0.5\ \text{mA}/90 = \mathbf{5.56\ \mu A}$$

The base current in the right transistor is

$$I_{B2} = 0.5\ \text{mA}/110 = \mathbf{4.55\ \mu A}$$

(*ii*) Voltage on left base, $V_{B1} = -^{*}(5.56\ \mu\text{A}) \times (33\ \text{k}\Omega) = \mathbf{-0.183\ V}$

Voltage on right base, $V_{B2} = -(4.55\ \mu\text{A}) \times (33\ \text{k}\Omega) = \mathbf{-0.15\ V}$

Since the transistors are not identical, the base currents and base voltages are different.

Example 25.9. *Most differential amplifiers are biased with a current source as shown in Fig. 25.18. Find the bias currents and voltages.*

---

* Note that for the ideal case, emitter of each transistor is at 0V.

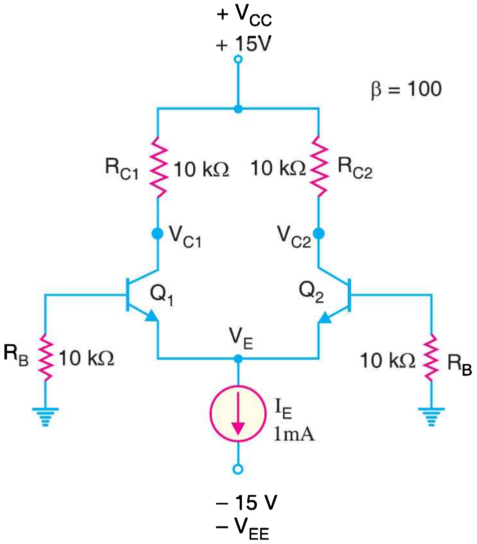

+ V_{CC}
+ 15V
β = 100
R_{C1}
10 kΩ
10 kΩ
R_{C2}
V_{C1}
V_{C2}
Q_1
Q_2
V_E
R_B
10 kΩ
10 kΩ
R_B
I_E
1mA
– 15 V
– V_{EE}

Fig. 25.18

Solution. In this circuit, the current I_E is given by the current source. Ignoring base current, the potential at each emitter is V_E **= –0.7 V.**

Emitter current in each transistor = $I_E/2$ = 1mA/2 = **0.5 mA**

Also $I_{C1} \simeq I_{E1}$ **= 0.5 mA** ; $I_{C2} \simeq I_{E2}$ **= 0.5 mA**

∴ $V_{C1} = V_{C2}$ = 15 – 0.5 mA × 10 kΩ = **10V**

Example 25.10. *Fig. 25.19 shows a differential amplifier constructed with pnp transistors. Find the bias currents and voltages.*

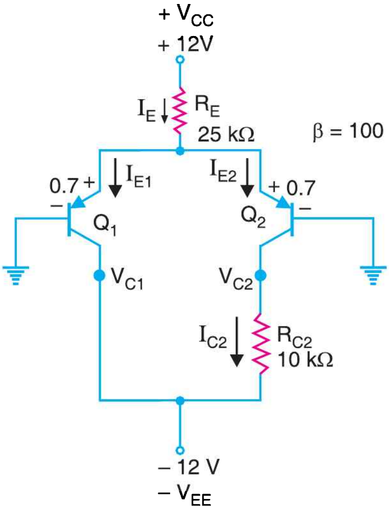

+ V_{CC}
+ 12V
I_E
R_E
25 kΩ
β = 100
0.7 +
–
I_{E1}
I_{E2}
+ 0.7
–
Q_1
Q_2
V_{C1}
V_{C2}
I_{C2}
R_{C2}
10 kΩ
– 12 V
– V_{EE}

Fig. 25.19

Solution. For the *pnp* transistor, the emitter voltage (V_E) is a diode drop above the base voltage. Therefore, V_E **= + 0.7 V.**

$$\text{Tail current, } I_E = \frac{V_{CC} - V_E}{R_E} = \frac{(12 - 0.7)V}{25\text{ k}\Omega} = \mathbf{0.452\ mA}$$

Current in each emitter of transistor = 0.452 mA/2 = **0.226 mA**

Now, $I_{C1} \simeq I_{E1} = \mathbf{0.226\ mA}$ and $I_{C2} \simeq I_{E2} = \mathbf{0.226\ mA}$

$$V_{C1} = -V_{EE} = \mathbf{-12V}\ ;\ V_{C2} = -V_{EE} + I_{C2}R_{C2} = -12 + 0.226\ \text{mA} \times 10\ \text{k}\Omega = \mathbf{-9.74\ V}$$

25.10 Overview of Differential Amplifier

Fig. 25.20 shows double-ended input and single-ended output differential amplifier (*DA*). In other words, there are two input signals and one output signal. *A DA is *normally operated in this fashion.* When input signal v_1 (input 1) is applied, the output signal is in phase with the input signal *i.e.*, there is no phase shift in the output signal. For this reason, input signal v_1 is called ***non-inverting input***. When input signal v_2 (input 2) is applied, the output signal is 180° out of phase with the input signal. For this reason, input signal v_2 is called ***inverting input***.

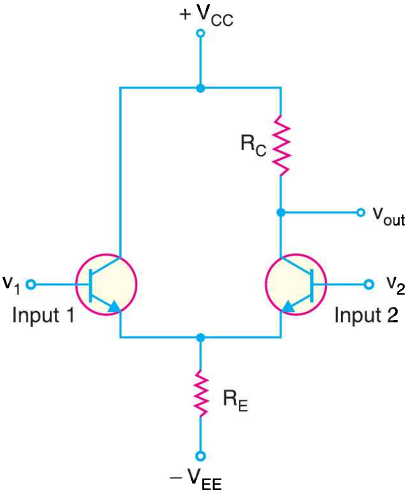


Fig. 25.20

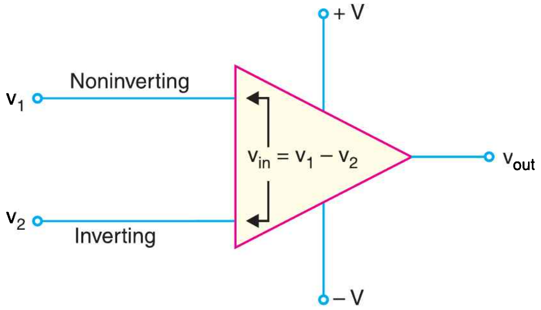


Fig. 25.21

The differential amplifier amplifies the difference between the two input voltages. This point is illustrated in Fig. 25.21. The difference between the input voltages is $v_{in} = v_1 - v_2$ *i.e.*,

$$v_{in} = v_1 - v_2$$

where v_1 = the voltage applied to the noninverting input

v_2 = the voltage applied to the inverting input

v_{in} = the difference voltage that will be amplified

It is important to remember that the differential amplifier is amplifying the difference between the input terminal voltages.

25.11 Parameters of DA (or OP–amp) due to Mismatch of Transistors

Our discussion on the differential amplifier (*DA*) has been based on the assumption that the transistors are ***perfectly matched*** *i.e.*, they have exactly the same electrical characteristics. In practice, this cannot happen. There will always be ***some*** difference between the characteristics of the two transistors. This leads us to the following two parameters of *DA* (or *OP*– amp) :

1. Output offset voltage **2.** Input offset current

1. Output Offset Voltage. Even though the transistors in the differential amplifier are very closely matched, there are some differences in their electrical characteristics. One of these differences is found in the values of V_{BE} for the twso transistors. When $V_{BE1} \neq V_{BE2}$, an imbalance is created in the differential amplifier. The *DA* (or *OP*-amp) may show some voltage at the output even when the voltage applied between two input terminals is zero. This is called *output offset voltage*. This point is illustrated in Fig. 25.22. Note that with the inputs of *DA* grounded, the output shows a measurable voltage. This voltage is a result of the imbalance in the differential amplifier, which causes one of the transistors to conduct harder than the other.

---

* One input can be grounded (*i.e.*, at 0V).

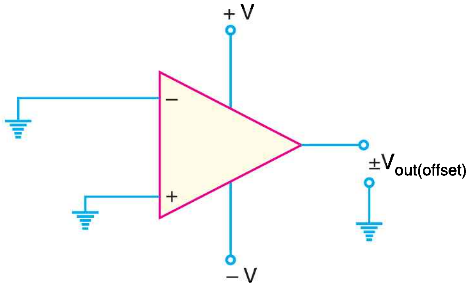


Fig. 25.22

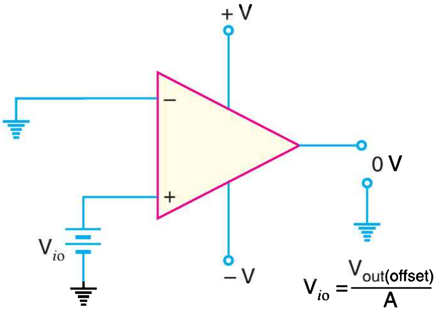


Fig. 25.23

There are several methods that may be used to eliminate output offset voltage. One of these is to apply an *input offset voltage* between the input terminals of *DA* (or *OP*- amp) so as to make output 0*V* as shown in Fig. 25.23. The value of input offset voltage (V_{i0}) required to eliminate the output offset voltage is given by;

$$V_{i0} = \frac{V_{out}(offset)}{A} \quad \text{...} A \text{ is voltage gain.}$$

2. Input Offset Current. When the output offset voltage of a *DA* (or *OP*- amp) is eliminated, there will be a slight difference between the input currents to the noninverting and inverting inputs of the device. This slight difference in input currents is called *input offset current* and is caused by a beta (β) mismatch between the transistors in the differential amplifier. As an example, suppose I_{B1} = 75 μA and I_{B2} = 65 μA. Then,

$$I_{in\,(offset)} = 75 - 65 = 10\ \mu\text{A}$$

The difference in the base currents indicates how closely matched the transistors are. If the transistors are identical, the input offset current is zero because both base currents will be equal. But in practice, the two transistors are different and the two base currents are not equal.

25.12 Input Bias Current

The inputs to an OP- amp require some amount of d.c. biasing current for the transistors in the differential amplifier. The *input bias current* is defined as the average of the two d.c. base currents *i.e.*,

$$I_{in(bias)} = \frac{I_{B1} + I_{B2}}{2}$$

For example, if I_{B1} = 85 μA and I_{B2} = 75 μA, then the input bias current is

$$I_{in(bias)} = \frac{85 + 75}{2} = 80\mu\text{A}$$

This means that when no signal is applied, the inputs of *OP*- amp (*i.e.*, *DA*) will draw a d.c. current of 80 μA.

The fact that both transistors in the differential amplifier require an input biasing current leads to the following operating restriction : ***An OP- amp will not work if either of its inputs is open.*** For example, look

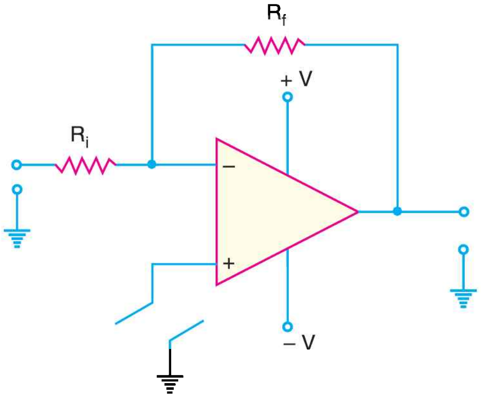


Fig. 25.24

at the circuit shown in Fig. 25.24. The *non-inverting input is shown to have an open between the OP- amp and ground. The open circuit would not allow the d.c. biasing current required for the operation of the differential amplifier (***The transistor associated with the inverting input would work but not the one associated with the non-inverting input***). Since the differential amplifier would not work, the overall *OP*-amp circuit would not work. Thus an input bias current path must always be provided for *both OP*-amp inputs.

Example 25.11. *In Fig. 25.25, the left transistor has* β_{dc} *= 90 and the right transistor has* β_{dc} *= 110. Find (i) the input offset current (ii) input bias current. Neglect* V_{BE}.

Solution.

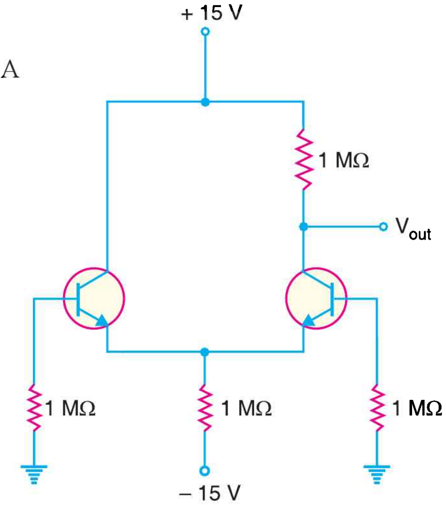


Fig. 25.25

(*i*) Tail current, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{(15-0)V}{1\,\text{M}\Omega} = 15\ \mu\text{A}$

The emitter current in each transistor is

$$I_{E1} = I_{E2} = I_E/2 = 15\mu\text{A}/2 = 7.5\ \mu\text{A}$$

The base current in the left transistor is

$$I_{B1} = \frac{I_{E1}}{\beta} = \frac{7.5\ \mu\text{A}}{90} = 83.3\ \text{nA}$$

The base current in the right transistor is

$$I_{B2} = \frac{I_{E2}}{\beta} = \frac{7.5\ \mu\text{A}}{110} = 68.2\ \text{nA}$$

∴ Input offset current is given by;

$$I_{in(offset)} = I_{B1} - I_{B2} = 83.3 - 68.2 = \mathbf{15.1\ nA}$$

(*ii*) The input bias current is the average of the two base currents.

∴ Input bias current, $I_{in(bias)} = \dfrac{I_{B1} + I_{B2}}{2} = \dfrac{83.3 + 68.2}{2} = \mathbf{75.8\ nA}$

Example 25.12. *The data sheet of an IC OP-amp gives these values :* $I_{in(offset)}$ *= 20 nA and* $I_{in(bias)}$ *= 80 nA. Find the values of two base currents.*

Solution. An $I_{in(offset)}$ of 20 nA means that one base current is 20 nA greater than the other. There is no way to tell which of the two base currents will be greater. It can go either way in mass production. Assume that I_{B1} is greater than I_{B2}. Then,

$$I_{B1} = I_{in(bias)} + \frac{I_{in(offset)}}{2} = 80\ \text{nA} + \frac{20\text{nA}}{2} = \mathbf{90\ nA}$$

$$I_{B2} = I_{in(bias)} - \frac{I_{in(offset)}}{2} = 80\ \text{nA} - \frac{20\text{nA}}{2} = \mathbf{70\ nA}$$

If I_{B2} is greater than I_{B1}, then the values are reversed *i.e.*, I_{B1} = 70 nA and I_{B2} = 90 nA.

Example 25.13. *In Fig. 25.26, what is the output offset voltage if* $I_{in(bias)}$ *= 80 nA and* $I_{in(offset)}$ *= 20 nA? Assume that voltage gain is A = 150. Assume only* β_{dc} *differences exist.*

Solution. The two base resistors are equal ; each being 100 kΩ.

∴ Input offset voltage, $V_{i0} = I_{in(offset)} \times R_B = (20\ \text{nA})\ (100\ \text{k}\Omega) = 2\ \text{mV}$

∴ Output offset voltage, $V_{out\,(offset)} = A \times V_{i0} = 150 \times 2\ \text{mV} = \mathbf{0.3\ V}$

---

* Recall that +sign indicates noninverting input and –sign indicates inverting input.

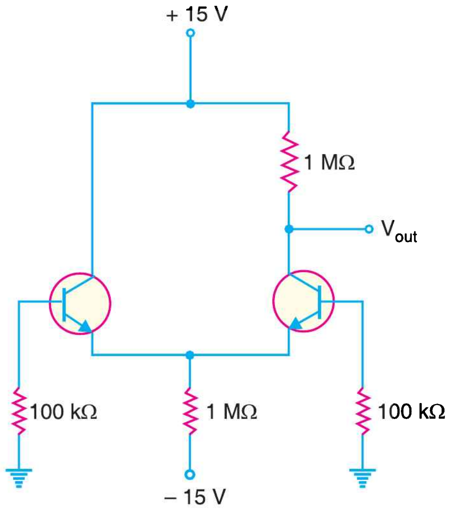


Fig. 25.26

25.13 A.C. Analysis of Differential Amplifier

A differential amplifier (*DA*) has a noninverting input and an inverting input. Fig. 25.27 shows the differential amplifier (*DA*) that is used in *IC OP*- amps. Note the circuit has double-ended input and single-ended output.

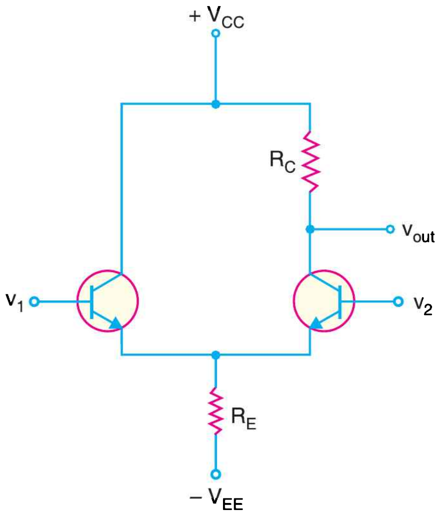


Fig. 25.27

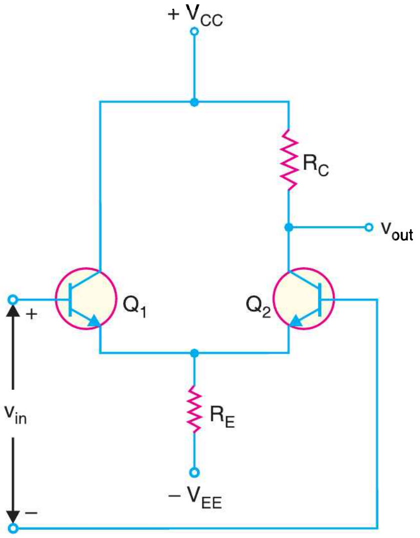


Fig. 25.28

If you look at the differential amplifier circuit in Fig. 25.27, it responds to the difference between the voltages at the two input terminals. In other words, *DA* responds to v_{in} (= $v_1 - v_2$). Therefore, the circuit shown in Fig. 25.27 can be drawn as shown in Fig. 25.28.

Ideally (*i.e.*, V_{BE} is negligible), the tail current I_E in Fig. 25.27 is $I_E = V_{EE}/R_E$. Once the values of V_{EE} and R_E are set, the tail current is constant. Therefore, to simplify a.c. analysis, we can replace the tail current by a current source (I_E) as shown in Fig. 25.29. This will simplify the a.c. analysis of the circuit with almost no loss of accuracy.

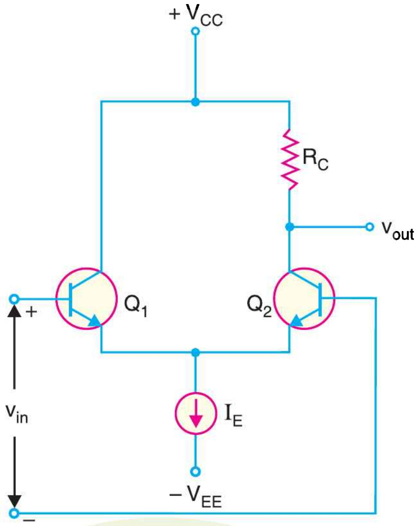


Fig. 25.29

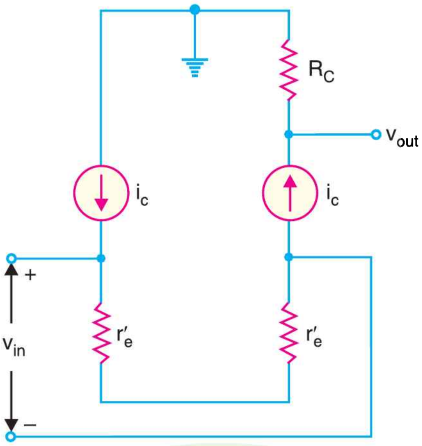


Fig. 25.30

A.C. Equivalent Circuit. We can easily find the a.c. equivalent circuit of differential amplifier by applying the usual rules to Fig. 25.29. The rules are to short all the capacitors, and reduce all d.c. sources to zero. Since a differential amplifier has no capacitors, all that we have to do is to reduce the d.c. sources to zero. Reducing a voltage source to zero is equivalent to replacing it by a short. Reducing a current source to zero is equivalent to opening it. In Fig. 25.29, this means ground the V_{CC} point, ground the V_{EE} point and open the current source. Applying these conditions to Fig. 25.29, we get the a.c. equivalent circuit of differential amplifier shown in Fig. 25.30.

Voltage gain. Fig. 25.30 shows the a.c. equivalent circuit of a differential amplifier. This is how a differential amplifier looks to an a.c. signal. Note that r'_e (= 25 mV/d.c. emitter current) is the a.c. emitter resistance. Since the two r'_es are in series, the same a.c. emitter current exists in both transistors. The a.c. emitter current is given by;

$$i_e = \frac{v_{in}}{2r'_e}$$

This expression is easy to remember because it is almost identical to a *CE* amplifier where $i_e = v_{in}/r'_e$. The only difference is the factor 2 because a differential amplifier uses two transistors.

The a.c. collector current is approximately equal to the a.c. emitter current *i.e.* $i_c \simeq i_e$.

$$\therefore \quad \text{Output voltage, } v_{out} = i_c R_C = \frac{v_{in}}{2r'_e} R_C \qquad \left[\because i_e \simeq i_c = \frac{v_{in}}{2r'_e}\right]$$

$$\therefore \quad \text{Voltage gain, } A = \frac{v_{out}}{v_{in}} = \frac{R_C}{2r'_e}$$

This gain of *DA* is referred to as differential-mode voltage gain and is usually denoted by A_{DM}.

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{R_C}{2r'_e}$$

Input impedance. The a.c. emitter current is given by;

$$i_e = \frac{v_{in}}{2r'_e} \simeq \beta\, i_b \qquad (\because i_c = \beta i_b \simeq i_e)$$

$$\therefore \quad \frac{v_{in}}{i_b} = 2\beta r_e'$$

Now i_b is the a.c. input current to the differential amplifier. Therefore, v_{in}/i_b is the input impedance.

$$\therefore \quad \text{Input impedance, } Z_i = 2\beta r_e'$$

Example 25.14. *What is* v_{out} *in Fig. 25.31 when (i)* $v_{in} = 1mV$ *(ii)* $v_{in} = -1mV$?

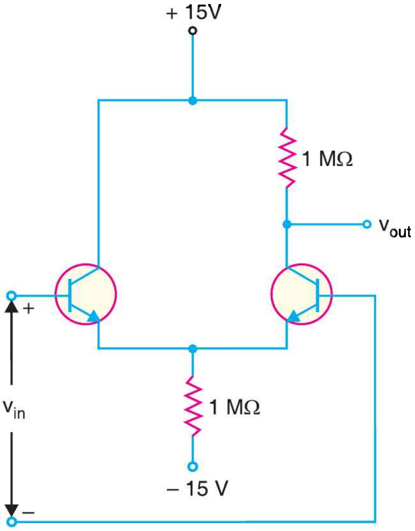


Fig. 25.31

Solution. The ideal tail current, $I_E = V_{EE}/R_E = 15\text{V}/1\text{M}\Omega = 15\ \mu\text{A}$. Therefore, d.c. emitter current in each transistor $= I_{E1} = I_{E2} = I_E/2 = 15\ \mu\text{A}/2 = 7.5\ \mu\text{A}$.

$$\therefore \quad \text{a.c. emitter resistance, } r_e' = \frac{25\text{ mV}}{I_{E1} \text{ or } I_{E2}} = \frac{25\text{ mV}}{7.5\ \mu\text{A}} = 3.33\text{ k}\Omega$$

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{R_C}{2r_e'} = \frac{1\,M\Omega}{2 \times 3.33\text{ k}\Omega} = 150$$

(*i*) Output voltage $= A_{DM} \times v_{in} = 150 \times (1\text{mV}) = 150\text{ mV} = \mathbf{0.15\ V}$

(*ii*) Output voltage, $v_{out} = A_{DM} \times v_{in} = 150 \times (-1\text{ mV}) = \mathbf{-\ 0.15\ V}$

Example 25.15. *For the circuit shown in Fig. 25.32, find (i) input impedance (ii) differential voltage gain.*

Solution.

$$(i) \quad \text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{(12 - 0.7)V}{100\text{ k}\Omega} = 113\ \mu\text{A}$$

The d.c. emitter current in each transistor is

$$I_{E1} = I_{E2} = I_E/2 = 113\ \mu\text{A}/2 = 56.5\ \mu\text{A}$$

$$\therefore \quad \text{a.c. emitter resistance, } r_e' = \frac{25\text{ mV}}{I_{E1} \text{ or } I_{E2}} = \frac{25\text{ mV}}{56.5\ \mu\text{A}} = 442\ \Omega$$

$$\therefore \quad \text{Input impedance, } Z_i = 2\beta r_e' = 2 \times 220 \times 442\ \Omega$$
$$= 194 \times 10^3 \Omega = \mathbf{194\ k\Omega}$$

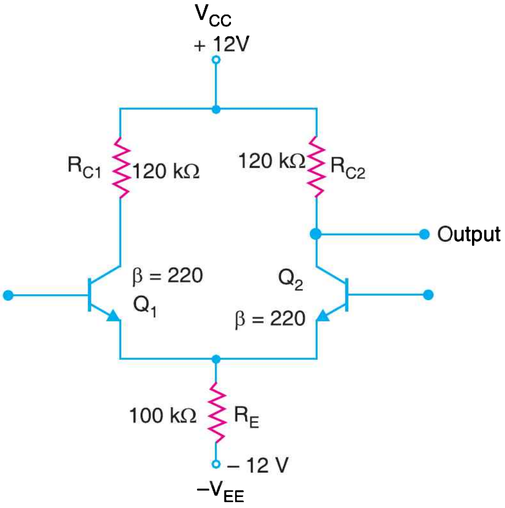

V_{CC}
+ 12V
R_{C1}
120 kΩ
120 kΩ
R_{C2}
Output
β = 220
Q₁
Q₂
β = 220
100 kΩ
R_E
– 12 V
–V_{EE}

Fig. 25.32

(*ii*) Differential voltage gain, $A_{DM} = \dfrac{R_{C1} \text{ or } R_{C2}}{2r_e'} = \dfrac{120\ \text{k}\Omega}{2 \times 442\ \Omega} = \mathbf{136}$

Example 25.16. *For the circuit shown in Fig. 25.33, find the differential-mode voltage gain.*

Solution. Because we are taking the output from Q_2, there is no need for collector resistor on Q_1. To find the relevant bias currents, we set the input sources to 0V, connecting the two bases to ground.

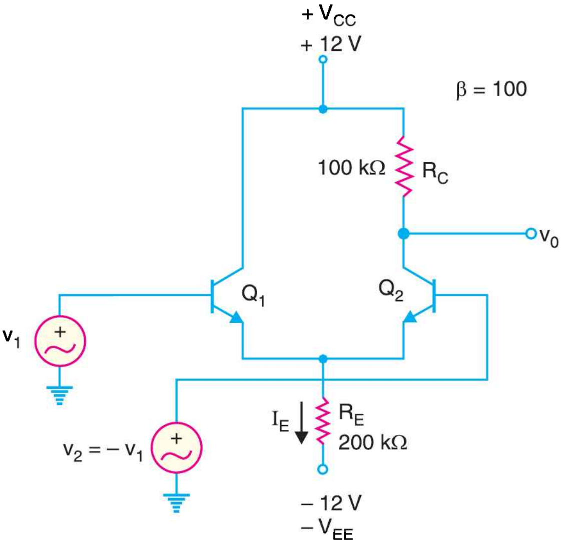

+ V_{CC}
+ 12 V
β = 100
100 kΩ
R_C
V₀
Q₁
Q₂
V₁
+
I_E
R_E
200 kΩ
V₂ = – V₁
+
– 12 V
– V_{EE}

Fig. 25.33

$$\text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{(12 - 0.7)V}{200\ \text{k}\Omega} = 0.0565\ \text{mA}$$

Therefore, emitter current in each transistor is

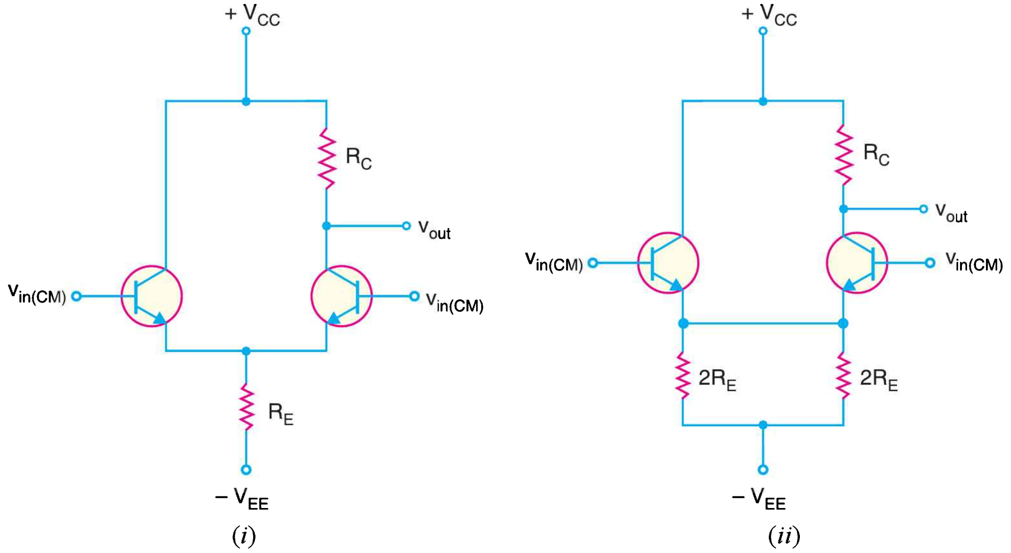
$$I_{E1} = I_{E2} = I_E/2 = 0.0565\ \text{mA}/2 = 0.0283\ \text{mA}$$

$$\therefore \quad \text{a.c. emitter resistance, } r'_e = \frac{25\text{ mV}}{I_{E1}} = \frac{25\text{ mV}}{0.0283\text{ mA}} = 883.4\ \Omega$$

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{R_C}{2r'_e} = \frac{100\text{ k}\Omega}{2 \times 883.4\ \Omega} = \mathbf{56.6}$$

25.14 Common-mode Voltage Gain (A_{CM})

The common-mode signals are equal in amplitude and have the same phase. Fig. 25.34(*i*) shows the common-mode operation of a differential amplifier (*DA*). Note that the same input voltage, $v_{in(CM)}$ is being applied to each base. Ideally, there is no a.c. output voltage with a common-mode input signal. It is because a differential amplifier is designed to respond to ***the difference between two input signals***. If there is no difference between the inputs, the output of *DA* is zero. In practice, the two halves of the differential amplifier are never completely balanced and there is a very small a.c. output voltage for the common-mode signal.



(*i*) (*ii*)

Fig. 25.34

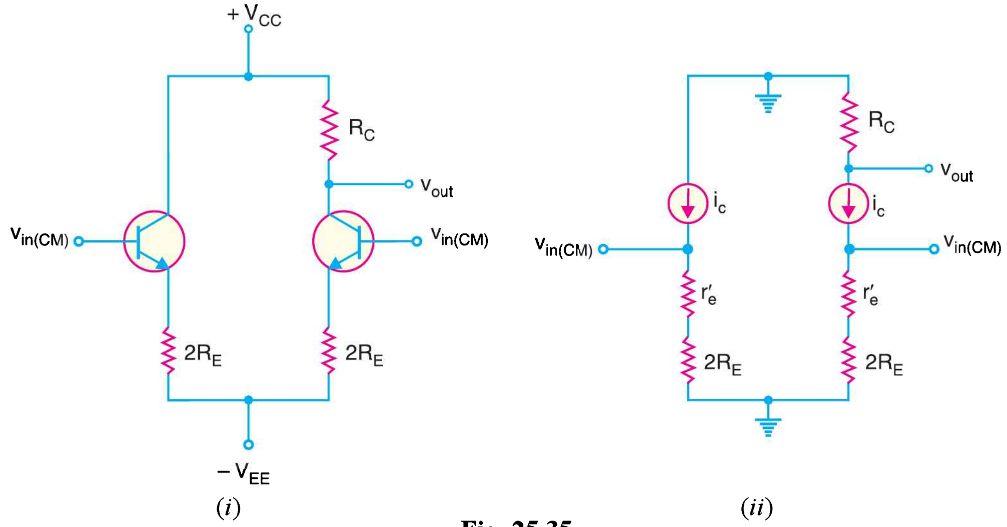
The circuit shown in Fig. 25.34(*i*) can be redrawn as shown in Fig. 25.34(*ii*). In this equivalent circuit, the two parallel resistances of 2 R_E produce an equivalent resistance of R_E. Therefore, this equivalent circuit will not affect the output voltage. Assuming identical transistors, the two emitter currents will be equal and produce the same voltage across emitter resistors. Therefore, there is no current through the wire between the emitters. We can remove this wire and the circuit becomes as shown in Fig. 25.35 (*i*).

A.C. equivalent circuit. To get the a.c. equivalent circuit, we can reduce both supply voltages to zero *i.e.*, we ground each supply point. Replacing the transistors by their a.c. equivalent circuits, we get a.c. equivalent circuit of differential amplifier for commom-mode operation as shown in Fig. 25.35 (*ii*). We can derive the voltage gain of an *unbypassed *CE* circuit. Here we will use 2 R_E in place of R_E.

$$\therefore \quad \text{Common-mode voltage gain, } A_{CM} = \frac{v_{out}}{v_{in(CM)}} = \frac{R_C}{r'_e + 2R_E}$$

---

* We have derived the voltage gain of bypassed capacitor *CE* amplifier in Art. 10.13 as : $A_v = R_C / r'_e$. Without bypass capacitor, the emitter is no longer at a.c. ground. Instead, R_E is seen by the a.c. signal between the emitter and ground and effectively adds to r'_e in the above formula. Therefore, voltage gain without the bypass capacitor becomes: $A_v = \dfrac{R_C}{r'_e + R_E}$


+ V_{CC}
R_C
V_{out}
$V_{in(CM)}$
$V_{in(CM)}$
$2R_E$
$2R_E$
$-V_{EE}$
R_C
V_{out}
i_c
i_c
$V_{in(CM)}$
$V_{in(CM)}$
r'_e
r'_e
$2R_E$
$2R_E$

(*i*) (*ii*)

Fig. 25.35

$$\text{where} \qquad r'_e = \text{a.c. emitter resistance} = \frac{25\text{ mV}}{\text{d.c. emitter current}}$$

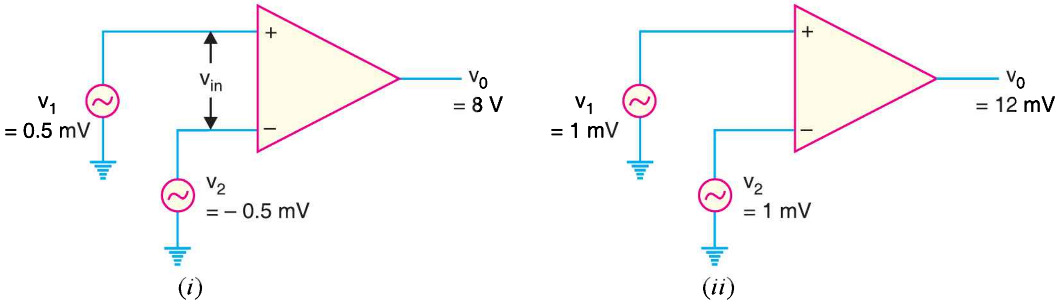
In most cases, r'_e is very small as compared to R_E, it (r'_e) is dropped from the formula.

$$\therefore \qquad A_{CM} = \frac{R_C}{2\,R_E}$$

The common-mode voltage gain (A_{CM}) is very small. For example, a typical *DA* may have R_C = 150 kΩ and R_E = 143 kΩ.

$$\therefore \qquad A_{CM} = \frac{R_C}{2\,R_E} = \frac{150\text{ k}\Omega}{2\times 143\text{ k}\Omega} = 0.52$$

Example 25.17. *Calculate the CMRR for the circuit measurements shown in Fig. 25.36.*


V_1 = 0.5 mV
V_{in}
+
−
V_0 = 8 V
V_2 = − 0.5 mV
V_1 = 1 mV
+
−
V_0 = 12 mV
V_2 = 1 mV

(*i*) (*ii*)

Fig. 25.36

Solution. Fig. 25.36(*i*) shows the differential-mode operation whereas Fig. 25.36(*ii*) shows the common-mode operation. Referring to Fig. 25.36(*i*), v_{in} = 0.5 – (–0.5) = 1mV.

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{v_o}{v_{in}} = \frac{8\text{V}}{1\text{ mV}} = 8000$$

Referring to Fig. 25.36(*ii*), $^*v_{in(CM)}$ = 1mV

$$\therefore \quad \text{Commom-mode voltage gain, } A_{CM} = \frac{12\text{ mV}}{1\text{ mV}} = 12$$

---

* Since the output voltage is 12mV, the common-mode signals are not exactly equal in magnitude.

$$\therefore \qquad CMRR = \frac{A_{DM}}{A_{CM}} = \frac{8000}{12} = \mathbf{666.7}$$

We can express *CMRR* in dB.

$$CMRR_{dB} = 20\log_{10} CMRR = 20\log_{10} 666.7 = \mathbf{56.48\ dB}$$

Example 25.18. *The data sheet of an OP-amp gives these typical values : A_{DM} = 200,000 and CMRR = 90 dB. What is the common-mode voltage gain?*

Solution. $$90\ dB = 20\log_{10} CMRR$$

$$\therefore \qquad CMRR = \text{antilog}\ \frac{90\ dB}{20} = 31{,}623$$

$$\therefore \qquad A_{CM} = \frac{A_{DM}}{CMRR} = \frac{200{,}000}{31{,}623} = \mathbf{6.32}$$

Example 25.19. *A differential amplifier has an open-circuit voltage gain of 100. This amplifier has a common input signal of 3.2 V to both terminals. This results in an output signal of 26 mV. Determine* (*i*) *common-mode voltage gain* (*ii*) *the CMRR in dB.*

Solution.

(*i*) $$v_{in(CM)} = 3.2\ \text{V}\ ;\ v_{out} = 26\ \text{mV} = 26 \times 10^{-3}\ \text{V}$$

$$\therefore \quad \text{Common-mode voltage gain, } A_{CM} = \frac{v_{out}}{v_{in(CM)}} = \frac{26 \times 10^{-3}}{3.2} = \mathbf{0.0081}$$

(*ii*) $$CMRR_{dB} = 20\log_{10}\frac{A_{DM}}{A_{CM}} = 20\log_{10}\frac{100}{0.0081} = \mathbf{81.8\ dB}$$

Example 25.20. *For the circuit shown in Fig. 25.37, find* (*i*) *the common-mode voltage gain* (*ii*) *the CMRR in dB.*

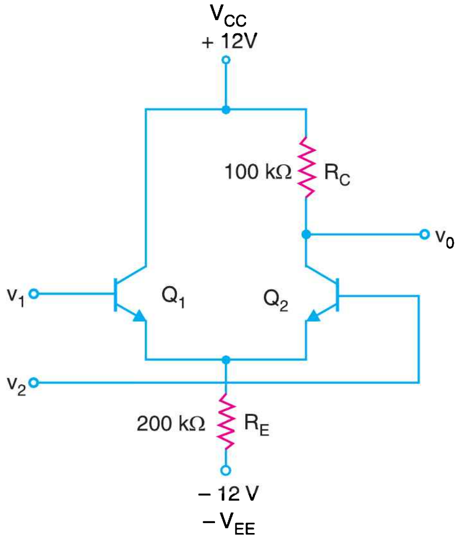


Fig. 25.37

Solution. (*i*) Common-mode voltage gain, $A_{CM} = \frac{R_C}{2R_E} = \frac{100\ \text{k}\Omega}{2 \times 200\text{k}\Omega} = \mathbf{0.25}$

(*ii*) In order to find differential voltage gain, we should first find d.c. emitter current.

$$\text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{(12 - 0.7)V}{200\ \text{k}\Omega} = 0.0565\ \text{mA}$$

The d.c. emitter current in each transistor is

$$I_{E1} = I_{E2} = I_E/2 = 0.0565\ \text{mA}/2 = 0.0283\ \text{mA}$$

$$\therefore \quad \text{a.c. emitter resistance, } r'_e = \frac{25\ \text{mV}}{I_{E1}} = \frac{25\ \text{mV}}{0.0283} = 883.4\ \Omega$$

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{R_C}{2r'_e} = \frac{100\ \text{k}\Omega}{2 \times 883.4\ \Omega} = 56.6$$

$$\therefore \quad CMRR_{dB} = 20\ \log_{10}\frac{A_{DM}}{A_{CM}} = 20\ \log_{10}\frac{56.6}{0.25} = \mathbf{47.09\ dB}$$

25.15 Operational Amplifier (OP- Amp)

Fig. 25.38 shows the block diagram of an operational amplifier (*OP*-amp). The input stage of an *OP*- amp is a differential stage followed by more stages of gain and a class *B* push-pull emitter follower.

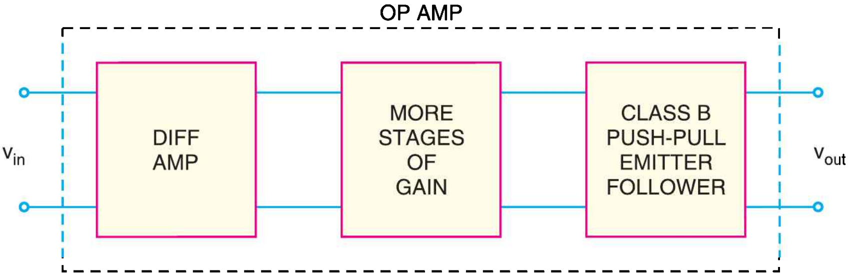


Fig. 25.38

The following are the important properties common to all operational amplifiers (*OP*-amps):

(*i*) An operational amplifier is a multistage amplifier. The input stage of an *OP*-amp is a differential amplifier stage.

(*ii*) An inverting input and a noninverting input.

(*iii*) A high input impedance (usually assumed infinite) at both inputs.

(*iv*) A low output impedance (< 200 Ω).

(*v*) A large open-loop voltage gain, typically 10^5.

(*vi*) The voltage gain remains constant over a wide frequency range.

(*vii*) Very large *CMRR* (> 90 dB).

25.16 Schematic Symbol of Operational Amplifier

Fig.25.39(*i*) shows the schematic symbol of an operational amplifier. The following points are worth noting :

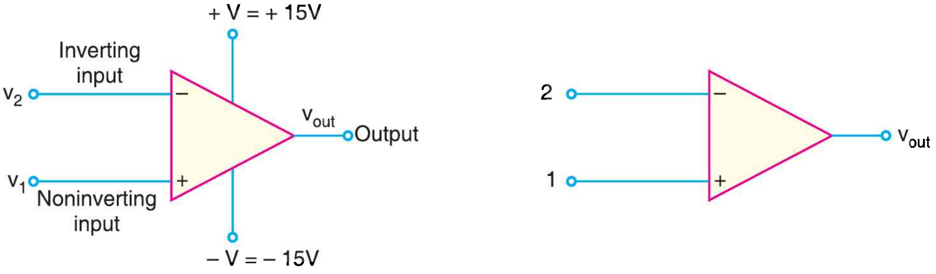
(*i*) The basic operational amplifier has *five terminals: two terminals for supply voltages +V and –V; two input terminals (inverting input and noninverting input) and one output terminal.

---

* Two other terminals, the *offset null terminals*, are used to ensure zero output when the two inputs are equal. These are normally used when small d.c. signals are involved.

(*ii*) Note that the input terminals are marked + and –. These are not polarity signs. The – sign indicates the ***inverting input*** while the + sign indicates the ***noninverting input.*** A signal applied to plus terminal will appear in the same phase at the output as at the input. A signal applied to the minus terminal will be shifted in phase 180° at the output.

(*iii*) The voltages v_1, v_2 and v_{out} are node voltages. This means that they are always measured w.r.t. ground. The differential input v_{in} is the difference of two node voltages v_1 and v_2. We normally do not show the ground in the symbol.



(*i*) (*ii*)

Fig. 25.39

(*iv*) For the sake of *simplicity, + *V* and – *V* terminals are often omitted from the symbol as shown in Fig. 25.39(*ii*). The two input leads are always shown on the symbol regardless of whether they are both used.

(*v*) In most cases, if only one input is required for an *OP*-amp circuit, the input not in use will be shown connected to ground. A single-input *OP*-amp is generally classified as either inverting or noninverting.

(*vi*) The *OP*-amp is produced as an integrated circuit (*IC*). Because of the complexity of the internal circuitry of an *OP*-amp, the *OP*-amp symbol is used exclusively in circuit diagrams.

25.17 Output Voltage From OP-Amp

The output voltage from an *OP*-amp for a given pair of input voltages depends mainly on the following factors:

1. The voltage gain of *OP*-amp.
2. The polarity relationship between v_1 and v_2.
3. The values of supply voltages, +*V* and –*V*.

1. Voltage gain of OP-amp. The *maximum* possible voltage gain from a given OP-amp is called *open-loop voltage gain* and is denoted by the symbol A_{OL}. The value of A_{OL} for an *OP*-amp is generally greater than 10,000.

The term open-loop indicates a circuit condition where there is *no feedback path from the output to the input of OP-amp.* The *OP*-amps are almost always operated with negative feedback *i.e.*, a part of the output signal is fed back in phase opposition to the input. Such a condition is illustrated in Fig. 25.40. Here R_i is the input resistance and R_f is the feedback resistor. Consequently, the voltage gain of *OP* amplifier is reduced. When a feedback path is present such as R_f connection in Fig. 25.40, the resulting circuit gain is referred to as *closed-loop voltage gain* (A_{CL}). The following points may be noted :

---

* Since two or more *OP*-amps are often contained in a single *IC* package, eliminating these terminals on the symbol eliminates unnecessary duplication.

(*i*) The maximum voltage gain of given OP-amp is A_{OL}. Its value is generally greater than 10,000.

(*ii*) The actual gain (A_{CL}) of an OP-amplifier is reduced when negative feedback path exists between output and input.

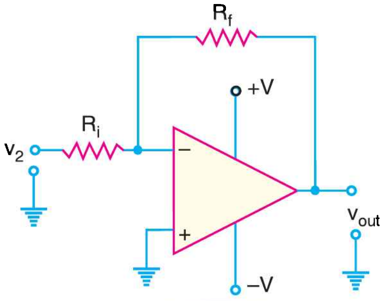


Fig. 25.40

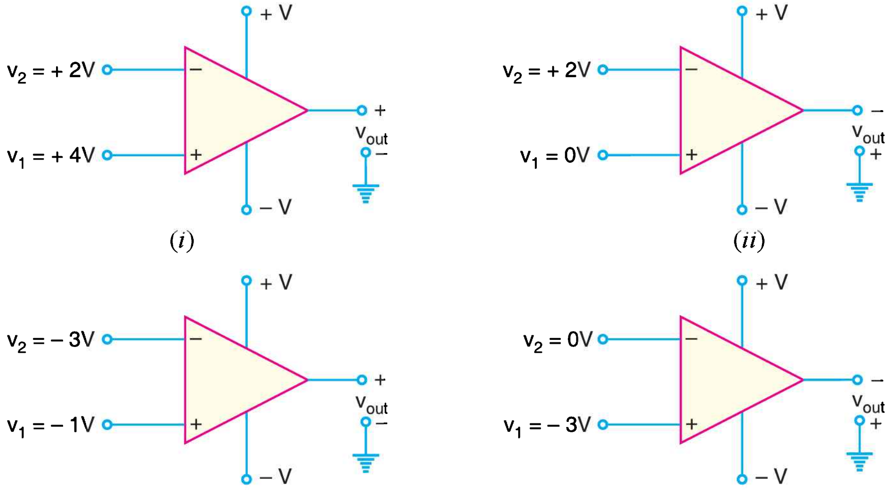
2. OP-Amp Input/Output Polarity Relationship. The polarity relationship between v_1 and v_2 will determine whether the *OP*-amp output voltage polarity is positive or negative. There is an easy method for it. We know the differential input voltage v_{in} is the difference between the non-inverting input (v_1) and inverting input (v_2) *i.e.*,

$$v_{in} = v_1 - v_2$$

When the result of this equation is ***positive***, the OP-amp output voltage will be ***positive***. When the result of this equation is ***negative***, the output voltage will be ***negative***.

Illustration. Let us illustrate *OP*-Amp input/output polarity relationship with numerical values.

(*i*) In Fig. 25.41(*i*), v_1 = + 4V and v_2 = + 2V so that $v_{in} = v_1 - v_2$ = (+ 4V) – (+ 2V) = 2V. Since v_{in} is ***positive***, the *OP*-amp output voltage will be ***positive***.



(*i*) (*ii*)

(*iii*) (*iv*)

Fig. 25.41

(*ii*) In Fig. 25.41 (*ii*), v_1 = 0V and v_2 = + 2V so that $v_{in} = v_1 - v_2$ = (0V) – (+2V) = –2V. Since v_{in} is ***negative***, the *OP*-amp output voltage will be ***negative***.

(*iii*) In Fig. 25.41 (*iii*), v_1 = –1V and v_2 = –3V so that $v_{in} = v_1 - v_2$ = (–1V) – (–3V) = 2V. Clearly, the *OP*-amp output voltage will be ***positive***.

(*iv*) In Fig. 25.41 (*iv*), v_1 = –3V and v_2 = 0V so that $v_{in} = v_1 - v_2$ = (–3V) – (0V) = –3V. Therefore, the *OP*-amp output voltage will be ***negative***.

3. Supply Voltages. The supply voltages for an *OP*-amp are normally equal in magnitude and opposite in sign *e.g.*, ± 15V, ± 12V, ± 18V. These supply voltages determine the limits of output voltage of *OP*-amp. These limits, known as ***saturation voltages,*** are generally given by;

$$+V_{sat} = +V_{supply} - 2V$$

$$-V_{sat} = -V_{supply} + 2V$$

Suppose an *OP*-amplifier has $V_{supply} = \pm\ 15V$ and open-loop voltage gain $A_{OL} = 20{,}000$. Let us find the differential voltage v_{in} to avoid saturation.

$$V_{sat} = V_{supply} - 2 = 15 - 2 = 13V$$

$$\therefore \quad V_{in} = \frac{V_{sat}}{A_{OL}} = \frac{13V}{20{,}000} = 650\ \mu\text{V}$$

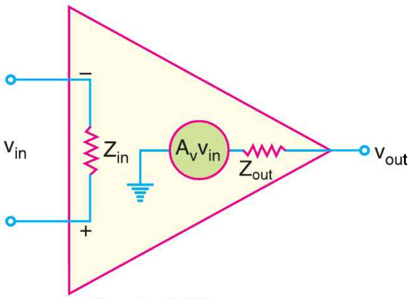
If the differential input voltage V_{in} exceeds this value in an *OP*-amp, it will be driven into saturation and the device will become non-linear.

Note : Although input terminals of an *OP*-amp are labeled as + and –, this does not mean you have to apply positive voltages to the + terminal and negative voltages to the –terminal. Any voltages can be applied to either terminal. The true meaning of the input terminal labels (+ and –) is that a *positive voltage applied to the + terminal drives the output voltage towards +V of d.c. supply; a positive voltage applied to the – terminal drives the output voltage towards –V of d.c. supply.

25.18 A.C. Analysis of OP-Amp

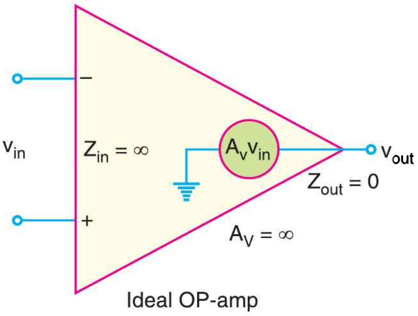
The basic *OP*-amp has two input terminals and one output terminal. The input terminals are labeled as + (noninverting input) and –(inverting input). As discussed earlier, a signal applied to the non-inverting input (+) will produce an output voltage that is in phase with the input voltage. However, a signal applied to the inverting input (–) will produce an output voltage that is 180° out of phase with the input signal.

(*i*) Practical OP–amp. Fig. 25.42 shows the a.c. equivalent circuit of a practical *OP*-amp. The characteristics of a practical OP-amp are : *very high voltage gain, very high input impedance* and *very low output impedance.* The input voltage v_{in} appears between the two input terminals and the output voltage is $A_v v_{in}$ taken through the output impedance Z_{out}. The consequences of these properties of a practical OP–amp are :



Practical OP -amp

Fig. 25.42



Ideal OP-amp

Fig. 25.43

---

* Note that positive and negative are relative terms. Thus if +4V is applied at +input terminal and +2V at – input terminal, then + terminal is at more positive potential. Therefore, the output voltage will swing towards +V of d.c. supply.

(*a*) Since the voltage gain (A_v) of a practical *OP*-amp is very high, an extremely small input voltage (v_{in}) will produce a large output voltage (v_{out}).

(*b*) Since the input impedance (Z_{in}) is very high, a practical OP-amp has very small input current.

(*c*) Since the output impedance (Z_{out}) of a practical OP-amp is very low, it means that output voltage is practically independent of the value of load connected to OP-amp.

(*ii*) **Ideal OP-amp.** Fig. 25.43 shows the a.c. equivalent circuit of an ideal OP-amp. The characteristics of an ideal OP-amp are : *infinite voltage gain, infinite input impedance* and *zero output impedance*. The consequences of these properties of an ideal *OP*-amp are :

(*a*) Since the voltage gain (A_v) of an ideal *OP*-amp is infinite, it means that we can set $v_{in} = 0V$.

(*b*) Since the input impedance (Z_{in}) is infinite, an ideal *OP*-amp has zero input current.

(*c*) Since the output impedance (Z_{out}) of an ideal *OP*-amp is zero, it means the output voltage does not depend on the value of load connected to *OP*-amp.

We can sum up the values of parameters of a practical *OP*-amp and an ideal *OP*-amp as under :

Practical *OP*-amp	**Ideal *OP*-amp**
$Z_{in} = 2\ \text{M}\Omega$	$Z_{in} \to \infty$ (Open circuit)
$A_v = 1 \times 10^5$	$A_v \to \infty$
$Z_{out} = 100\ \Omega$	$Z_{out} = 0\Omega$

25.19 Bandwidth of an OP-Amp

All electronic devices work only over a limited range of frequencies. This range of frequencies is called **bandwidth.** Every *OP*-amp has a bandwidth *i.e.*, the range of frequencies over which it will work properly. The bandwidth of an *OP*-amp depends upon the closed-loop gain of the *OP*-amp circuit. One important parameter is **gain-bandwidth product (GBW).** It is defined as under :

$$A_{CL} \times f_2 = f_{unity} = \text{GBW}$$

where A_{CL} = closed-loop gain at frequency f_2

f_{unity} = frequency at which the closed-loop gain is unity

It can be proved that the gain-bandwidth product of an OP-amp is constant. Since an *OP*-amp is capable of operating as a d.c. amplifier, its bandwidth is ($f_2 - 0$). The gain-bandwidth product of an OP-amp is an important parameter because it can be used to find :

(*i*) The maximum value of A_{CL} at a given value of f_2.

(*ii*) The value of f_2 for a given value of A_{CL}.

Example 25.21. *An OP-amp has a gain-bandwidth product of 15 MHz. Determine the bandwidth of OP-amp when A_{CL} = 500. Also find the maximum value of A_{CL} when f_2 = 200 kHz.*

Solution.
$$f_2 = \frac{f_{unity}}{A_{CL}} = \frac{15\text{MHz}}{500} = 30\ \text{kHz}$$

Since the *OP*-amp is capable of operating as a d.c. amplifier, bandwidth *BW* = **30 kHz.**

$$A_{CL} = \frac{f_{unity}}{f_2} = \frac{15\text{MHz}}{200\ \text{kHz}} = \mathbf{75\ or\ 37.5\ db}$$

Example 25.22. *An OP-amp has a gain-bandwidth product of 1.5 MHz. Find the operating bandwidth for the following closed-loop gains* (*i*) A_{CL} = 1 (*ii*) A_{CL} = 10 (*iii*) A_{CL} = 100.

Solution. Bandwidth, $BW = \dfrac{GBW}{A_{CL}}$

(*i*) $$\text{For } A_{CL} = 1,\ BW = \frac{1.5\ \text{MHz}}{1} = \mathbf{1.5\ MHz}$$

(*ii*) $$\text{For } A_{CL} = 10,\ BW = \frac{1.5\ \text{MHz}}{10} = \mathbf{150\ kHz}$$

(*iii*) $$\text{For } A_{CL} = 100,\ BW = \frac{1.5\ \text{MHz}}{100} = \mathbf{15\ kHz}$$

From this example, we conclude that :

(*a*) The higher the gain (A_{CL}) of an *OP*-amp, the narrower its bandwidth.

(*b*) The lower the gain of an *OP*-amp, the wider its bandwidth.

25.20 Slew Rate

The slew rate of an *OP*-amp is a measure of *how fast the output voltage can change* and is measured in volts per microsecond (V/μs). If the slew rate of an *OP*-amp is 0.5V/μs, it means that the output from the amplifier can change by 0.5 V every μs. Since frequency is a function of time, the *slew rate can be used to determine the maximum operating frequency of the OP-amp* as follows:

$$\text{Maximum operating frequency, } f_{max} = \frac{\text{Slew rate}}{2\pi\, V_{pk}}$$

Here V_{pk} is the peak output voltage.

Example 25.23. *Determine the maximum operating frequency for the circuit shown in Fig. 25.44. The slew rate is 0.5 V/μs.*

Solution. The maximum peak output voltage(V_{pk}) is approximately *8V. Therefore, maximum operating frequency (f_{max}) is given by;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\, V/\mu\text{s}}{2\pi \times 8}$$

$$= \frac{500\ \text{kHz}}{2\pi \times 8} \quad (\because\ 0.5\ \text{V}/\mu\text{s} = 500\ \text{kHz})$$

$$= \mathbf{9.95\ kHz}$$

While 9.95 kHz may not seem to be a very high output frequency, you must realise that the amplifier was assumed to be operating at its maximum output voltage. Let us see what happens when peak output voltage is reduced (See example 25.24).

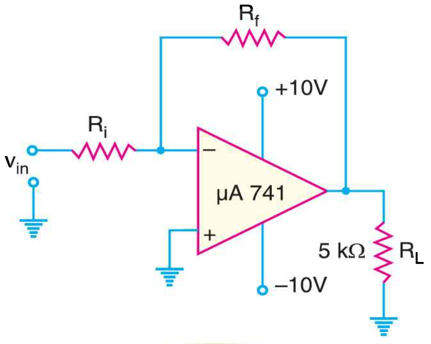


Fig. 25.44

Example 25.24. *The amplifier in Fig. 25.44 is being used to amplify an input signal to a peak output voltage of 100 mV. What is the maximum operating frequency of the amplifier?*

Solution. The maximum operating frequency (f_{max}) of the amplifier is given by;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\, V/\mu\text{s}}{2\pi \times 0.1} \quad (\because\ 100\ \text{mV} = 0.1\text{V})$$

$$= \frac{500\ \text{kHz}}{2\pi \times 0.1} = \mathbf{796\ kHz} \quad (\because\ 0.5\text{V}/\mu\text{s} = 500\ \text{kHz})$$

The above examples show that an *OP*-amp can be operated at a much higher frequency when being used as a small-signal amplifier than when being used as a large-signal amplifier.

---

* $+V_{sat} = +V_{supply} - 2 = 10 - 2 = 8V$

25.21 Frequency Response of an OP-Amp

The operating frequency has a significant effect on the operation of an *OP*-amp. The following are the important points regarding the frequency response of an *OP*-amp :

(*i*) The maximum operating frequency of an *OP*-amp is given by;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}}$$

Thus, the *peak output voltage limits the maximum operating frequency.*

(*ii*) When the maximum operating frequency of an *OP*-amp is exceeded, the result is a distorted output waveform.

(*iii*) Increasing the operating frequency of an *OP*-amp beyond a certain point will :

(*a*) Decrease the maximum output voltage swing.

(*b*) Decrease the open-loop voltage gain.

(*c*) Decrease the input impedance.

(*d*) Increase the output impedance.

25.22 OP-Amp with Negative Feedback

An *OP*-amp is almost always operated with negative feedback *i.e.*, a part of the output is fed back in phase opposition to the input (See Fig. 25.45). The reason is simple. The open-loop voltage gain of an *OP*-amp is very high (usually greater than 100,000). Therefore, an extremely small input voltage drives the *OP*-amp into its saturated output stage. For example, assume v_{in} = 1mV and A_{OL} = 100,000. Then,

$$v_{out} = A_{OL} v_{in} = (100{,}000) \times (1 \text{ mV}) = 100 \text{ V}$$

Since the output level of an *OP*-amp can never reach 100 V, it is driven deep into saturation and the device becomes non-linear.

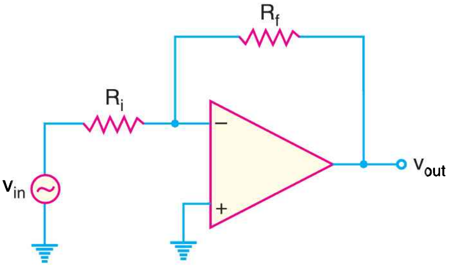


Fig. 25.45

With negative feedback, the voltage gain (A_{CL}) can be reduced and controlled so that OP-amp can function as a linear amplifier. In addition to providing a controlled and stable gain, negative feedback also provides for control of the input and output impedances and amplifier bandwidth. The table below shows the general effects of negative feedback on the performance of OP-amps.

	Voltage gain	**Input Z**	**Output Z**	**Bandwidth**
Without negative feedback	A_{OL} is too high for linear amplifier applications	Relatively high	Relatively low	Relatively narrow
With negative feedback	A_{CL} is set by the feedback circuit to desired value	Can be increased or reduced to a desired value depending on type of circuit	Can be reduced to a desired value	Significantly wider

25.23 Applications of OP-Amps

The operational amplifiers have many practical applications. The *OP*-amp can be connected in a large number of circuits to provide various operating characteristics. In the sections to follow, we shall discuss important applications of *OP*-amps.

25.24 Inverting Amplifier

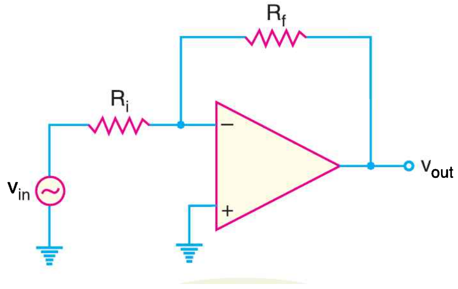
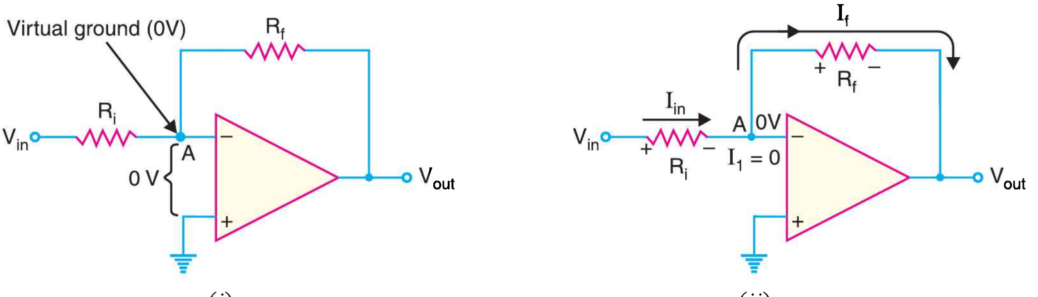


Fig. 25.46

An *OP* amplifier can be operated as an inverting amplifier as shown in Fig. 25.46. An input signal v_{in} is applied through input resistor R_i to the minus input (inverting input). The output is fed back to the same minus input through feedback resistor R_f. The plus input (noninverting input) is grounded. Note that the resistor R_f provides the **negative feedback*. Since the input signal is applied to the inverting input (–), the output will be inverted (*i.e.* 180° out of phase) as compared to the input. Hence the name inverting amplifier.

Voltage gain. An OP-amp has an infinite input impedance. This means that there is zero current at the inverting input. If there is zero current through the input impedance, then there must be *no* voltage drop between the inverting and non-inverting inputs. This means that voltage at the inverting input (–) is zero (point *A*) because the other input (+) is grounded. The 0V at the inverting input terminal (point *A*) is referred to as **virtual ground.** This condition is illustrated in Fig. 25.47. The point *A* is said to be at virtual ground because it is at 0V but is not physically connected to the ground (*i.e.* $V_A = 0V$).



(*i*) (*ii*)

Fig. 25.47

Referring to Fig. 25.47 (*ii*), the current I_1 to the inverting input is zero. Therefore, current I_{in} flowing through R_i entirely flows through feedback resistor R_f. In other words, $I_f = I_{in}$.

Now
$$I_{in} = \frac{\text{Voltage across } R_i}{R_i} = \frac{V_{in} - V_A}{R_i} = \frac{V_{in} - 0}{R_i} = \frac{V_{in}}{R_i}$$

and
$$I_f = \frac{\text{Voltage across } R_f}{R_f} = \frac{V_A - V_{out}}{R_f} = \frac{0 - V_{out}}{R_f} = \frac{-V_{out}}{R_f}$$

$$\text{Since } I_f = I_{in}, \quad -\frac{V_{out}}{R_f} = \frac{V_{in}}{R_i}$$

$$\therefore \quad \text{Voltage gain, } A_{CL} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$$

---

* The output voltage is 180° out of phase with the input. Since the voltage drop across R_f is of the opposite polarity to the applied voltage, the circuit is providing negative feedback.

The negative sign indicates that output signal is inverted as compared to the input signal. The following points may be noted about the inverting amplifier :

(*i*) The closed-loop voltage gain (A_{CL}) of an inverting amplifier is the ratio of the feedback resistance R_f to the input resistance R_i. *The closed-loop voltage gain is independent of the OP-amp's internal open-loop voltage gain.* Thus the negative feedback stabilises the voltage gain.

(*ii*) The inverting amplifier can be designed for unity gain. Thus if $R_f = R_i$, then voltage gain, $A_{CL} = -1$. Therefore, the circuit provides a unity voltage gain with 180° phase inversion.

(*iii*) If R_f is some multiple of R_i, the amplifier gain is constant. For example, if $R_f = 10\ R_i$, then $A_{CL} = -10$ and the circuit provides a voltage gain of exactly 10 along with a 180° phase inversion from the input signal. If we select precise resistor values for R_f and R_i, we can obtain a wide range of voltage gains. *Thus the inverting amplifier provides constant voltage gain.*

25.25 Input and Output Impedance of Inverting Amplifier

It is worthwhile to give a brief discussion about the input impedance and output impedance of inverting amplifier.

(*i*) **Input impedance.** While an *OP*-amp has an extremely high input impedance, the inverting amplifier does not. The reason for this can be seen by referring back to Fig. 25.47(*i*). As this figure shows, the voltage source "sees" an input resistance (R_i) that is going to virtual ground. Thus the input impedance for the inverting amplifier is

$$Z_i \simeq R_i$$

The value of R_i will always be much less than the input impedance of the *OP*-amp. Therefore, the overall input impedance of an inverting amplifier will also be much lower than the *OP*-amp input impedance.

(*ii*) **Output impedance.** Fig. 25.48 shows the inverting amplifier circuit. You can see from this figure that the output impedance of the inverting amplifier is the parallel combination of R_f and the output impedance of *OP*-amp itself.

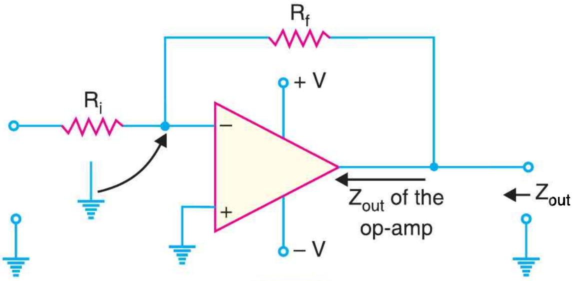


Fig. 25.48

The presence of the negative feedback circuit reduces the output impedance of the amplifier to a value that is less than the output impedance of *OP*-amp.

Example 25.25. *Given the OP-amp configuration in Fig. 25.49, determine the value of R_f required to produce a closed-loop voltage gain of –100.*

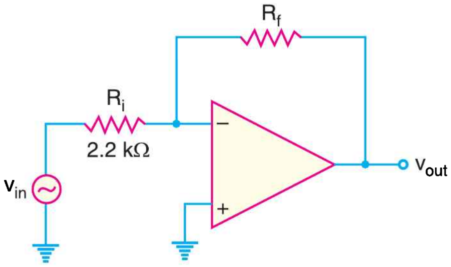


Fig. 25.49

Solution. $A_{CL} = -\frac{R_f}{R_i}$ or $-100 = -\frac{R_f}{2.2}$

$\therefore$ $R_f = 100 \times 2.2 = \mathbf{220\ k\Omega}$

Example 25.26. *Determine the output voltage for the circuit of Fig. 25.50.*

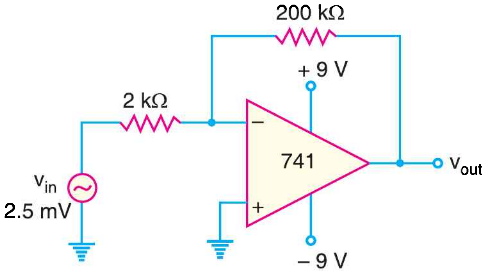

200 kΩ
+ 9 V
2 kΩ
741
V_{out}
V_{in}
2.5 mV
– 9 V

Fig. 25.50

Solution. $A_{CL} = -\frac{R_f}{R_i} = -\frac{200\ k\Omega}{2\ k\Omega} = -100$

$\therefore$ Output voltage, $v_{out} = A_{CL} \times v_{in} = (-100) \times (2.5\ mV) = -250\ mV = \mathbf{-0.25\ V}$

Example 25.27. *Find the output voltage for the circuit shown in Fig. 25.51.*

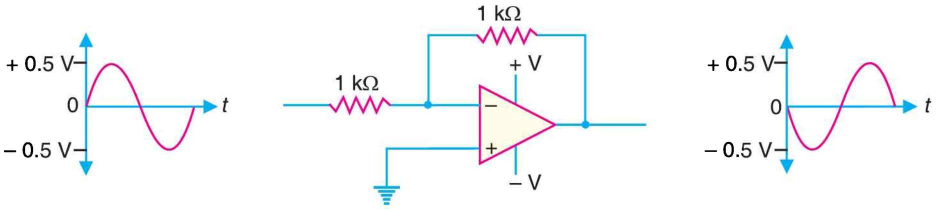

+ 0.5 V
0
– 0.5 V
t
1 kΩ
1 kΩ
+ V
– V
+ 0.5 V
0
– 0.5 V
t

Fig. 25.51

Solution. Voltage gain, $A_{CL} = -\frac{R_f}{R_i} = -\frac{1\ k\Omega}{1\ k\Omega} = -1$

Since the voltage gain of the circuit is –1, the **output will have the same amplitude but with 180° phase inversion.**

Example 25.28. *Find the output voltage for the circuit shown in Fig. 25.52.*

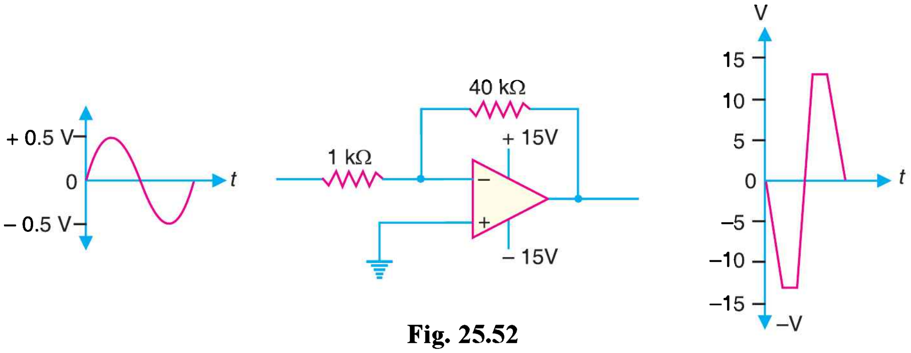

+ 0.5 V
0
– 0.5 V
t
40 kΩ
1 kΩ
+ 15V
– 15V
V
15
10
5
0
–5
–10
–15
–V
t

Fig. 25.52

Solution. Voltage gain, $A_{CL} = -\frac{R_f}{R_i} = -\frac{40\ k\Omega}{1\ k\Omega} = -40$

Note that the input signal is the same as in example 25.27 but now the voltage gain is –40 instead of –1. Since the supply voltages are ± 15 V, the *saturation occurs at ± 13 V. Since the output voltage far exceeds the saturation level, the *OP*-amp will be driven to deep saturation and it will behave as a non-linear amplifier. This means that the output will not have the same shape as input but will clip at the saturation voltage. Note that 180° phase inversion does occur.

Example 25.29. *For the circuit shown in Fig. 25.53, find (i) closed-loop voltage gain (ii) input impedance of the circuit (iii) the maximum operating frequency. The slew rate is 0.5V/µs.*

Solution.

(*i*) Closed-loop voltage gain, $A_{CL} = -\frac{R_f}{R_i} = -\frac{100\text{ k}\Omega}{10\text{ k}\Omega} = \mathbf{-10}$

(*ii*) The input impedance Z_i of the circuit is

$$Z_i \simeq R_i = \mathbf{10\ k\Omega}$$

(*iii*) To calculate the maximum operating frequency (f_{max}) for this inverting amplifier, we need to determine its peak output voltage. With values of $V_{in} = 1\ V_{pp}$ and $A_{CL} = 10$, the peak-to-peak output voltage is

$$V_{out} = (1V_{pp})\,(A_{CL})$$
$$= (1V_{pp}) \times 10 = 10\ V_{pp}$$

Therefore, the peak output voltage is

$$V_{pk} = 10/2 = 5\text{ V}$$

$$\therefore \quad f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\text{ V}/\mu\text{s}}{2\pi\times 5}$$

$$= \frac{500\text{ kHz}}{2\pi\times 5} = \mathbf{15.9\ kHz}$$

$(\because\ 0.5\text{ V}/\mu\text{s} = 500\text{ kHz})$

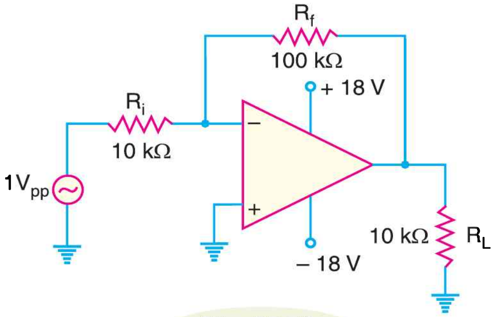


Fig. 25.53

Example 25.30. *You have the following resistor values available:*

1 kΩ; 5 kΩ ; 10 kΩ and 20 kΩ

Design the OP-amp circuit to have a voltage gain of –4.

Solution. Since the voltage gain is negative, the *OP*-amp is operating as an inverting amplifier.

Now, $$A_{CL} = -\frac{R_f}{R_i} = -4$$

We need to use resistors that have a ratio of 4 : 1. The two resistors which satisfy this requirement are : R_f = **20 kΩ** and R_i = **5kΩ.**

Example 25.31. *Fig. 25.54 shows an inverting OP-amp. Find the closed-loop gain if (i)* R_{source} = 0Ω *(ii)* R_{source} = 1 kΩ.

Solution. (*i*) When $R_{source} = 0\ \Omega$; $A_{CL} = -\frac{R_f}{R_i} = -\frac{100\text{ k}\Omega}{1\text{ k}\Omega} = \mathbf{-100}$

(*ii*) When $R_{source} = 1\text{ k}\Omega$; $A_{CL} = -\frac{R_f}{R_{source} + R_i} = -\frac{100\text{ k}\Omega}{1\text{ k}\Omega + 1\text{ k}\Omega} = \mathbf{-50}$

Note that we have lost half of the voltage gain.

---

* $+V_{sat} = +V_{supply} - 2\text{ V} = +15\text{ V} - 2\text{ V} = +13\text{ V}$
$-V_{sat} = -V_{supply} + 2\text{ V} = -15\text{ V} + 2\text{ V} = -13\text{ V}$

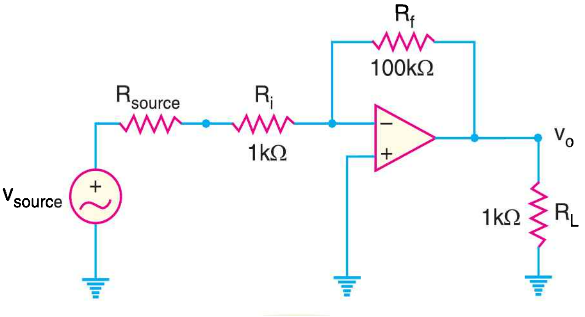


Fig. 25.54

25.26 Noninverting Amplifier

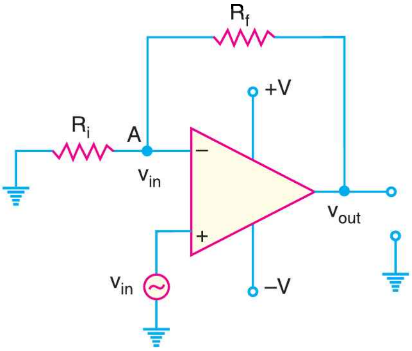


Fig. 25.55

There are times when we wish to have an output signal of the same polarity as the input signal. In this case, the *OP*-amp is connected as noninverting amplifier as shown in Fig. 25.55. The input signal is applied to the noninverting input (+). The output is applied back to the input through the feedback circuit formed by feedback resistor R_f and input resistance R_i. Note that resistors R_f and R_i form a voltage divide at the inverting input (–). This produces **negative feedback* in the circuit. Note that R_i is grounded. Since the input signal is applied to the noninverting input (+), the output signal will be noninverted i.e., the output signal will be in phase with the input signal. Hence, the name non-inverting amplifier.

Voltage gain. If we assume that we are not at saturation, the potential at point A is the same as V_{in}. Since the input impedance of *OP*-amp is very high, all of the current that flows through R_f also flows through R_i. Keeping these things in mind, we have,

$$\text{Voltage across } R_i = V_{in} - 0 \ ; \ \text{Voltage across } R_f = V_{out} - V_{in}$$

Now $$\text{Current through } R_i = \text{Current through } R_f$$

or $$\frac{V_{in} - 0}{R_i} = \frac{V_{out} - V_{in}}{R_f}$$

or $$V_{in} R_f = V_{out} R_i - V_{in} R_i$$

or $$V_{in}(R_f + R_i) = V_{out} R_i$$

or $$\frac{V_{out}}{V_{in}} = \frac{R_f + R_i}{R_i} = 1 + \frac{R_f}{R_i}$$

$$\therefore \quad \text{Closed-loop voltage gain, } A_{CL} = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$$

The following points may be noted about the noninverting amplifier :

(*i*) $$A_{CL} = 1 + \frac{R_f}{R_i}$$

---

* If the output voltage increases, the voltage at the inverting input will also increase. Since the voltage being amplified is the difference between the voltages at the two input terminals, the differential voltage will decrease when the output voltage increases. Therefore, the circuit provides negative feedback.

The voltage gain of noninverting amplifier also depends upon the values of R_f and R_i.

(*ii*) The voltage gain of a non-inverting amplifier can be made equal to or greater than 1.

(*iii*) The voltage gain of a non-inverting amplifier will always be greater than the gain of an equivalent inverting amplifier by a value of 1. If an inverting amplifier has a gain of 150, the equivalent noninverting amplifier will have a gain of 151.

(*iv*) The voltage gain is positive. This is not surprising because output signal is in phase with the input signal.

Non-inverting operational amplifier.

25.27 Voltage Follower

The voltage follower arrangement is a special case of noninverting amplifier where all of the output voltage is fed back to the inverting input as shown in Fig. 25.56. Note that we remove R_i and R_f from the noninverting amplifier and short the output of the amplifier to the inverting input. The voltage gain for the voltage follower is calculated as under :

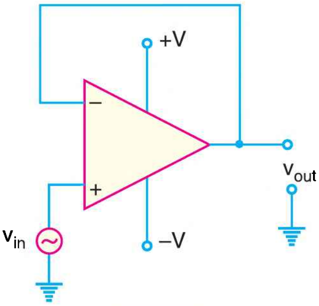


Fig. 25.56

$$A_{CL} = 1+\frac{R_f}{R_i} = 1+\frac{0}{R_i} = 1 \qquad (\because R_f = 0\Omega)$$

Thus the closed-loop voltage gain of the voltage follower is 1. The most important features of the voltage follower configuration are its *very high input impedance* and its *very low output impedance*. These features make it a nearly ideal buffer amplifier to be connected between high-impedance sources and low-impedance loads.

Example 25.32. *Calculate the output voltage from the noninverting amplifier circuit shown in Fig. 25.57 for an input of 120 μV.*

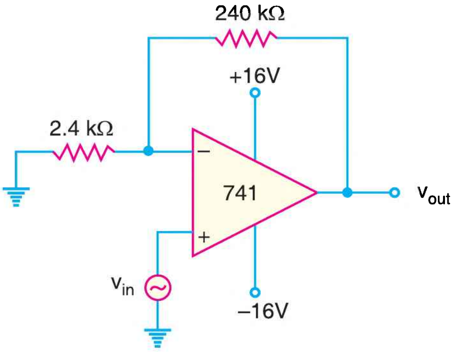


Fig. 25.57

Solution. Voltage gain, $A_{CL} = 1+\frac{R_f}{R_i}=1+\frac{240\text{ k}\Omega}{2.4\text{ k}\Omega}=1+100=101$

Output voltage, $v_{out} = A_{CL}\times v_{in}=(101)\times(120\ \mu\text{V}) = \mathbf{12.12\ mV}$

Example 25.33. *For the noninverting amplifier circuit shown in Fig. 25.58, find the output voltage for an input voltage of (i) 1 V (ii) –1 V.*

Solution. Voltage gain, $A_{CL} = 1+\frac{R_f}{R_i}=1+\frac{10\text{ k}\Omega}{1\text{ k}\Omega}=1+10=11$

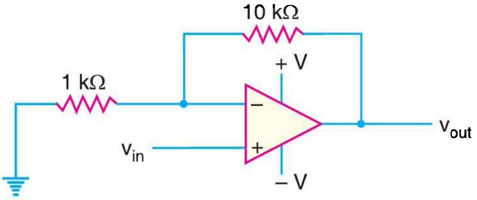


Fig. 25.58

(*i*) For $v_{in} = 1$ V ; $v_{out} = A_{CL}\times v_{in} = 11\times 1\text{ V} = \mathbf{11\ V}$

(*ii*) For $v_{in} = -1$ V ; $v_{out} = A_{CL}\times v_{in} = 11\times(-1\text{ V}) = \mathbf{-\ 11\ V}$

Example 25.34. *For the noninverting amplifier circuit shown in Fig. 25.59, find peak-to-peak output voltage.*

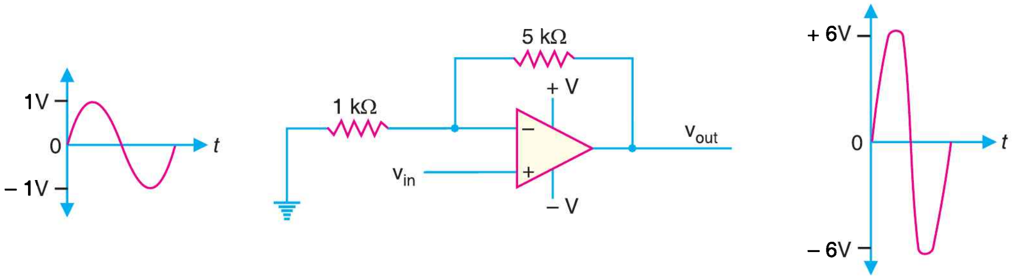


Fig. 25.59

Solution. The input signal is 2 *V* peak-to-peak.

Voltage gain, $A_{CL} = 1+\frac{R_f}{R_i}=1+\frac{5\text{ k}\Omega}{1\text{ k}\Omega}=1+5=6$

∴ Peak-to-peak output voltage $= A_{CL}\times v_{inpp} = 6\times 2 = \mathbf{12\ V}$

Example 25.35. *For the noninverting amplifier circuit shown in Fig. 25.60, find (i) closed-loop voltage gain (ii) maximum operating frequency. The slew rate is 0.5 V/µs.*

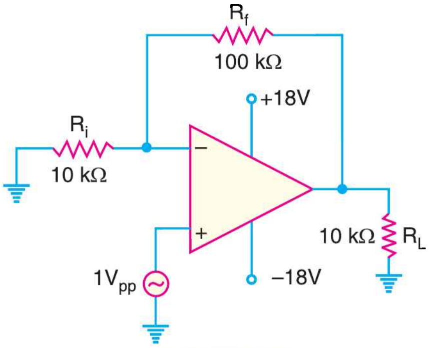


Fig. 25.60

Solution.

(*i*) Voltage gain, $A_{CL} = 1+\frac{R_f}{R_i} = 1+\frac{100\ \text{k}\Omega}{10\ \text{k}\Omega} = 1+10 = \mathbf{11}$

(*ii*) To determine the value of maximum operating frequency (f_{max}), we need to calculate the peak output voltage for the amplifier. The peak-to-peak output voltage is

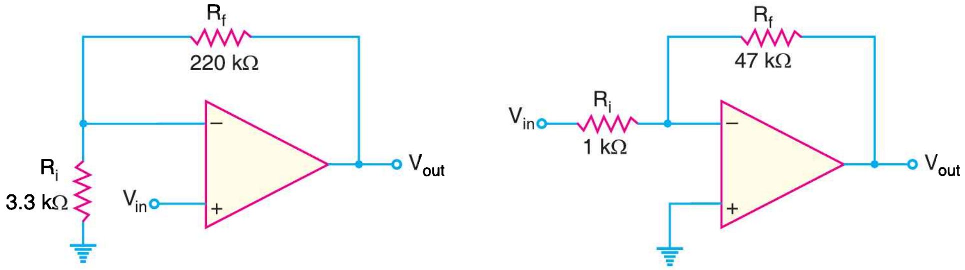
$$v_{out} = A_{CL} \times v_{in} = 11 \times (1V_{pp}) = 11V_{pp}$$

∴ Peak output voltage, $V_{pk} = 11/2 = 5.5\ \text{V}$

$$\therefore \quad f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\ \text{V}/\mu\text{s}}{2\pi \times 5.5}$$

$$= \frac{500\ \text{kHz}}{2\pi \times 5.5} = \mathbf{14.47\ kHz} \qquad (\because\ 0.5\ \text{V}/\mu\text{s} = 500\ \text{kHz})$$

Example 25.36. *Determine the bandwidth of each of the amplifiers in Fig. 25.61. Both OP-amps have an open-loop voltage gain of 100 dB and a unity-gain bandwidth of 3MHz.*



(*i*) (*ii*)

Fig. 25.61

Solution.

(*i*) For the noninverting amplifier shown in Fig. 25.61 (*i*), the closed-loop voltage gain (A_{CL}) is

$$A_{CL} = 1+\frac{R_f}{R_i} = 1+\frac{220\ \text{k}\Omega}{3.3\ \text{k}\Omega} = 1+66.7 = 67.7$$

$$\therefore \quad \text{Bandwidth, } BW = \frac{\text{Unity-gain } BW}{A_{CL}} = \frac{3\ \text{MHz}}{67.7} = \mathbf{44.3\ kHz}$$

(*ii*) For the inverting amplifier shown in Fig. 25.61 (*ii*),

$$A_{CL} = -\frac{R_f}{R_i} = -\frac{47\ \text{k}\Omega}{1\ \text{k}\Omega} = -47$$

$$\therefore \quad \text{Bandwidth, } BW = \frac{3\ \text{MHz}}{47} = \mathbf{63.8\ kHz}$$

Example 25.37. *Fig. 25.62 shows the circuit of voltage follower. Find* (*i*) *the closed-loop voltage gain and* (*ii*) *maximum operating frequency. The slew rate is 0.5 V/µs.*

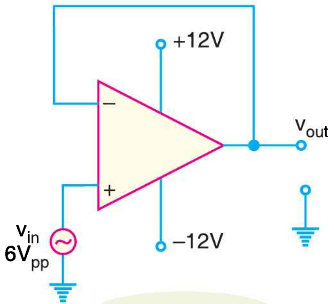


Fig. 25.62

Solution.

(*i*) For the voltage follower, $A_{CL} = \mathbf{1}$

(*ii*) Since $A_{CL} = 1$ for the circuit, $v_{out} = v_{in}$. Therefore, peak output voltage (V_{pk}) is one-half of $6V_{pp}$ *i.e.*, $V_{pk} = 6/2 = 3$ V. The maximum operating frequency (f_{max}) is given by ;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5 \text{ V/}\mu\text{s}}{2\pi \times 3}$$

$$= \frac{500 \text{ kHz}}{2\pi \times 3} = \mathbf{26.53\ kHz} \qquad (\because\ 0.5 \text{ V/}\mu\text{s} = 500 \text{ kHz})$$

25.28 Multi-stage OP-Amp Circuits

When a number of OP-amp stages are connected in series, the overall voltage gain is equal to the product of individual stage gains. Fig. 25.63 shows connection of three stages. The first stage is connected to provide noninverting gain. The next two stages provide inverting gains.

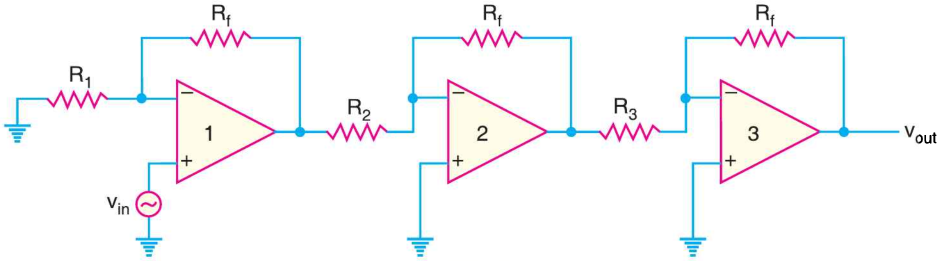


Fig. 25.63

The overall voltage gain A of this circuit is given by;

$$A = A_1 A_2 A_3$$

where A_1 = Voltage gain of first stage = $1 + (R_f/R_1)$

A_2 = Voltage gain of second stage = $-R_f/R_2$

A_3 = Voltage gain of third stage = $-R_f/R_3$

Since the overall voltage gain is positive, the circuit behaves as a noninverting amplifier.

Example 25.38. *Fig. 25.63 shows the multi-stage OP-amp circuit. The resistor values are :* $R_f = 470\ k\Omega$; $R_1 = 4.3\ k\Omega$; $R_2 = 33\ k\Omega$ *and* $R_3 = 33\ k\Omega$. *Find the output voltage for an input of 80* μV.

Solution. Voltage gain of first stage, $A_1 = 1 + (R_f/R_1) = 1 + (470\ \text{k}\Omega/4.3\ \text{k}\Omega) = 110.3$

Voltage gain of second stage, $A_2 = -R_f/R_2 = -470\ \text{k}\Omega/33\ \text{k}\Omega = -14.2$

Voltage gain of third stage, $A_3 = -R_f/R_3 = -470\ \text{k}\Omega/33\ \text{k}\Omega = -14.2$

$\therefore$ Overall voltage gain, $A = A_1 A_2 A_3 = (110.3) \times (-14.2) \times (-14.2) = 22.2 \times 10^3$

Output voltage, $v_{out} = A \times v_{in} = 22.2 \times 10^3 \times (80\ \mu\text{V}) = \mathbf{1.78V}$

Example 25.39. *A three-stage OP-amp circuit is required to provide voltage gains of +10, –18 and –27. Design the OP-amp circuit. Use a 270 kΩ feedback resistor for all three circuits. What output voltage will result for an input of 150* μV?

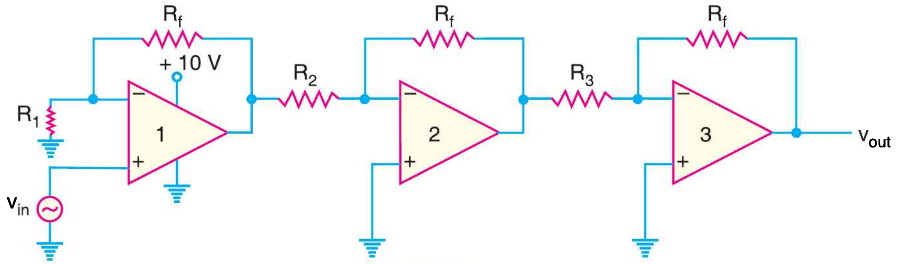


Fig. 25.64

Solution. Designing the above OP-amp circuit means to find the values of R_1, R_2 and R_3. The first stage gain is +10 so that this stage operates as noninverting amplifier.

Now $$+10 = 1+\frac{R_f}{R_1} \quad \therefore \quad R_1 = \frac{R_f}{10-1} = \frac{270\ \text{k}\Omega}{9} = \mathbf{30\ k\Omega}$$

The second stage gain is –18 so that this stage operates as an inverting amplifier.

$$\therefore \quad -18 = -\frac{R_f}{R_2} \quad \text{or} \quad R_2 = \frac{R_f}{18} = \frac{270\ \text{k}\Omega}{18} = \mathbf{15\ k\Omega}$$

The third stage gain is –27 so that this stage operates as an inverting amplifier.

$$\therefore \quad -27 = -\frac{R_f}{R_3} \quad \text{or} \quad R_3 = \frac{R_f}{27} = \frac{270\ \text{k}\Omega}{27} = \mathbf{10\ k\Omega}$$

$$\text{Overall voltage gain, } A = A_1A_2A_3 = (10) \times (-18) \times (-27) = 4860$$

$$\text{Output voltage, } v_{out} = A \times v_{in} = (4860) \times (150\ \mu\text{V}) = \mathbf{0.729\ V}$$

Example 25.40. *Show the connection of three OP-amp stages using an LM 348 IC to provide outputs that are 10, 20, and 50 times larger than the input and 180° out of phase w.r.t. input. Use a feedback resistor of R_f = 500 kΩ in all stages.*

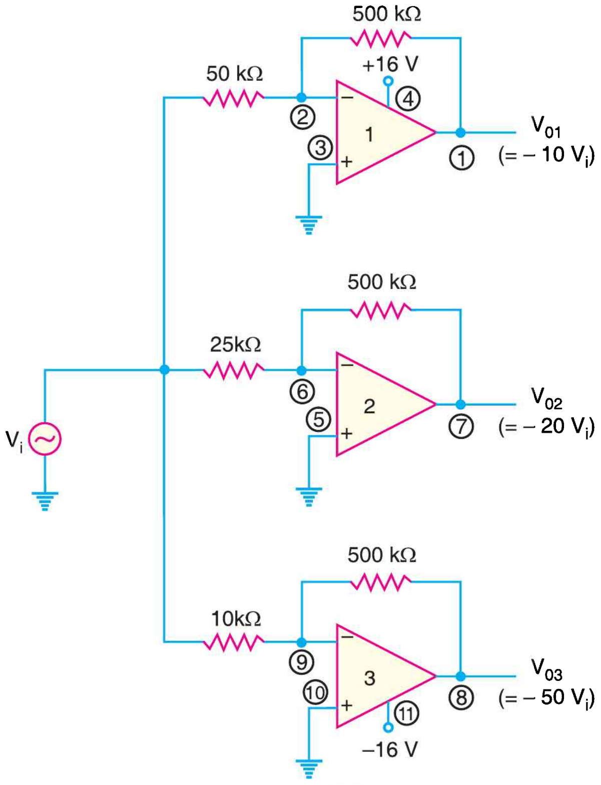


Fig. 25.65

Solution. The resistor component for each stage will be :

$$R_1 = -\frac{R_f}{A_1} = -\frac{500\ \text{k}\Omega}{-10} = \mathbf{50\ k\Omega}$$

$$R_2 = -\frac{R_f}{A_2} = -\frac{500\ \text{k}\Omega}{-20} = \mathbf{25\ k\Omega}$$

$$R_3 = -\frac{R_f}{A_3} = -\frac{500\ \text{k}\Omega}{-50} = \mathbf{10\ k\Omega}$$

The resulting circuit is shown in Fig. 25.65.

25.29 Effect of Negative Feedback on OP-Amp Impedances

In a negative feedback amplifier, a part of the output is fed in phase opposition to the input. The negative feedback produces remarkable changes in the circuit performance. The advantages of negative feedback are : stable gain, less distortion, increased bandwidth and affecting the input impedance and output impedance of the circuit. We now discuss the effect of negative feedback on the impedances of both noninverting and inverting amplifiers.

(*i*) Noninverting Amplifier. (Fig. 25.66). The expressions for the input and output impedances on account of negative voltage feedback in noninverting amplifier are the same as for discrete amplifier (Art. 13.4).

$$Z_{in}\,(*NI) = Z_{in}(1 + m_v A_{OL})$$

$$Z_{out}\,(NI) = \frac{Z_{out}}{1 + m_v\,A_{OL}}$$

where Z_{in}, Z_{out} = impedance values without feedback

$Z_{in}(NI), Z_{out}(NI)$ = impedance values with negative feedback

m_v = feedback factor

A_{OL} = voltage gain without feedback = open-loop gain

Note that negative feedback in noninverting amplifier has greatly increased the input impedance and at the same time decreased the output impedance. The increased impedance is an advantage because the amplifier will now present less of a load to its source circuit.

The decreased output impedance is also a benefit because the amplifier will be better suited to drive low impedance loads.

Voltage-follower (*VF*) impedances. Since voltage follower is a special case of noninverting amplifier with feedback fraction $m_v = 1$,

$$\therefore \quad Z_{in(VF)} = Z_{in}\,(1 + A_{OL})$$

$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{OL}}$$

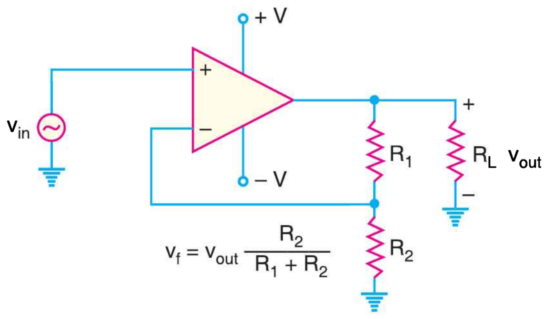


Fig. 25.66

Noninverting feedback amplifier.

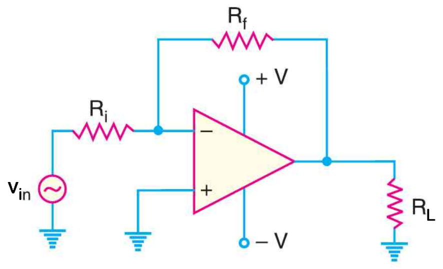


Fig. 25.67

Inverting feedback amplifier.

---

* Note that '*NI*' means noninverting amplifier.

Note that the voltage-follower input impedance is greater for given Z_{in} and A_{OL} than for the non-inverting configuration with the voltage-divider feedback circuit. Also, its output impedance is much smaller.

(*ii*) **Inverting Amplifier.** Fig. 25.67 shows the inverting amplifier. It can be shown that :

Input impedance, $Z_{in(*I)} \simeq R_i$

Output impedance, $Z_{out(I)} \simeq Z_{out}$ of *OP*-amp

Note that *the addition of negative voltage feedback to the inverting OP-amp reduces the input impedance of the circuit.* The reduction of Z_{in} is the primary difference betwen the inverting and the noninverting negative feedback circuits. Otherwise, the effects of negative voltage feedback are nearly identical for the two circuits.

Example 25.41. (*i*) *Determine the input and output impedances of the amplifier in Fig. 25.68. The OP-amp date sheet gives* $Z_{in} = 2\ \text{M}\Omega$, $Z_{out} = 75\ \Omega$ *and open loop gain of 200,000.*

(*ii*) *Find the closed-loop voltage gain.*

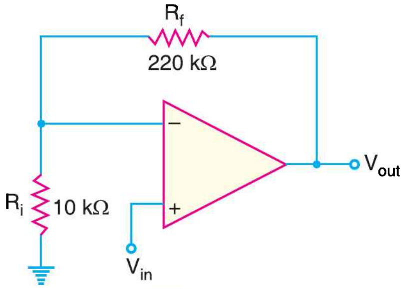


Fig. 25.68

Solution.

(*i*) Feedback fraction, $m_v = \dfrac{R_i}{R_i + R_f} = \dfrac{10\ \text{k}\Omega}{10\ \text{k}\Omega + 220\ \text{k}\Omega} = \dfrac{10\ \text{k}\Omega}{230\ \text{k}\Omega} = 0.043$

$$\text{Input impedance, } Z_{in(NI)} = Z_{in}(1 + A_{OL}m_v)$$
$$= (2\text{M}\Omega)\ [(1 + 200,000 \times 0.043)]$$
$$= (2\text{M}\Omega)\ [1 + 8600] = \mathbf{17{,}202\ M\Omega}$$

$$\text{Output impedance, } Z_{out(NI)} = \frac{Z_{out}}{1 + A_{OL}m_v} = \frac{75\ \Omega}{1 + 8600} = \mathbf{8.7 \times 10^{-3}\ \Omega}$$

(*ii*) Closed-loop voltage gain, $A_{CL} = 1 + \dfrac{R_f}{R_i} = 1 + \dfrac{220\ \text{k}\Omega}{10\ \text{k}\Omega} = \mathbf{23}$

Comments. Note the effect of negative voltage feedback on noninverting amplifier.

(*a*) Input and output signals are in phase.

(*b*) A virtually infinite input impedance.

(*c*) Virtually zero output impedance.

Example 25.42. *The same OP-amp in example 25.41 is used in a voltage-follower arrangement. Determine the input and output impedances.*

Solution. For voltage follower, feedback factor $m_v = 1$.

$$\therefore \quad Z_{in(VF)} = Z_{in}(1 + A_{OL}) = 2\text{M}\Omega\ (1 + 200{,}000) = \mathbf{400{,}002\ M\Omega}$$

$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{OL}} = \frac{75\ \Omega}{1 + 200{,}000} = \mathbf{0.38 \times 10^{-3}\ \Omega}$$

---

* Note that "*I*" means inverting amplifier.

Note that $Z_{in(VF)}$ is much greater than $Z_{in(NI)}$ and $Z_{out(VF)}$ is much less than $Z_{out(NI)}$ from example 25.41.

Example 25.43. *Find the values of the input and output impedances in Fig. 25.69. Also determine the closed-loop voltage gain. The OP-amp has the following parameters:* $Z_{in} = 4\ M\Omega$; $Z_{out} = 50\ \Omega$ *and open-loop voltage gain* $= 50{,}000$.

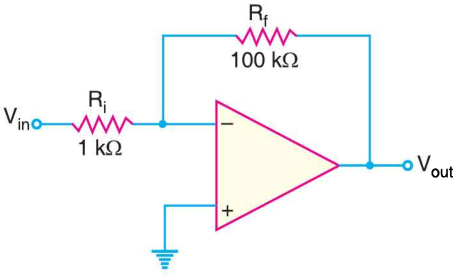


Fig. 25.69

Solution.

$$Z_{in}(I) \simeq R_i = \mathbf{1\ k\Omega}$$

$$Z_{out}(I) \simeq Z_{out} = \mathbf{50\ \Omega}$$

$$A_{CL} = -\frac{R_f}{R_i} = -\frac{100\ k\Omega}{1\ k\Omega} = \mathbf{-100}$$

25.30 Faults in Feedback Circuit

A failure of the feedback circuit in an *OP*-amp is one of the easiest problems in the world to locate. The most noticeable effect is that *voltage gain of the amplifier will change drastically.* Sometimes the gain will increase; sometimes it will decrease. It all depends on which component goes bad. For example, consider the circuit shown in Fig. 25.70.

(*i*) Under normal conditions: Under normal conditions, the output from the amplifier is $v_{out} = A_{CL}\, v_{in}$. The waveform would be correct. This is shown in Fig. 25.70 (*i*)

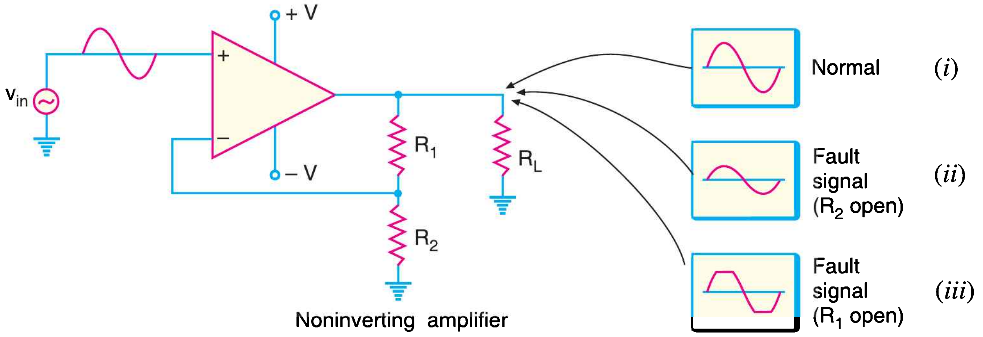


Fig. 25.70

(*ii*) When R_2 is open: If R_2 opens, the feedback circuit would consist solely of R_1. In this case, the gain would *drop*. It is because the circuit would now act as a *voltage follower. In other words, the circuit would now be a buffer with an output voltage that is equal to the input voltage. Thus we would have the output signal as shown in Fig. 25.70 (*ii*). The waveform would be correct but we would have unity gain.

(*iii*) When R_1 is open: When R_1 opens, the entire feedback circuit would be effectively removed. This would cause the gain of the amplifier to increase to the value of open-loop gain A_{OL}. Clearly, the output voltage will clip at or near the values of $+V$ and $-V$. This results in the distorted output signal as shown in Fig. 25.70 (*iii*).

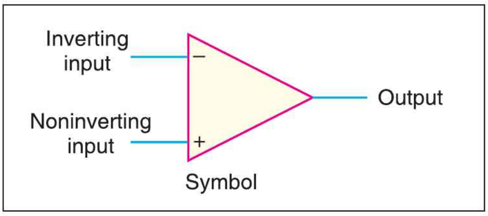
---

* $A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{R_1}{R_2} = 1 + \frac{R_1}{\infty} = 1 + 0 = 1$

Under these conditions, the closed-loop voltage gain would be unity.

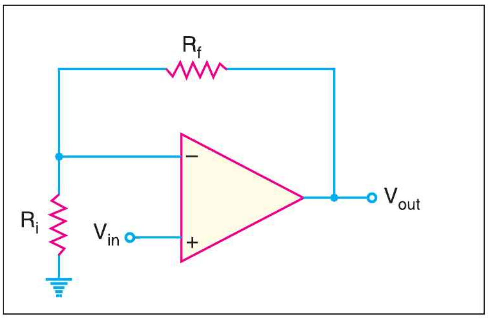
25.31 Summary of OP-AMP Configurations

Basic OP-AMP



- Very high open-loop voltage gain
- Very high input impedance
- Very low output impedance

Noninverting Amplifier



- Voltage gain:

$$A_{CL}(NI) = 1 + \frac{R_f}{R_i}$$

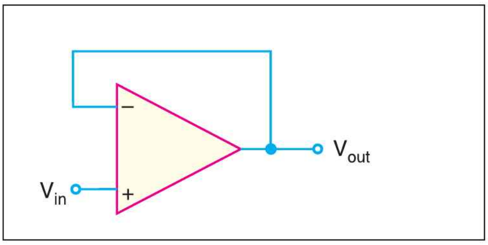
- Input impedance:

$$Z_{in(NI)} = (1 + A_{OL} m_v)\, Z_{in}$$

- Output impedance:

$$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{OL} m_v}$$

Voltage Follower



- Voltage gain:

$$A_{CL(VF)} = 1$$

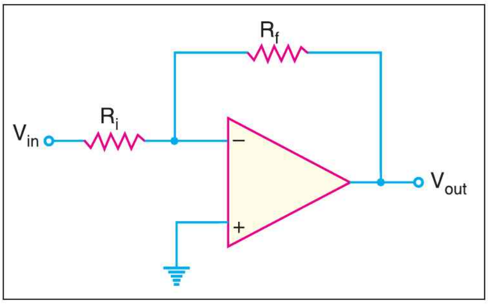
- Input impedance:

$$Z_{in(VF)} = (1 + A_{OL})\, Z_{in}$$

- Output impedance:

$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{OL}}$$

Inverting Amplifier



- Voltage gain:

$$A_{CL} = -\frac{R_f}{R_i}$$

- Input impedance:

$$Z_{in(I)} \simeq R_i$$

- Output impedance:

$$Z_{out(I)} \simeq Z_{out}$$

25.32 Summing Amplifiers

A summing amplifier is an inverted *OP*-amp that can accept two or more inputs. *The output voltage of a summing amplifier* is *proportional to the negative of the algebraic sum of its input voltages.* Hence the name **summing amplifier**. Fig. 25.71 shows a three-input summing amplifier but any number of inputs can be used. Three voltages V_1, V_2 and V_3 are applied to the inputs and produce currents I_1, I_2 and I_3. Using the concepts of infinite impedance and virtual ground, you can see that inverting input of the *OP*-amp is at virtual ground (0*V*) and there is no current to the input. This means that the three input currents I_1, I_2 and I_3 combine at the summing point *A* and form the total current (I_f) which goes through R_f as shown in Fig. 25.71.

$$\therefore \quad I_f = I_1 + I_2 + I_3$$

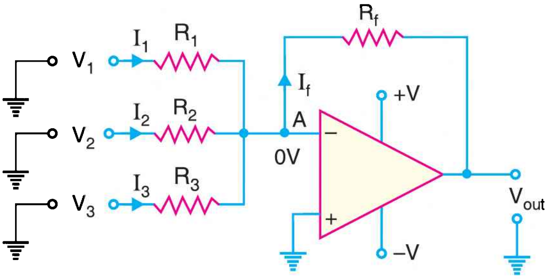


Fig. 25.71

When all the three inputs are applied, the output voltage is

$$\text{Output voltage, } V_{out} = -I_f R_f = -R_f (I_1 + I_2 + I_3)$$

$$= -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

$$\therefore \quad V_{out} = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

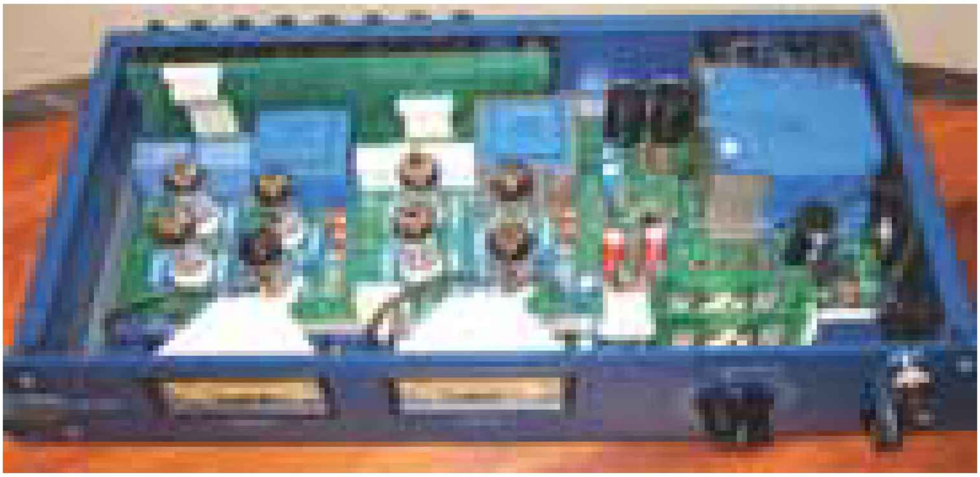
If $R_1 = R_2 = R_3 = R$, then, we have,

$$V_{out} = -\frac{R_f}{R} (V_1 + V_2 + V_3)$$

Thus the output voltage is proportional to the algebraic sum of the input voltages (of course neglecting negative sign). An interesting case results when the **gain of the amplifier is unity.** In that case, $R_f = R_1 = R_2 = R_3$ and output voltage is

$$V_{out} = -(V_1 + V_2 + V_3)$$

Thus, when the gain of summing amplifier is unity, the output voltage is the algebraic sum of the input voltages.



Summing Amplifier

Summing amplifier with gain greater than unity. When R_f is larger than the input resistors, the amplifer has a gain of R_f/R where R is the value of each input resistor. The general expression for the output voltage is

$$V_{out} = -\frac{R_f}{R}(V_1 + V_2 + V_3 + \ldots)$$

As you can see, the output voltage is the sum of input voltages multiplied by a constant determined by the ratio R_f/R.

Example 25.44. *Determine the output voltage for the summing amplifier in Fig. 25.72.*

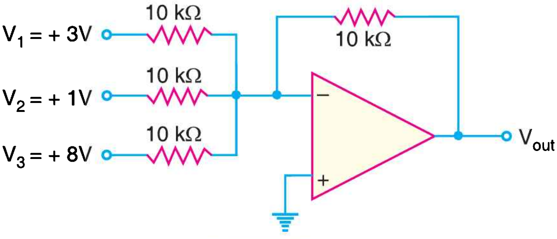


Fig. 25.72

Solution. Referring to Fig. 25.72, all the three input resistor values are equal and each is equal to the value of feedback resistor. Therefore, the gain of the summing amplifier is 1. As a result, the output voltage is the algebraic sum of three input voltages.

$\therefore \quad V_{out} = -(V_1 + V_2 + V_3) = -(3 + 1 + 8) = \mathbf{-12\ V}$

Example 25.45. *Determine the output voltage for the summing amplifier shown in Fig. 25.73.*

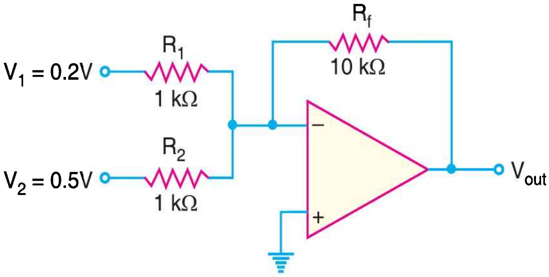


Fig. 25.73

Solution. $R_f = 10$ kΩ and $R_1 = R_2 = R = 1$ kΩ. Therefore, gain of the amplifier = $-R_f/R$ = – 10 kΩ/1kΩ = – 10.

Now $$V_{out} = -\frac{R_f}{R}(V_1 + V_2) = -\frac{10\text{ k}\Omega}{1\text{k}\Omega}(0.2 + 0.5) = \mathbf{-7V}$$

Note that the output voltage is not equal to the sum of input voltages. Rather it is equal to the sum of input voltages multiplied by the amplifier gain. In other words, the output voltage is proportional to the sum of the input voltages.

Example 25.46. *Determine the output voltage for the summing amplifier shown in Fig. 25.74.*

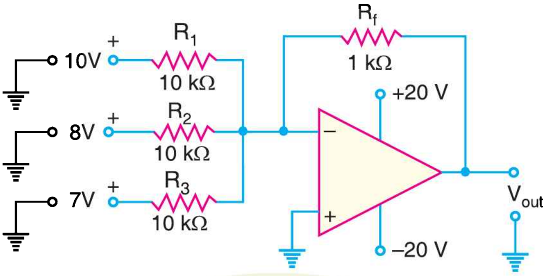


Fig. 25.74

Solution. $R_f = 1$ kΩ and $R_1 = R_2 = R_3 = R = 10$ kΩ. Therefore, gain of the amplifier $= -R_f/R = -1$ kΩ/10 kΩ $= -1/10$.

Now
$$V_{out} = -\frac{R_f}{R}(V_1 + V_2 + V_3) = -\frac{1\,\text{k}\Omega}{10\,\text{k}\Omega}(10 + 8 + 7) = \mathbf{-2.5\ V}$$

Note that output voltage of the amplifier is not equal to the sum of input voltages, but rather is proportional to the sum of input voltages. In this case, it is equal to one-tenth of the input sum. Picking random values of V_1, V_2 and V_3 will show that this circuit always provides an output voltage that is one-tenth of the sum of input voltages.

Example 25.47. *Two voltages of + 0.6V and – 1.4 V are applied to the two input resistors of a summing amplifier. The respective input resistors are 400 kΩ and 100 kΩ and feedback resistor is 200 kΩ. Determine the output voltage.*

Solution. The output voltage of the summing amplifier is given by:

$$V_{out} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

Here $R_f = 200$ kΩ; $R_1 = 400$ kΩ; $R_2 = 100$ kΩ; $V_1 = +0.6$V; $V_2 = -1.4$ V

$$\therefore \quad V_{out} = -200\,k\Omega\left(\frac{0.6}{400\,k\Omega} + \frac{-1.4}{100\,k\Omega}\right) = \mathbf{2.5\ V}$$

Note that a summing amplifier produces an output voltage that is proportional to the *algebraic sum of* the input voltages.

Example 25.48. *Determine the output voltage from the circuit shown in Fig. 25.75 for each of the following input combinations*:

V_1(V)	V_2(V)	V_3(V)
+ 10	0	+10
0	+10	+10
+10	+10	+10

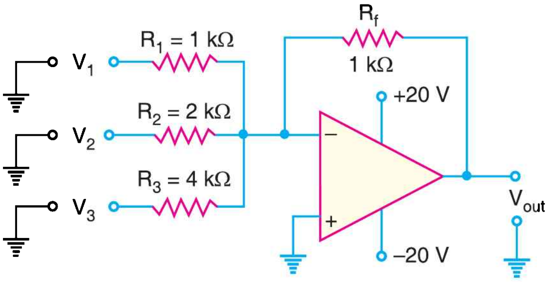


Fig. 25.75

Solution. The output voltage from the circuit is given by:

$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$$= -\left(\frac{1k\Omega}{1\,k\Omega}V_1 + \frac{1k\Omega}{2\,k\Omega}V_2 + \frac{1k\Omega}{4\,k\Omega}V_3\right)$$

$$\therefore \quad V_{out} = -(V_1 + 0.5\,V_2 + 0.25\,V_3)$$

The output voltage for the first set of inputs is

$$V_{out} = -(10 + 0.5 \times 0 + 0.25 \times 10) = \mathbf{-12.5\ V}$$

The output voltage for the second set of inputs is

$$V_{out} = -(0 + 0.5 \times 10 + 0.25 \times 10) = \mathbf{-7.5\ V}$$

The output voltage for the third set of inputs is

$$V_{out} = -(10 + 0.5 \times 10 + 0.25 \times 10) = \mathbf{-17.5\ V}$$

Example 25.49. *Calculate the output voltage for the circuit of Fig. 25.76. The inputs are V_1 = 50 sin (1000 t) mV and V_2 = 10 sin (3000t) mV.*

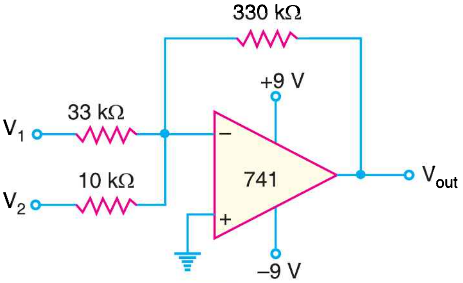


Fig. 25.76

Solution. The output voltage for the circuit is

$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right) = -\left(\frac{330k\Omega}{33k\Omega}V_1 + \frac{330k\Omega}{10k\Omega}V_2\right)$$

$$= -(10\,V_1 + 33\,V_2) = -[10 \times 50 \sin(1000t) + 33 \times 10 \sin(3000t)]\ \text{mV}$$

$$= \mathbf{-[0.5 \sin(1000\,t) + 0.33 \sin(3000t)]\ V}$$

25.33 Applications of Summing Amplifiers

By proper modifications, a summing amplifier can be made to perform many useful functions. There are a number of applications of summing amplifiers. However, we shall discuss the following two applications by way of illustration:

1. As averaging amplifier
2. As subtractor

1. As averaging amplifier. By using the proper input and feedback resistor values, a summing amplifier can be designed to provide an output voltage that is equal to the *average* of input voltages. A summing amplifier will act as an averaging amplifier when *both* of the following conditions are met:

(*i*) All input resistors (R_1, R_2 and so on) are *equal in value.*

(*ii*) The ratio of any input resistor to the feedback resistor is equal to the number of input circuits.

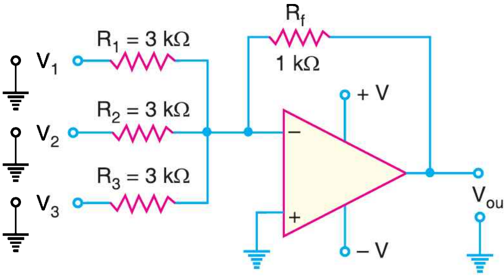


Fig. 25.77

Fig. 25.77 shows the circuit of averaging amplifier. Note that it is a summing amplifier meeting the above two conditions. All input resistors are equal in value (3 kΩ). If we take the ratio of any input resistor to the feedback resistor, we get 3 kΩ/ 1 kΩ = 3. This is equal to the number of inputs to the circuit. Referring to the circuit in Fig. 25.77, the output voltage is given by;

$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Now $$\frac{R_f}{R_1} = \frac{R_f}{R_2} = \frac{R_f}{R_3} = \frac{1\,\text{k}\Omega}{3\,\text{k}\Omega} = \frac{1}{3}$$

∴ $$V_{out} = -\left(\frac{V_1 + V_2 + V_3}{3}\right)$$

Note that V_{out} is equal to the average of the three inputs. The negative sign shows the phase reversal.

2. As subtractor. A summing amplifier can be used to provide an output voltage that is equal to the difference of two voltages. Such a circuit is called a **subtractor** and is shown in Fig. 25.78. As we shall see, this circuit will provide an output voltage that is equal to the difference between V_1 and V_2.

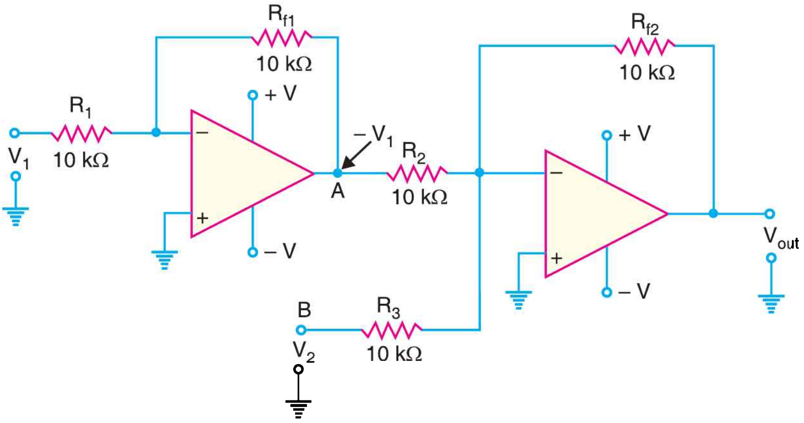


Fig. 25.78

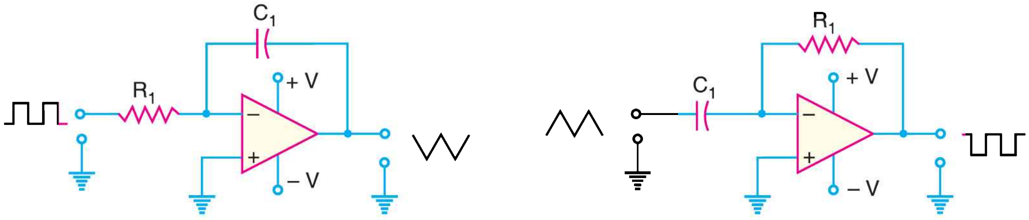
The voltage V_1 is applied to a standard inverting amplifier that has *unity gain*. Because of this, the output from the inverting amplifier will be equal to $-V_1$. This output is then applied to the summing amplifier (also having unity gain) along with V_2. Thus output from second *OP*-amp is given by;

$$V_{out} = -(V_A + V_B) = -(-V_1 + V_2) = V_1 - V_2$$

It may be noted that the gain of the second stage in the subtractor can be varied to provide an output that is proportional to (rather than equal to) the difference between the input voltages. However, if the circuit is to act as a subtractor, the input inverting amplifier ***must*** have unity gain. Otherwise, the output will not be proportional to the true difference between V_1 and V_2.

25.34 OP-Amp Integrators and Differentiators

A circuit that performs the mathematical integration of input signal is called an *integrator*. The output of an integrator is proportional to the area of the input waveform over a period of time. A circuit that performs the mathematical differentiation of input signal is called a *differentiator*. The output of a differentiator is proportional to the rate of change of its input signal. Note that the two operations are opposite.



OP-amp Integrator

(*i*)

OP-amp differentiator

(*ii*)

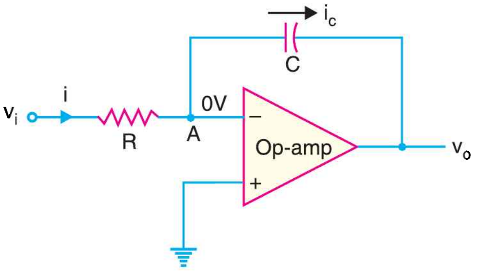
Fig. 25.79

Fig.25.79 shows *OP*-amp integrator and differentiator. As you can see, the two circuits are nearly identical in terms of their construction. Each contains a single *OP*-amp and an *RC* circuit. However, the difference in resistor/capacitor placement in the two circuits causes them to have input/output relationships that are exact opposites. For example, if the input to the integrator is a square wave, the output will be a triangular wave as shown in Fig. 25.79 (*i*). However, the differentiator will convert a triangular wave into square wave as shown in Fig. 25.79 (*ii*).

25.35 *OP*-Amp Integrator

As discussed above, an integrator is a circuit that performs integration of the input signal. The most popular application of an integrator is to produce a *ramp* output voltage (*i.e.* a linearly increasing or decreasing voltage). Fig. 25.80 shows the circuit of an *OP*-amp integrator. It consists of an *OP*-amp, input resistor *R* and feedback capacitor *C*. Note that the feedback component is a capacitor instead of a resistor.

As we shall see, when a signal is applied to the input of this circuit, the output-signal waveform will be the integration of input-signal waveform.



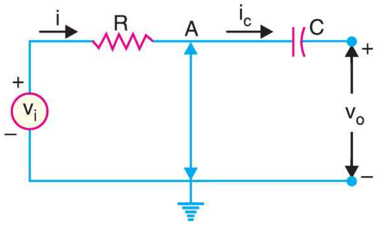


Fig. 25.80

Fig. 25.81

Circuit Analysis. Since point *A* in Fig. 25.80 is at virtual ground, the *virtual-ground equivalent circuit of operational integrator will be as shown in Fig. 25.81. Because of virtual ground and infinite impedance of the *OP*-amp, all of the input current *i* flows through the capacitor *i.e.* $i = i_c$.

Now $$i = \frac{v_i - 0}{R} = \frac{v_i}{R} \qquad ...(i)$$

Also voltage across capacitor is $v_c = 0 - v_o = -v_o$

$$\therefore \quad i_c = \frac{C\,dv_c}{dt} = -C\frac{dv_o}{dt} \qquad ...(ii)$$

---

* Recall that virtual ground means that point *A* is 0V but it is not mechanically grounded. Therefore, no current flows from point *A* to ground.

From eqs. (*i*) and (*ii*), $$\frac{v_i}{R} = -C\frac{dv_o}{dt}$$

or $$\frac{dv_o}{dt} = -\frac{1}{RC}v_i \quad ...(iii)$$

To find the output voltage, we integrate both sides of eq. (*iii*) to get,

$$v_o = -\frac{1}{RC}\int_0^t v_i\, dt \quad ...(iv)$$

Eq. (*iv*) shows that the output is the integral of the input with an inversion and scale multiplier of $1/RC$.

Output voltage. If a fixed voltage is applied to the input of an integrator, eq. (*iv*) shows that the output voltage grows over a period of time, providing a ramp voltage. Eq. (*iv*) also shows that the output voltage ramp (for a fixed input voltage) is opposite in polarity to the input voltage and is multiplied by the factor $1/RC$. As an example, consider an input voltage v_1 = 1V to the integrator circuit of Fig. 25.82 (*i*). The scale factor of $1/RC$ is

$$-\frac{1}{RC} = -\frac{1}{(1\,\text{M}\Omega)\,(1\mu\text{F})} = -1$$

so that the output is a negative ramp voltage as shown in Fig. 25.82 (*ii*).

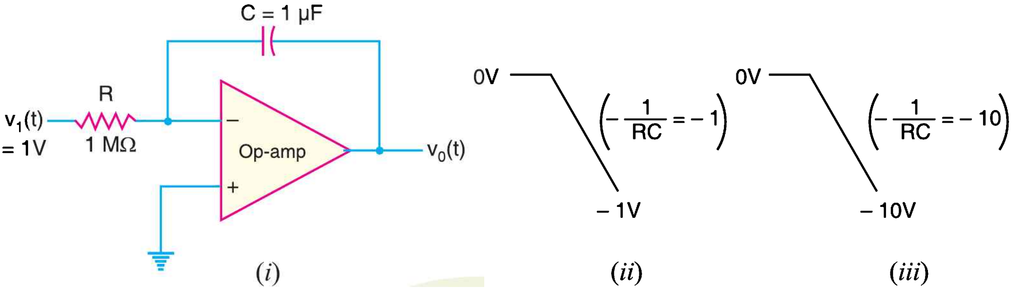


Fig. 25.82

If the scale factor is changed by making R = 100 kΩ, then,

$$-\frac{1}{RC} = -\frac{1}{(100\,\text{k}\Omega)\,(1\mu\text{F})} = -10$$

and output is then a steeper ramp voltage as shown in Fig. 25.82 (*iii*).

25.36 Critical Frequency of Integrators

The integrator shown in Fig. 25.80 (Refer back) has no feedback at 0 Hz. This is a serious disadvantage in low-frequency applications. By connecting a feedback resistor R_f in parallel with the capacitor, precise closed-loop voltage gain is possible. The circuit shown in Fig. 25.83 is an integrator with a feedback resistor R_f to provide increased stability.

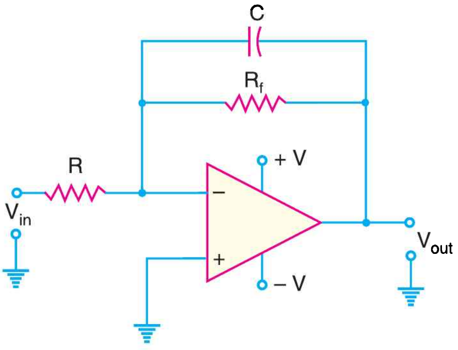
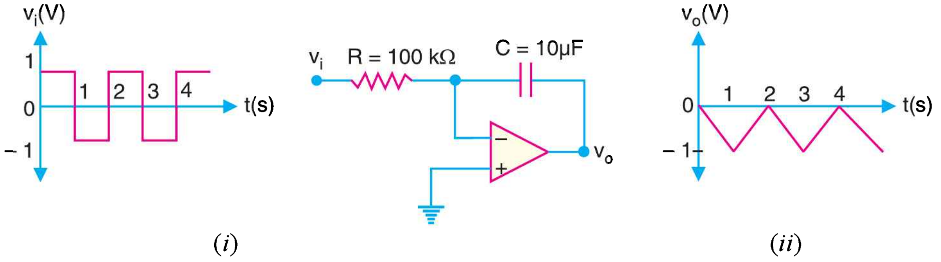


Fig. 25.83

All integrators have a critical frequency f_c below which they do not perform proper integration. If the input frequency is less than f_c, the circuit behaves like a simple inverting amplifier and no integration occurs. The following equation is used to calculate the critical frequency of an integrator:

$$f_c = \frac{1}{2\pi R_f C}$$

Example 25.50. *Fig. 25.84 (i) shows the OP-amp integrator and the square wave input. Find the output voltage.*



(*i*) (*ii*)

Fig. 25.84

Solution. The output voltage of this circuit is given by;

$$v_o = -\frac{1}{RC}\int_0^t v_i\,dt$$

Now $RC = (100\text{ k}\Omega)(10\ \mu\text{F}) = (100 \times 10^3\Omega)(10 \times 10^{-6}\text{ F}) = 1\text{s}$

$$\therefore \quad v_o = -\int_0^t v_i\,dt$$

When we integrate a constant, we get a straight line. In other words, when input voltage to an integrator is constant, the output is a linear ramp. Therefore, the integration of the square wave results in the triangular wave as shown in Fig. 25.84 (*ii*). Since the input to the integrator is applied to the inverting input, the output of the circuit will be 180° out of phase with the input. Thus, when the input goes positive, the output will be a negative ramp. When the input is negative, the output will be a positive ramp. Fig. 25.84 (*ii*) shows this relationship.

Example 25.51. *Determine the lower frequency limit (critical frequency) for the integrator circuit shown in Fig. 25.85.*

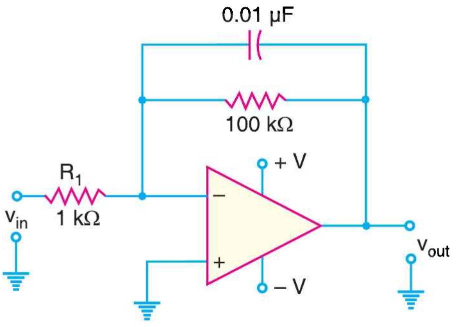


Fig. 25.85

Solution. The critical frequency for the integrator circuit shown in Fig. 25.85 is given by;

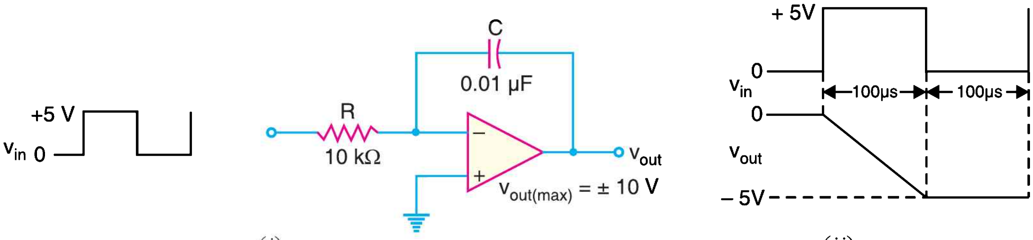
$$f_c = \frac{1}{2\pi R_f C}$$

Here $R_f = 100\text{ k}\Omega = 10^5\Omega$; $C = 0.01\ \mu\text{F} = 0.01 \times 10^{-6}$ F

$$\therefore \qquad f_c = \frac{1}{2\pi \times (10^5) \times (0.01 \times 10^{-6})} = \mathbf{159\ Hz}$$

Example 25.52. (*i*) *Determine the rate of change of the output voltage in response to a single pulse input to the integrator circuit shown in Fig. 25.86* (*i*).

(*ii*) *Draw the output waveform.*



(*i*) (*ii*)

Fig. 25.86

Solution.

(*i*) Output voltage, $v_{out} = -\frac{1}{RC}\int_0^t v_{in}\,dt$

Therefore, the rate of change of output voltage is

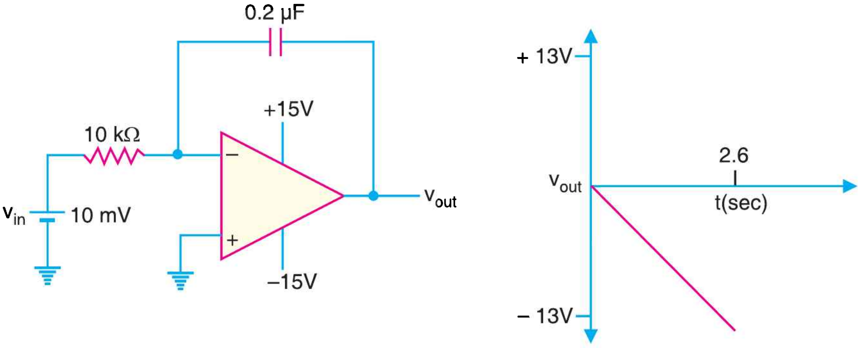
$$\frac{\Delta v_{out}}{dt} = -\frac{v_{in}}{RC} = -\frac{5\text{ V}}{(10\text{ k}\Omega)\,(0.01\,\mu\text{F})} = -\,50\text{ kV/s} = \mathbf{-\,50\ mV/\mu s}$$

(*ii*) The rate of change of output voltage is – 50 mV/μ*s*. When the input is at + 5 V, the output is a negative-going ramp. When the input is at 0 V, the output is a constant level. In 100 μ*s*, the output voltage decreases.

$$\therefore \qquad \Delta\, v_{out} = \frac{\Delta v_{out}}{dt} \times dt = -\frac{50\text{ mV}}{\mu\text{s}} \times 100\,\mu\text{s} = -\,5\text{V}$$

Therefore, the negative-going ramp reaches – 5 V at the end of the pulse (*i.e.* after 100 μ*s* from the initial condition). The output voltage then remains constant at – 5 V for the time the input is zero. Fig. 25.86 (*ii*) shows the output waveform.

Example 25.53. *For the integrator circuit shown in Fig. 25.87 (i), how long does it take for the output to reach saturation ?*



(*i*) (*ii*)

Fig. 25.87

Solution.

$$\text{Output voltage, } v_{out} = -\frac{1}{RC}\int_0^t v_{in}\,dt$$

Since the input voltage v_{in} (= 10 mV) is constant,

$$\therefore \quad v_{out} = -\frac{1}{RC}v_{in}t = -\frac{1}{(10\,k\Omega)\,(0.2\,\mu F)}\times(10\,mV)\times t$$

$$\text{or} \quad v_{out} = -\,5t \text{ volts}$$

$$\text{Now} \quad \text{Saturation voltage, } V_s = -\,V_{supply} + 2 = -\,15 + 2 = -\,13\text{ V}$$

$$\therefore \quad \text{Time required, } t = \frac{V_s}{-5} = \frac{-13}{-5} = \mathbf{2.6\ seconds}$$

Fig. 25.87 (*ii*) shows the output waveform.

25.37 OP-Amp Differentiator

A differentiator is a circuit that performs differentiation of the input signal. In other words, a differentiator produces an output voltage that is proportional to the rate of change of the input voltage. Its important application is to produce a rectangular output from a ramp input. Fig. 25.88 shows the circuit of OP-amp differentiator. It consists of an OP-amp, an input capacitor *C* and feedback resistor *R*. Note how the placement of the capacitor and resistor differs from the integrator. The capacitor is now the input element.

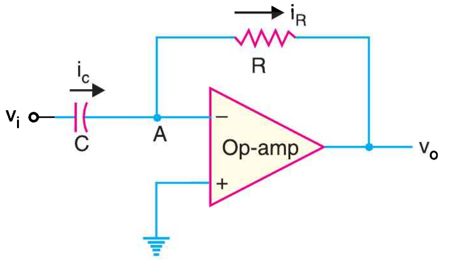


Fig. 25.88

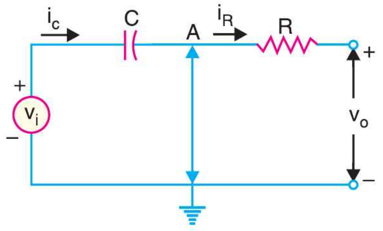


Fig. 25.89

Circuit analysis. Since point *A* in Fig. 25.88 is at virtual ground, the virtual-ground equivalent circuit of the operational differentiator will be as shown in Fig. 25.89. Because of virtual ground and infinite impedance of OP-amp, all the input current i_c flows through the feedback resistor *R* *i.e.* $i_c = i_R$.

$$\therefore \quad i_R = \frac{0 - v_o}{R} = -\frac{v_o}{R} \quad \text{and} \quad v_c = v_i - 0 = v_i$$

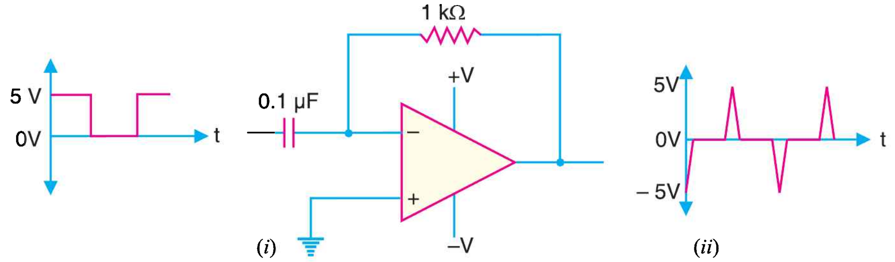
$$\text{Also} \quad i_c = C\frac{dv_c}{dt} = C\frac{dv_i}{dt}$$

$$\therefore \quad -\frac{v_o}{R} = C\frac{dv_i}{dt} \qquad (\because\ i_R = i_c)$$

$$\text{or} \quad v_o = -RC\frac{dv_i}{dt} \qquad \text{...}(i)$$

Eq. (*i*) shows that output is the differentiation of the input with an inversion and scale multiplier of *RC*. If we examine eq. (*i*), we see that if the input voltage is constant, dv_i/dt is zero and the output voltage is zero. The faster the input voltage changes, the larger the magnitude of the output voltage.

Example 25.54. *Fig. 25.90 (i) shows the square wave input to a differentiator circuit. Find the output voltage if input goes from 0V to 5V in 0.1 ms.*



(*i*) (*ii*)

Fig. 25.90

Solution. Output voltage, $v_o = -RC\dfrac{dv_i}{dt}$

Now, $RC = (1\text{ k}\Omega)\times(0.1\ \mu\text{F}) = (10^3\ \Omega)\,(0.1\times10^{-6}\text{F}) = 0.1\times10^{-3}\,s$

Also, $\dfrac{dv_i}{dt} = \dfrac{5\text{V}}{0.1\text{ ms}} = \dfrac{5\times10^4\text{ V}}{s} = 5\times10^4\text{ V/s}$

$\therefore\quad v_o = -(0.1\times10^{-3})\,(5\times10^4) = \mathbf{-5V}$

The signal quickly returns to zero as the input signal becomes constant. The output will be as shown in Fig. 25.90 (*ii*).

Example 25.55. *For the differentiator circuit shown in Fig. 25.91, determine the output voltage if the input goes from 0V to 10V in 0.4s. Assume the input voltage changes at constant rate.*

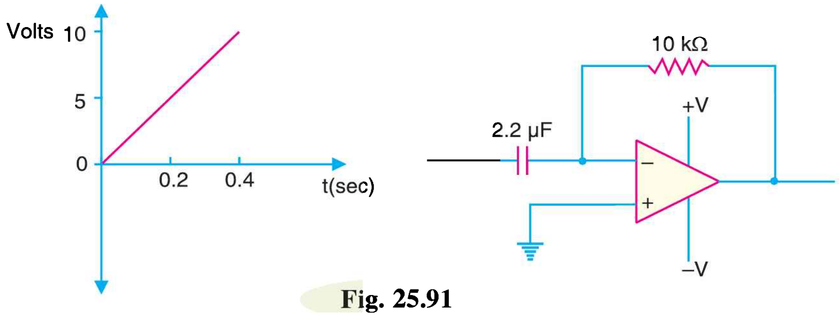


Fig. 25.91

Solution. Output voltage, $v_o = -RC\dfrac{dv_i}{dt}$

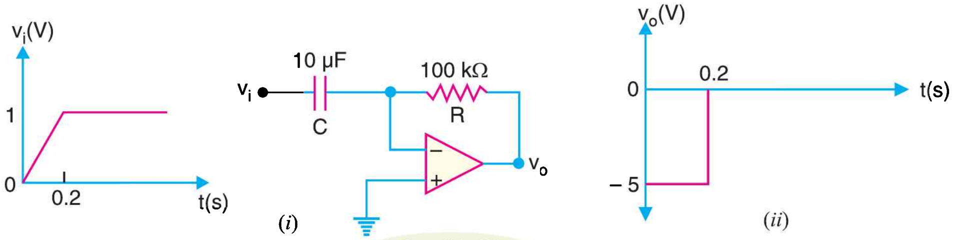
Now, $RC = (10\text{ k}\Omega)\times(2.2\ \mu\text{F}) = (10^4\ \Omega)\,(2.2\times10^{-6}\text{ F}) = 2.2\times10^{-2}\,s$

Also, $\dfrac{dv_i}{dt} = \dfrac{(10-0)\,V}{0.4s} = \dfrac{10\text{V}}{0.4\text{s}} = 25\text{ V/s}$

$\therefore\quad v_o = -(2.2\times10^{-2})\times25 = \mathbf{-0.55\ V}$

The output voltage stays constant at – 0.55 V.

Example 25.56. *For the differentiator circuit shown in Fig. 25.92(i), determine (i) the expression for the output voltage (ii) the output voltage for the given input.*



(*i*) (*ii*)

Fig. 25.92

Solution.

(*i*) For the differentiator shown in Fig. 25.92 (*i*), the output voltage is given by;

$$v_o = -RC\,\frac{dv_i}{dt} = -(100\,\text{k}\Omega)\times(10\,\mu\text{F})\,\frac{dv_i}{dt}$$

$$= -(100\times10^{3}\,\Omega)\times(10\times10^{-6}\,\text{F})\,\frac{dv_i}{dt} = -\frac{dv_i}{dt}$$

(*ii*) Since the input voltage is a straight line between 0 and 0.2*s*, the output voltage is

$$v_o = -\frac{dv_i}{dt} = -\frac{(1-0)}{0.2} = \mathbf{-5V}$$

Therefore, between 0 to 0.2*s*, the output voltage is constant at – 5 V. For *t* > 0.2*s*, the input is constant so that output voltage is zero. Fig. 25.92 (*ii*) shows the output waveform.

25.38. Comparators

Often we want to compare one voltage to another to see which is larger. In this situation, a *comparator* may be used. A *comparator is an OP-amp circuit without negative feedback* and takes advantage of very high open-loop voltage gain of OP-amp. A comparator has two input voltages (noninverting and inverting) and one output voltage. Because of the high open-loop voltage gain of an *OP*-amp, a very small difference voltage between the two inputs drives the amplifier to saturation. For example, consider an *OP*-amp having A_{OL} = 100,000. A voltage difference of only 0.25 mV between the inputs will produce an output voltage of (0.25 mV) (100,000) = 25V. However, most of OP-amps have output voltages of less than ± 15V because of their d.c. supply voltages. Therefore, a very small differential input voltage will drive the OP-amp to saturation. This is the key point in the working of comparator.

Fig. 25.93 illustrates the action of a comparator. The input voltages are v_1 (signal) and v_2 (*reference voltage). If the differential input is positive, the circuit is driven to saturation and output goes to maximum positive value (**$+V_{sat} = +13$V). Reverse happens when the differential input goes negative *i.e.* now output is maximum negative ($-V_{sat} = -13$V). This circuit is called comparator because it compares v_1 to v_2 to produce a saturated positive or negative output voltage. Note that output voltage rapidly changes from – 13V to + 13V and *vice-versa*.

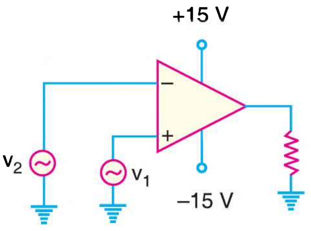


Fig. 25.93

25.39 Comparator Circuits

A comparator circuit has the following two characteristics :

(*i*) It uses no feedback so that the voltage gain is equal to the open-loop voltage gain (A_{OL}) of *OP*-amp.

(*ii*) It is operated in a non-linear mode.

These properties of a comparator permit it to perform many useful functions.

Two comparator integrated circuits.

---

* If this terminal is grounded, v_2 = 0V.

** Since in our case supply voltages are ± 15V,

$$+V_{sat} = +V_{supply} - 2 = 15 - 2 = +13\text{V}$$
$$-V_{sat} = -V_{supply} + 2 = -15 + 2 = -13\text{V}$$

1. As a square wave generator. A comparator can be used to produce a square wave output from a sine wave input. Fig. 25.94 shows the circuit of a comparator to produce square wave output. Note that inverting terminal (–) is grounded and signal (v_{in}) is applied to the noninverting terminal (+). Since the gain of a comparator is equal to A_{OL}, virtually any difference voltage at the inputs will cause the output to go to one of the voltage extremes (+ V_{sat} or – V_{sat}) and stay there until the voltage difference is removed. The polarity of the input difference voltage will determine to which extreme (+V_{sat} or – V_{sat}) the output of the comparator goes.

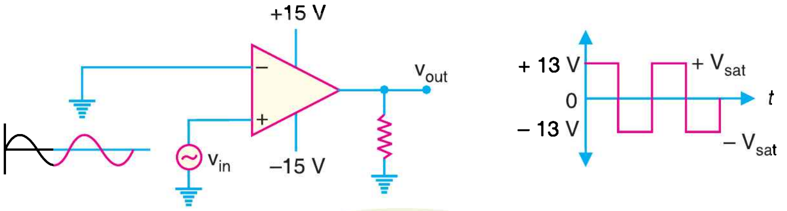


Fig. 25.94

When the input signal goes positive, the output jumps to about + 13 V. When the input goes negative, the output jumps to about – 13 V. The output changes rapidly from – 13 V to + 13 V and *vice-versa*. This change is so rapid that we get a square wave output for a sine wave input.

2. As a zero-crossing detector. When one input of a comparator is connected to ground, it is known as zero-crossing detector because the output changes when the input crosses 0 V. The zero-crossing circuit is shown in Fig. 25.95. The input and output waveforms are also shown. When the input signal is positive-going, the output is driven to positive maximum value (*i.e.* + V_{sat} = + 13 V). When the input crosses the zero axis and begins to go negative, the output is driven to negative maximum value (*i.e.* – V_{sat} = – 13 V).

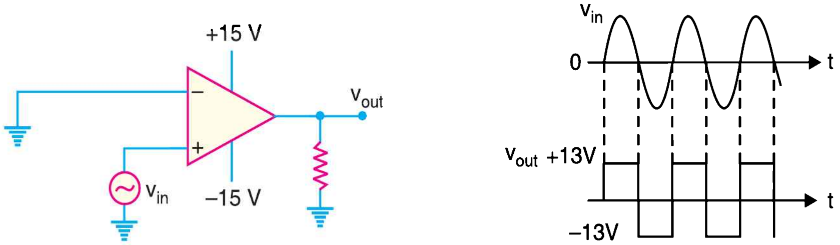


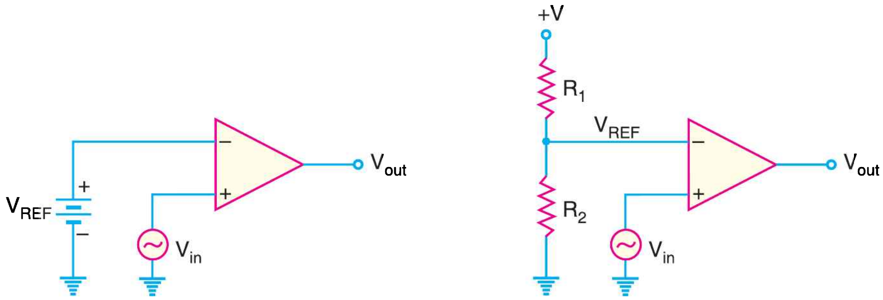
Fig. 25.95

From the input/output waveforms, you can see that every time the input crosses 0 V going positive, the output jumps to + 13 V. Similarly, every time the input crosses 0 V going negative, the output jumps to – 13 V. Since the change (+ 13 V or – 13 V) occurs every time the input crosses 0 V, we can tell when the input signal has crossed 0 V. Hence the name zero-crossing detector.

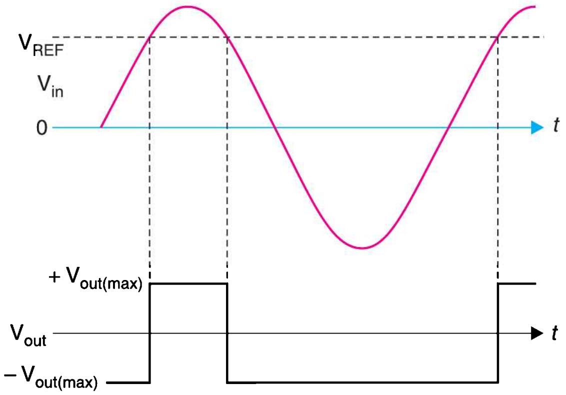
3. As a level detector. When a comparator is used to compare a signal amplitude to a fixed d.c. level (reference voltage), the circuit is referred to as a level detector. We can modify zero-crossing detector circuit to construct level detector. This can be done by connecting a fixed reference voltage V_{REF} to the inverting input as shown in Fig. 25.96 (*i*). A more practical arrangement is shown in Fig. 25.96 (*ii*) using a voltage divider to set the reference voltage as follows :

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V)$$

where + V is the positive *OP*-amp d.c. supply voltage.



(*i*) Battery reference (*ii*) Voltage-divider reference



(*iii*) Waveforms

Fig. 25.96

The circuit action is as follows. Suppose the input signal v_{in} is a sine wave. When the input voltage is less than the reference voltage (*i.e.* $V_{in} < V_{REF}$), the output goes to maximum negative level. It remains here until V_{in} increases above V_{REF}. When the input voltage exceeds the reference voltage (*i.e.* $V_{in} > V_{REF}$), the output goes to its maximum positive state. It remains here until V_{in} decreases below V_{REF}. Fig. 25.96 (*iii*) shows the input/output waveforms. Note that this circuit is used for non zero-level detection.

MULTIPLE-CHOICE QUESTIONS

1. A differential amplifier ....
(*i*) is a part of an OP-amp
(*ii*) has one input and one output
(*iii*) has two outputs
(*iv*) answers (*i*) and (*iii*)

2. When a differential amplifier is operated single-ended, ...
(*i*) the output is grounded
(*ii*) one input is grounded and signal is applied to the other
(*iii*) both inputs are connected together
(*iv*) the output is not inverted

3. In differential-mode, ...
(*i*) opposite polarity signals are applied to the inputs
(*ii*) the gain is one
(*iii*) the outputs are of different amplitudes
(*iv*) only one supply voltage is used

4. In the common-mode, ...
(*i*) both inputs are grounded
(*ii*) the outputs are connected together
(*iii*) an identical signal appears on both inputs
(*iv*) the output signals are in-phase

5. The common-mode gain is ....
(*i*) very high (*ii*) very low
(*iii*) always unity (*iv*) unpredictable

6. The differential gain is ....
(*i*) very high (*ii*) very low
(*iii*) dependent on input voltage
(*iv*) about 100

7. If $A_{DM} = 3500$ and $A_{CM} = 0.35$, the *CMRR* is ....
(*i*) 1225
(*ii*) 10,000
(*iii*) 80 *dB*
(*iv*) answers (*ii*) and (*iii*)

8. With zero volts on both inputs, an OP-amp ideally should have an output ....
(*i*) equal to the positive supply voltage
(*ii*) equal to the negative supply voltage
(*iii*) equal to zero
(*iv*) equal to the *CMRR*

9. Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is ....
(*i*) 1 (*ii*) 2000
(*iii*) 80 *dB* (*iv*) 100,000

10. A certain OP-amp has bias currents of 50 μA and 49.3 μA. The input offset current is ....
(*i*) 700 n*A* (*ii*) 99.3 μ*A*
(*iii*) 49.7 μ*A* (*iv*) none of these

11. The output of a particular OP-amp increases 8 V in 12 μs. The slew rate is ....
(*i*) 90 V/μs (*ii*) 0.67 V/μs
(*iii*) 1.5 V/μs (*iv*) none of these

12. For an OP-amp with negative feedback, the output is ....
(*i*) equal to the input
(*ii*) increased
(*iii*) fed back to the inverting input
(*iv*) fed back to the noninverting input

13. The use of negative feedback ....
(*i*) reduces the voltage gain of an OP-amp
(*ii*) makes the OP-amp oscillate
(*iii*) makes linear operation possible
(*iv*) answers (*i*) and (*iii*)

14. Negative feedback ....
(*i*) increases the input and output impedances
(*ii*) increases the input impedance and bandwidth
(*iii*) decreases the output impedance and bandwidth
(*iv*) does not affect impedance or bandwidth

15. A certain noninverting amplifier has R_i of 1 kΩ and R_f of 100 kΩ. The closed-loop voltage gain is ....
(*i*) 100,000 (*ii*) 1000
(*iii*) 101 (*iv*) 100

16. If feedback resistor in *Q*.15 is open, the voltage gain ....
(*i*) increases (*ii*) decreases
(*iii*) is not affected (*iv*) depends on R_i

17. A certain inverting amplifier has a closed-loop voltage gain of 25. The OP-amp has an open-loop voltage gain of 100,000. If an OP-amp with an open-loop voltage gain of 200,000 is substituted in the arrangement, the closed-loop gain ....
(*i*) doubles (*ii*) drops to 12.5
(*iii*) remains at 25 (*iv*) increases slightly

18. A voltage follower ....
(*i*) has a voltage gain of 1
(*ii*) in noninverting
(*iii*) has no feedback resistor
(*iv*) has all of these

19. The OP-amp can amplify ....
(*i*) a.c. signals only
(*ii*) d.c. signals only
(*iii*) both a.c. and d.c. signals
(*iv*) neither d.c. nor a.c. signals

20. The input offset current equals the ....
(*i*) difference between two base currents
(*ii*) average of two base currents
(*iii*) collector current divided by current gain
(*iv*) none of these

21. The tail current of a differential amplifier is ....
(*i*) half of either collector current

(*ii*) equal to either collector current
(*iii*) two times either collector current
(*iv*) equal to the difference in base currents

22. The node voltage at the top of the tail resistor is closest to ....
(*i*) collector supply voltage
(*ii*) zero
(*iii*) emitter supply voltage
(*iv*) tail current times base resistance

23. The tail current in a differential amplifier equals ....
(*i*) difference between two emitter currents
(*ii*) sum of two emitter currents
(*iii*) collector current divided by current gain
(*iv*) collector voltage divided by collector resistance

24. The differential voltage gain of a differential amplifier is equal to R_C divided by ....
(*i*) r'_e
(*ii*) $r'_e/2$
(*iii*) $2\,r'_e$
(*iv*) R_E

25. The input impedance of a differential amplifier equals r'_e times ....
(*i*) β
(*ii*) R_E
(*iii*) R_C
(*iv*) 2β

26. A common-mode signal is applied to ....
(*i*) the noninverting input
(*ii*) the inverting input
(*iii*) both inputs
(*iv*) top of the tail resistor

27. The common-mode voltage gain is ....
(*i*) smaller than differential voltage gain
(*ii*) equal to differential voltage gain
(*iii*) greater than differential voltage gain
(*iv*) none of the above

28. The input stage of an OP-amp is usually a ....
(*i*) differential amplifier
(*ii*) class *B* push-pull amplifier
(*iii*) *CE* amplifier
(*iv*) swamped amplifier

29. The common-mode voltage gain of a differential amplifier is equal to R_C divided by ....
(*i*) r'_e
(*ii*) $2\,r'_e$
(*iii*) $r'_e/2$
(*iv*) $2\,R_E$

30. Current cannot flow to ground through ....
(*i*) a mechanical ground
(*ii*) an a.c. ground
(*iii*) a virtual ground
(*iv*) an ordinary ground

Answers to Multiple-Choice Questions

1. (*iv*)	**2.** (*ii*)	**3.** (*i*)	**4.** (*iii*)	**5.** (*ii*)
6. (*i*)	**7.** (*iv*)	**8.** (*iii*)	**9.** (*iv*)	**10.** (*i*)
11. (*ii*)	**12.** (*iii*)	**13.** (*iv*)	**14.** (*ii*)	**15.** (*iii*)
16. (*i*)	**17.** (*iii*)	**18.** (*iv*)	**19.** (*iii*)	**20.** (*i*)
21. (*iii*)	**22.** (*ii*)	**23.** (*ii*)	**24.** (*iii*)	**25.** (*iv*)
26. (*iii*)	**27.** (*i*)	**28.** (*i*)	**29.** (*iv*)	**30.** (*iii*)

Chapter Review Topics

1. What is an operational amplifier (OP-amp)?
2. Give the block diagram of an operational amplifier.
3. What is a differential amplifier?
4. Draw the basic circuit of a differential amplifier.
5. Discuss the operation of a differential amplifier.
6. What do you mean by noninverting and inverting input of a differential amplifier?
7. What are common-mode and differential-mode signals?
8. What do you mean by *CMRR*?

9. What is the importance of *CMRR*?
10. Explain the d.c. analysis of a differential amplifier.
11. What do you mean by (*i*) output offset voltage (*ii*) input offset current?
12. Derive an expression for differential-mode voltage gain of a differential amplifier.
13. Derive an expression for the common-mode voltage gian of a differential amplifier.
14. Draw the schematic symbol of an operational amplifier indicating the various terminals.
15. What do you-mean by (*i*) open-loop voltage gain (*ii*) closed-loop voltage gain of an OP-amp?
16. Discuss OP-amp input/output polarity relationship.
17. What do you mean by bandwidth of an OP-amp?
18. What do you mean by slew rate of an OP-amp?
19. Discuss the frequency response of an OP-amp.
20. What is the need of negative feedback in an OP-amp?
21. Derive an expression for the voltage gain of an inverting amplifier.
22. Derive an expression for the voltage gain of a noninverting amplifier.
23. What is a voltage follower?
24. Draw the circuit of multistage OP-amp.
25. What is the effect of negative feedback on (*i*) noninverting amplifier (*ii*) inverting amplifier ?
26. Discuss the operation of a summing amplifier.
27. Discuss two applications of summing amplifiers.
28. Discuss the operation of an OP-amp integrator.
29. What is the most important application of an OP-amp integrator?
30. Discuss the operation of OP-amp differentiator.

Problems

1. In Fig 25.97, the transistors are identical with $\beta_{dc} = 200$. What is the output voltage? **[7.5 V]**

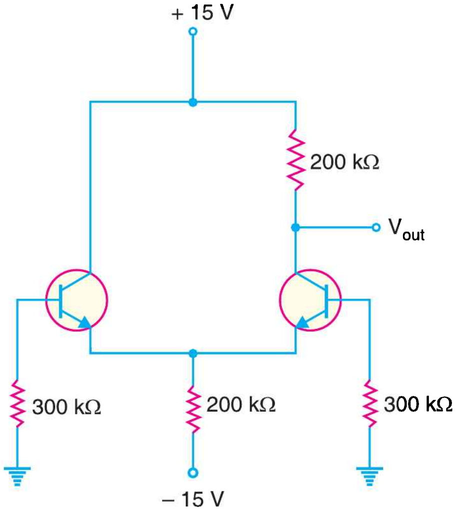


Fig. 25.97

2. In Fig. 25.97, the left transistor has $\beta_{dc} = 225$ and the right transistor has $\beta_{dc} = 275$. What are the base voltages? **[– 0.05 V ; – 0.0409 V]**

3. A data sheet gives an input bias current of 20 *nA* and an input offset current of 3 nA. What are the base currents? **[18.5 nA ; 21.5 nA]**

4. Find bias voltages and currents for the differential amplifier circuit in Fig. 25.98.

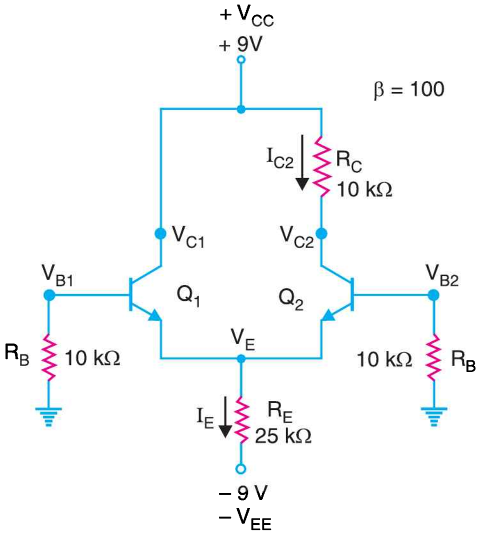

+ VCC
+ 9V
β = 100
I_C2
R_C
10 kΩ
V_C1
V_C2
V_B1
V_B2
Q_1
Q_2
V_E
R_B
10 kΩ
10 kΩ
R_B
I_E
R_E
25 kΩ
– 9 V
– V_EE

Fig. 25.98

[V_E = – 0.7 V ; I_E = 0.332 mA ; $I_{E1} = I_{E2}$ = 0.166 mA ; $I_{C1} = I_{C2}$ = 0.166 mA ; $I_{B1} = I_{B2}$ = 1.66 μA; V_{C1} = 9 V ; V_{C2} = 7.34 V]

5. Find the bias voltages and currents for the differential amplifier circuit shown in Fig. 25.99.

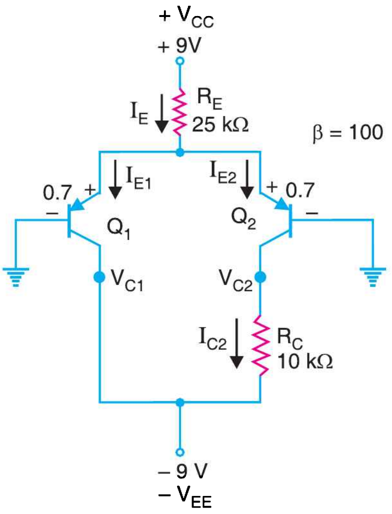

+ V_CC
+ 9V
I_E
R_E
25 kΩ
β = 100
I_E1
I_E2
0.7
+
–
+
0.7
–
Q_1
Q_2
V_C1
V_C2
I_C2
R_C
10 kΩ
– 9 V
– V_EE

Fig. 25.99

[V_E = 0.7 V ; I_E = 0.332 mA ; $I_{E1} = I_{E2}$ = 0.166 mA ; $I_{C1} = I_{C2}$ = 0.166 mA ; $I_{B1} = I_{B2}$ = 1.66 μA; V_{C1} = – 9 V ; V_{C2} = – 7.34 V]

6. For the circuit shown in Fig. 25.100, determine (*i*) common-mode voltage gain (*ii*) differential-mode voltage gain (*iii*) *CMRR*. **[(*i*) 0.42 (*ii*) 90.6 (*iii*) 216]**

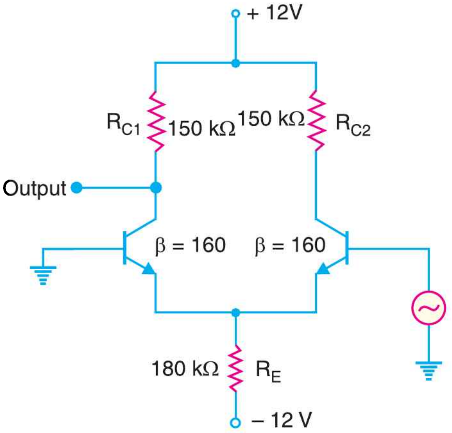

+ 12V
R_{C1}
150 kΩ
150 kΩ
R_{C2}
Output
β = 160
β = 160
180 kΩ
R_E
– 12 V

Fig. 25.100

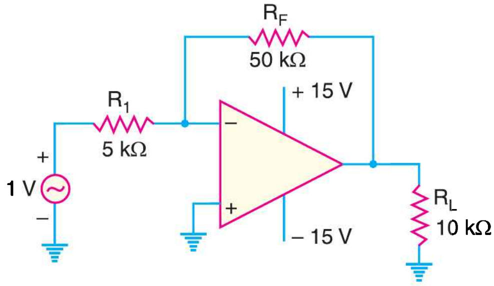

R_F
50 kΩ
+ 15 V
R_1
5 kΩ
+
1 V
–
–
+
– 15 V
R_L
10 kΩ

Fig. 25.101

7. For the circuit shown in Fig. 25.101, find (*i*) closed-loop voltage gain (*ii*) the instantaneous voltage across R_F when the signal voltage is + 1*V* (*iii*) the instantaneous voltage on the –terminal when the signal voltage is + 1*V*. **[(*i*) 10 (*ii*) 10 *V* (*iii*) 0 *V*]**

8. A noninverting amplifier has an R_i of 1 kΩ and an R_f of 100 kΩ. Determine (*i*) V_f (*ii*) feedback factor if V_{out} = 5 V. **[(*i*) 49.5 mV ; (*ii*) 9.9 × 10^{-3}]**

9. Determine the closed-loop voltage gain for the circuit shown in Fig. 25.102. **[11]**

10. Determine the closed-loop voltage gain for the circuit shown in Fig. 25.103. **[101]**

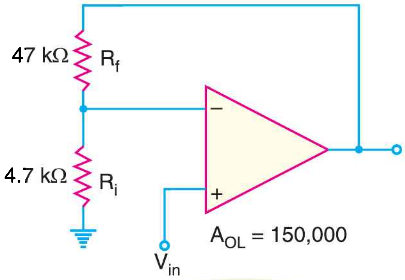

47 kΩ
R_f
–
4.7 kΩ
R_i
+
A_{OL} = 150,000
V_{in}

Fig. 25.102

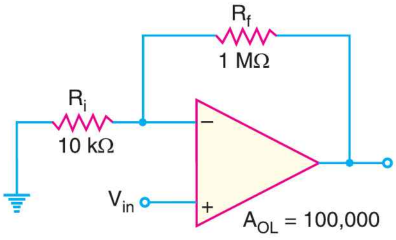

R_f
1 MΩ
R_i
10 kΩ
–
V_{in}
+
A_{OL} = 100,000

Fig. 25.103

11. Find the closed-loop voltage gain for each of the circuits shown in Fig. 25.104. **[1 ; – 1]**

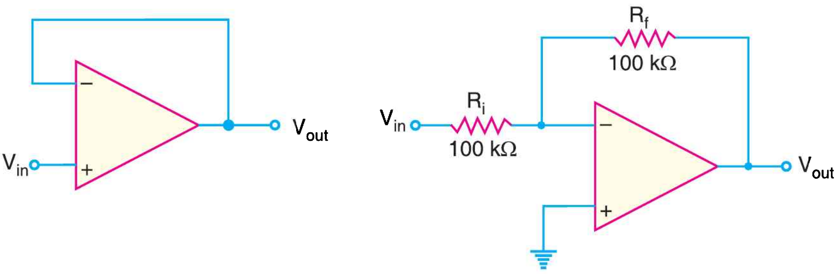
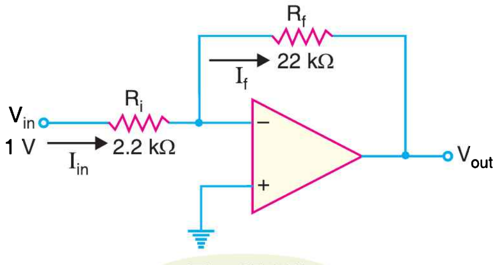

–
V_{out}
V_{in}
+
R_f
100 kΩ
R_i
V_{in}
100 kΩ
–
V_{out}
+

Fig. 25.104

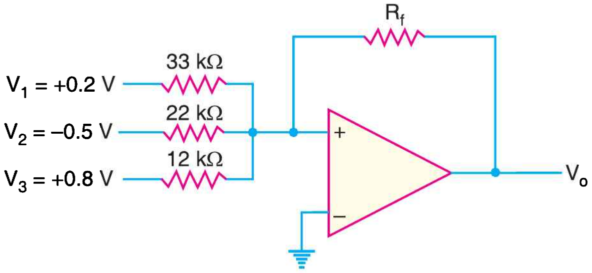
12. Determine the approximate values of (*i*) I_{in} (*ii*) I_f (*iii*) V_{out} (*iv*) closed-loop voltage gain for the circuit in Fig. 25.105. **[(*i*) 455 μ*A* (*ii*) 455 μ*A* (*iii*) – 10*V* (*iv*) – 10]**



R_f
22 kΩ
I_f
R_i
V_in
1 V
2.2 kΩ
I_in
–
+
V_out

Fig. 25.105

13. Calculate the output voltage of the circuit in Fig. 25.106 for $R_f = 68$ kΩ. **[$V_o = -3.39$ V]**



R_f
33 kΩ
V₁ = +0.2 V
22 kΩ
V₂ = –0.5 V
12 kΩ
V₃ = +0.8 V
+
–
V_o

Fig. 25.106

14. What output voltage results in the circuit of Fig. 25.107 for $V_1 = +0.5$ V? **[$V_o = 0.5$ V]**

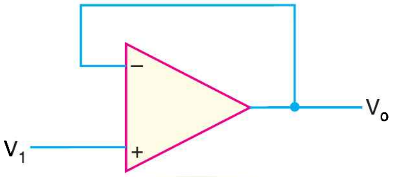
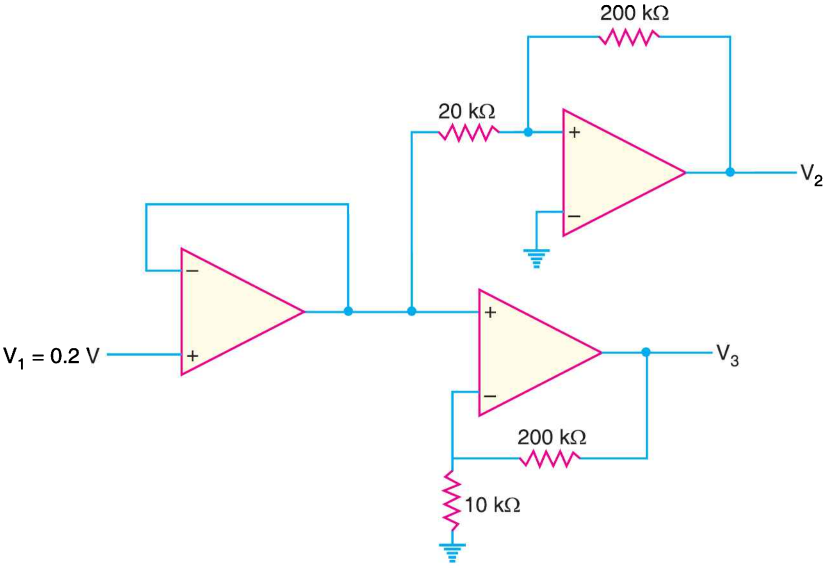


Fig. 25.107

15. Calculate the output voltages V_2 and V_3 in the circuit of Fig. 25.108. **[$V_2 = -2$ V ; $V_3 = 4.2$ V]**



200 kΩ
20 kΩ
+
–
V₂
–
+
V₁ = 0.2 V
+
–
V₃
200 kΩ
10 kΩ

Fig. 25.108

Discussion Questions

1. What is the difference between a discrete circuit and an integrated circuit (IC)?
2. Why are OP-amps produced as IC?
3. What is the difference between differential amplifier and the conventional amplifier?
4. What do + and – signs on the symbol of an OP-amp indicate?
5. Why is OP-amp generally operated with negative feedback?
6. Why is common-mode gain of a DA very low?
7. What is the importance of CMRR?
8. When is OP-amp driven to saturation?
9. In which circuit we take the advantage of high open-loop voltage gain of an OP-amp?
10. What is a noninverting amplifier?
11. Why is the input impedance of an OP-amp very high?
12. Why is the open-loop voltage gain of an OP-amp high?
13. What do you mean by virtual ground?
14. Why is the output impedance of an OP-amp very low?
15. What are the advantages of negative feedback in OP-amps?

26

Digital Electronics

26.1 Analog and Digital Signals
26.3 Binary Number System
26.5 Decimal to Binary Conversion
26.7 Octal Number System
26.9 Binary-Coded Decimal Code (BCD Code)
26.11 Three Basic Logic Gates
26.13 AND Gate
26.15 Combination of Basic Logic Gates
26.17 Exclusive OR Gate
26.19 Advantages and Disadvantages of Digital Electronics
26.21 Boolean Theorems
26.23 Operator Precedence
26.25 Boolean Expressions for Combinational Logic Circuits
26.27 Truth Table from Logic Circuit
26.29 Sum-of-Products Form
26.31 Binary Addition
26.33 Flip - Flops

INTRODUCTION

A continuously varying signal (voltage or current) is called an *analog signal*. For example, a sinusoidal voltage is an analog signal. In the previous chapter, we studied the behaviour of diodes and transistors primarily from the analog or continuous-signal point of view. In an analog electronic circuit, the output voltage changes continuously according to the input voltage variations. In other words, the output voltage can have an infinite number of values. A signal (voltage or current) which can have only two discrete values is called a *digital signal*. For example, a square wave is a digital signal. The semiconductors devices (*e.g.* diodes, transistors etc.) can be designed for two-state operation *viz.*, saturation and cut off. In that case, the output voltage can have only two states (*i.e.*, values), either *low or high. An electronic circuit that is designed for two-state operation is called a **digital circuit**.

---

* The exact value of voltage is unimportant if the voltage is distinguishable as low or high.

The branch of electronics which deals with digital circuits is called **digital electronics**. When most of us hear the term *digital*, we immediately think of "digital calculator" or "digital computer". This is attributed to the dramatic way the low-cost, powerful calculators and computers have become accessible to an average person. Now digital circuits are being used in many electronic products such as video games, microwave ovens and oscilloscopes. Digital techniques have also replaced a lot of the older "analog circuits" used in consumer products such as radios, TV sets and high-fidelity sound recording and playback equipment. In this chapter, we shall discuss the fundamental aspects of digital electronics.

26.1 Analog and Digital Signals

(*i*) **Analog signal.** A continuously varying signal (voltage or current) is called an *analog signal*. For example, an alternating voltage varying sinusoidally is an analog signal [See Fig. 26.1]. If such an analog signal is applied to the input of a transistor amplifier, the output voltage will also vary sinusoidally. This is the analog operation *i.e.*, the output voltage can have an infinite number of values. Due to many-valued output, the analog operation is less reliable.

(*ii*) **Digital signal.** A signal (voltage or current) that can have only two discrete values is called a *digital signal*. For example, a square wave is a digital signal [See Fig. 26.2]. It is because this signal has only two values viz, +5 V and 0 V and no other value. These values are labelled as *High* and *Low*. The High voltage is + 5 V and the Low voltage is 0 V. If proper digital signal is applied to the input of a transistor, the transistor can be driven between *cut off* and *saturation*. In other words, the transistor will have two-state operations *i.e.*, output is either low or high. Since digital operation has only two states (*i.e.*, *ON* or *OFF*), it is far more reliable than many-valued analog operation. It is because with two-states operation, all the signals are easily recognised as either low or high.

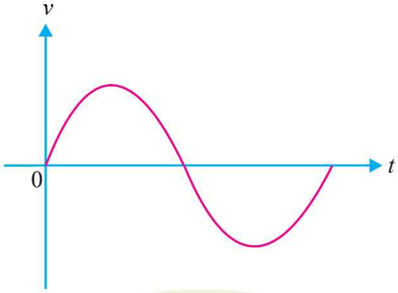


Fig. 26.1

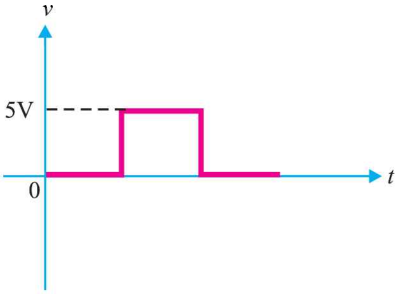


Fig. 26.2

26.2 Digital Circuit

An electronic circuit that handles only a digital signal is called a **digital circuit.**

The output voltage of a digital circuit is either low or high and no other value. In other words, digital operation is a two-state operation. These states are expressed as (*High* or *Low*) or (*ON* or *OFF*) or (1 or 0). Therefore, a digital circuit is one that expresses the values in digits 1's or 0's. Hence the name digital. The numbering concept that uses only the two digits 1 and 0 is the *binary numbering system.* Therefore, the first step would be to discuss this number system.

26.3 Binary Number System

A number system is a code that uses symbols to count the number of items. The most common and familiar number system is the decimal number system. The decimal number system uses the symbols 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9. Thus, the decimal system uses 10 digits for counting the items. A binary system uses only two digits (0 and 1) for counting the items. The reader may wonder how to count the items in a binary system. Let us see how it is done.

Counting in Decimal and Binary systems. Figure 26.3 shows the counting of stones in decimal as well as binary system. As you will see, the counting in the binary number system is performed much the same way as in the decimal number system.

Stones	**Decimal**	**Binary**
No stone	0	0
●	1	1
●●	2	10
●●●	3	11
●●●●	4	100
●●●●●	5	101
●●●●●●	6	110
●●●●●●●	7	111
●●●●●●●●	8	1000
●●●●●●●●●	9	1001

Fig. 26.3

(*i*) Let us first see how items are counted in decimal system. In this system, the count starts as 0, 1, ..., 9. After 9, we are to write the next number. To do so, we use the second digit of the decimal system (*i.e.*, 1) followed by the first digit (*i.e.*, 0). So after 9, the next number is 10. The count again continues as 10, 11, 12 ....., 19. After 19, we use the third digit of the system (*i.e.*, 2) followed by the first digit (*i.e.*, 0) and the count continues as 20, 21, ... etc. In this way, we get the number upto 99. In order to represent a number next to 99, we use three decimal digits (100). That is to say second digit of the decimal system (*i.e.*, 1) followed by two first digits (*i.e*, two zeros).

(*ii*) Let us now turn to binary system. Note that 0 and 1 count in the binary system is the same as in the decimal counting. To represent 2 stones, we use the second binary digit (*i.e.*, 1) followed by the first (*i.e.*, 0). This gives binary number 10 (read as one-zero and not ten) as an equivalent of 2 in the decimal system. Likewise, 3 in the decimal system can be represented by the binary number 11 (read as one-one and not eleven). After this, the two binary digits are exhausted. We shall use three digits to represent the next binary number. Thus, to represent 4 (four), we use the second binary digit followed by two first binary digits. This gives the binary *100 (read as one-zero-zero) as equivalent to 4 in the decimal system. Here is a simple way to find binary equivalents. *Each time the two digits 1 and 0 in one position are exhausted (counted as high as they will go), a 1 is added at the left, all digits to the right are made 0, and the count continues.* The reader may apply this simple rule to find next binary numbers.

Notes :

(*i*) Each binary digit (0 or 1) is referred to as a *bit.* A string of four bits is called as a *nibble* and eight bits make a *byte.* Thus, 1001 is a nibble and 10010110 is a binary byte.

(*ii*) The binary number system is the most useful in digital circuits because there are only two digits (0 and 1).

26.4 Place Value

Consider the decimal number 642. This can be expressed as :

$$642 = 600 + 40 + 2$$

Note that in a multidigit decimal number (*i.e.*, 642 in the present case), each position has a value that is 10 times the value of the next position to its immediate right. In other words, every position can be expressed as :

---

* Note that the procedure is similar to that which was used to write 100 (hundred) in the decimal system.

$$642 = 6 \times 10^2 + 4 \times 10^1 + 2 \times 10^0$$

Thus, we find that values of various positions in a decimal number system are powers of 10 *i.e.*, equal to the number of digits used in the system. This number is called *base* or *radix* of the system. Thus, the decimal system has base of 10 (ten).

For the decimals, the digit to the extreme right is referred to as the *least significant digit* (*LSD*) because its positional value or weight is the lowest. For the decimal number 642, 2 is the *LSD*. The left-most digit in the decimal number is the *most significant digit* (*MSD*) because its positional value or weight is the highest. For the decimal number 642, 6 is the *MSD* with a value of 600.

Binary number system. In the binary number system, only two digits (0 and 1) are used. Therefore, the *base* of this system is 2. In a binary number, each position has a value that is 2 times the value of the next position to its immediate right. In other words, every position can be expressed by 2 raised to some power. We know that binary number 1001 is equal to the decimal number 9. This can be readily shown as under :

$$1001 = 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 9$$

For binary numbers, the digit at the extreme right is referred to as *least significant bit* (*LSB*). In the binary number 1001, the 1 at the right is the *LSB*. The left-most digit is called the *most significant bit* (*MSB*). In the binary number 1001, the 1 at the left is the *MSB* with the value of 8 in decimal terms.

26.5 Decimal to Binary Conversion

There are many methods to perform this conversion. The method described here is called *double-dabble* because it requires successive divisions by 2. This method can be summarised as under :

Divide progressively the decimal number by 2 and write down the remainder after each division. Continue this process till you get a quotient of 0 and remainder of 1, the conversion is now complete. The remainders, taken in reverse order, form the binary number [See Fig. 26.4].

Note that 13 is first divided by 2, giving a quotient of 6 with a remainder of 1. This remainder becomes the 2^0 position in the binary number. The 6 is then divided by 2, giving a quotient of 3 with a remainder of 0. This remainder becomes the 2^1 position in the binary number.

Continuing this procedure, the equivalent binary number is 1101.

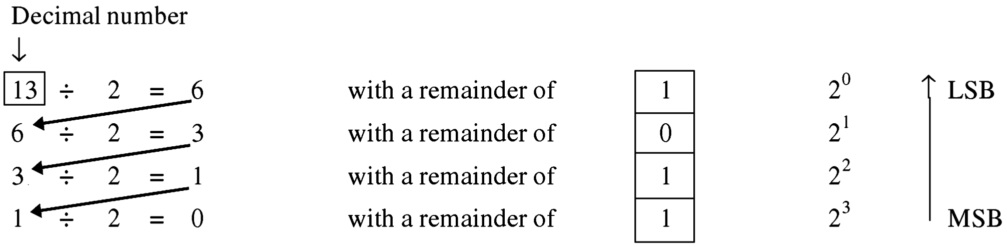

Decimal number
13 ÷ 2 = 6 with a remainder of 1 2^0
6 ÷ 2 = 3 with a remainder of 0 2^1
3 ÷ 2 = 1 with a remainder of 1 2^2
1 ÷ 2 = 0 with a remainder of 1 2^3
LSB
MSB

Fig. 26.4

Example 26.1. *Convert the decimal number 37 to its equivalent binary number.*

Solution. Using double-dabble method, we find that the equivalent binary number is 100101. It is a usual practice to mention the base of the number system. The decimal system has a base of 10 while binary system has a base of 2.

$$\therefore \qquad (37)_{10} = \mathbf{(100101)_2}$$

Note. This notation avoids the confusion that may arise because decimal number also involves the digits 0 and 1. Thus, $(101)_{10}$ denotes the decimal number hundred one while the binary number $(101)_2$ is equivalent to decimal number 5.

2	37
2	18 − 1
2	9 − 0
2	4 − 1
2	2 − 0
2	1 − 0
	0 − 1

Example 26.2. *Convert the decimal number 23 to its equivalent binary number.*

Solution. Using double-dabble method, we find that the equivalent binary number is 10111.

$$\therefore \quad (23)_{10} = \mathbf{(10111)_2}$$

Note that binary number 10111 has five bits.

2	23
2	11 − 1
2	5 − 1
2	2 − 1
2	1 − 0
	0 − 1

26.6 Binary to Decimal Conversion

Binary numbers can be converted to equivalent decimal numbers quite easily. Suppose you are given the binary number 110011. Its conversion to equivalent decimal number involves the following two steps :

(*i*) Place the decimal value of each position of the binary number.

(*ii*) Add all the decimal values to get the decimal number.

1	1	0	0	1	1
2^5	2^4	2^3	2^2	2^1	2^0

Thus,

$$\begin{aligned}(110011)_2 &= 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 \\ &= 32 + 16 + 0 + 0 + 2 + 1 = 51\end{aligned}$$

$$\therefore \quad (110011)_2 = (51)_{10}$$

Note. In binary to decimal conversion, all positions containing 0 can be ignored. Only add the decimal values of the positions where 1 appears. Thus, in case of the above binary number,

$$\begin{aligned}(110011)_2 &= 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^1 + 1 \times 2^0 \\ &= 32 + 16 + 2 + 1 = 51\end{aligned}$$

Example 26.3. *Convert the binary number 110001 to its equivalent decimal number.*

Solution. The binary number along with its decimal values of various positions is shown.

1	1	0	0	0	1
2^5	2^4	2^3	2^2	2^1	2^0

$$\begin{aligned}\therefore \quad (110001)_2 &= 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^0 \\ &= 32 + 16 + 1 = 49\end{aligned}$$

or

$$(110001)_2 = \mathbf{(49)_{10}}$$

26.7 Octal Number System

The octal number system has a radix of *eight* so that it uses eight digits : 0, 1, 2, 3, 4, 5, 6 and 7. The position weights in the system are powers of eight. The digit positions of first six powers of eight are:

$$8^0 = 1 \;;\; 8^1 = 8 \;;\; 8^2 = 64$$

$$8^3 = 512 \;;\; 8^4 = 4096 \;;\; 8^5 = 32768$$

The octal number system is frequently used in digital circuits due to two principal reasons. First, it can be easily converted to binary. Secondly, there are significantly fewer digits in any given octal number than in the corresponding binary number so that it is much easier to work with shorter octal numbers.

1. Decimal-to-Octal Conversion. To convert a decimal number to octal, we employ the same repeated-division method that we used in decimal-to-binary conversion. However, here the division factor is 8 instead of two. The following examples illustrate decimal-to-octal conversion.

(*i*) To convert decimal number 91 to octal number, the procedure is as under :

Division	*Remainder*	
$91 \div 8 = 11$	3	(LSB)
$11 \div 8 = 1$	3	
$1 \div 8 = 0$	1	(MSB)

$$\therefore \quad (91)_{10} = (133)_8$$

(*ii*) As another example, consider the conversion of decimal number 266 to octal number.

Division	*Remainder*	
$266 \div 8 = 33$	2	(LSB)
$33 \div 8 = 4$	1	

$4 \div 8 = 0 \qquad 4 \quad \text{(MSB)}$

$$\therefore \qquad (266)_{10} = (412)_8$$

2. Octal-to-Decimal Conversion. An octal-to-decimal conversion can be done in the same manner as a binary-to-decimal conversion *i.e.* simply add up the position weights to obtain the decimal number. The following examples illustrate octal-to-decimal conversion.

(*i*) To convert octal number $(133)_8$ to decimal number, the procedure is as under :

Position weights	8^2	8^1	8^0
Octal number	1	3	3

$$\therefore \qquad (133)_8 = (8^2 \times 1) + (8^1 \times 3) + (8^0 \times 3)$$

$$= 64 + 24 + 3 = 91$$

$$\therefore \qquad (133)_8 = (91)_{10}$$

(*ii*) As another example, consider the conversion of octal number $(372)_8$ to decimal number.

Position weights	8^2	8^1	8^0
Octal number	3	7	2

$$\therefore \qquad (372)_8 = (8^2 \times 3) + (8^1 \times 7) + (8^0 \times 2)$$

$$= 192 + 56 + 2 = 250$$

$$\therefore \qquad (372)_8 = (250)_{10}$$

3. Octal-to-Binary Conversion. The advantage of octal number system is the ease with which an octal number can be converted to a binary number and vice-versa. It is because eight is the third power of two, providing a direct correlation between three-bit groups in a binary number and the octal digits *i.e.* each three-bit group of binary bits can be represented by one octal digit. Therefore, conversion from octal to binary is performed by converting *each* octal digit to its 3-bit binary equivalent. The eight possible digits are converted as shown in the adjoining table.

Octal and Binary Equivalents

Octal Digit	Binary Bits
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

(*i*) The conversion of octal number $(472)_8$ to binary number is done as under :

$$\begin{array}{ccc} 4 & 7 & 2 \\ \downarrow & \downarrow & \downarrow \\ 100 & 111 & 010 \end{array}$$

Therefore, octal 472 is equivalent to binary 100111010 *i.e.*

$$(472)_8 = (100111010)_2$$

(*ii*) As another example, consider the conversion of octal number $(5431)_8$ to binary number.

$$\begin{array}{cccc} 5 & 4 & 3 & 1 \\ 101 & 100 & 011 & 001 \end{array}$$

Therefore, octal 5431 is equivalent to binary 101100011001 *i.e.*

$$(5431)_8 = (101100011001)_2$$

4. Binary-to-Octal Conversion. The conversion of binary number to octal number is simply the reverse of the above process. The bits of the binary number are grouped into groups of *three* bits starting at the LSB. Then each group is converted to its octal equivalent. To illustrate this method, consider the conversion of binary number $(100111010)_2$ to octal number. The procedure is as under:

$$\begin{array}{ccc} \underbrace{100} & \underbrace{111} & \underbrace{010} \\ \downarrow & \downarrow & \downarrow \\ 4 & 7 & 2 \end{array}$$

$\therefore \quad (100111010)_2 = (472)_8$

Note that there are fewer digits in the octal number than in the corresponding binary number. Therefore, it is much easier to work with shorter octal numbers.

Sometimes the binary number will not have even groups of 3 bits. In that case, we can add one or two 0s to the left of the MSB of the binary number to fill the last group. This point is illustrated below for the binary number 11010110.

$$\begin{array}{ccc} \underbrace{011} & \underbrace{010} & \underbrace{110} \\ 3 & 2 & 6 \end{array}$$

Note that a 0 is placed to the left of the MSB to produce even groups of 3 bits.

Example 26.4. *Convert the following decimal numbers to octal equivalent.*

(*i*) *76* (*ii*) *255* (*iii*) *372*

Solution.

(*i*)

Division	*Remainder*	
$76 \div 8 = 9$	4	(LSB)
$9 \div 8 = 1$	1	
$1 \div 8 = 0$	1	(MSB)

$\therefore \quad (76)_{10} = \mathbf{(114)_8}$

(*ii*)

Division	*Remainder*	
$255 \div 8 = 31$	7	(LSB)
$31 \div 8 = 3$	7	
$3 \div 8 = 0$	3	(MSB)

$\therefore \quad (255)_{10} = \mathbf{(377)_8}$

(*iii*)

Division	*Remainder*	
$372 \div 8 = 46$	4	(LSB)
$46 \div 8 = 5$	6	
$5 \div 8 = 0$	5	(MSB)

$\therefore \quad (372)_{10} = \mathbf{(564)_8}$

Example 26.5. *Convert octal number $(24.6)_8$ to the equivalent decimal number.*

Solution.

$$\begin{aligned} (24.6)_8 &= (2 \times 8^1) + (4 \times 8^0) + (6 \times 8^{-1}) \\ &= 16 + 4 + 0.75 = 20.75 \end{aligned}$$

$\therefore \quad (24.6)_8 = \mathbf{(20.75)_{10}}$

Example 26.6. *Convert $(177)_{10}$ to its 8-bit binary equivalent by first converting to octal.*

Solution. We shall first convert $(177)_{10}$ to its equivalent octal number as under :

Division	*Remainder*	
$177 \div 8 = 22$	1	(LSB)
$22 \div 8 = 2$	6	
$2 \div 8 = 0$	2	(MSB)

$\therefore \quad (177)_{10} = (261)_8$

We now convert the octal number $(261)_8$ to its equivalent binary number as under :

$$\begin{array}{ccc} 2 & 6 & 1 \\ \downarrow & \downarrow & \downarrow \\ 010 & 110 & 001 \end{array}$$

Therefore, the binary equivalent is 010110001. We remove the leading zero to express the result as 8 bits

$$\therefore \qquad (177)_{10} = \mathbf{(10110001)_2}$$

26.8 Hexadecimal Number System

The hexadecimal system uses a radix of 16. Therefore, it has 16 possible digit symbols. The first ten digits in the hexadecimal system are represented by the numbers 0 through 9 (0, 1, 2, 3, 4, 5, 6, 7, 8 and 9) and the letters A though F are used to represent the numbers 10, 11, 12, 13, 14 and 15 respectively. The adjoining table shows the relationships among hexadecimal, decimal and binary. Note that each hexadecimal digit represents a group of four binary digits.

As is true for binary and decimal numbers, each digit in the hexadecimal system has a positional value or weight. For the right most digit of a hex (abbreviation for hexadecimal) number, the positional weight is 16^0 (= 1), the next digit to the left has a positional weight of 16^1 (= 16) and so on. The positional weight distribution of a hex number system is given below:

$$\begin{array}{ccccc} & 16^3 & 16^2 & 16^1 & 16^0 \\ \overset{\text{etc.}}{\leftarrow} & 4096 & 256 & 16 & 1 \end{array}$$

Hexadecimal	Decimal	Binary
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
A	10	1010
B	11	1011
C	12	1100
D	13	1101
E	14	1110
F	15	1111

1. Decimal-to-Hex Conversion. To convert a decimal number to hex number, the technique is the same as used for decimal-to-binary conversion or decimal-to-octal conversion. Recall that we did decimal-to-binary conversion using repeated division by 2 and decimal-to-octal conversion using repeated division by 8. Likewise, decimal-to-hex conversion is done using repeated division by 16. Let us illustrate the decimal-to-hex conversion procedure. Suppose we are to convert the decimal number 423 to hex number.

$$\begin{array}{rclcl} & \textit{Division} & & \textit{Remainder} & \\ 423 \div 16 & = & 26 & 7 & \text{(LSB)} \\ 26 \div 16 & = & 1 & 10 & \\ 1 \div 16 & = & 0 & 1 & \text{(MSB)} \end{array}$$

$$\therefore \qquad (423)_{10} = (1\,\mathrm{A}7)_{16}$$

Note that 10 is represented by the letter A.

2. Hex-to-Decimal Conversion. In order to convert a hex number to its decimal equivalent, simply add up the position weight of each digit in the hex number. The following example illustrates this conversion.

$$\begin{aligned} (356)_{16} &= (3 \times 16^2) + (5 \times 16^1) + (6 \times 16^0) \\ &= 768 + 80 + 6 = 854 \end{aligned}$$

$$\therefore \qquad (356)_{16} = (854)_{10}$$

3. Hex-to-Binary Conversion. The conversion from hex to binary is performed by converting each hex digit to its 4-bit binary equivalent (See above table). The following example illustrates this point. Here, we shall convert hex number $(9\,\mathrm{F}2)_{16}$ to its binary equivalent.

$$\begin{array}{ccc} 9 & F & 2 \\ \downarrow & \downarrow & \downarrow \\ 1001 & 1111 & 0010 \end{array}$$

$$\therefore \quad (9F2)_{16} = (100111110010)_2$$

4. Binary-to-Hex Conversion. The conversion from binary to hex is just the reverse of the above process. The binary number is grouped into groups of *four* bits and each group is converted to its equivalent hex digit. The following example illustrates this point. Here, we shall convert binary number $(1110100110)_2$ to its *equivalent hex number.

$$\underbrace{0011}_{3} \quad \underbrace{1010}_{A} \quad \underbrace{0110}_{6}$$

$$\therefore \quad (1110100110)_2 = (3A6)_{16}$$

Example 26.7. *Convert decimal number 541 to hexadecimal.*

Solution.

Division	*Remainder*	
$541 \div 16 = 33$	13	(LSB)
$33 \div 16 = 2$	1	
$2 \div 16 = 0$	2	(MSB)

$$\therefore \quad (541)_{10} = \mathbf{(21D)_{16}}$$

Example 26.8. *Convert decimal number 378 to a 16-bit number by first converting to hexadecimal.*

Solution.

Division	*Remainder*
$378 \div 16 = 23$	10 (LSB)
$23 \div 16 = 1$	7
$1 \div 16 = 0$	1 (MSB)

Thus $(378)_{10} = (17A)_{16}$. We can easily convert this hex number to binary 000101111010. Therefore, we can express $(378)_{10}$ as a 16-bit binary number by adding four leading 0s.

$$(378)_{10} = \mathbf{(0000000101111010)_2}$$

Example 26.9. *Convert $(B2F)_{16}$ to octal.*

Solution. It is easier to first convert hex to binary and then to octal.

$$\begin{array}{lllllll} (B2F)_{16} & = & 1011 & 0010 & 1111 & & \text{.... conversion to binary} \\ & = & 101 & 100 & 101 & 111 & \text{.... 3-bit groupings} \\ & = & 5 & 4 & 5 & 7 & \\ \therefore \quad (B2F)_{16} & = & \mathbf{(5457)_8} & & & & \end{array}$$

26.9. Binary-Coded Decimal Code (BCD Code)

Circuits and machines can deal readily with binary numbers, but people are used to working with decimal numbers. Moreover, there are considerably fewer decimal digits required to represent a number than there are binary. It is much easier to remember just a few digits than it is to remember many. Thus whenever there is an interface between digital circuits and people, the interface data usually takes the decimal from. As a result, the digital circuits must utilise some binary code to conveniently represent the decimal numbers. The code used for this purpose is called BCD code. *In a BCD code, each decimal number is represented by a 4-bit binary number.* For example, to convert decimal number $(489)_{10}$ to BCD, the procedure is as under :

---

* Zeros are added, as needed, to complete 4-bit group.

$$\begin{array}{ccc} 4 & 8 & 9 \\ 0100 & 1000 & 1001 \end{array}$$

Note that the highest BCD value that a 4-bit binary number could represent is 9 which would be $(1001)_2$ in binary. Clearly, only the 4-bit binary numbers from 0000 through 1001 are used.

The adjoining table shows the BCD code. Each of the decimal digits (0 through 9) is represented by its binary equivalent. Since a decimal digit can be as large as 9, four bits are required to code each decimal digit (the binary code for 9 is 1001).

Note that each decimal digit is assigned a 4-bit binary number even though the binary equivalent may require fewer than four binary places. This way, circuits which use BCD always handle the string of binary bits in four - place groups. When using BCD code, remember that all zeros must be retained, unlike a binary number where leading zeros can be dropped. The BCD code is used when it is necessary to transfer decimal information into and out of a digital machine. Examples of digital machines include the digital clocks, calculators, digital voltmeters and frequency counters.

BCD code	Decimal digit
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9

Example 26.10. *What decimal number is represented by the BCD string given below ?*

0100 0000 0010

Solution. Divide the BCD number into 4-bit groups and convert each to decimal.

$$\underbrace{0100}_{4} \quad \underbrace{0000}_{0} \quad \underbrace{0010}_{2}$$

Therefore, the equivalent decimal number is $\mathbf{(402)_{10}}$.

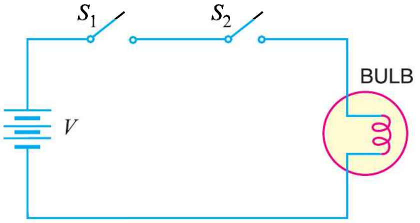
Note. To avoid confusion between BCD and true binary, a BCD string is often separated into groups of 4 binary bits or a subscript BCD is sometimes attached to the string as illustrated under :

0100 0000 0010 or 010000000010_{BCD}

26.10 Logic Gates

A digital circuit with one or more input signals but only one output signal is called a **logic gate**.

Since a logic gate is a switching circuit (*i.e.* a digital circuit), its output can have only one of the two possible states *viz*., either a high voltage (1) or a low voltage (0) — it is either *ON* or *OFF*. Whether the output voltage of a logic gate is high (1) or low (0) will depend upon the conditions at its input. Fig. 26.5 shows the basic idea of a *logic gate using switches.



(*i*)

S_1	S_2	Bulb
open	open	OFF
open	closed	OFF
closed	open	OFF
closed	closed	ON

(*ii*)

Truth Table

S_1	S_2	Output
0	0	0
0	1	0
1	0	0
1	1	1

(*iii*)

Fig. 26.5

---

* In itself, the circuit is not actually a logic gate but the logic is similar. The actual gate circuits are made with diodes and transistors. In other words, switches S_1 and S_2 are replaced by diodes or transistors.

(*i*) When S_1 and S_2 are open, the bulb is *OFF*.

(*ii*) When S_1 is open and S_2 closed, the bulb is *OFF*.

(*iii*) When S_2 is open and S_1 closed, the bulb is *OFF*.

(*iv*) When both S_1 and S_2 are closed, the bulb is *ON*.

Note that output (*OFF* or *ON*) depends upon the conditions at the input.

The four possible combinations of switches S_1 and S_2 are shown in the table on the previous page. It is clear that when either of the switches (S_1 or S_2) or both are open, the bulb is *OFF*. In binary language, when either of the inputs or both the inputs are low (0), the output is low. When both switches are closed, the bulb is *ON*. In terms of binary language, when both the inputs are high (1), the output is high. It is usual practice to show the conditions at the input and output of a logic gate in the binary form as shown in the table on the previous page. Such a table is called **truth table**.

The term "logic" is usually used to refer to a decision-making process. A logic gate makes logical decisions regarding the existence of output depending upon the nature of the input. Hence, such circuits are called logic circuits.

26.11 Three Basic Logic Gates

A logic gate is a circuit that has one or more input signals but only one output signal. All logic gates can be analysed by constructing a truth table. A truth table lists all input possibilities and the corresponding output for each input. The three basic logic gates that make up all digital circuits are **(*i*)** OR gate **(*ii*)** AND gate and **(*iii*)** NOT gate. We shall first discuss these three basic logic gates and then the combination of these gates. The following points may be noted about logic *gates :

(*i*) A binary 0 represents 0 V and binary 1 represents + 5V**. It is common to refer to binary 0 as LOW input or output and binary 1 as HIGH input or output.

(*ii*) A logic gate has only one output signal. The output will depend upon the input signal/signals and the type of gate.

(*iii*) The operation of a logic gate may be described either by **truth table** or **Boolean algebra.**

26.12 OR Gate

An OR gate is a logic gate that has two or more inputs but only one output. However, the output *Y* of an OR gate is LOW when *all* inputs are LOW. The output *Y* of an OR gate is HIGH if any or all the inputs are HIGH.

It is called OR gate because the output is high if any or all the inputs are high. For the same reason, an OR gate is sometimes called "any or all gate". For example, consider a 2-input OR gate. The output *Y* will be high if either or both inputs are high.

OR gate operation. Fig. 26.6 (*i*) shows one way to build a 2-input OR gate while Fig. †26.6 (*ii*) shows its simplified schematic diagram. The input voltages are labeled as *A* and *B* while the output voltage is *Y*. Note that negative terminal of the battery is grounded and corresponds to 0 state (LOW level). The positive terminal of the battery (+5 V) corresponds to 1 state (HIGH level). There are only four input-output possibilities.

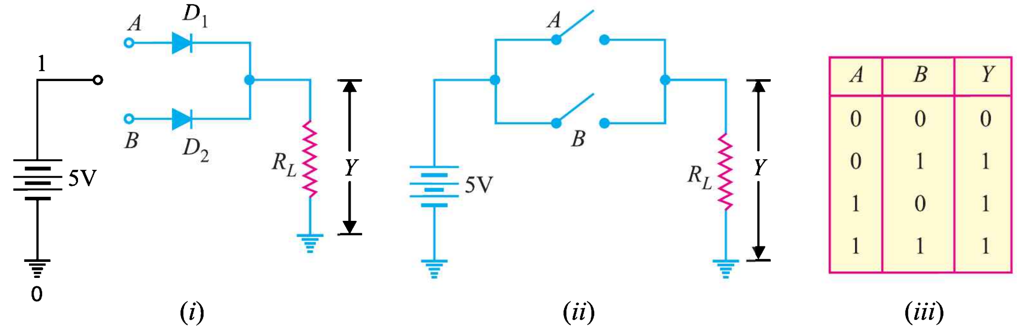
---

* A *gate* can be regarded as a *barrier* which when closed prevents the passgae of information but if open allows the signal/signals to pass through freely.

** In digital systems, the binary information is represented by two voltage levels, generally +5 V and 0 V. So 5 V is used to represent binary 1 and 0 V is used to represent binary 0.

† As you can see in Fig. 26.6 (*ii*) that output is high when *either* or *both* of the input switches are closed but not when both are open.

(*i*) When both A and B are connected to ground, both diodes are non-conducting. Hence, the output voltage is ideally zero (low voltage). In terms of binary, when $A = 0$ and $B = 0$, then $Y = 0$ as shown in the truth table in Fig. 26.6 (*iii*).



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(*i*) (*ii*) (*iii*)

Fig. 26.6

(*ii*) When A is connected to ground and B connected to the positive terminal of the battery, diode D_2 is forward biased and diode D_1 is non-conducting. Therefore, diode D_2 conducts and the output voltage is ideally +5 V. In terms of binary, when $A = 0$ and $B = 1$, then $Y = 1$ [See Fig. 26.6 (*iii*)].

(*iii*) When A is connected to the positive terminal of the battery and B to the ground, diode D_1 is on and diode D_2 is off. Again the output voltage is +5 V. In binary terms, when $A = 1$ and $B = 0$, then $Y = 1$ [See Fig. 26.6 (*iii*)].

(*iv*) When both A and B are connected to the positive terminal of the battery, both diodes are on. Since the diodes are in parallel, the output voltage is +5 V. In binary terms, when $A = 1$ and $B = 1$, then $Y = 1$ [See Fig. 26.6 (*iii*)].

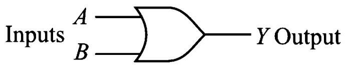


Fig. 26.7

It is clear from the truth table that *for OR gate, the output is high if any or all of the inputs are high. The only way to get a low output is by having all inputs low.* Fig. 26.7 shows the logic symbol of OR gate. Note that the symbol has curved line at the input.

Boolean expression. The algebra used to symbolically describe logic functions is called Boolean algebra. The "+" sign in Boolean algebra refers to the logical OR function. The Boolean expression for OR function is

$$A \underset{\substack{\uparrow \\ \text{OR symbol}}}{+} B = Y$$

$A + B$	=	Y
0 + 0	=	0
0 + 1	=	1
1 + 0	=	1
1 + 1	=	1

The adjoining table shows possibilities for the inputs. According to this table, when 0 is ORed with 0, the result equals 0. Also, any variable ORed with 1 equals 1. The OR function can be summed up as under :

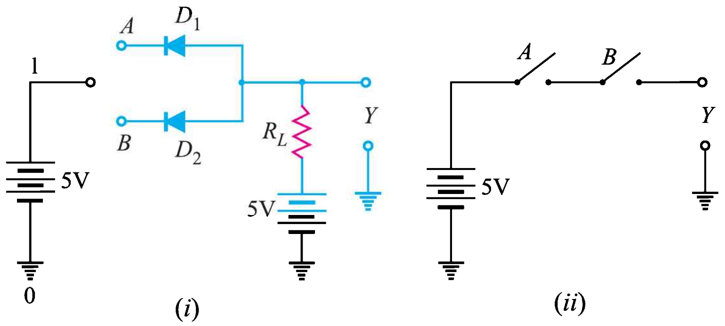
0 ORed with 0 equals 0
0 ORed with 1 equals 1
1 ORed with 1 equals 1

26.13 AND Gate

The AND gate is a logic gate that has two or more inputs but only one output. The output Y of AND gate is HIGH when all inputs are HIGH. However, the output Y of AND gate is LOW if any or all inputs are LOW.

It is called AND gate because output is HIGH only when all the inputs are HIGH. For this reason, the AND gate is sometimes called "all or nothing gate". For example, consider a 2-input AND gate. The output will be HIGH when both the inputs are HIGH.

AND gate operation. Fig. 26.8 (*i*) shows one way to build a 2-input AND gate while *Fig. 26.8 (*ii*) shows its simplified schematic diagram. There are only four input-output possibilities.



(*i*) (*ii*)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(*iii*)

Fig. 26.8

(*i*) When both A and B are connected to ground, both the diodes (D_1 and D_2) are forward biased and hence they conduct current. Consequently, the two diodes are grounded and output voltage is zero. In terms of binary, when $A = 0$ and $B = 0$, then $Y = 0$ as shown in truth table in Fig. 26.8 (*iii*).

(*ii*) When A is connected to the ground and B connected to the positive terminal of the battery, diode D_1 is forward biased while diode D_2 will not conduct. Therefore, diode D_1 conducts and is grounded. Again output voltage will be zero. In binary terms, when $A = 0$ and $B = 1$, then $Y = 0$. This fact is shown in the truth table.

(*iii*) When B is connected to the ground and A connected to the positive terminal of the battery, the roles of diodes are interchanged. Now diode D_2 will conduct while diode D_1 does not conduct. As a result, diode D_2 is grounded and again output voltage is zero. In binary terms, when $A = 1$ and $B = 0$, then $Y = 0$. This fact is indicated in the truth table.

(*iv*) When both A and B are connected to the positive terminal of the battery, both the diodes do not conduct. Now, the output voltage is +5 V because there is no current through R_L.

It is clear from the truth table that *for AND gate, the output is high if all the inputs are high. However, the output is low if any or all inputs are low.* Fig. 26.9 shows the logic symbol of AND gate. This is the symbol you should memorise and use from now on for AND gates.

Boolean expression. The Boolean expression for AND function is

$$\underset{\substack{\uparrow \\ \text{AND symbol}}}{A\,.\,B} = Y$$

where the multiplication **dot stands for the AND operation. The adjoining table shows the possibilities for the inputs. Table tells us that 0 ANDed with any variable equals 0. Also, 1 ANDed with 1 equals one. The AND function can be summed up as under :

$A\,.\,B$	=	Y
0 . 0	=	0
0 . 1	=	0
1 . 0	=	0
1 . 1	=	1

0 ANDed with 0 equals 0
0 ANDed with 1 equals 0
1 ANDed with 1 equals 1

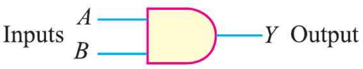


Fig. 26.9

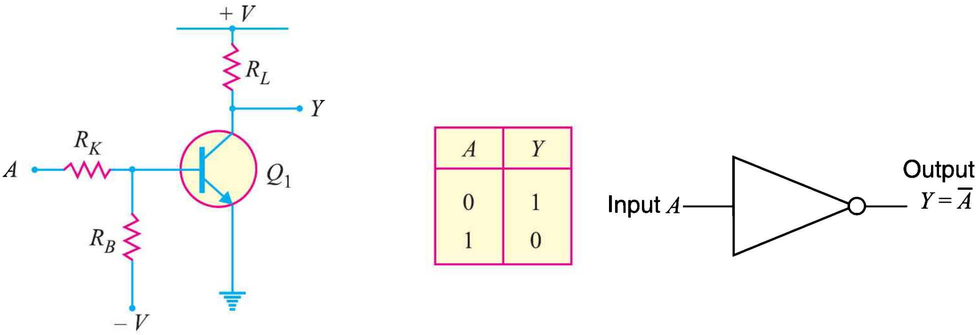
---

* Note that two switches used to represent the OR function were connected in parallel. If the switches are connected in series [See Fig. 26.8 (*ii*)], AND function is obtained. The output is high if both the switches are closed. The output will be low if either switch is open.

** Note that the multiplication dot is often omitted, so expression may appear as $AB = Y$.

26.14 NOT Gate or Inverter

The NOT gate or inverter is the simplest of all logic gates. It has only one input and one output, where the output is opposite of the input. The NOT gate is often called inverter because it inverts the input.



A	Y
0	1
1	0

(*i*) (*ii*) (*iii*)

Fig. 26.10

Figure 26.10 (*i*) shows a *typical inverter circuit. When A is connected to ground, the base of transistor Q_1 will become negative. This negative potential causes the transistor to cut off and collector current is zero and output is + V volts. In binary terms, when $A = 0$, $Y = 1$. If sufficiently large positive voltage is applied at A, the base of the transistor will become positive, causing the transistor to conduct heavily. Therefore, the output voltage is zero. In binary terms, when $A = 1$, $Y = 0$. Fig. 26.10 (*ii*) shows truth table for an inverter. It is clear from the truth table that whatever the input to the inverter, the output assumes opposite polarity. If the input is 0, the output will be 1 ; if the input is 1, the output will be 0.

Figure 26.10 (*iii*) shows the logic symbol for NOT gate or inverter. Note that small bubble on the inverter symbol represents inversion. The Boolean expression for NOT function is

$$Y = \overline{A}$$

Note that bar above the input A represents inversion.

If $A = 0$, then $Y = \overline{0}$ or $Y = 1$.

If $A = 1$, then $Y = \overline{1}$ or $Y = 0$.

26.15 Combination of Basic Logic Gates

The OR, AND and NOT gates are the three basic circuits that make up all digital circuits. We shall discuss a few combinations of these basic circuits.

(*i*) **NAND gate.** It is a combination of AND gate and NOT gate. In other words, output of AND gate is connected to the input of a NOT gate as shown in Fig. 26.11 (*i*). Clearly, the output of a NAND gate is opposite to the AND gate. This is illustrated in the truth table for the NAND gate. Note that truth table for NAND gate is developed by *inverting the outputs* of the AND gate.

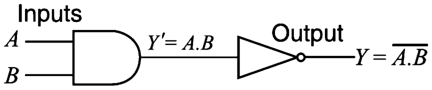
The Boolean expression for NAND function is

$$Y = \overline{A \cdot B}$$

This Boolean expression can be read as $Y =$ not $A \, . \, B$. To perform the Boolean algebra operation, first the inputs must be ANDed and then the inversion is performed. *Note that output from a NAND gate is always 1 except when all of the inputs are 1.* Fig. 26.11 (*iii*) shows the logic symbols for a NAND gate. The little bubble (small circle) on the right end of the symbol means to invert the AND.

---

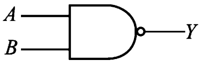
* Note that resistors R_K and R_B form a voltage divider between ground and the negative voltage.



(*i*)

Inputs		Output	
A	*B*	AND (*Y′*)	NAND (*Y*)
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

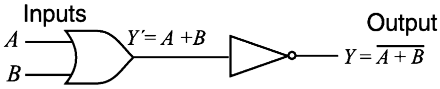
(*ii*)



(*iii*)

Fig. 26.11

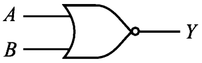
(*ii*) **NOR gate.** It is a combination of OR gate and NOT gate. In other words, output of OR gate is connected to the input of a NOT gate as shown in Fig. 26.12 (*i*). Note that output of OR gate is inverted to form NOR gate. This is illustrated in the truth table for NOR gate. It is clear that truth table for NOR gate is developed by *inverting the outputs* of the OR gate.



(*i*)

Inputs		Output	
A	*B*	OR (*Y′*)	NOR (*Y*)
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

(*ii*)



(*iii*)

Fig. 26.12

The Boolean expression for NOR function is

$$Y = \overline{A + B}$$

This Boolean expression can be read as Y = not A or B. To perform the Boolean algebra operation, first the inputs must be ORed and then the inversion is performed. *Note that output from a NOR gate is high (1) only when all the inputs are low (0). If any of the inputs is high (1), the output is low (0).* Fig. 26.12 (*iii*) shows the logic symbol for a NOR gate. The bubble (small circle) at the Y output indicates inversion.

26.16 NAND Gate as a *Universal Gate

The NAND gate is universal gate because its repeated use can produce other logic gates. The table below shows how NAND gates can be connected to produce inverter (*i.e.*, NOT gate), AND gate and OR gate.

---

* It may be noted that NOR gate is also a universal gate.

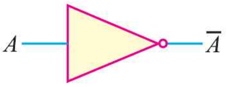
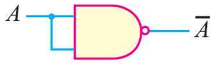
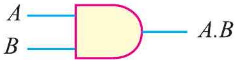
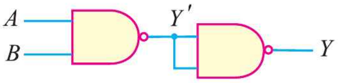
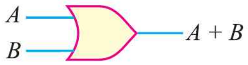
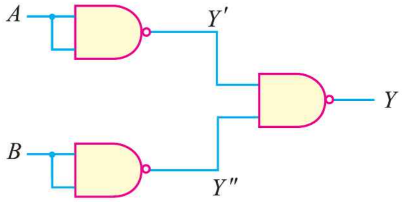
Logic Function	Symbol	Circuit using NAND gates only
Inverter		
AND		
OR		

Fig. 26.13

(*i*) **NOT gate from NAND gate.** When two inputs of NAND gate are joined together so that it has one input, the resulting circuit is NOT gate. The truth table also shows this fact.

A	$B\ (= A)$	Y
0	0	1
1	1	0

(*ii*) **AND gate from NAND gates.** For this purpose, we use two NAND gates in a manner as shown above. The output of first NAND gate is given to the second NAND gate acting as inverter (*i.e.*, inputs of NAND gate joined). The resulting circuit is the AND gate. The output Y' of first NAND gate (AND gate followed by NOT gate) is inverted output of AND gate. The second NAND gate acting as inverter further inverts it so that the final output Y is that of AND gate. The truth table also shows this fact.

A	B	Y'	Y
0	0	1	0
1	0	1	0
0	1	1	0
1	1	0	1

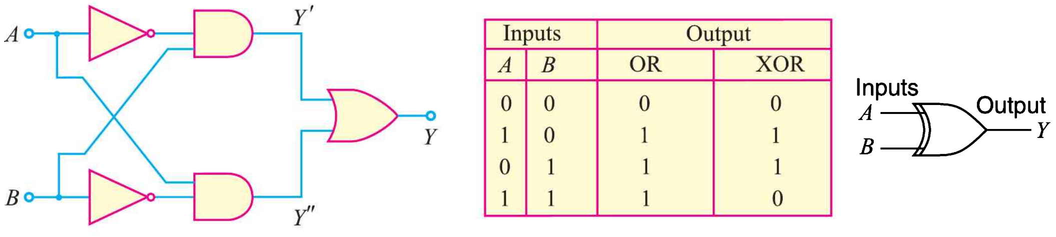
(*iii*) **OR gate from NAND gates.** For this purpose, we use three NAND gates in a manner as shown above. The first two NAND gates are operated as NOT gates and their outputs are fed to the third. The resulting circuit is OR gate. This fact is also indicated by the truth table.

A	B	$Y' = \overline{A}$	$Y'' = \overline{B}$	Y
0	0	1	1	0
1	0	0	1	1
0	1	1	0	1
1	1	0	0	1

26.17 Exclusive OR Gate

The name exclusive OR gate is usually shortened to XOR gate. The XOR gate can be obtained by using OR, AND and NOT gates as shown in Fig. 26.14 (*i*).

Fig. 26.14 (*ii*) shows the truth table for XOR gate. The table shows that the output is HIGH (1) if any but not all of the inputs are HIGH (1). This *exclusive* feature eliminates the similarity to the OR gate. The OR gate truth table is also given so that you can compare the OR gate truth table with XOR gate truth table. The logic symbol for XOR gate is shown in Fig. 26.14 (*iii*). Note that the symbol is similar to that of OR gate except for the additional curved line at the input side.



Inputs		Output	
A	B	OR	XOR
0	0	0	0
1	0	1	1
0	1	1	1
1	1	1	0

(*i*) (*ii*) (*iii*)

Fig. 26.14

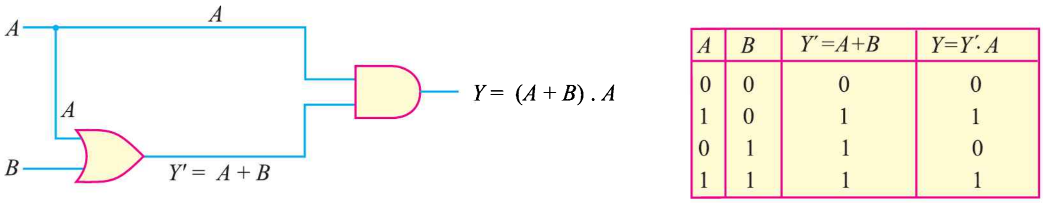
The logic operations in the circuit are as under :

A	B	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot B = Y'$	$A \cdot \overline{B} = Y''$	$Y = Y' + Y''$
0	0	1	1	0	0	0
1	0	0	1	0	1	1
0	1	1	0	1	0	1
1	1	0	0	0	0	0

Note that 0 ANDed with 1 is 0 and 1 ANDed with 1 is 1.

Example 26.11. *Obtain the truth table for the circuit shown in Fig. 26.15 (i).*

Solution. Figure 26.15 (*ii*) shows the truth table for the circuit. The truth table can be obtained very easily if the reader remembers the following simple Boolean operations :



A	B	$Y' = A + B$	$Y = Y' \cdot A$
0	0	0	0
1	0	1	1
0	1	1	0
1	1	1	1

(*i*) (*ii*)

Fig. 26.15

(*i*) *0 *ORed with 0 = 0 ; 1 ORed with 1 = 1 ; 1 ORed with 0 = 1*

(*ii*) *0 **ANDed with 0 = 0 ; 0 ANDed with 1 = 0 ; 1 ANDed with 1 = 1*

Thus, when $A = 0$ and $B = 0$, then A ORed with $B = 0$ *i.e.*, $Y' = 0$. When Y' (= 0) is ANDed with A (= 0), the result is 0. Again when $A = 1$ and $B = 0$, then A ORed with B is 1 *i.e.*, $Y' = 1$. Now Y' (= 1) ANDed with A (= 1), the result is 1.

Example 26.12. *Obtain the truth table for the circuit shown in Fig. 26.16.*

---

* Note that $A + B$ means A ORed with B.

** Note that $A \,.\, B$ means A ANDed with B.

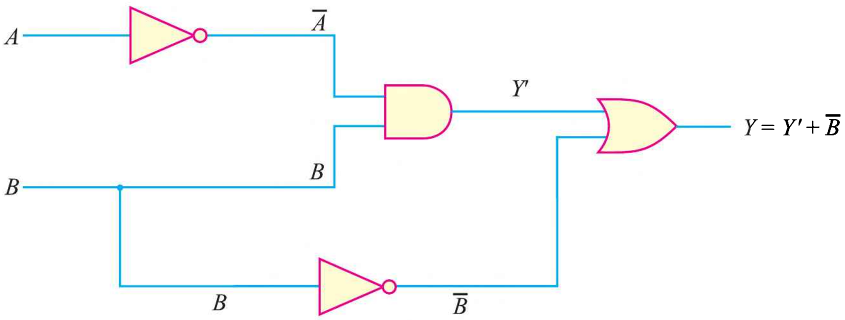


Fig. 26.16

Solution. The truth table for the circuit is shown below :

A	B	$\overline{A}$	$Y' = \overline{A} \cdot B$	$\overline{B}$	$Y = Y' + \overline{B}$
0	0	1	0	1	1
1	0	0	0	1	1
0	1	1	1	0	1
1	1	0	0	0	0

(*i*) When $A = 0$ and $B = 0$, then $\overline{A} = 1$. Now Y' is equal to $\overline{A}$ (= 1) ANDed with B (= 0). The result is 0. Then Y' (= 0) ORed with $\overline{B}$ (= 1) is 1 *i.e.*, $Y = 1$.

(*ii*) When $A = 1$ and $B = 0$, then $\overline{A} = 0$. Now Y' is equal to $\overline{A}$ (= 0) ANDed with B (= 0) and the result is 0 *i.e.*, $Y' = 0$. Then Y' (= 0) ORed with $\overline{B}$ (= 1) is 1 *i.e.*, $Y = 1$.

The reader can proceed in a similar way to find the other output values.

26.18 Encoders and Decoders

A digital circuit can process numbers in binary form. However, most of the information we handle is in decimal form. Therefore, a digital machine must perform the following functions :

(*i*) Convert the information from decimal to digital (binary) form.

(*ii*) Process the digital information.

(*iii*) Convert the digital output back to decimal form.

The circuit that converts decimal form to digital (binary) form is called **encoder** and the circuit that converts digital form to decimal form is called **decoder.** Fig. 26.17 shows encoding and decoding in a digital calculator. Here the input is the decimal number 5 punched in at the keyboard. The encoder changes the decimal number 5 to the digital form as the binary digit 0101. The central processing unit (CPU) contains digital logic circuits for necessary calculations. Here all operations are carried out in binary form. The output of

Encoders and Decoders

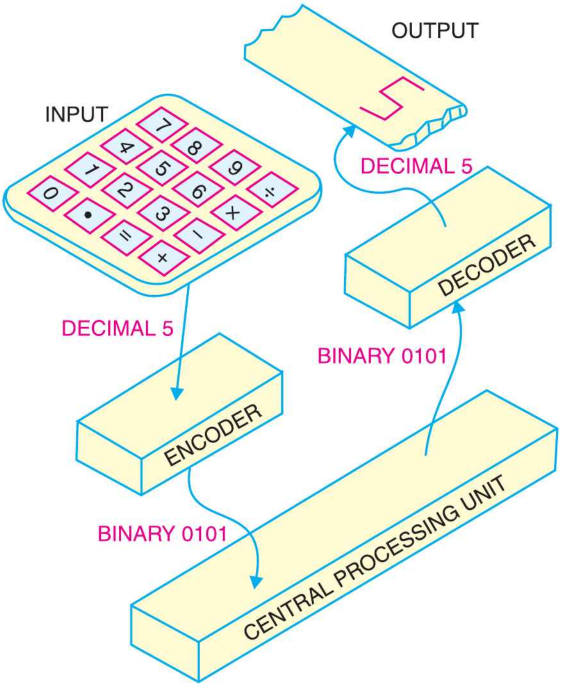


Fig. 26.17

CPU is fed to the decoder which changes the binary signal back to the decimal form. The output display is in the decimal form, showing the original number 5.

26.19 Advantages and Disadvantages of Digital Electronics

The world of electronics can be classified as either digital or analog circuits. An increasing majority of applications in electronics use digital techniques to perform operations that were once performed using analog methods. It is worthwhile to give advantages and disadvantages of digital electronics.

Advantages. The chief reasons for the shift to digital technology are :

(*i*) *Digital systems are generally easier to design.* It is because the circuits that are used are *switching circuits* where *exact* values of voltages or currents are not important, only the range (HIGH or LOW) in which they fall is important.

(*ii*) *Digital circuits provide greater accuracy and precision.* It is because digital circuits can handle as many digits of precision as you need simply by adding more switching circuits. In analog systems, precision is usually limited to three or four digits because the values of voltage and current are directly dependent on the circuit components.

(*iii*) *Digital circuits are less affected by noise.* Suprious fluctuations in voltage (noise) are not as critical in digital systems as in analog systems. It is because in a digital circuit, the exact value of a voltage is not important as long as the noise is not large enough to prevent us from distinguishing a HIGH from a LOW.

(*iv*) *More digital circuitry can be fabricated on IC chips.* Analog system uses such devices (high-value capacitors, inductors, transformers) that cannot be economically integrated. For this reason, analog systems cannot achieve the same degree of integration as digital circuits.

(*v*) Information storage is easy with digital circuits.

Disadvantages. (*i*) The real world is mainly analog. However, the digital circuits can handle only digital signals. This necessitates encoders and decoders which increase the cost of the equipment.

(*ii*) There are situations where using only analog techniques is simpler and more economical. For example, the process of signal amplification is most easily accomplished using analog circuitry.

However, advantages of digital techniques outweigh the disadvantages. For this reason, we are fast switching to digital techniques.

26.20 Boolean Algebra

Digital circuits perform the binary arithmetic operations with binary digits 1 and 0. These operations are called logic functions or logical operations. *The algebra used to symbolically describe logic functions is called* **Boolean algebra.** Boolean algebra is a set of rules and theorems by which logical operations can be expressed symbolically in equation form and be manipulated mathematically. As with the ordinary algebra, the *letters of alphabet (*e.g.* A, B, C etc.) can be used to represent the variables. Boolean algebra differs from ordinary algebra in that Boolean constants and variables can have only two values ; 0 and 1. There are four connecting symbols used in Boolean algebra *viz.*

(*i*) equals sign (=) (*ii*) plus sign (+)
(*iii*) multiply sign (·) (*iv*) bar (–)

(*i*) **Equals sign (=).** The equals sign in Boolean algebra refers to the standard mathematical equality. In other words, the logical value on one side of the sign is identical to the logical value on the other side of the sign. Suppose we are given two logical variables such that $A = B$. Then if $A = 1$, then $B = 1$ and if $A = 0$, then $B = 0$.

(*ii*) **Plus sign (+).** The plus sign in Boolean algebra refers to the logical *OR operation*. Thus, when the statement $A + B = 1$ appears in Boolean algebra, it means A ORed with B equals 1. Consequently, either $A = 1$ or $B = 1$ or both equal 1.

(*iii*) **Multiply sign (·).** The multiply sign in Boolean algebra refers to *AND operation*. Thus, when the statement $A \cdot B = 1$ appears in Boolean algebra, it means A ANDed with B equals 1. Consequently, $A = 1$ and $B = 1$. The function $A \cdot B$ is often written as AB, omitting the dot for convenience.

(*iv*) **Bar sign (–).** The bar sign in Boolean algebra refers to *NOT operation*. The NOT has the effect of inverting (complementing) the logical value. Thus, if $A = 1$, then $\overline{A} = 0$.

26.21 Boolean Theorems

We now discuss the basic Boolean theorems that are useful in manipulating and simplifying Boolean expressions. For convenience, we divide the theorems into two groups :

(*i*) Single variable theorems

(*ii*) Multivariable theorems

(*i*) **Single variable theorems.** These theorems refer to the condition when only one input to the logic gate is variable. Table 26.1 gives single variable Boolean theorems.

---

* For example, A might represent a certain digital circuit input or output and at any time, we must have either $A = 0$ or $A = 1$.

Table 26.1

Theorem 1 :	$A + 0 = A$
Theorem 2 :	$A \cdot 1 = A$
Theorem 3 :	$A + \overline{A} = 1$
Theorem 4 :	$A \cdot \overline{A} = 0$
Theorem 5 :	$A + A = A$
Theorem 6 :	$A \cdot A = A$
Theorem 7 :	$A + 1 = 1$
Theorem 8 :	$A \cdot 0 = 0$
Theorem 9 :	$\overline{\overline{A}} = A$

Theorem 1. ($A + 0 = A$). This theorem can be verified by ORing a variable A with a 0 and is illustrated in Fig. 26.18. Here one input to OR gate is always 0 and the other input A can be a value 1 or 0. When A is at 1, the output is 1 which is equal to A. When A is at 0, the output is 0 which is also equal to A (= 0). Therefore, a variable ORed with 0 is equal to the value of the variable. This is easy to remember since 0 added to anything does not effect the value of the variable, either in regular addition or OR addition.

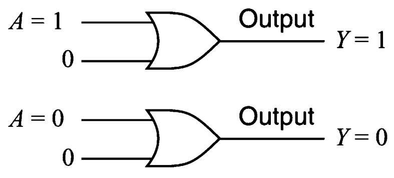


Fig. 26.18

Theorem 2. (A . $1 = A$). This theorem can be verified by ANDing a variable A with a 1 and is illustrated in Fig. 26.19. Here one input to AND gate is always 1 and the other can be a value 1 or 0. If A is 1, the output of the AND gate is 1 because both the inputs are now 1's. If A is 0, the output of the AND gate is a 0. Therefore, a variable ANDed with a 1 is equal to the value of the variable ($A \cdot 1 = A$). This is easy to remember because AND operation is just like ordinary multiplication.

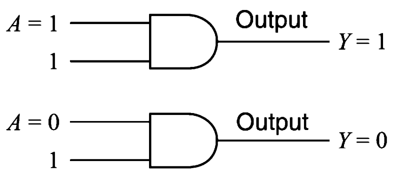


Fig. 26.19

Theorem 3. $\left(A + \overline{A} = 1\right)$. This theorem can be easily explained. If a variable A and its complement $\left(\overline{A}\right)$ are ORed, the result is always 1. If A is a 0, then $0 + \overline{0} = 0 + 1 = 1$. If A is a 1, then $1 + \overline{1} = 1 + 0 = 1$. Fig. 26.20 illustrates this theorem.

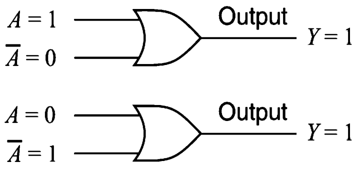


Fig. 26.20

Theorem 4. $\left(A \cdot \overline{A} = 0\right)$. This theorem states that if a variable A is ANDed with its complement, the result is zero. This is readily apparent because either A or $\overline{A}$ will always be 0. Therefore, when one of the inputs to an AND gate is 0, the output is always 0. Fig. 26.21 illustrates this theorem.

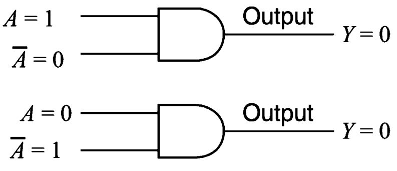


Fig. 26.21

Theorem 5. $\left(A + A = A\right)$. This theorem states that when a variable A is ORed with itself, the output is equal to the variable. Thus, if A is a 0, then $0 + 0 = 0$ and if A is a 1, then 1 + 1 = 1. Fig. 26.22 illustrates this theorem.

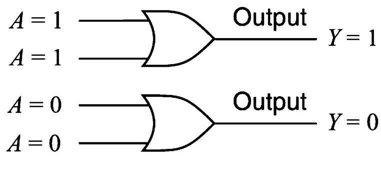


Fig. 26.22

Theorem 6. ($A \cdot A = A$). This theorem states that if a variable A is ANDed with itself, the result is equal to the variable. For example, if $A = 0$, then $0 \cdot 0 = 0$ and if $A = 1$, then $1 \cdot 1 = 1$. For either case, the output of an AND gate is equal to the value of the input variable A. Fig. 26.23 illustrates this theorem.

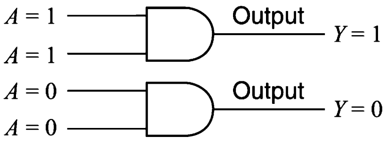


Fig. 26.23

Theorem 7. ($A + 1 = 1$). This theorem states that when a variable A is ORed with 1, the outuput is always equal to 1. Fig. 26.24 illustrates this theorem. One input to an OR gate is always 1 and the other input A can be either 1 or 0. Now 1 on an input to OR gate produces 1 on the output regardless of the value of the variable on the other input.

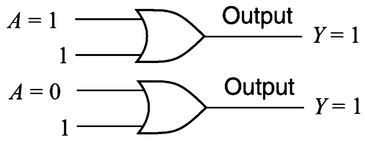


Fig. 26.24

Theorem 8. ($A \cdot 0 = 0$). This theorem states that variable A ANDed with 0 always produces 0. Recall that any time one input to an AND gate is 0, the output is 0 regardless of the value of the variable A on the other input. This theorem is illustrated in Fig. 26.25.

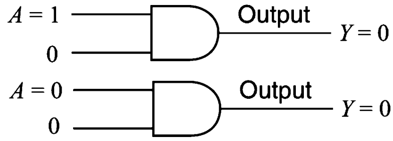


Fig. 26.25

Theorem 9. $(\overline{\overline{A}} = A)$. This theorem states that if a variable A is complemented twice, the result is the variable itself. Starting with A and inverting (complementing) it once gives $\overline{A}$. Inverting it once more gives A — the original value. This theorem is illustrated in Fig. 26.26.

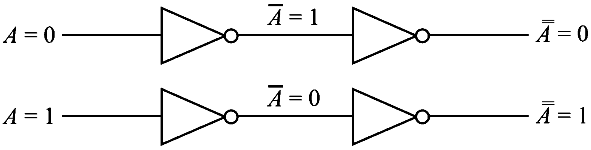


Fig. 26.26

Duality Principle. Before moving to multivariable theorems, this would be the right place to mention an important property of Boolean algebra called *duality principle.* It is stated below :

The duality principle states that a Boolean expression remains valid if operators OR and AND are interchanged and 1's and 0's in the expression are also interchanged.

In order to understand this principle, consider the Boolean Theorem 1 *viz.*

$$A + 0 = A$$

According to duality principle, this Boolean expression remains valid if OR function is replaced by AND function and 0 by 1. In that case, the Boolean expression becomes :

$$A \cdot 1 = A$$

Note that this is Boolean Theorem No. 2. Therefore, Boolean Theorem 2 is dual of Boolean Theorem 1 and *vice-versa.* Applying duality principle, Theorem 4 is dual of Theorem 3 and *vice-versa,* Theorem 6 is dual of Theorem 5 and *vice-versa*, Theorem 8 is dual of Theorem 7 and *vice-versa.* To apply duality principle to a Boolean expression, we simply interchange OR and AND operator and replace 1's by 0's and 0's by 1's.

(*ii*) **Multivariable theorems.** These theorems refer to the condition when more than one input to the logic gate are variable. Table 26.2 gives multivariable Boolean theorems.

Table 26.2

Theorem 10	:	$A + B = B + A$	*Commutative Law*
Theorem 11	:	$A \cdot B = B \cdot A$	
Theorem 12	:	$A + (B + C) = (A + B) + C$	*Associative Law*
Theorem 13	:	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$	
Theorem 14	:	$A \cdot (B + C) = A \cdot B + A \cdot C$	*Distributive Law*
Theorem 15	:	$(A + B) \cdot (C + D) = A \cdot C + B \cdot C + A \cdot D + B \cdot D$	
Theorem 16	:	$A + A \cdot B = A$	
Theorem 17	:	$(\overline{A+B}) = \overline{A} \cdot \overline{B}$	*De Morgan's Theorems*
Theorem 18	:	$(\overline{A \cdot B}) = \overline{A} + \overline{B}$	

The following points may be noted about these theorems :

(***a***) Theorems 10 and 11 obey **commutative law**. *This law states that the order in which the variables are ORed or ANDed makes no difference.*

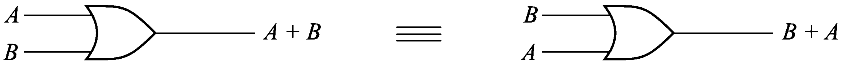


Fig. 26.27

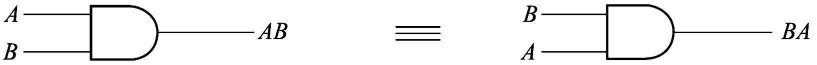


Fig. 26.28

Figure 26.27 illustrates the commutative law as applied to the OR gate while Fig. 26.28 illustrates the commutative law as applied to an AND gate.

(***b***) Theorems 12 and 13 obey **associative law.** *This law states that in the ORing or ANDing of several variables, the result is the same regardless of the grouping of the variables.*

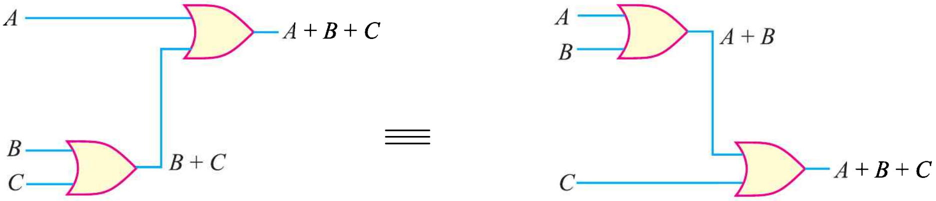


Fig. 26.29

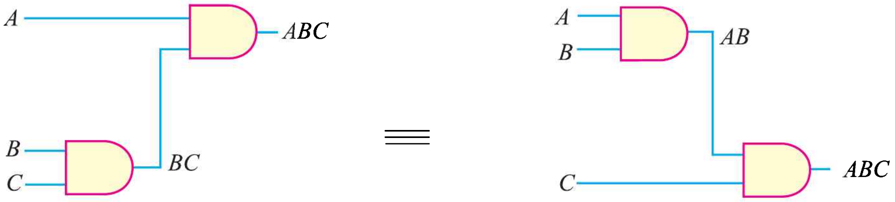


Fig. 26.30

Figure 26.29 illustrates the associative law as applied to the OR gate, while Fig. 26.30 illustrates the associative law as applied to an AND gate.

(***c***) Theorems 14 and 15 obey **distributive law**. *This law states that a Boolean expression can be expanded by multiplying term-by-term just the same as in ordinary algebra.*

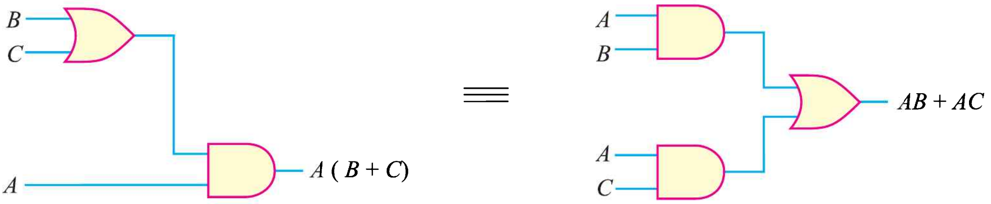


Fig. 26.31

Fig. 26.31 illustrates the distributive law in terms of gate implementation.

(*d*) We will prove Theorem 16 by factoring and using Theorems 2, 7, 10 and 14.

$$A + A \cdot B = A \cdot 1 + A \cdot B \quad \text{...Theorem 2}$$

$$= A \cdot (1 + B) \quad \text{...Theorem 14}$$

$$= A \cdot (B + 1) \quad \text{...Theorem 10}$$

$$= A \cdot 1 \quad \text{...Theorem 7}$$

$$= A \quad \text{...Theorem 2}$$

(*e*) Theorems 17 and 18 are the two most important theorems of Boolean algebra and were contributed by the great mathematician named *De Morgan*. Therefore, these theorems are called De Morgan's theorems.

26.22 De Morgan's Theorems

De Morgan's theorems are extremely useful in simplifying expressions in which a product or sum of variables is inverted. The two theorems are :

(*i*) $(\overline{A+B}) = \overline{A} \cdot \overline{B}$

(*ii*) $(\overline{A.B}) = \overline{A} + \overline{B}$

(*i*) The first De Morgan's theorem may be stated as under :

When the OR sum of two variables is inverted, this is equal to inverting each variable individually and then ANDing these inverted variables i.e.,

$$(\overline{A+B}) = \overline{A} \cdot \overline{B}$$

In this expression, *A* and *B* are the two variables. The L.H.S. is the complement of the OR sum of the two variables. The R.H.S. is the AND product of individual inverted variables.

(*ii*) The second De Morgan's theorem may be stated as under :

When the AND product of two variables is inverted, this is equal to inverting each variable individually and then ORing them i.e.,

$$(\overline{A \cdot B}) = \overline{A} + \overline{B}$$

In this expression, *A* and *B* are the two variables. The L.H.S. is the complement of the AND product of the two variables. The R.H.S. is the OR sum of the individual inverted variables.

26.23 Operator Precedence

The operator precedence for evaluating Boolean expression is (*i*) parenthesis (*ii*) NOT (*iii*) AND and (*iv*) OR. In other words, the expression inside the parenthesis must be evaluated before all other operations. The next operation that holds precedence is the complement, then follows the AND and finally the OR. For example, consider the Boolean expression :

$$A + \overline{B} . (C + D)$$

The sequence of operations will be :

(*i*) The expression inside the parenthesis (*i.e.* $C + D$) will be evaluated first.

(*ii*) Then $\overline{B}$ will be evaluated.

(*iii*) Then the results of the two (*i.e.* $\overline{B}$ and $C + D$) will be ANDed.

(*iv*) Finally, the result of the product will be ORed with A.

Example 26.13. *Using Boolean algebraic techniques, simplify the following expression* :

$$Y = A \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot \overline{D}$$

Solution.

$$Y = A \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot \overline{D} \qquad \text{...}(i)$$

Step 1 : Take out the common factors as below :

$$Y = B\,\overline{C}\,\overline{D}\,(A + \overline{A}) + B\,C\,\overline{D}\,(A + \overline{A})$$

Step 2 : Apply Theorem 3 $(A + \overline{A} = 1)$:

$$Y = B\,\overline{C}\,\overline{D} + B\,C\,\overline{D}$$

Step 3 : Again factorise :

$$Y = B\,\overline{D}\,(C + \overline{C})$$

Step 4 : Apply Theorem 3 $(C + \overline{C} = 1)$:

$$Y = B\,\overline{D} \cdot 1 = B\overline{D}$$

This is the simplified form of exp. (*i*).

Example 26.14. *Using Boolean techniques, simplify the following expression* :

$$Y = AB + A\,(B + C) + B\,(B + C)$$

Solution.

$$Y = AB + A\,(B + C) + B\,(B + C) \qquad \text{...}(i)$$

Step 1 : Apply Theorem 14 (distributive law) to second and third terms:

$$Y = AB + AB + AC + BB + BC$$

Step 2 : Apply Theorem 6 $(B \cdot B = B)$:

$$Y = AB + AB + AC + B + BC$$

Step 3 : Apply Theorem 5 $(AB + AB = AB)$:

$$Y = AB + AC + B + BC$$

Step 4 : Factor B out of last 2 terms :

$$Y = AB + AC + B\,(1 + C)$$

Step 5 : Apply commutative law and Theorem 7 $(1 + C = C + 1 = 1)$:

$$Y = AB + AC + B \cdot 1$$

Step 6 : Apply Theorem 2 $(B \cdot 1 = B)$:

$$Y = AB + AC + B$$

Step 7 : Factor B out of first and third terms :

$$Y = B\,(A + 1) + AC$$

Step 8 : Apply Theorem 7 $(A + 1 = 1)$:

$$Y = B \cdot 1 + AC$$

Step 9 : Apply Theorem 2 $(B \cdot 1 = B)$:

$$Y = B + AC$$

This is the simplified form of exp. (*i*).

Example 26.15. *Simplify the following Boolean expressions to a minimum number of literals :*

(*i*) $Y = A + \bar{A}B$ (*ii*) $Y = AB + \bar{A}C + BC$

Solution. (*i*)

$$Y = A + \bar{A}B$$

$$= A + AB + \bar{A}B \qquad [\because A = A + AB \text{ from Theorem 16}]$$

$$= A + B\,(A + \bar{A})$$

$$= A + B \qquad [\because A + \bar{A} = 1 \text{ from Theorem 3}]$$

$$\therefore \quad Y = A + B$$

(*ii*)

$$Y = AB + \bar{A}C + BC$$

$$= AB + \bar{A}C + BC \cdot (A + \bar{A})$$

$$= AB + \bar{A}C + ABC + \bar{A}BC$$

$$= AB\,(1 + C) + \bar{A}C\;(1 + B)$$

$$= AB + \bar{A}C$$

$$\therefore \quad Y = AB + \bar{A}C$$

Example 26.16. *Determine output expression for the circuit shown below and simplify it using De Morgan's theorem.*

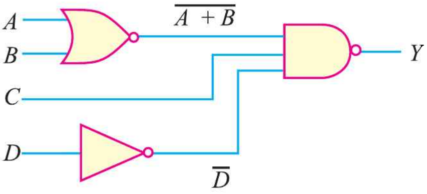


Fig. 26.32

Solution. The output expression for the circuit shown above is :

$$Y = \overline{[(\overline{A + B}) \cdot C \cdot \bar{D}]}$$

Using De Morgan's theorem :

$$Y = (A + B) + \bar{C} + D$$

$$\therefore \quad Y = A + B + \bar{C} + D$$

Example 26.17. *Find the complement of the expressions given below :*

(*i*) $Y = AB\bar{C} + A\bar{B}\bar{C}$

(*ii*) $Y = \bar{A} + (B\bar{C} + \bar{B}C)$

Solution. (*i*)

$$Y = AB\bar{C} + A\bar{B}\bar{C}$$

$$\bar{Y} = \overline{(AB\bar{C} + A\bar{B}\bar{C})}$$

Applying De Morgan's theorem :

$$\bar{Y} = \overline{(AB\bar{C})} \cdot \overline{(A\bar{B}\bar{C})}$$

Again applying De Morgan's theorem to the each expression inside the brackets :

$$\bar{Y} = (\bar{A} + \bar{B} + C) \cdot (\bar{A} + B + C)$$

(*ii*)

$$Y = \bar{A}\,(B\bar{C} + \bar{B}C)$$

$$\overline{Y} = \overline{\overline{A}\,(B\overline{C} + \overline{B}C)}$$

Applying De Morgan's theorem :

$$\overline{Y} = A + \overline{(B\overline{C} + \overline{B}C)}$$

Again applying De Morgan's theorem to the expression inside the bracket :

$$\overline{Y} = A + \overline{(B\overline{C})} \cdot \overline{(\overline{B}C)}$$

Applying De Morgan's theorem for the third time we get :

$$\overline{Y} = A + (\overline{B} + C) \cdot (B + \overline{C})$$

or $$\overline{Y} = A + \overline{BC} + BC$$

Example 26.18. *Simplify the following Boolean expressions* :

(*i*) $Y = (A + B + C) \cdot (A + B)$

(*ii*) $Y = AB + ABC + AB\overline{C}$

(*iii*) $Y = 1 + A\,(B \cdot \overline{C} + BC + \overline{B}\,\overline{C}) + A\overline{B}C + AC$

(*iv*) $Y = \overline{(A + \overline{B} + C) + (B + \overline{C})}$

Solution. (*i*)

$$Y = (A + B + C) \cdot (A + B)$$

$$= A \cdot A + A \cdot B + B \cdot A + B \cdot B + C \cdot A + C \cdot B$$

$$\text{Using } A \cdot A = A, \text{ we get,}$$

$$Y = A + AB + AB + B + AC + BC$$

$$= A + AB + B + AC + BC \qquad [\because AB + AB = AB]$$

$$= A + B + AC + BC \qquad [\because A + AB = A]$$

$$= A\,(1 + C) + B\,(1 + C)$$

$$= A \cdot 1 + B \cdot 1 \qquad [\because 1 + C = 1]$$

$$\therefore \quad Y = A + B$$

(*ii*)

$$Y = AB + ABC + AB\overline{C}$$

$$= AB + AB\,(C + \overline{C})$$

$$= AB + AB \qquad [\because C + \overline{C} = 1]$$

$$\therefore \quad Y = AB$$

(*iii*)

$$Y = 1 + A\,(B \cdot \overline{C} + BC + \overline{B}\,\overline{C}) + A\overline{B}C + AC$$

$$\text{Using } 1 + A = 1, \text{ we get,}$$

$$Y = 1 + A\overline{B}C + AC \qquad [\because 1 + A\,(B\overline{C} + BC + \overline{BC}) = 1]$$

$$= 1 + AC$$

$$\therefore \quad Y = 1$$

Thus, because of the first term *Y* reduces to 1. Therefore, any Boolean expression ORed with 1, results in 1.

(*iv*)

$$Y = \overline{(A + \overline{B} + C) + (B + \overline{C})}$$

Applying De Morgan's theorem :

$$Y = \overline{(A + \overline{B} + C)} \cdot \overline{(B + \overline{C})}$$

Again applying De Morgan's theorem :

$$Y = (\overline{A} \cdot B \cdot \overline{C}) \cdot (\overline{B} \cdot C) = 0 \qquad [\because B \cdot \overline{B} = 0,\ C \cdot \overline{C} = 0]$$

Example 26.19. *Simplify the following Boolean expression :*

$$Y = A\overline{B}D + A\overline{B}\,\overline{D}$$

Solution. $Y = A\overline{B}D + A\overline{B}\,\overline{D}$

Factoring out the common variables $A\overline{B}$ (using Theorem 14), we get ,

$$Y = A\overline{B}(D + \overline{D})$$

Using Theorem 3, $D + \overline{D} = 1.$

$\therefore \quad Y = A\overline{B}\cdot 1$

Using Theorem 2, we get,

$$Y = A\overline{B}$$

Example 26.20. *Simplify the following Boolean expression :*

$$Y = (\overline{A} + B)(A + B)$$

Solution. $Y = (\overline{A} + B)(A + B)$

The expression can be expanded by multiplying out the terms [Theorem 15].

$$Y = \overline{A}\cdot A + \overline{A}\cdot B + B\cdot A + B\cdot B$$

Using Theorem 4, $\overline{A}\cdot A = 0.$ Also $B\,.\,B = B$ [Theorem 6].

$$\therefore \quad Y = 0 + \overline{A}\cdot B + B\cdot A + B$$

$$= \overline{A}\cdot B + AB + B$$

Factoring out the variable B [Theorem 14], we have,

$$Y = B(\overline{A} + A + 1)$$

Using Theorem 7, $A + 1 = 1.$

$\therefore \quad Y = B(\overline{A} + 1)$

Again using Theorem 7, $\overline{A} + 1 = 1.$

$\therefore \quad Y = B\cdot 1$

Finally, using Theorem 2, we have,

$$Y = B$$

26.24 Combinational Logic Circuits

We can combine two or more logic gates to form a logic circuit or digital circuit. When the resulting logic or digital circuit has no feedback and no memory, it is often called combinational logic circuit.

A logic circuit consisting of two or more logic gates that has no feedback and no memory is called a ***combinational logic circuit.***

A combinational logic circuit is constructed using OR, AND and NOT gates. Therefore, the basic building block for combinational circuits is the logic gate. Since a combinational logic circuit has no feedback and no memory, its output depends *only* on the current value of its inputs.

26.25 Boolean Expressions for Combinational Logic Circuits

A combinational logic circuit (or digital circuit) often consists of several different logic gates, interconnected in such a way as to perform a specific logic function. By using the laws, theorems and techniques of Boolean algebra, we can find the Boolean expression for any combinational logic circuit. Let us find Boolean expression for some logic circuits.

(*i*) Fig. 26.33 shows a logic circuit. It consists of two AND gates and one OR gate. Each of the three gates has two input variables. Because gate G_1 is an AND gate and its two inputs are A and B, its output is AB. The gate G_2 is also an AND gate and its two inputs are C and D so that its output is CD. The gate G_3 is an OR gate so that its output is the ORing of AB and CD, producing $AB + CD$. Therefore, the Boolean expression for the output of this logic circuit is

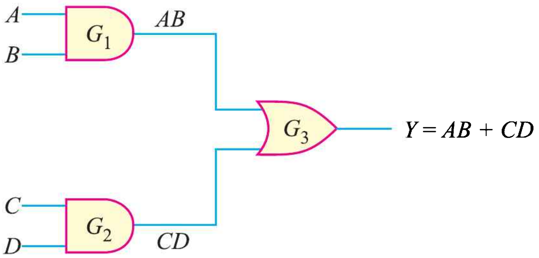


Fig. 26.33

$$Y = AB + CD$$

(*ii*) Fig. 26.34 shows a logic circuit consisting of two AND gates and one OR gate. There are four (A, B, C and D) input variables.

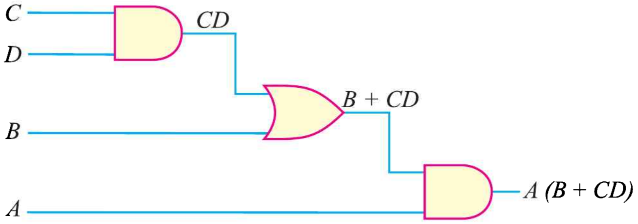


Fig. 26.34

The variable C is ANDed with D and its output is CD. Then CD is ORed with B, giving an output ($B + CD$). This sum is then ANDed with A, resulting in the following Boolean expression :

$$Y = A(B + CD)$$

(*iii*) Fig. 26.35 shows a logic circuit consisting of three AND gates and one OR gate. There are six input variables *viz.* A, B, C, D, E and F.

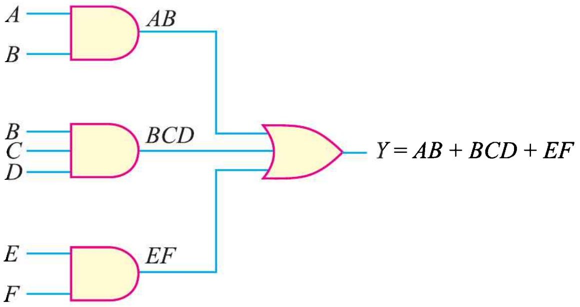


Fig. 26.35

The variables A and B are ANDed to produce AB, B, C and D are ANDed to produce BCD and E and F are ANDed to produce EF. The input to OR gate is AB, BCD and EF so the output of this gate is the ORing of the inputs *i.e.*

$$Y = AB + BCD + EF$$

26.26 AND and OR Operations in Boolean Expression

It is very important to interpret AND and OR operations in the Boolean expression. Sometimes, there may be confusion as to which operation (AND or OR) in a Boolean expression is to be performed first. For example, the Boolean expression *$A \cdot B + C$ can be interpreted in two different ways *viz.*

(*i*) $A \cdot B$ is ORed with C *or* (*ii*) A is ANDed with the term $B + C$

In order to avoid this confusion, it will be understood that if Boolean expression contains both AND and OR operations, the AND operations are performed first unless there are brackets in the expression in which case the operation inside the brackets is to be performed first. This is the same rule that is used in ordinary algebra to determine the order of operations. Let us illustrate this important point with examples.

(*i*) Consider the Boolean expression: $Y = A \cdot B + C$. Since there are no brackets in this expression, AND operation is to be performed first. In other words, first A and B are ANDed to produce $A \cdot B$ and then $A \cdot B$ is ORed with C to give the final function: $Y = A \cdot B + C$. The logic circuit representing this Boolean expression is shown in Fig. 26.36.

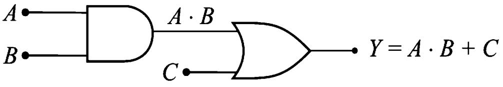


Fig. 26.36

(*ii*) Consider the Boolean expression: $Y = (A + B) \cdot C$. Since $A + B$ is in the bracket, the OR operation is to be performed first. In other words, A is ORed with B to give $(A + B)$ and then $(A + B)$ is ANDed with C to produce $Y = (A + B) \cdot C$. The logic circuit representing this Boolean expression is shown in Fig. 26.37.

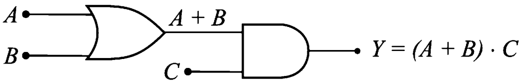


Fig. 26.37

Example 26.21. *Write the Boolean expression for the digital circuit shown in Fig. 26.38.*

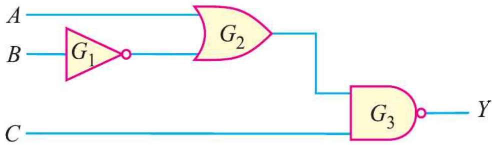


Fig. 26.38

Solution. The output of G_2 is $A + \overline{B}$. This output of G_2 is NANDed with C to yield $Y = \overline{(A + \overline{B})\,C}$. Note that bracket around $(A + \overline{B})$ is required otherwise the expression may be interpreted that A is NORed with $\overline{B}\,C$.

Example 26.22. *Write the Boolean expression for the logic circuit (digital circuit) shown in Fig. 26.39.*

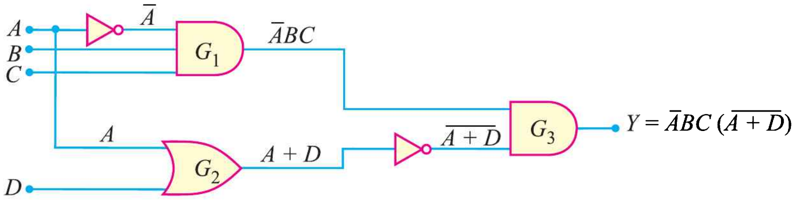


Fig. 26.39

Solution. There are two AND gates (viz. G_1 and G_3) and one OR gate (G_2). Also the circuit has two inverters. The input A is fed to G_1 through the inverter. Therefore, $\overline{A}$, B and C are ANDed by G_1 to produce an output of $\overline{A}\,BC$. The input A is ORed with D by G_2 to produce an output of $(A + D)$. The inputs $\overline{A}BC$ and $\overline{(A + D)}$ to G_3 are ANDed to produce the final output :

$$Y = \overline{A}BC\;\overline{(A + D)}$$

---

* Recall that it indicates A ANDed with B and can be expressed as $A \cdot B$ or AB.

Example 26.23. *Write the Boolean expression for the digital circuit shown in Fig. 26.40.*

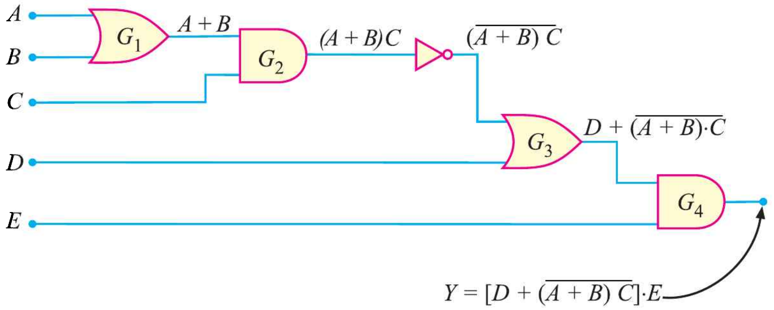

A
B
C
D
E
G_1
$A + B$
G_2
$(A + B)C$
$\overline{(A + B)\ C}$
G_3
$D + \overline{(A + B)\cdot C}$
G_4
$Y = [D + \overline{(A + B)\ C}]\cdot E$

Fig. 26.40

Solution. The output of G_1 is $A + B$. Then $(A + B)$ and C are ANDed to produce an output of $(A + B)\ C$. It is easy to see $\overline{(A + B)\ C}$ and D are ORed by G_3 to produce an output of $D + \overline{(A + B)\cdot C}$. Finally, $D + \overline{(A + B)\cdot C}$ and E are ANDed by G_4 to produce the final output Y given by ;

$$Y = [D + \overline{(A + B)\ C}\ ]\cdot E$$

Example 26.24. *Illustrate the commutative law of (i) addition and (ii) multiplication of two variables.*

Solution.

(*i*) The commutative law of addition states that the order in which the variables are ORed makes no difference. This law for the addition of two variables A and B can be written as :

$$A + B = B + A$$

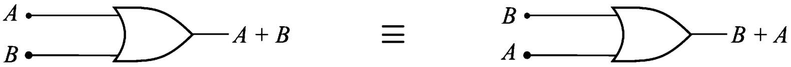


Fig. 26.41

Fig. 26.41 illustrates the commutative law as applied to the OR gate.

(*ii*) The commutative law of multiplication states that the order in which the variables are ANDed makes no difference. This law for the multiplication of two variables A and B can be written as :

$$AB = BA$$

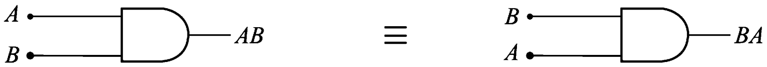


Fig. 26.42

Fig. 26.42 illustrates the commutative law as applied to the AND gate.

Example 26.25. *Illustrate associative law of (i) addition and (ii) multiplication as applied to Boolean algebra.*

Solution.

(*i*) The associative law of addition states that in the ORing of several variables, the result is the same regardless of the grouping of the variables. This law for the addition of the three variables A, B and C can be written as:

$$A + (B + C) = (A + B) + C$$

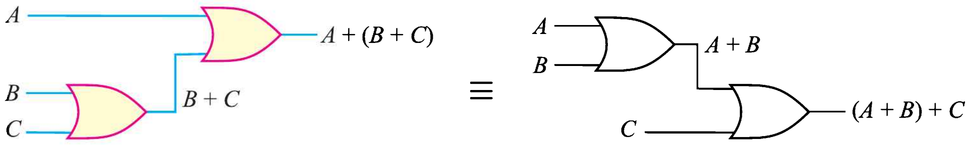


Fig. 26.43

Fig. 26.43. illustrates this law as applied to OR gates.

(*ii*) The associative law of multiplication states that it makes no difference in what order the variables are grouped when ANDing several variables. This law for the multiplication of the three variables A, B and C can be written as :

$$A\,(BC) = (AB)C$$

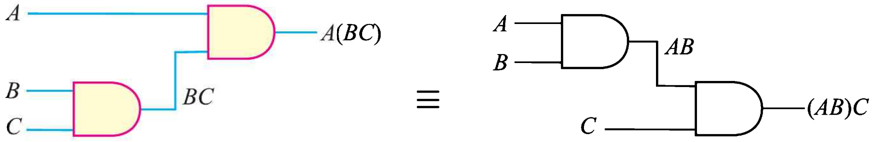


Fig. 26.44

Fig. 26.44 illustrates this law as applied to AND gates.

Example 26.26. *Illustrate distributive law as applied to Boolean algebra.*

Solution. This law states that ORing several variables and ANDing the result with a single variable is equivalent to ANDing the single variable with each of the several variables and ORing the products. The distributive law can be written for three variables (A, B and C) as under :

$$A\,(B + C) = AB + BC$$

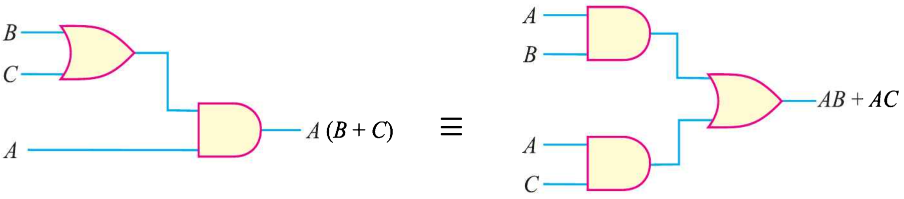


Fig. 26.45

Fig. 26.45 illustrates the distributive law in terms of gate implementation.

Note. The commutative law, the associative law and the distributive law of Boolean algebra are applicable regardless of the number of variables involved.

26.27 Truth Table from Logic Circuit

The output of a logic circuit for the given inputs can be determined directly from the circuit *without* using the Boolean expression. The procedure is to take a given set of inputs and work through each gate of the circuit to determine the final output. Let us illustrate the procedure with an example. Consider the logic circuit shown in Fig. 26.46. It consists of two AND gates and one OR gate. Each of the three gates has two input variables. Each of the input variables can be either a high (1) or a low (0). Since there are four input variables, there are 16 possible combinations of the input variables ($2^4 = 16$). We shall develop the truth table for the circuit without using the Boolean expression for the circuit.

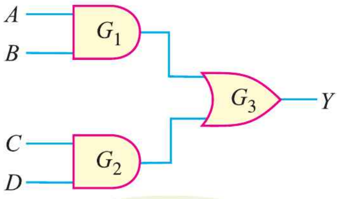


Fig. 26.46

First, suppose each input is low (*i.e.* $A = 0$, $B = 0$, $C = 0$ and $D = 0$). Under this condition, we shall examine the output of each gate in the circuit to arrive at the final output Y. If the inputs to gate G_1 are low (0), the output of G_1 is low (0). Also the output of G_2 is low (0) because both inputs are low (0). The two low inputs to G_3 also make its output low (0). Therefore, the output of the logic circuit is low when all the inputs are low as shown in the truth table. Similarly, we can find the output of the circuit for the remaining 15 input combinations.

Truth Table

$$Y = AB + CD$$

Inputs *A B C D*	*G_1 Output* *(AB)*	*G_2 Output* *(CD)*	*G_3 Output* *Y*
0 0 0 0	0	0	0
0 0 0 1	0	0	0
0 0 1 0	0	0	0
0 0 1 1	0	1	1
0 1 0 0	0	0	0
0 1 0 1	0	0	0
0 1 1 0	0	0	0
0 1 1 1	0	1	1
1 0 0 0	0	0	0
1 0 0 1	0	0	0
1 0 1 0	0	0	0
1 0 1 1	0	1	1
1 1 0 0	1	0	1
1 1 0 1	1	0	1
1 1 1 0	1	0	1
1 1 1 1	1	1	1

Note. We can also construct the truth table by developing the Boolean expression from the logic circuit. The logic circuit shown above (See Fig. 26.46) is redrawn as shown in Fig. 26.47. The Boolean expression for this logic circuit is

$$Y = AB + CD$$

Now simply put in the values for each combination of inputs and use the Boolean rules and laws to determine the final output Y. For example, when $A = 1$, $B = 1$, $C = 1$ and $D = 0$, the final output is

$$\begin{aligned} Y &= AB + CD \\ &= 1.1 + 1.0 \\ &= 1 + 0 \\ &= 1 \end{aligned}$$

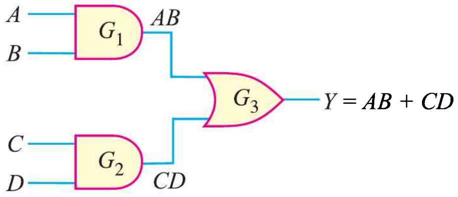


Fig. 26.47

Similary, we can find Y for the remaining 15 input combinations to get the truth table shown above.

26.28 Developing Logic Circuit from its Boolean Expression

We have seen how we can derive the Boolean expression for a given logic circuit. We now do the opposite *i.e.* create the logic circuit from its Boolean expression. Consider the following Boolean expression :

$$X = AB + CD$$

The function is composed of two terms, AB and CD, and it contains four variables. The first term is formed by ANDing A and B and the second term is formed by ANDing C and D. These two terms are then ORed to form the function X. The logic gates required to implement $X = AB + CD$ are as follows :

(*i*) Two two-input AND gates to form AB and CD.

(*ii*) One two-input OR gate to form the final function X (= $AB + CD$).

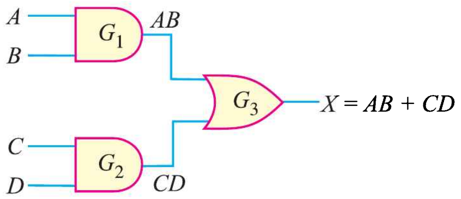


Fig. 26.48

The logic circuit that performs the function $X = AB + CD$ is shown in Fig. 26.48.

Example 26.27. *Drawn the logic circuit that implements the expression* $X = AB + CDE$.

Solution.

$$X = AB + CDE$$

The function is composed of two terms, AB and CDE, and it contains a total of five variables. The first term is formed by ANDing A and B and the second term is formed by ANDing C, D and E. These two terms are then ORed to form the function X. The logic gates required to implement $X = AB + CDE$ are as follows :

(*i*) One two-input AND gate to form AB.

(*ii*) One three-input AND gate to form CDE.

(*iii*) One two-input OR gate to form the final function X (= $AB + CDE$).

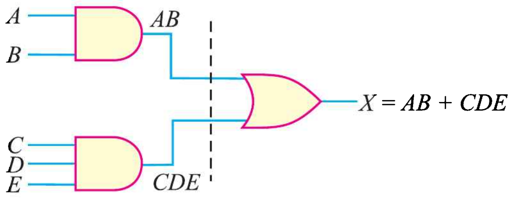


Fig. 26.49

The logic circuit that performs the function $X = AB + CDE$ is shown in Fig. 26.49.

Example 26.28. *Draw the logic circuit that implements the expression* $X = AB + \overline{B}C$.

Solution.

$$X = AB + \overline{B}C$$

The function is composed of two terms, AB and $\overline{B}C$, and it contains three variables. The first term is formed by ANDing A and B and the second term is formed by ANDing $\overline{B}$ and C. These two terms are then ORed to form the final function. The logic gates required to implement $X = AB + \overline{B}C$ are as follows :

(*i*) One inverter to form $\overline{B}$.

(*ii*) Two two-input AND gates to form AB and $\overline{B}C$.

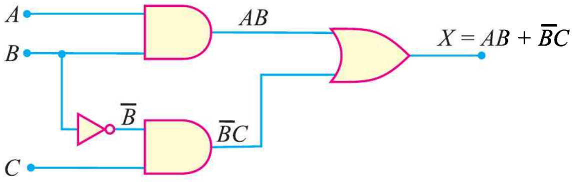


Fig. 26.50

(*iii*) One two-input OR gate to form the final function X (= $AB + \overline{B}C$).

The logic circuit that performs the function $X = AB + \overline{B}C$ is shown in Fig. 26.50.

Example 26.29. *Draw the logic circuit that implements the expression* $X = AB\,(C\bar{D} + EF)$.

Solution.

$$X = AB\,(C\bar{D} + EF)$$

A breakdown of this equation shows that the term AB and the term $C\bar{D} + EF$ are ANDed. The term AB is formed by ANDing the variables A and B. The term $C\bar{D} + EF$ is formed first by ANDing C and $\bar{D}$, ANDing E and F and then ORing these two terms. The logic gates required to implement $X = AB\,(C\bar{D} + EF)$ are as follows :

(*i*) One inverter to form $\bar{D}$.

(*ii*) Two two-input AND gates to form $C\bar{D}$ and EF.

(*iii*) One two-input OR gate to form $C\bar{D} + EF$.

(*iv*) One two-input AND gate to form AB.

(*v*) One two-input AND gate to form $X\,[=AB\,(C\bar{D} + EF)]$.

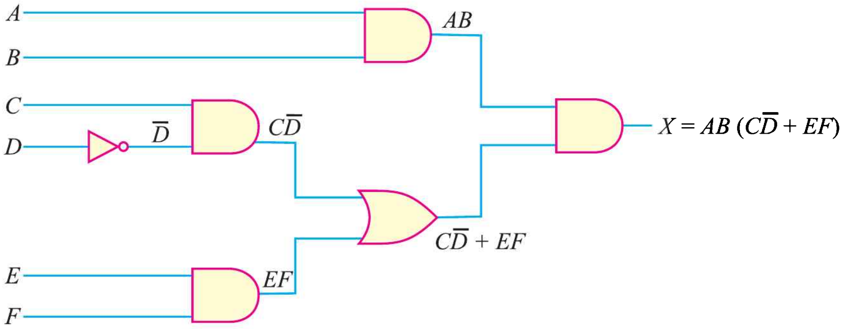


Fig. 26.51

The logic circuit that forms the function $X = AB\,(C\bar{D} + EF)$ is shown in Fig. 26.51.

26.29 Sum-of-Products Form

The sum-of-products form of a Boolean expression consists of two or more AND terms (*i.e.* products) that are ORed together. For example, $AB + CD$ is a sum-of-products expression. Here AND terms AB and CD are ORed (added). Other examples of this form are :

(*i*) $ABC + \bar{A}B\bar{C}$

(*ii*) $A\bar{B}C + DEF + A\overline{EF}$

(*iii*) $\bar{A} + BC\bar{D} + EFG$

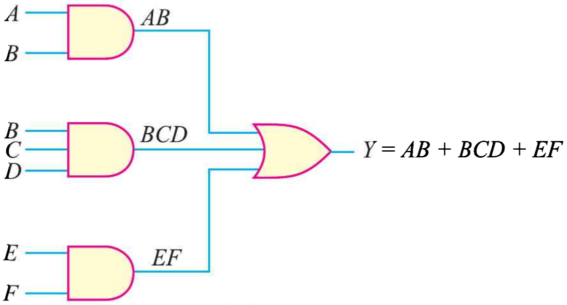


Fig. 26.52

The sum-of-products is a very useful form of a Boolean expression due to the straightforward manner is which it can be implemented in logic gates. For example, Fig. 26.52 shows the logic circuit that results in a sum-of-products form. It has simply two steps: ANDing and then ORing. Therefore, this form is always only a *two-level* gate network *i.e.* the maximum number of gates through which a signal must pass in going form input to output is two (excluding inversions, but these can also be worked in).

26.30 Simplification of Boolean Expressions

The form of Boolean expression determines how many and which types of logic gates are needed as well as how they are connected together. The more complicated the Boolean expression, the more complex the logic circuit will be. It is, therefore, desirable to simplify an expression as much as possible to get the simplest logic circuit. Note that the new expression can be used to implement a logic circuit that is equivalent to the original logic circuit but contains fewer gates and connections. While simplifying a Boolean expression, the following two steps may be very helpful:

(*i*) Put the original expression into the sum-of-products form by the repeated use of rules, theorems and techniques of Boolean algebra.

(*ii*) Once it is in this form, the product terms are checked for common factors and factoring is performed wherever possible.

Illustration. Fig. 26.53 shows the logic circuit. The Boolean expression for this circuit is

$$X = AC\bar{D} + \bar{A}B\,(CD + BC)$$

We require *five AND gates*, *two OR gates* and *two inverters* to implement this expression. In all, nine gates are needed. We shall now use laws, rules and techniques of Boolean algebra to get the simplest expression for the given function.

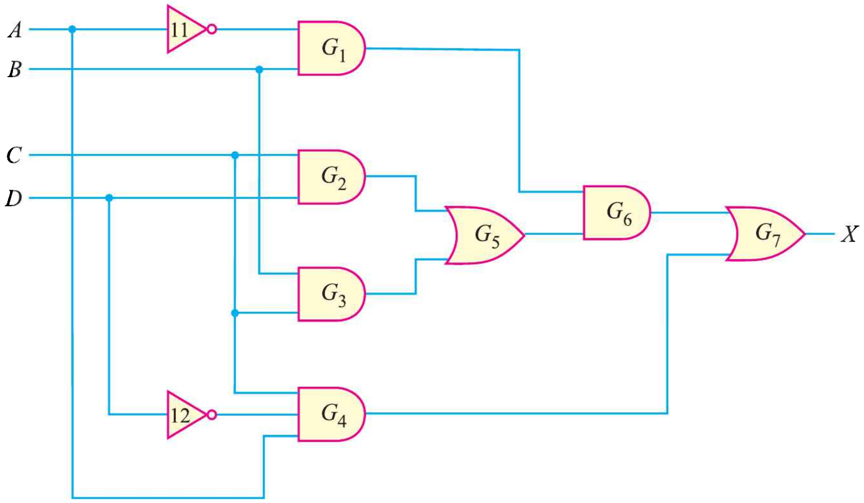


Fig. 26.53

Step 1. Apply distributive law to the second term by multiplying the term $CD + BC$ by $\bar{A}B$. The result is :

$$X = AC\bar{D} + \bar{A}BCD + \bar{A}BBC$$

Step 2. Applying the rule $BB = B$ to the third term, we have,

$$X = AC\bar{D} + \bar{A}BCD + \bar{A}BC$$

Step 3. Note that C is common to every term so that it can be factored out using distributive law.

$$\therefore \quad X = C\,(A\bar{D} + \bar{A}BD + \bar{A}B)$$

Step 4. We see that the term $\bar{A}B$ appears in the last two terms within the bracket and can be factored out of those two terms.

$$\therefore \quad X = C\,[A\bar{D} + \bar{A}B\,(D + 1)]$$

$$\text{Since } D + 1 = 1, \quad X = C\,(A\bar{D} + \bar{A}B)$$

It appears that this equation cannot be simplified any further, but is can be written in a slightly different way by applying the distributive law (this results in the sum-of-products form):

$$X = AC\bar{D} + \bar{A}BC$$

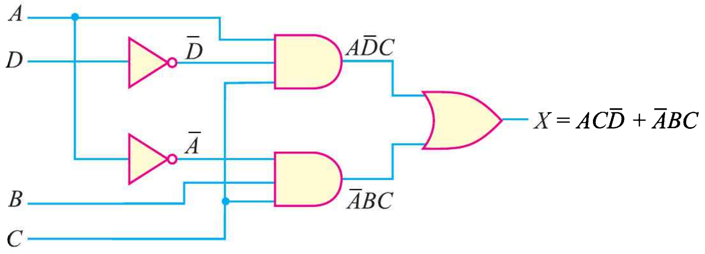


Fig. 26.54

Implementing this equation (*i.e.* $X = AC\bar{D} + \bar{A}BC$) into the logic circuit, it only requires *two three-input AND gates*, *two inverters* and *one two-input OR gate* as shown in Fig. 26.54. Note that this minimised circuit is equivalent to the original circuit of Fig. 26.53 but only requires five gates (instead of nine).

Example 26.30. *Simplify the expression :*

$$X = \bar{A}\bar{B}C + A\bar{B}C + AB\bar{C} + ABC$$

Solution.

$$X = \bar{A}\bar{B}C + A\bar{B}C + AB\bar{C} + ABC$$

Step 1. Note that the first two terms have $\bar{B}C$ as common factors while the last two terms have AB as common factors.

$$\therefore \quad X = \bar{B}C\,(A + \bar{A}) + AB\,(C + \bar{C})$$

Step 2. $A + \bar{A} = 1$ and $C + \bar{C} = 1$ so that :

$$X = \bar{B}C \cdot 1 + AB \cdot 1$$

Step 3. Since $\bar{B}C \cdot 1 = \bar{B}C$ and $AB{\cdot}1 = AB$ so that :

$$\boldsymbol{X = AB + \bar{B}C}$$

Note that not only is the Boolean expression simplified, but so is the resultant logic circuit.

Example 26.31. *Simplify the expression :*

$$X = AB + A\,(B + C) + B\,(B + C)$$

Solution.

$$X = AB + A\,(B + C) + B\,(B + C)$$

Step 1. Applying distributive law to the second and third terms, we have,

$$X = AB + AB + AC + BB + BC$$

Step 2. Now $BB = B$ and $AB + AB = AB$ so that :

$$X = AB + AC + B + BC$$

Step 3. $B + BC = B(1 + C) = B \cdot 1 = B$

$\therefore$ $X = AB + AC + B$

Step 4. Factoring B out, we have,

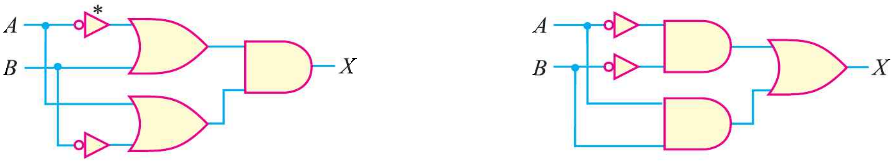
$$X = B(A + 1) + AC$$

Step 5. $A + 1 = 1$ so that $B(A + 1) = B \cdot 1 = B$.

$\therefore$ $\mathbf{X = B + AC}$

The original expression is simplified as far as it can go. Once you get acquainted with Boolean simplification techniques, you can combine many individual steps.

Example 26.32. *Simplify the circuit of Fig. 26.55 (i).*



(*i*) (*ii*)

Fig. 26.55

Solution. The Boolean expression for the circuit shown in Fig. 26.55 (*i*) is

$$X = (\overline{A} + B)\,(A + \overline{B})$$

Step 1. Multiplying out to get the sum-of-products form, we have,

$$X = \overline{A}A + \overline{A}\,\overline{B} + BA + B\overline{B}$$

Step 2. Now $\overline{A}A = 0$ and $B\overline{B} = 0$ so that :

$$X = \overline{A}\,\overline{B} + AB$$

This expression is implemented in Fig. 26.55 (*ii*). If you compare the circuit with the original circuit, you see that both circuits contain the same number of gates and connections. *Therefore, the simplification process has not produced a simpler circuit but it has produced an alternative circuit.*

26.31 Binary Addition

The addition of two binary numbers is performed in exactly the same manner as the addition of decimal numbers. In fact, binary addition is simpler, because we have only two digits (0 and 1). When adding binary numbers, the following rules apply :

$$0 + 0 = 0$$
$$1 + 0 = 1$$
$$1 + 1 = 10 = 0 + \text{carry of 1 into next position}$$
$$1 + 1 + 1 = 11 = 1 + \text{carry of 1 into next position}$$

It is not necessary to consider the addition of more than two binary numbers at a time. It is because the circuitry that actually performs the addition in a digital system can handle only two numbers at a time. When more than two numbers are to be added, the first two are added together and then their sum is added to the third number and so on.

Examples. Let us illustrate binary addition with two examples.

---

* This is the alternate symbol for the inverter.

(*i*) Let us add the following two binary numbers :

$$\begin{array}{r} 1\,0\,1 \\ +\ \underline{0\,1\,0} \\ 1\,1\,1 \end{array}$$

The addition is done column by column starting at the right as it is in the decimal number system. For the first column, 1 + 0 = 1 and for the second column, 0 + 1 = 1. For the third or last column, 1 + 0 = 1. This produces a sum of 111.

(*ii*) Let us now add the following two binary numbers :

$$\begin{array}{r} 1\,0\,1\,1\,1 \\ +\ \underline{1\,0\,0\,1\,0} \\ 1\,0\,1\,0\,0\,1 \end{array}$$

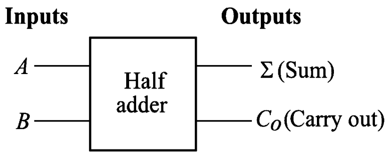
For the first column, 1 + 0 = 1. In the second column, we have, 1 + 1 = 10 = 0 with a carry of 1. For the third column, we have, 1 + 0 + carry of 1 = 1 + 1 = 10 = 0 with a carry of 1. For the fourth column, 1 + 0 + 0 = 1 + 0 = 1. For the fifth column, we have 1 + 1 = 10 = 0 with a carry of 1. This produces a sum of 101001.

Binary addition is the most important arithmetic operation in digital systems. It is because the operations of subtraction, multiplication and division as they are performed in most modern digital computers and calculators actually use only addition as their basic operation. To be an intelligent worker on digital equipment, you must master binary addition.

26.32 Electronic Adders

A logic circuit that performs the function of binary addition is called **electronic adder** *or* **adder.** The adder circuit consists of properly connected logic gates. There are usually two forms of the adder in common applications *viz.* (*i*) half adder (*ii*) full adder.

(*i*) Half Adder (HA). A logic circuit that can add two binary bits is called a half adder (*HA*). Fig. 26.56 (*i*) shows the block symbol for the half adder. The adder circuit would need two inputs and two outputs. The two inputs are for the two digits to be added, either 0 or 1. One output terminal is for the sum of the two inputs and the other output is for the carry, if necessary. Fig. 26.56 (*ii*) shows the addition table of the adder and can be thought of as a truth table. The numbers being added are on the input side of the table. The truth table has two output columns, one column for the sum and one column for the carry. The sum column is labeled with summation symbol Σ. The carry column is labeled with C_o. The C_o stands for carry output or *carry out.* Thus the half adder circuit has two inputs (A, B) and two outputs (Σ, C_o).



(*i*)

Truth Table

Inputs		Outputs	
B	*A*	Σ	C_o
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1
Binary digits to be added		Sum	Carry out
		XOR	AND

(*ii*)

Fig. 26.56

The half adder would behave according to the truth table shown in Fig. 26.56 (*ii*). Take a careful look at the truth table. The output columns (sum and carry) can be produced by using two gates as under :

(*a*) The sum column is the output of XOR gate. Remember that XOR gate has HIGH output when either input is HIGH but not when both inputs are the same.

(*b*) The carry column is the output of the AND gate. Both inputs must be HIGH for there to be a HIGH in the output.

Thus we can produce half adder using a two-input AND gate and a two-input XOR gate as shown in Fig. 26.57. The half adder circuit adds only the LSB column (1s column) in a binary addition problem. The reason is that it has no input for a carry-in.

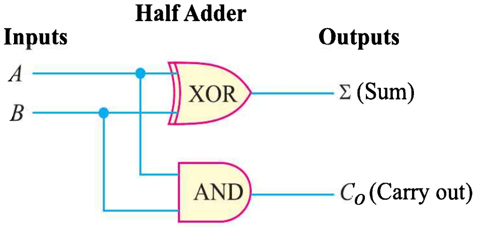
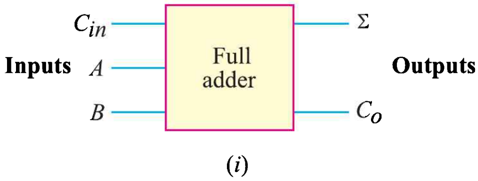


Fig. 26.57

(*ii*) **Full Adder (FA).** A full adder adds two binary bits plus a carry input (C_{in}) to produce the sum (Σ) and carry (C_o) outputs. Fig. 26.58 (*i*) shows the block diagram of a full adder. It is formed by using two half adder circuits and an OR gate as shown in Fig. 26.58 (*iii*). Note the carry-in input which requires the extra half adder. The output of the OR gate forms the carry-out (C_o) output.

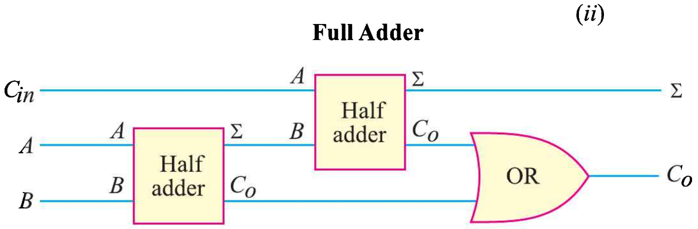


(*i*)

Truth Table

Inputs			Outputs	
C_{in}	B	A	Σ	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
Carry + B + A			Sum	Carry out

(*ii*)



(*iii*)

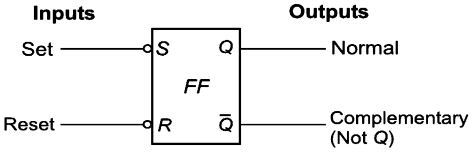
Fig. 26.58

The full adder has three inputs : C_{in}, *A* and *B*. These three inputs must be added to get the Σ and C_o outputs. Fig. 26.58 (*ii*) shows the truth table for a full adder. It shows all the possible combinations of *A, B* and C_{in}. The full adder is used for binary addition in all places except the 1s place which means 2s, 4s, 8s etc.

26.33 Flip-Flops

A *flip-flop* is a bistable circuit made up of logic gates. A bistable circuit can exist in either of two stable states indefinitely and can be made to change its state by means of some external signal. The most important use of this property is that a flip-flop can "store" binary information. We have seen that a logic gate can make a logical decision based on the immediate conditions at the input terminals. However, the gates normally do not have a memory characteristic to retain the input data. On the other hand, flip-flops have the valuable feature of remembering. The reason is that a flip-flop circuit is bistable. Because the flip-flop's output remains at a 0 or 1 depending on the last input signal, the flip-flop can be said to "remember". Another name for the flip-flop is *bistable multivibrator.* We shall discuss two important types of flip-flops *viz.* (*i*) *R–S* flip-flop and (*ii*) *J–K* flip-flop.

(*i*) R–S Flip-Flop. The **R–S* type is the basic flip-flop logic circuit. Fig. 26.59 (*i*) shows the logic symbol for an *R–S* flip flop. It has two inputs called *set* (*S*) and *reset* (*R*). The two outputs are labeled as Q and $\bar{Q}$. In flip-flops, the outputs are always opposite or complementary. In other words, if output $Q = 1$, then output $\bar{Q} = 0$ and so on. Note the small bubbles for inversion at the *S* and *R* input terminals. The bubbles show that this *FF* has active LOW inputs. Logic 0 is required to activate the *R* or *S* input.



(*i*)

Truth Table

Mode of operation	Inputs		Outputs	
	S	*R*	*Q*	$\bar{Q}$
Prohibited	0	0	1	1
Set	0	1	1	0
Reset	1	0	0	1
Disabled	1	1	No change	

(*ii*)

Fig. 26.59

The exact behaviour of a flip-flop is defined by its truth table shown in Fig. 26.59 (*ii*). In the left column, the four modes of operation are :

(*a*) *Prohibited mode.* When the *S* and *R* inputs are both 0, both outputs go to a logical 1. This is called a prohibited state for the flip-flop. This mode is not used because it drives both outputs HIGH. A flip-flop must operate with complementary outputs.

(*b*) *Set mode.* The second line of truth table shows that when input *S* is 0 and *R* is 1, the *Q* output is set to logical 1. This is called the set mode. In this *FF*, the bubble at *S* means that a LOW here makes *Q* go HIGH.

(*c*) *Reset mode.* The third line of the truth table shows that when input *R* is 0 and *S* is 1, output *Q* is reset (cleared) to 0. This is called the reset mode. In this *FF*, the bubble at *R* means a LOW here resets *Q* to make it LOW.

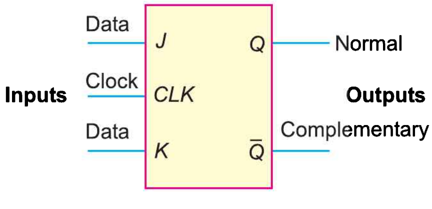
(*d*) *Disabled mode.* The fourth line of the truth table shows both inputs (*R* and *S*) at 1. This is the idle or at rest condition and leaves Q and $\bar{Q}$ in their previous complementary states. This is called disabled state because there is no change. The outputs stay as they were, with *Q* either set or reset. Because of the disabled mode, the flip-flop "remembers" the preceding state by remaining at that state until it is switched. That operation is possible because a flip-flop is a bistable circuit.

(*ii*) J–K Flip-Flop. The *J–K* flip-flop is probably the most widely used and is considered the universal flip-flop because it can be used in many ways. The logic symbol for the *J–K* flip-flop is illustrated in Fig. 26.60 (*i*). The inputs labeled *J* and *K* are the data inputs. The input labeled *CLK* is the clock input. Outputs Q and $\bar{Q}$ are the usual normal and complementary outputs.

Fig. 26.60(*ii*) shows the truth table for the *J–K* flip-flop. This table shows four useful modes of operation. When the *J* and *K* inputs are both 0, the flip-flop is in the *hold* (or *disabled*) *mode.* In the hold mode, the data inputs have no effect on the outputs. The outputs "hold" the last data present. Lines 2 and 3 of the truth table show the reset and set conditions for the *Q* output. Line 4 of the truth table illustrates the useful *toggle* position of the *J–K* flip-flop. When both data inputs *J* and *K* are at 1, repeated *clock pulses cause the output to turn off-on-off-on-off-on and so on. This off-on action is like a toggle switch and is called *toggling*. Each clock pulse toggles the outputs to switch to their opposite states.

---

* It is reset/set type flip-flop and hence the name *R–S* flip-flop.



(*i*)

Truth Table

Mode of operation	Inputs			Outputs		
	CLK	*J*	*K*	Q	$\bar{Q}$	Effect on output Q
Hold	⎍	0	0	No change		No change – disable
Reset	⎍	0	1	0	1	Reset or cleared to 0
Set	⎍	1	0	1	0	Set to 1
Toggle	⎍	1	1	Toggle		Changes to opposite state

(*ii*)

Fig. 26.60

MULTIPLE-CHOICE QUESTIONS

1. The binary number 10101 is equivalent to decimal number ....

(*i*) 19 (*ii*) 12

(*iii*) 27 (*iv*) 21

2. The universal gate is ....

(*i*) NAND gate (*ii*) OR gate

(*iii*) NOT gate (*iv*) none of the above

3. The inverter is ....

(*i*) NOT gate (*ii*) OR gate

(*iii*) AND gate (*iv*) none of the above

4. The inputs of a NAND gate are connected together. The resulting circuit is ....

(*i*) OR gate (*ii*) AND gate

(*iii*) NOT gate (*iv*) none of the above

5. The NOR gate is OR gate followed by ....

(*i*) AND gate (*ii*) NAND gate

(*iii*) NOT gate (*iv*) none of the above

6. The NAND gate is AND gate followed by ....

(*i*) NOT gate (*ii*) OR gate

(*iii*) AND gate (*iv*) none of the above

7. Digital circuit can be made by the repeated use of ....

(*i*) OR gates (*ii*) NOT gates

(*iii*) NAND gates (*iv*) none of the above

8. The only function of NOT gate is to ....

(*i*) stop a signal

(*ii*) invert input signal

(*iii*) act as a universal gate

(*iv*) none of the above

9. When an input signal 1 is applied to a NOT gate, the output is ....

(*i*) 0

(*ii*) 1

(*iii*) either 0 or 1

(*iv*) none of the above

10. In Boolean algebra, the bar sign (–) indicates ....

(*i*) OR operation

(*ii*) AND operation

(*iii*) NOT operation

(*iv*) none of the above

---

* The clock pulses occur at some fixed interval, say after every 10 microsecond.

11. The given Boolean expression is

$$Y = A\,\overline{B} + B\,\overline{A}$$

If $A = 1$ and $B = 1$, then $Y =$

(*i*) 1 (*ii*) 0

(*iii*) either 1 or 0 (*iv*) none of the above

12. In Boolean algebra, the plus sign (+) indicates ....

(*i*) AND operation

(*ii*) OR operation

(*iii*) NOT operation

(*iv*) none of the above

13. $\overline{(A + B)}$ = ...

(*i*) $\overline{A} + \overline{B}$ (*ii*) $\overline{A} - \overline{B}$

(*iii*) $\overline{A} \cdot \overline{B}$ (*iv*) none of the above

14. $\overline{(A \cdot B)}$ = ...

(*i*) $\overline{A} + \overline{B}$ (*ii*) $\overline{A} \cdot \overline{B}$

(*iii*) $\overline{A} - \overline{B}$ (*iv*) none of the above

15. $A + A \cdot B =$ ....

(*i*) B (*ii*) A

(*iii*) $\overline{A} + B$ (*iv*) none of the above

Answers to Multiple-Choice Questions

1.	(*iv*)	**2.**	(*i*)	**3.**	(*i*)	**4.**	(*iii*)	**5.**	(*iii*)
6.	(*i*)	**7.**	(*iii*)	**8.**	(*ii*)	**9.**	(*i*)	**10.**	(*iii*)
11.	(*ii*)	**12.**	(*ii*)	**13.**	(*iii*)	**14.**	(*i*)	**15.**	(*ii*)

Chapter Review Topics

1. Write a short note on analog and digital signals.
2. What is a digital circuit ?
3. What is binary number system ?
4. How will you make decimal to binary conversion ?
5. How will you make binary to decimal conversion ?
6. What is a logic gate ?
7. What are the three basic logic gates ?
8. Describe OR function with a 2-input OR gate.
9. Explain AND function with a 2-input AND gate.
10. What is a NAND gate ?
11. What is a NOR gate ?
12. How will you obtain NOT gate from NAND gate ?
13. What is indicated by plus (+), dot (.) and bar (—) in a Boolean expression ?
14. State De Morgan's theorems.
15. What are encoders and decoders ?

Problems

1. Convert decimal number 23 into equivalent binary number. **[$(10111)_2$]**
2. Simplify the expression $Y = A\,C\,D + \overline{A}\,B\,C\,D.$ **[Y = $A\overline{C} + \overline{B}D$]**
3. Simplify the expression $Y = \overline{(\overline{A} + C) \cdot (B + \overline{D})}$ to one having only single variables inverted. **[Y = $A\overline{C} + \overline{B}D$]**
4. Find the complement function of $Y = \overline{A}\,B\,\overline{C} + \overline{A}\,\overline{B}\,C.$ **[(A + $\overline{B}$ + C) (A + B + $\overline{C}$)]**
5. Simplify the expression $Y = A \cdot B + A \cdot \overline{B}$. **[Y = A]**
6. Simplify the expression $Y = A \cdot B \cdot C + B \cdot C.$ **[Y = B · C]**

7. Simplify the following Boolean expression to a minimum number of literals :

$$Y = A(\bar{A} + B) \qquad \textbf{[Y = AB]}$$

8. Simplify the following Boolean function to a minimum number of literals :

$$Y = \bar{A}\,\bar{B}\,C + \bar{A}\,B\,C + A\,\bar{B} \qquad [\mathbf{Y} = \bar{A}\,C + A\bar{B}\,]$$

9. Simplify the expression : $Y = (A + B)(\bar{A} + C)(B + C)$ $\quad$ **[Y = (A + B)** $(\bar{A} + C)$ **]**

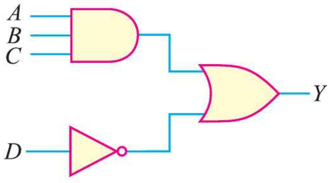
10. Find the complement of the function :

$$Y = A(\bar{B}\,\bar{C} + B\,C)\,H \qquad [\bar{Y} = \bar{A} + (B + C)(\bar{B} + \bar{C})]$$

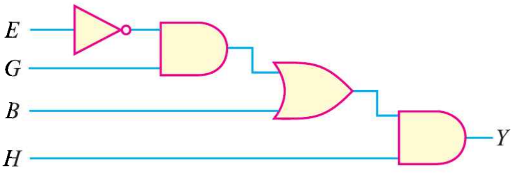
11. Draw the logic circuit for the following Boolean expressions :

(*i*) $Y = ABC + \bar{D}$ $\qquad$ (*ii*) $Y = (\bar{E}G + B)\,H$

Ans.



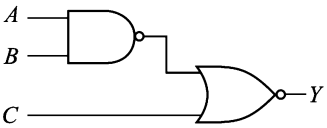
(*i*)



(*ii*)

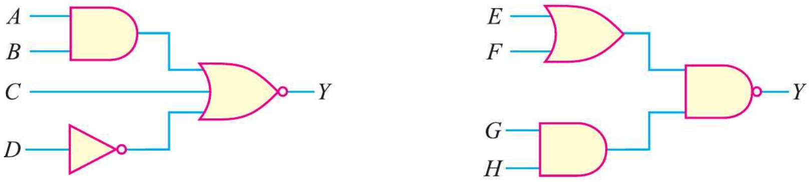
12. A logic circuit is given by the Boolean escperssion : $Y = \overline{\overline{AB} + C}$. Draw the logic circuit for this expression.

Ans.



(*iii*)

13. Write the Boolean expressions for the logic circuits shown in Fig. 26.61.



(*i*) (*ii*)

Fig. 26.61

[Ans. :- (*i*) $Y = \overline{AB + C + \bar{D}}$ (*ii*) $Y = \overline{(E + F)(GH)}$

14. Write the Boolean expression for the logic circuit shown in Fig. 26.62.

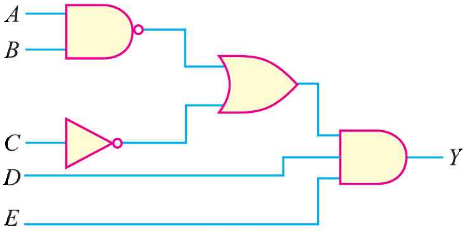


Fig. 26.62

[Ans. :- $Y = (\overline{AB} + \bar{C})\,DE$ **]**

15. Write the BCD code for 829.

[100000101001]

16. What is the decimal number for 10000111000 BCD ?

[438]

Discussion Questions

1. Why is logic circuit name so ?

2. What is the importance of digital techniques ?

3. Why is analog system unreliable ?

4. What is the importance of NAND gate ?

5. What is Boolean algebra ?

6. What is the importance of De Morgan's theorems in Boolean Algebra ?

7. What is the meaning of + sign in Boolean expression ?

8. Give two differences between decimal and binary systems.

9. What are the disadvantages of digital circuits ?

10. What are the advantages of Boolean theorems ?

11. What is the meaning of sign **.** in Boolean expression ?

12. What is a universal gate ? Why is it so named?

13. Most of information we handle is in decimal form. Will a digital circuit process this information as such?

14. What role is played by encoder and decoder?

INDEX

A

Acceptor atoms, **64**
A.C. equivalent circuit, **248**
A. C. load line, **251**
Active region, **475**
Alpha, **148**
Amplitude modulation, **414**
Amplification, **146**
Amplifier:
  Class A power, **312**
  bandwidth, **284**
  Class B power, **312**
  Class C power, **313**
  Class C tuned, **402**
  direct coupled, **299**
  distortion in, **311**
AND gate, **740**
Anode, **33**
Antenna, **413**
Astable multivibrator, **478**
Audio amplifier, **307**
Avalanche breakdown, **72**

B

Band:
  conduction, **51**
  valence, **51**
Bandwidth, **284**
Barrier potential, **67**
Base, **143**
Bel power gain, **283**
Bel voltage gain, **284**
Beta, **153**
Binary system, **730**
Bipolar transistor, **146**
Bi-stable multivibrator, **482**
Boolean algebra, **748**
Breakdown:
  Avalanche, **72**
  Zener, **108**
Bridge rectifier, **92**
Bypass capacitor, **242**

C

Capacitor filter, **103**
Cathode, **33**
Cathode ray oscilloscope, **616**
CE amplifier, **164**
Chassis, **24**
Chip, semiconductor, **628**
Choke input filter, **104**
Clampers, **495**
Class A operation, **312**
Class B operation, **312**
Class C operation, **313**

Clippers, **487**
Collector, **143**
Collector feedback bias, **209**
Colpitts oscillator, **372**
CB amplifier, **148**
Complementary-symmetry, **330**
Conduction band, **51**
Constant current source, **9**
Constant voltage source, **8**
Coupling capacitor, **242**
Covalent bond, **56**
Crystal oscillator, **383**
Current feedback, **347**
Current gain, **173**
Cut-off frequency, **285**

D

D. C. amplifier, **299**
D. C. equivalent circuit, **247**
Decibel, **283**
Depletion layer, **67**
Diac, **586**
Differential amplifier, **664-687**
Diffusion, **67**
Digital circuit, **730**
Diode circuits, **76-124**
Direct coupling, **299**
Discrete circuit, **627**
Distortion, **311**
Donor atom, **63**
Doping, **62**
Double based diode, **590**
Drain-source curve, **511**
Driver stage, **325**
Dynamic resistance, **79**
Dual-in-line pack, **635**

E

Efficiency:
  Half-wave rectifier, **88**
  Full-wave rectifier, **94**
Electromagnetic deflection, **618**
Electrons, **4**
Electron emission, **28–37**
Electron gun, **617**
Electron-hole pair, **61**
Emitter, **143**
Emitter follower, **349**
Encoder, **746**
Energy band theory, **50**
Equivalent circuit of amplifier, **272**
Equivalent circuit with signal source, **272**
Epitaxial layer, **630**
Exclusive OR gate, **744**
Extrinsic semiconductor, **62**
Expression for collector :
  efficiency, **313**

F

Feedback, **335**
Feedback amplifier, **337**
JFET importance, **510**
Field effect transistor, **507**
Field emission, **34**
Filter circuit, **103**
Forward bias, **68**
Forbidden gap, **51**
Free electron, **6**
Free-running multivibrator, **478**
Frequency modulation, **426**
Frequency response, **283**

G

Gain:
  power, **173**
  voltage, **173**
  gate, **507**
  ground, **24**

H

Hartley oscillator, **374**

Holding current, **558**
Hole current, **61**
Heat sink, **322**
Hybrid, **643**

I

Inductor filter, **104**
Insulated gate, **536**
Integrated circuit, **628**
Interstage coupling, **281**
Intermediate frequency, **434**
Intrinsic semiconductor, **62**
Intrinsic stand off ratio, **592**
Impedance matching, **296**
Input impedance, **172**

J

Junction, pn, **66**
Junction diode, **77**
Junction transistor, **142**

K

Knee voltage, **72**

L

Large signal operation, **312**
LC oscillators, **371–376**
Leakage current, **71**
Light-emitting diode (LED), **126**
Load D.C. and A.C., **248, 249**
Load line:
  a.c., **251**
  d.c., **249**
Local oscillator, **433**
Logic gates, **738**

M

Max. A.C. power output , **314**
Max. collector efficiency, **314**
Majority carriers, **65**
Microelectronics, **627**
Minority carriers, **65**
Modulation:
  AM, **414**
  FM, **426**
Monolithic IC, **629**
MOSFET, **535**
Multicolour LEDs, **128**
Multivibrators :
  astable, **478**
  bistable, **482**
  monostable, **480**

N

NAND gate, **742**
Negative feedback, **336**
n-p-n transistor, **142**
n-type semiconductor, **62**
Noise, **311**
NOR gate, **743**
NOT gate, **742**

O

Operational Amplifiers, **662-728**
  Block diagram, **663**
  Input/output Polarity relation, **689**
  Voltage gain, **688**
  Values of supply voltage, **690**
Optoisolator, **133**
OR gate, **739**
Oscillators:
  Collpits. **372**
  Crystal, **383**
  Hartley, **374**
  L.C., **371-376**
  Phase shift, **377**
  Tuned collector, **371**
  Wein bridge, **378**
Oscilloscope, **616**
Output resistance, **172**
Over voltage detector, **595**
Oxide coated emitter, **32**

P

p-type semiconductor, **64**
Peak inverse voltage, **73**
Pentavalent atoms, **63**

Phase-shift oscillator, **377**
Photo-diode, **130**
Photo-emission, **35**
Piezo-electric effect, **380**
π-filter, **104**
Pinch off voltage, **513**
p-n-junction, **66**
p-n-p transistor, **142**
Positive clipper, **487**
Power dissipation, **311**
Power gain, **173**
Push-pull amplifier, **326**

Q

Quartz crystal, **381**
Quiescent point, **167**

R

RC differentiator, **483**
RC integrator, **486**
RC oscillator, **377**
RC coupling, **289**
Rectifiers, **87**
Relaxation oscillator, **595**
Reverse bias, **68**
Ripple factor, **101**

S

Saturation collector current, **473**
Saturation region, **474**
Sawtooth wave, **619**
Secondary emission, **34**
SCR, **555**
Semiconductors, **56**
Shockley diode, **137**
Sideband frequencies, **418**
Stabilisation, **197**
Stand off voltage, **592**
Substrate, **629**
Superhetrodyne receiver, **433**

T

Thermal runaway, **197**
Thermionic emisssion, **30**
Thevenin's theorem, **15**
Thyristor, **555**
Transformer coupling, **294**
Transistor:
  AM modulator, **419**
  CB, **148**
  CC, **162**
  CE, **152**
Trivalent impurity, **64**
Tuned collector oscillator, **371**
Tunnel diode, **134**

U

Uni-junction transistor, **589**
Unipolar transistor, **510**

V

Varactor-diode, **136**
Voltage divider bias, **212**
Voltage regulator, **448**
Voltmeter, electronic, **609**

W

Wein bridge oscillator, **378**
Window, **631**

X

X-cut, **380**

Y

Y-cut, **380**

Z

Zener breakdown, **108**
Zener diode, **108**
Zener diode regulator, **110**
Zener symbol, **109**